8-Channel VARIABLE GAIN AMPLIFIER

FEATURES

- **LOW INPUT NOISE:**
  – 1.2nV/√Hz at f_{IN} = 5MHz
- **EXTREMELY LOW POWER OPERATION:**
  – 75mW/CHANNEL at 3V
- **INTEGRATED LOW-PASS, 2-POLE FILTER**
  – 14MHz BANDWIDTH
- **INTEGRATED INPUT LNA**
- **INTEGRATED INPUT CLAMP DIODES**
- **DIFFERENTIAL OUTPUT**
- **READABLE CONTROL REGISTERS**
- **INTEGRATED CONTINUOUS WAVE (CW) PROCESSOR**

APPLICATIONS

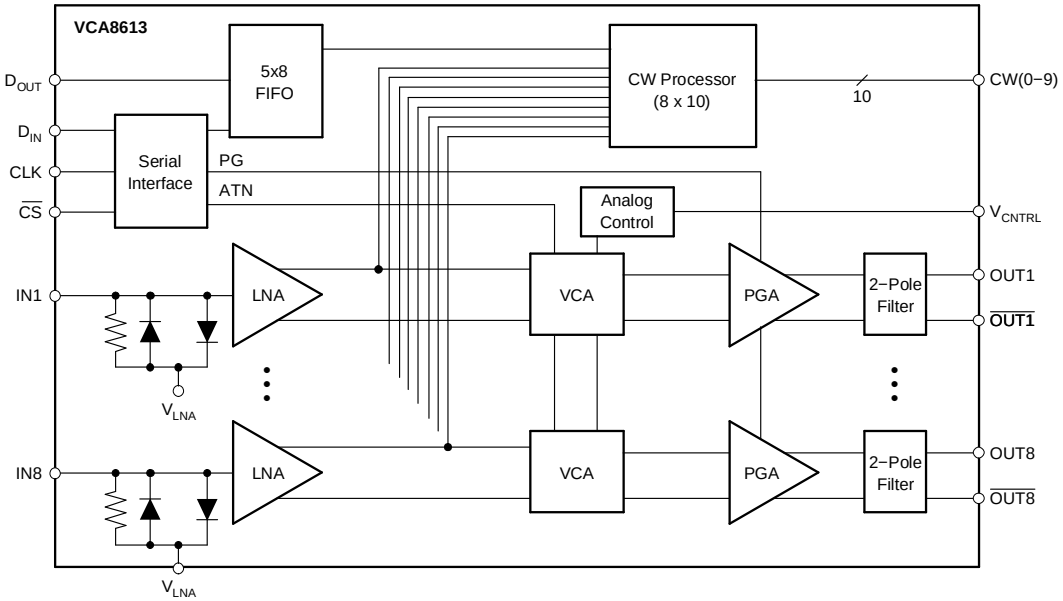
- **Medical and Industrial Ultrasound Systems**

DESCRIPTION

The VCA8613 is an 8-channel variable gain amplifier ideally suited to portable ultrasound applications. Excellent dynamic performance enables use in low-power, high-performance portable applications. Each channel consists of a Low-Noise pre-Amplifier (LNA) and a Variable Gain Amplifier (VGA). The differential outputs of the LNA can be switched through the 8x10 cross-point switch, which is programmable through the serial interface port.

The output of the LNA is fed directly into the VGA stage. The VGA consists of two parts, a Voltage Controlled Attenuator (VCA) and a Programmable Gain Amplifier (PGA). The gain and gain range of the PGA can be digitally configured separately. The gain of the PGA can be varied between two discrete settings of 21dB and 26dB. The VCA has four programmable maximum attenuation settings: 29dB, 33dB, 36.5dB, and 40dB. Also, the VCA can be continuously varied by a control voltage from 0dB to a maximum of 29dB, 33dB, 36.5dB, and 40dB.

The output of the PGA feeds directly into an integrated 2-pole, low-pass filter, allowing for direct connection to a differential input Analog-to-Digital Converter (ADC), such as the ADS5121 or ADS5122 from Texas Instruments. The VCA8613 is available in a TQFP-64 package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VCA8613	TQFP-64	PAG	–40°C to +85°C	VCA8613Y	VCA8613YT	Tape and Reel, 250
					VCA8613YR	Tape and Reel, 1500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

$+AV_{DD}$	+3.6V
Analog Input	–0.3V to $+AV_{DD}$ + 0.3V
Logic Input	–0.3V to $+AV_{DD}$ + 0.3V
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C
Thermal Resistance, Junction-to-Ambient (θ_{JA})	66.6°C/W
Thermal Resistance, Junction-to-Case (θ_{JC})	4.3°C/W

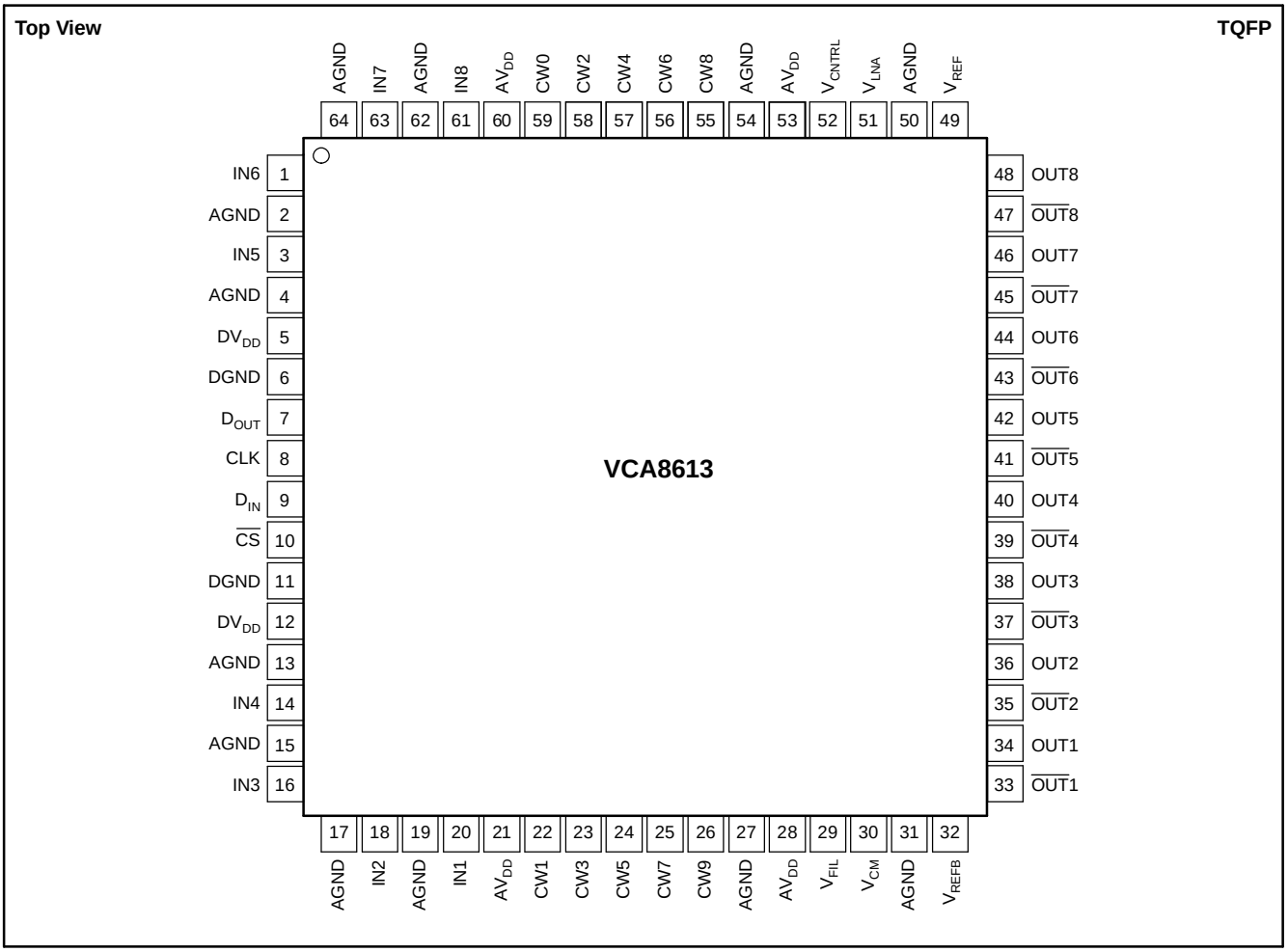
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS: $AV_{DD} = DV_{DD} = 3V$

At T_A = +25°C, load resistance = 500Ω on each output to ground; the input to the preamp (LNA) is single-ended; f_{IN} = 2MHz, ATN = 01, PG = 00, and the output from the VCA is differential, unless otherwise noted.

PARAMETER	CONDITIONS	VCA8613			UNIT
		MIN	TYP	MAX	
PREAMPLIFIER (LNA)					
Input Resistance			4.5		kΩ
Input Capacitance(1)			80		pF
Input Bias Current			1		nA
Maximum Input Voltage(2)			110		mV_{PP}
Input Voltage Noise	TGC-mode, f_{IN} = 5MHz		1.2		$nV/\sqrt{Hz}$
Input Voltage Noise	CW-mode, f_{IN} = 5MHz		1.6		$nV/\sqrt{Hz}$
Output Swing (Differential)			2		V_{PP}
Bandwidth			70		MHz
Gain	TGC-Mode, SE-to-Differential		24.5		dB
Input Common-Mode Voltage			2.4		V
ACCURACY					
Gain Slope	V_{CNTRL} = 0.2V to 1.7V		20		dB/V
Gain Error	V_{CNTRL} = 0.2V to 1.7V			2	dB
Output Offset Voltage	Differential		±20		mV
GAIN CONTROL INTERFACE					
Input Voltage (V_{CNTRL}) Range			0 to 2.0		V
Input Resistance			1		MΩ
Response Time	40dB Gain Change, ATN = 00		0.2		µs
PROGRAMMABLE VGA AND LOW-PASS FILTER					
–3dB Cutoff (low-pass)			14		MHz
–3dB Cutoff (high-pass)			800		kHz
Slew Rate			300		V/µs
Output Impedance			10		Ω
Crosstalk			49		dB
Output Common-Mode Voltage			1		V
Output Swing (Differential)(3)				2	V_{PP}
2nd-Harmonic Distortion	V_{OUT} = 500mV_{PP}		–55	–45	dBc
3rd-Harmonic Distortion	V_{OUT} = 500mV_{PP}		–50	–40	dBc
Group Delay Variation			±3		ns
CONTINUOUS WAVE PROCESSOR					
CW Output Compliance Voltage		3		3.3	V
V/I Converter Transconductance		10.35	11.5	12.65	mA/V
Maximum CW Output Swing			2.0		mA_{PP}
LOGIC INPUTS					
V_{IN} LOW (input low voltage)		0		0.6	V
V_{IN} HIGH (input high voltage)		2.1		V_{DD}	V
Input Current				±1	µA
Input Pin Capacitance			5		pF
Clock Input Frequency		10k		25M	Hz
POWER SUPPLY					
Supply Voltage		2.85	3.0	3.15	V
Power-Down Delay			5		µs
Power-Up Delay			20		µs
Power Dissipation (TGC Mode)	Operating All Channels		600	700	mW

(1) Includes internal clamping diodes.
(2) Under conditions that input signal is within linear range of LNA.
(3) Under conditions that signal is within linear range of output amplifier.



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
5, 12	DV_{DD}	Digital Supplies
2, 4, 13, 15, 17, 19, 27, 31, 50, 54, 62, 64	AGND	Analog Ground
1, 3, 14, 16, 18, 20, 61, 63	IN(1–8)	Single-Ended LNA Inputs
22–26, 55–59	CW(0–9)	Continuous Wave Processor Outputs
51	V_{LNA}	Reference Voltage for LNA–internally generated; requires external bypass cap.
29	V_{FIL}	Reference Voltage for Output Filter–internally generated; requires external bypass cap.
30	V_{CM}	Common-Mode Voltage–internally generated; requires external bypass cap.
34, 36, 38, 40, 42, 44, 46, 48	OUT(1–8)	Positive Polarity PGA Outputs
33, 35, 37, 39, 41, 43, 45, 47	$\overline{OUT}$(1–8)	Negative Polarity PGA Outputs
52	V_{CNTRL}	Attenuator Control Voltage Input
9	D_{IN}	Serial Data Input Pin
10	$\overline{CS}$	Serial Data Chip Select
8	CLK	Serial Data Input Clock
7	D_{OUT}	Serial Data Output Pin
21, 28, 53, 60	AV_{DD}	Analog Supplies
6, 11	DGND	Digital Ground
49	V_{REF}	Reference Voltage for Attenuator–internally generated; requires external bypass cap.
32	V_{REFB}	Bandgap Reference Voltage—internally generated; requires external bypass cap.

INPUT REGISTER BIT MAPS

Table 1. Byte 1—Control Byte Register Map

BIT #	NAME	DESCRIPTION
LSB	1	Start bit; always a '1'—40-bit countdown starts upon first '1' after chip select.
1	$\overline{W}$/R	1 = Write, 0 = Read—Read prevents latching of DATA only—Control register still latched.
2	P_{WR}	Entire chip. Power Control—'1' = Off. Otherwise, chip is on.
3	A0	Attenuator control bit (LSB): ATN [A1:A0].
4	A1	Attenuator control bit (MSB).
5	Mode	'1' = TGC mode (CW powered down), '0' = Doppler mode (TGC powered down)
6	PG0	LSB of PGA Gain Control; PG [PG1:PG0].
MSB	PG1	MSB of PGA Gain Control

Table 2. Byte 2—First Data Byte

BIT #	NAME	DESCRIPTION
LSB	Data 1:0	Channel 1, LSB of Matrix Control
1	Data 1:1	Channel 1, Matrix Control
2	Data 1:2	Channel 1, Matrix Control
3	Data 1:3	Channel 1, MSB of Matrix Control
4	Data 2:0	Channel 2, LSB of Matrix Control
5	Data 2:1	Channel 2, Matrix Control
6	Data 2:2	Channel 2, Matrix Control
MSB	Data 2:3	Channel 2, MSB of Matrix Control

Table 3. Byte 3—Second Data Byte

BIT #	NAME	DESCRIPTION
LSB	Data 3:0	Channel 3, LSB of Matrix Control
1	Data 3:1	Channel 3, Matrix Control
2	Data 3:2	Channel 3, Matrix Control
3	Data 3:3	Channel 3, MSB of Matrix Control
4	Data 4:0	Channel 4, LSB of Matrix Control
5	Data 4:1	Channel 4, Matrix Control
6	Data 4:2	Channel 4, Matrix Control
MSB	Data 4:3	Channel 4, MSB of Matrix Control

Table 4. Byte 4—Third Data Byte

BIT #	NAME	DESCRIPTION
LSB	Data 5:0	Channel 5, LSB of Matrix Control
1	Data 5:1	Channel 5, Matrix Control
2	Data 5:2	Channel 5, Matrix Control
3	Data 5:3	Channel 5, MSB of Matrix Control
4	Data 6:0	Channel 6, LSB of Matrix Control
5	Data 6:1	Channel 6, Matrix Control
6	Data 6:2	Channel 6, Matrix Control
MSB	Data 6:3	Channel 6, MSB of Matrix Control

Table 5. Byte 5—Fourth Data Byte

BIT #	NAME	DESCRIPTION
LSB	Data 7:0	Channel 7, LSB of Matrix Control
1	Data 7:1	Channel 7, Matrix Control
2	Data 7:2	Channel 7, Matrix Control
3	Data 7:3	Channel 7, MSB of Matrix Control
4	Data 8:0	Channel 8, LSB of Matrix Control
5	Data 8:1	Channel 8, Matrix Control
6	Data 8:2	Channel 8, Matrix Control
MSB	Data 8:3	Channel 8, MSB of Matrix Control

DATA SHIFT SEQUENCE

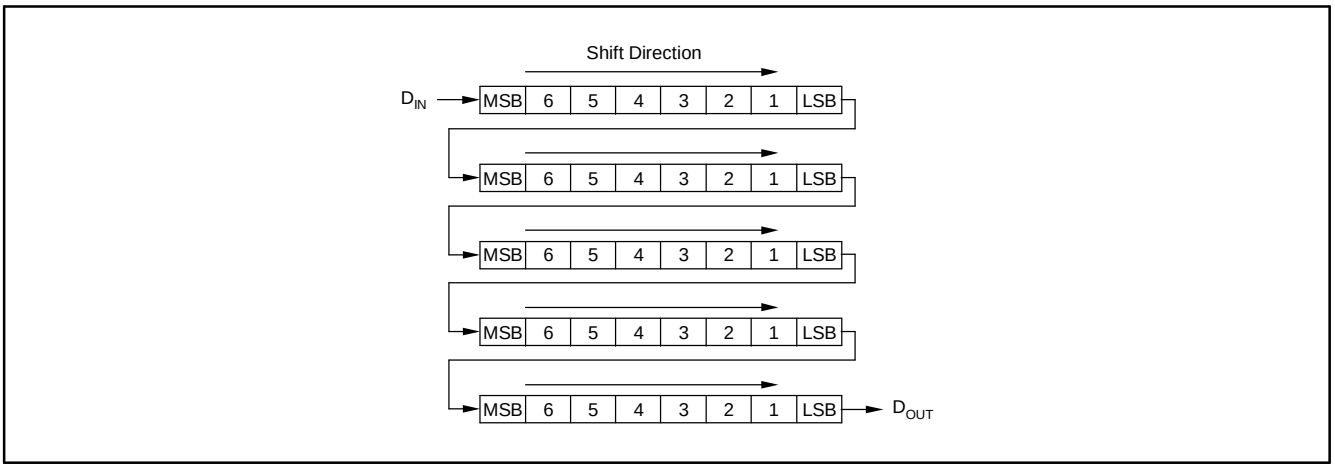


Table 6. Maximum Attenuation

A1, A0	MAXIMUM ATTENUATION
0, 0	29dB
0, 1	33dB
1, 0	36.5dB
1, 1	40dB

Table 7. PGA Gain Settings

PG1, PG0	PGA GAIN
0, 0	21dB
0, 1	26dB
1, 0	Invalid
1, 1	Invalid

Table 8. CW Coding for Each Channel

NUMBER	CW CODING (MSB, LSB)	CHANNEL DIRECTED TO:
0	0000	Output CW0
1	0001	Output CW1
2	0010	Output CW2
3	0011	Output CW3
4	0100	Output CW4
5	0101	Output CW5
6	0110	Output CW6
7	0111	Output CW7
8	1000	Output CW8
9	1001	Output CW9
10	1010	Channel tied to +V (internal)
11	1011	Channel tied to +V (internal)

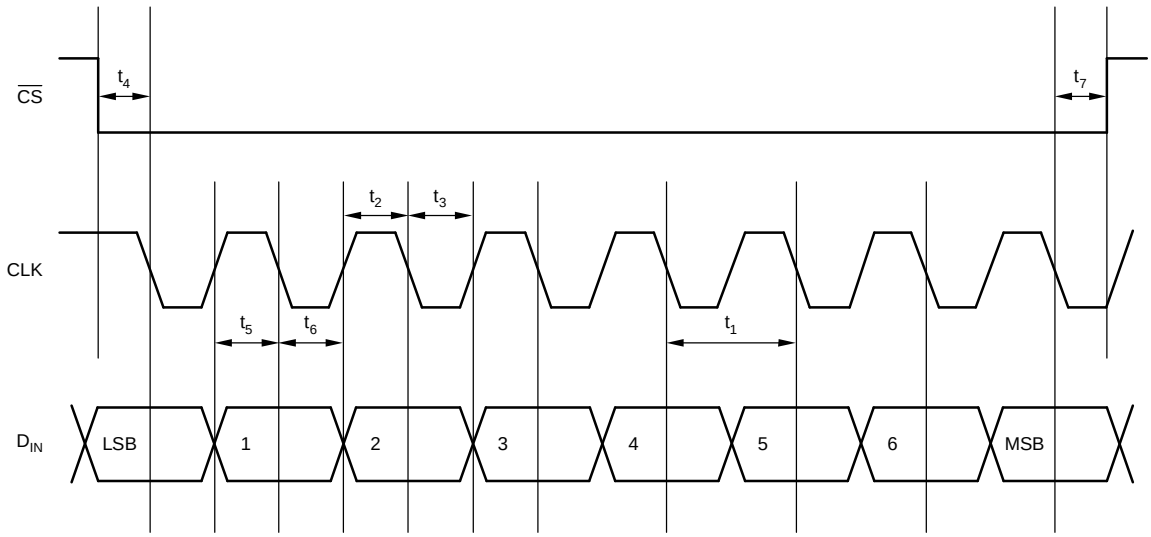
Table 8. CW Coding for Each Channel (continued)

NUMBER	CW CODING (MSB, LSB)	CHANNEL DIRECTED TO:
12	1100	Channel tied to +V (internal)
13	1101	Channel tied to +V (internal)
14	1110	Channel tied to +V (internal)
15	1111	Channel tied to +V (internal)
Applies to bytes 2 through 5.		

WRITE/READ TIMING

Generally follows SPI Timing Specification:

- All writes and reads will be 5 bytes at a time. Each byte consists of 8 bits;
- Separate write and read data lines;
- Reads will follow the same bit stream pattern seen in the write cycle;
- Reads will extract data from the FIFO, not the latched register;
- D_{OUT} data is continuously available and need not be enabled with a read cycle. Selecting a read cycle in the control register only prevents latching of data. The control register is still latched.



NOTE: It is highly recommended that the clock be turned off after the required data has been programmed into the VCA8613.

SERIAL PORT TIMING TABLE

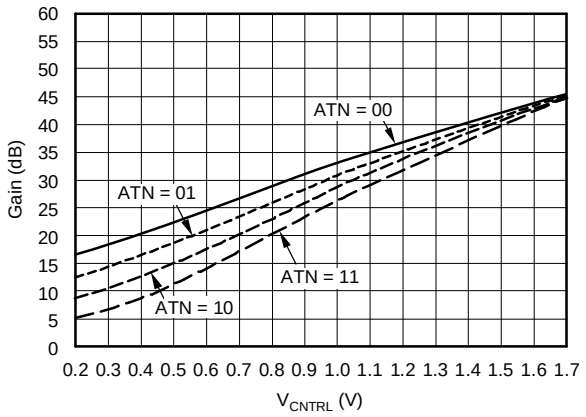
Chip Select ($\overline{CS}$) must be held low (active LOW) during transfer. $\overline{CS}$ can be held permanently low.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Serial CLK Period	40			ns
t_2	Serial CLK HIGH Time	20			ns
t_3	Serial CLK LOW Time	20			ns
t_4	$\overline{CS}$ Falling Edge to Serial CLK Falling Edge	10			ns
t_5	Data Setup Time	5			ns
t_6	Data Hold Time	5			ns
t_7	Serial CLK Falling Edge to $\overline{CS}$ Rising Edge	10			ns

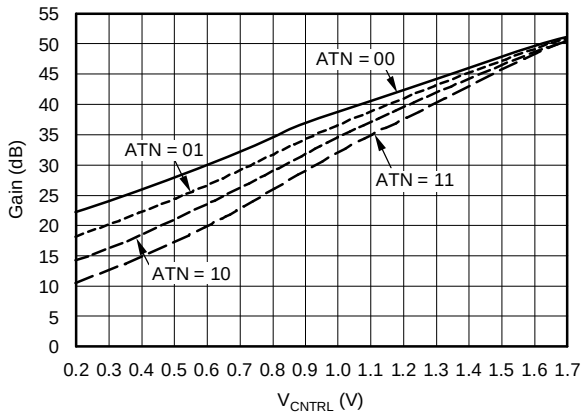
TYPICAL CHARACTERISTICS

At T_A = +25°C, f_{IN} = 2MHz, ATN = 01, PG = 00, V_{CNTRL} = 1.7V; differential output, 750mV$_{PP}$, and AV_{DD} = DV_{DD} = 3.0V, unless otherwise noted.

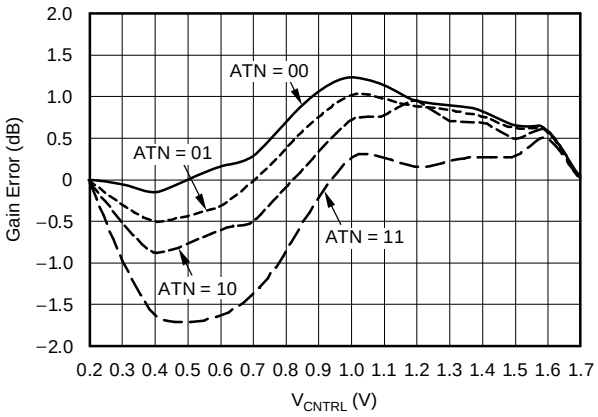
GAIN vs V_{CNTRL} (PG = 00)



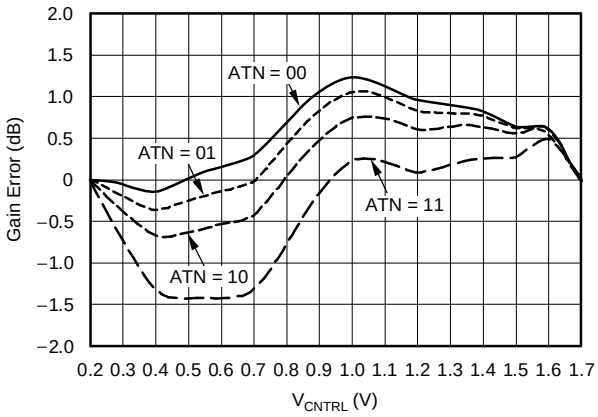
GAIN vs V_{CNTRL} (PG = 01)



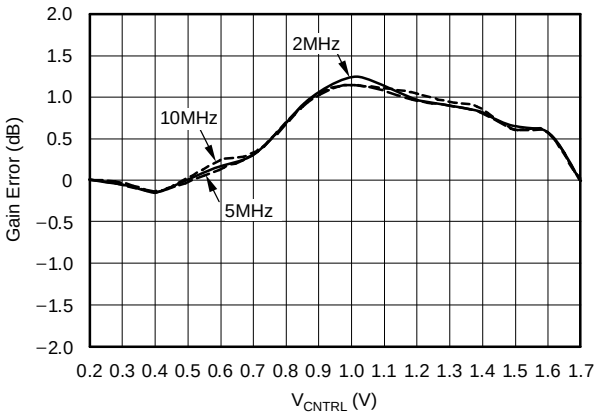
GAIN ERROR vs V_{CNTRL} (PG = 00)



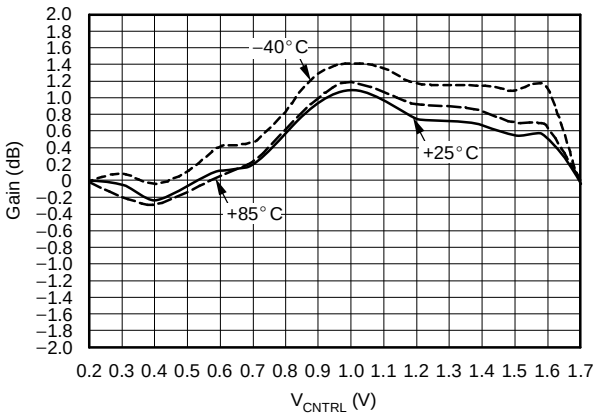
GAIN ERROR vs V_{CNTRL} (PG = 01)



GAIN ERROR vs V_{CNTRL}



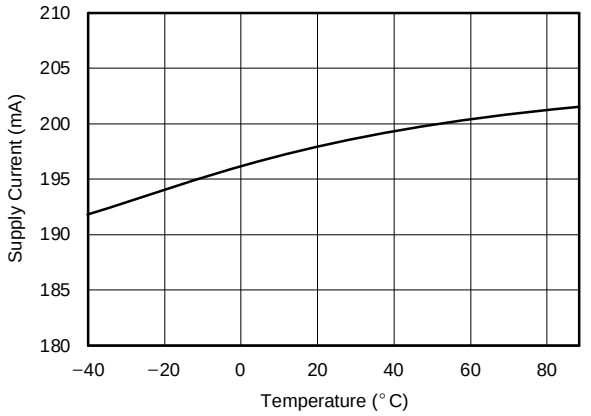
GAIN ERROR vs V_{CNTRL} vs TEMPERATURE



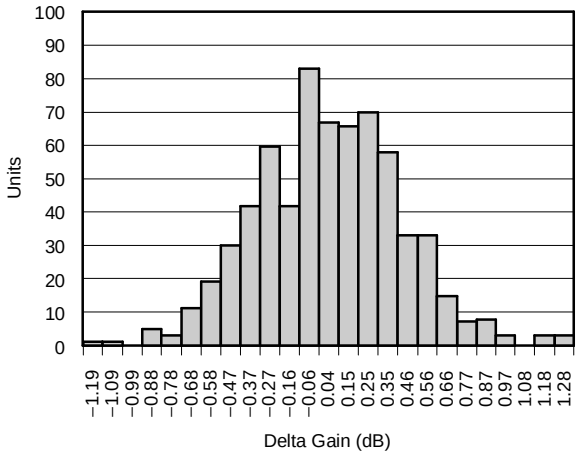
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, f_{IN} = 2MHz, ATN = 01, PG = 00, V_{CNTRL} = 1.7V; differential output, 750mV$_{PP}$, and AV_{DD} = DV_{DD} = 3.0V, unless otherwise noted.

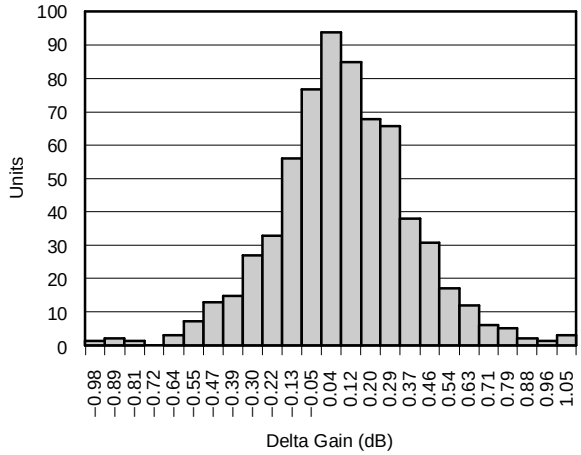
SUPPLY CURRENT (TGC MODE) vs TEMPERATURE



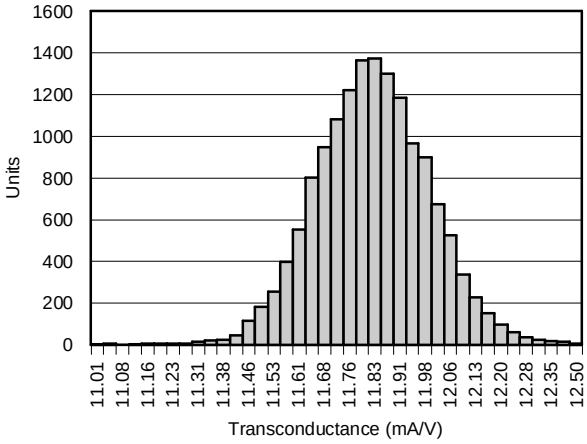
GAIN MATCH (V_{CNTRL} = 0.2V)



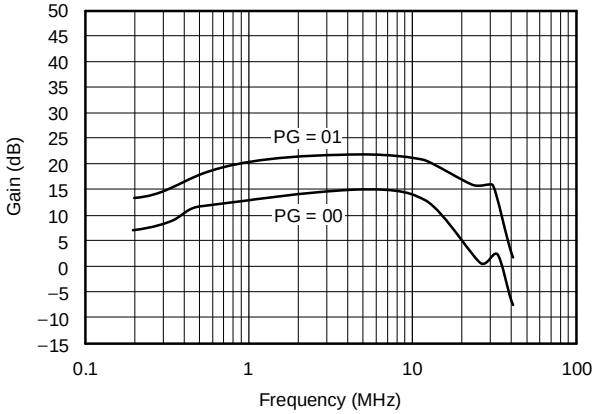
GAIN MATCH (V_{CNTRL} = 1.7V)



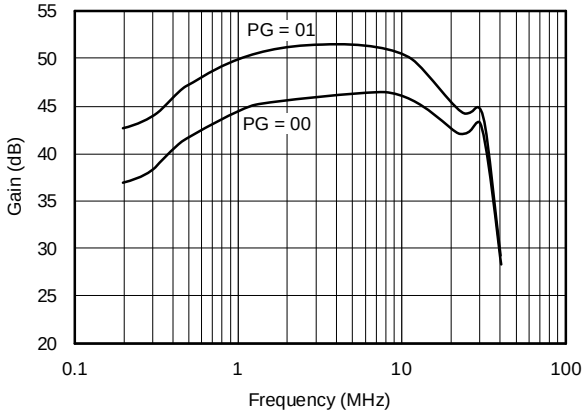
CW ACCURACY



GAIN vs FREQUENCY (ATN = 00, V_{CNTRL} = 0.2V)



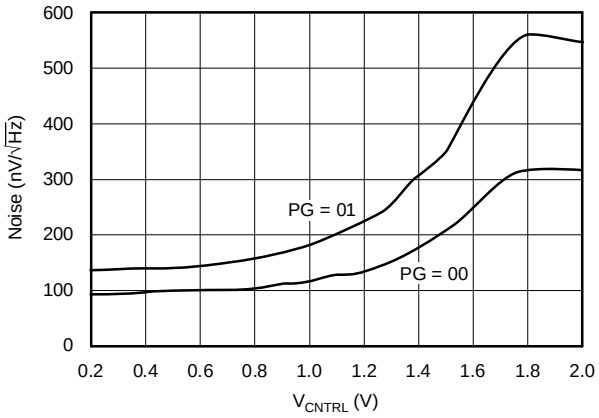
GAIN vs FREQUENCY (ATN = 00, V_{CNTRL} = 1.7V)



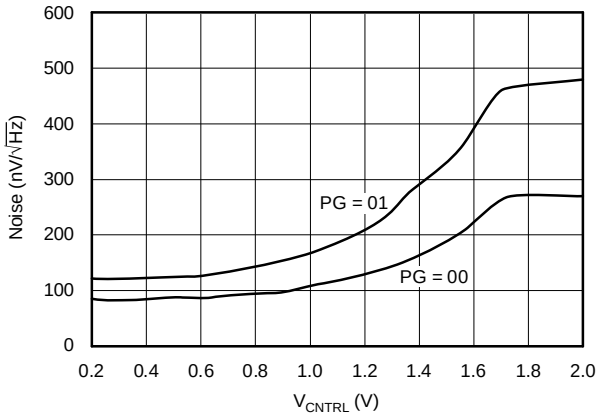
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, f_{IN} = 2MHz, ATN = 01, PG = 00, V_{CNTRL} = 1.7V; differential output, 750mV$_{PP}$, and AV_{DD} = DV_{DD} = 3.0V, unless otherwise noted.

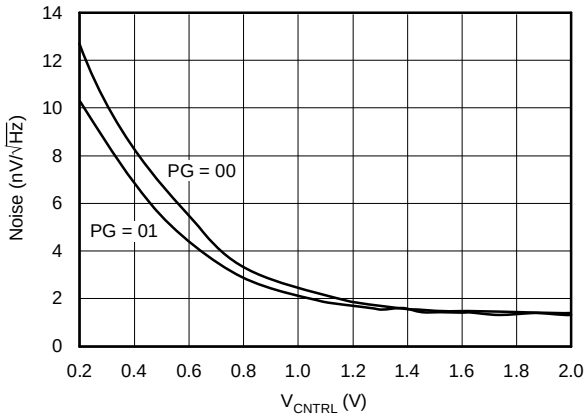
OUTPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 00, f_{IN} = 2MHz)



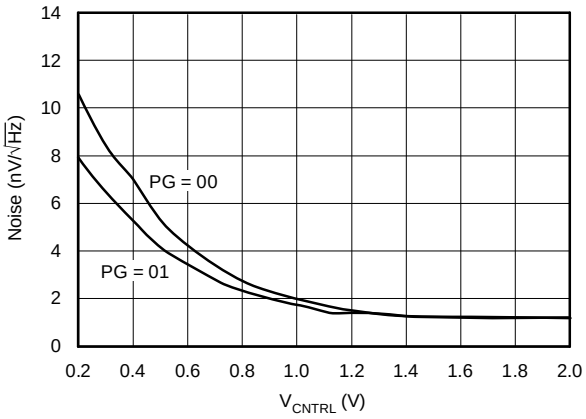
OUTPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 00, f_{IN} = 5MHz)



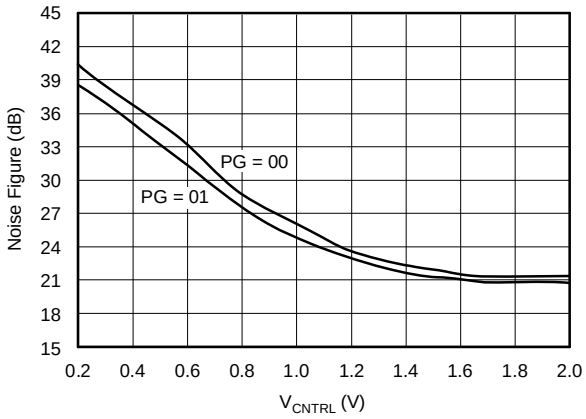
INPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 00, f_{IN} = 2MHz)



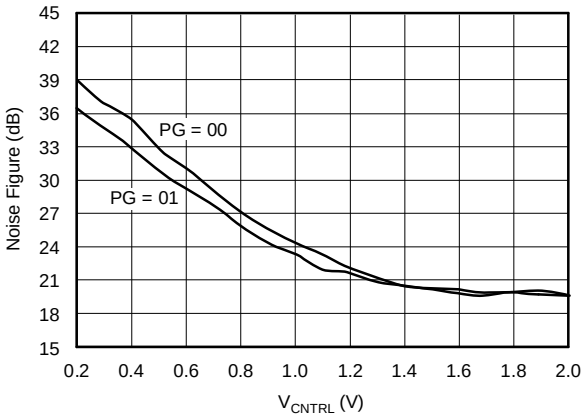
INPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 00, f_{IN} = 5MHz)



NOISE FIGURE vs V_{CNTRL} (ATN = 00, f_{IN} = 2MHz)



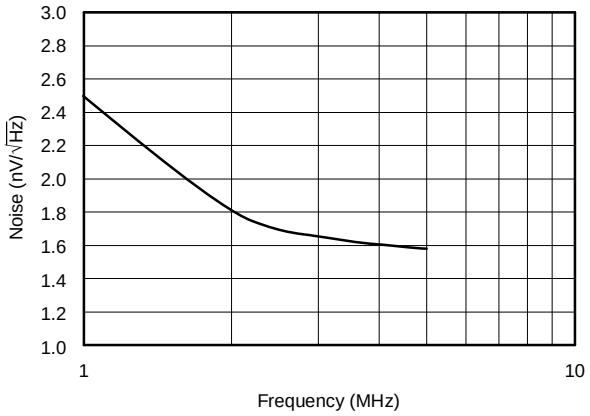
NOISE FIGURE vs V_{CNTRL} (ATN = 00, f_{IN} = 5MHz)



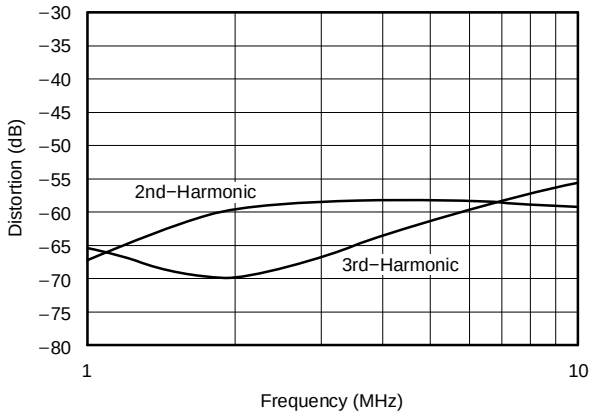
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, f_{IN} = 2MHz, ATN = 01, PG = 00, V_{CNTRL} = 1.7V; differential output, 750mV$_{PP}$, and AV_{DD} = DV_{DD} = 3.0V, unless otherwise noted.

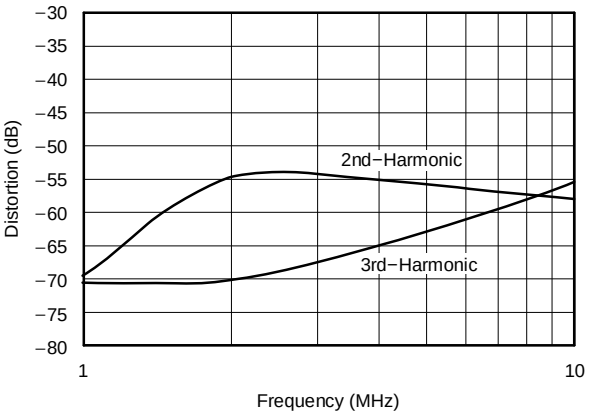
INPUT-REFERRED NOISE (CW Output)



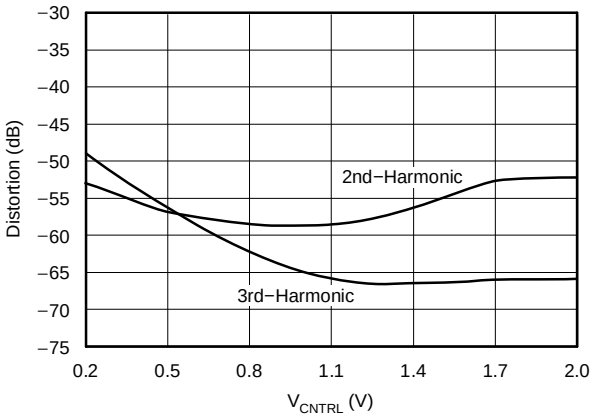
DISTORTION vs FREQUENCY (ATN = 00, PG = 00, V_{CNTRL} = 2.0V)



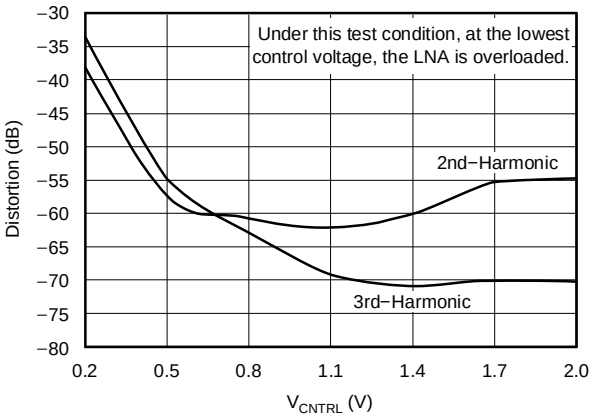
DISTORTION vs FREQUENCY (ATN = 00, PG = 01, V_{CNTL} = 2.0V)



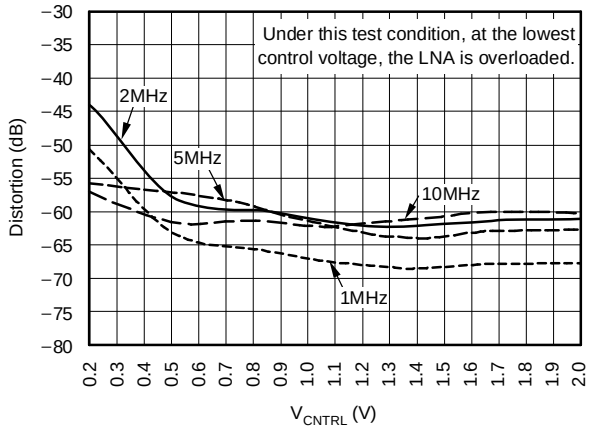
DISTORTION vs V_{CNTRL} (ATN = 00, PG = 01, f_{IN} = 2MHz, 750mV$_{PP}$)



DISTORTION vs V_{CNTRL} (ATN = 01, PG = 01, f_{IN} = 2MHz, 750mV$_{PP}$)



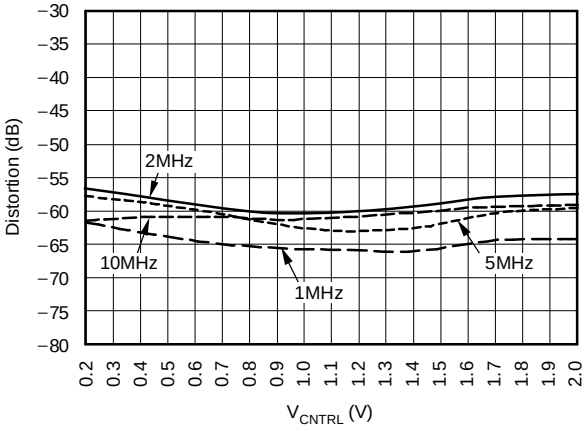
DISTORTION vs V_{CNTRL} (ATN = 00, PG = 00, 500mV$_{PP}$, 2nd-Harmonic)



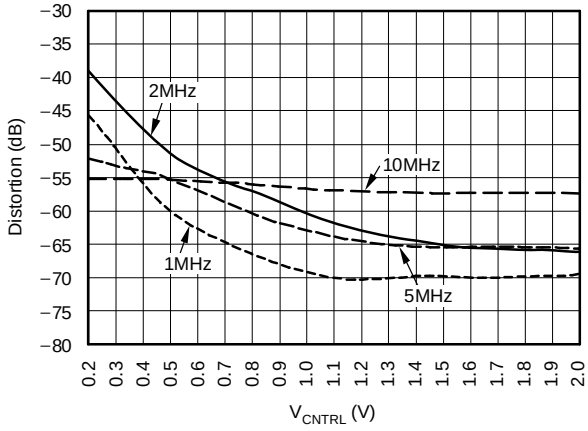
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, f_{IN} = 2MHz, ATN = 01, PG = 00, V_{CNTRL} = 1.7V; differential output, 750mV$_{PP}$, and AV_{DD} = DV_{DD} = 3.0V, unless otherwise noted.

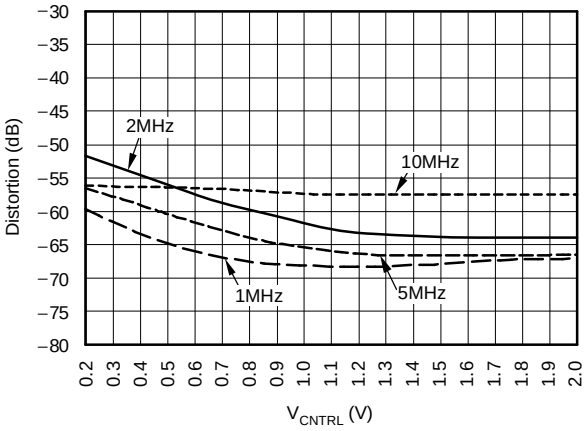
DISTORTION vs V_{CNTRL} (ATN = 00, PG = 01, 500mV$_{PP}$, 2nd-Harmonic)



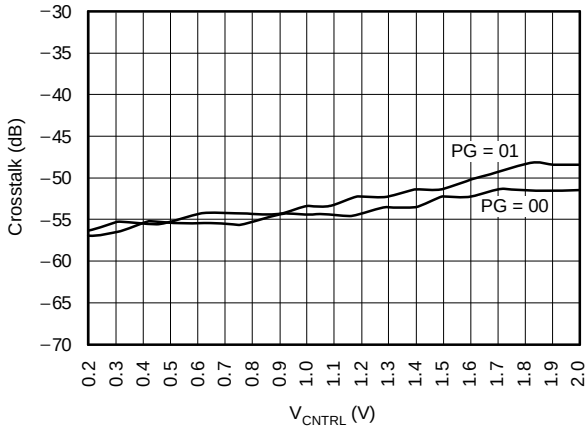
DISTORTION vs V_{CNTRL} (ATN = 00, PG = 00, 500mV$_{PP}$, 3rd-Harmonic)



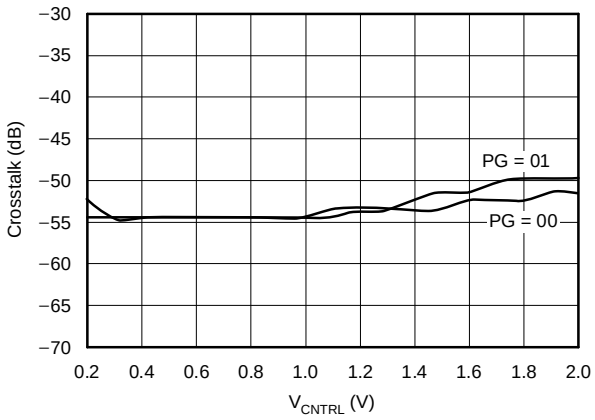
DISTORTION vs V_{CNTRL} (ATN = 00, PG = 01, 500mV$_{PP}$, 3rd-Harmonic)



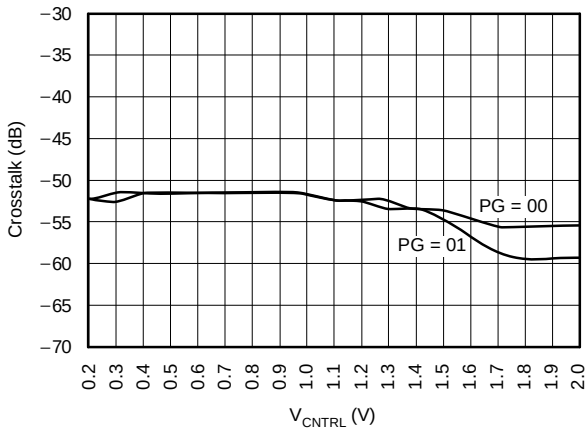
CROSSTALK vs V_{CNTRL} (ATN = 00, f_{IN} = 2MHz, CH4 to CH5)



CROSSTALK vs V_{CNTRL} (ATN = 00, f_{IN} = 5MHz, CH4 to CH5)



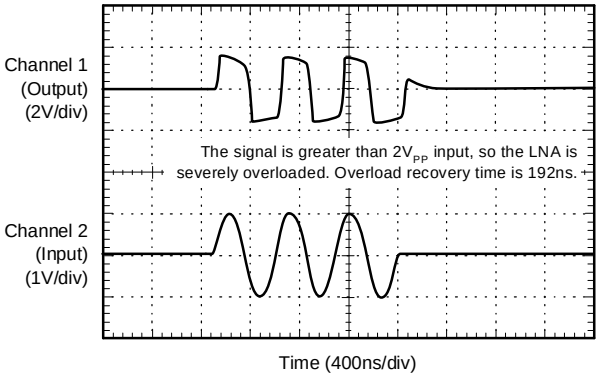
CROSSTALK vs V_{CNTRL} (ATN = 00, f_{IN} = 10MHz, CH4 to CH5)



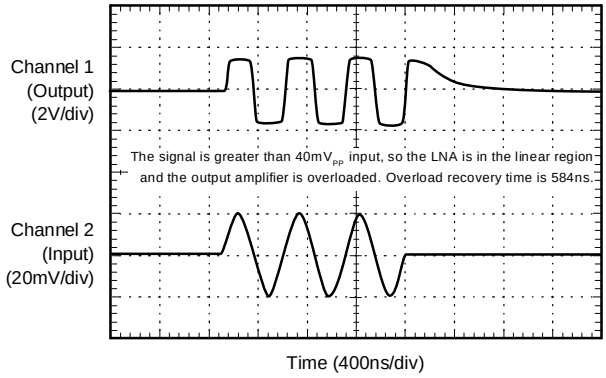
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, f_{IN} = 2MHz, ATN = 01, PG = 00, V_{CNTRL} = 1.7V; differential output, 750mV$_{PP}$, and AV_{DD} = DV_{DD} = 3.0V, unless otherwise noted.

OVERLOAD RECOVERY vs TIME
(ATN = 00, PG = 00, V_{CNTRL} = 1V)



OVERLOAD RECOVERY vs TIME
(ATN = 00, PG = 01, V_{CNTRL} = 2V)



APPLICATION INFORMATION

INPUT CIRCUIT

The input of the VCA8613 integrates several commonly used elements. Prior to reaching the input of the VCA, the receive signal should be coupled with a capacitor of at least 1nF, preferably more. When this AC coupling element is inserted, the LNA input bias point is held to a common-mode value of 2.4V by an integrated 4.5kΩ resistor. This common-mode value will change with temperature and may also vary from chip to chip, but for each chip, it will be held constant. In parallel with this resistor are two back-to-back clipping diodes. These diodes prevent excessive input voltages from passing through to the LNA input, preventing deep saturation effects in the LNA itself.

LOW-NOISE PRE-AMPLIFIER (LNA)

The VCA8613 integrates a low-noise pre-amplifier. Because of the high level of integration in the system, noise performance was traded for power consumption, resulting in an extremely low-power pre-amplifier, with 1.2nV/$\sqrt{Hz}$ noise performance at 5MHz. The LNA is configured as a fixed-gain 24.5dB amplifier. Of this total gain, 6dB results from the single-ended to differential conversion accomplished within the LNA itself. The output of the LNA is limited to approximately $2V_{PP}$ differential swing. This implies a maximum input voltage swing of approximately 110mV to be operating in the linear range at 5MHz. Larger input signals can be accepted by the LNA, but distortion performance will degrade with high-level input signals.

CW DOPPLER PROCESSOR

The VCA8613 integrates many of the elements necessary to allow for the implementation of a simple CW Doppler processing circuit. One circuit that was integrated was a V/I converter following the LNA (see Figure 1). The V/I converter converts the LNA voltage output to a current which is then passed through an 8x10 switch matrix (see Figure 2). Within this switch matrix, any of the eight LNA outputs can be connected to any of ten CW output pins. This is a simple current-summing circuit such that each CW output can represent the sum of any or all the channel currents. The output current for each LNA is equal to the single-ended LNA output voltage swing divided by an internally integrated 700Ω resistor. This resistor value may change ±5% from chip to chip.

The CW output pins need a compliance voltage between 3V to 3.3V. The 3V to 3.3V can be applied through either an inductor (see Figure 3) tied to the 3V to 3.3V source or from the inverting input of an op amp circuit (see Figure 4). The architecture of the V/I converter requires a 2mA to 2.5mA current that is generated by the compliance voltage.

The CW outputs are typically routed to a passive delay line, allowing coherent summing of the signals. After summing, IQ separation and down conversion to base-band precedes a pair of high-resolution, low sample rate ADCs.

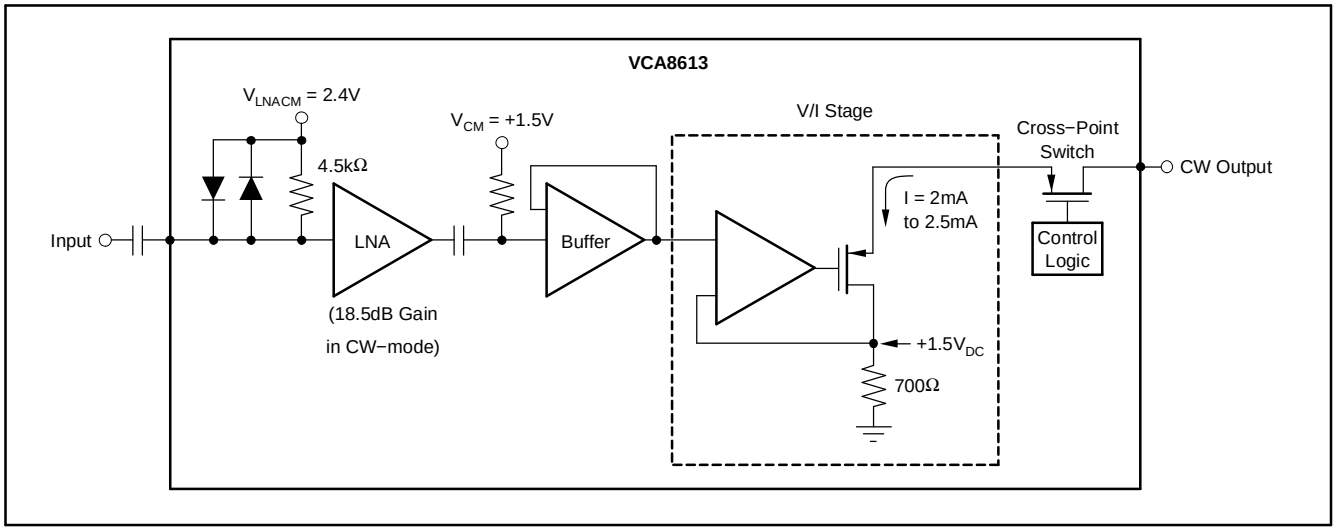


Figure 1. Basic CW Processing Block Diagram

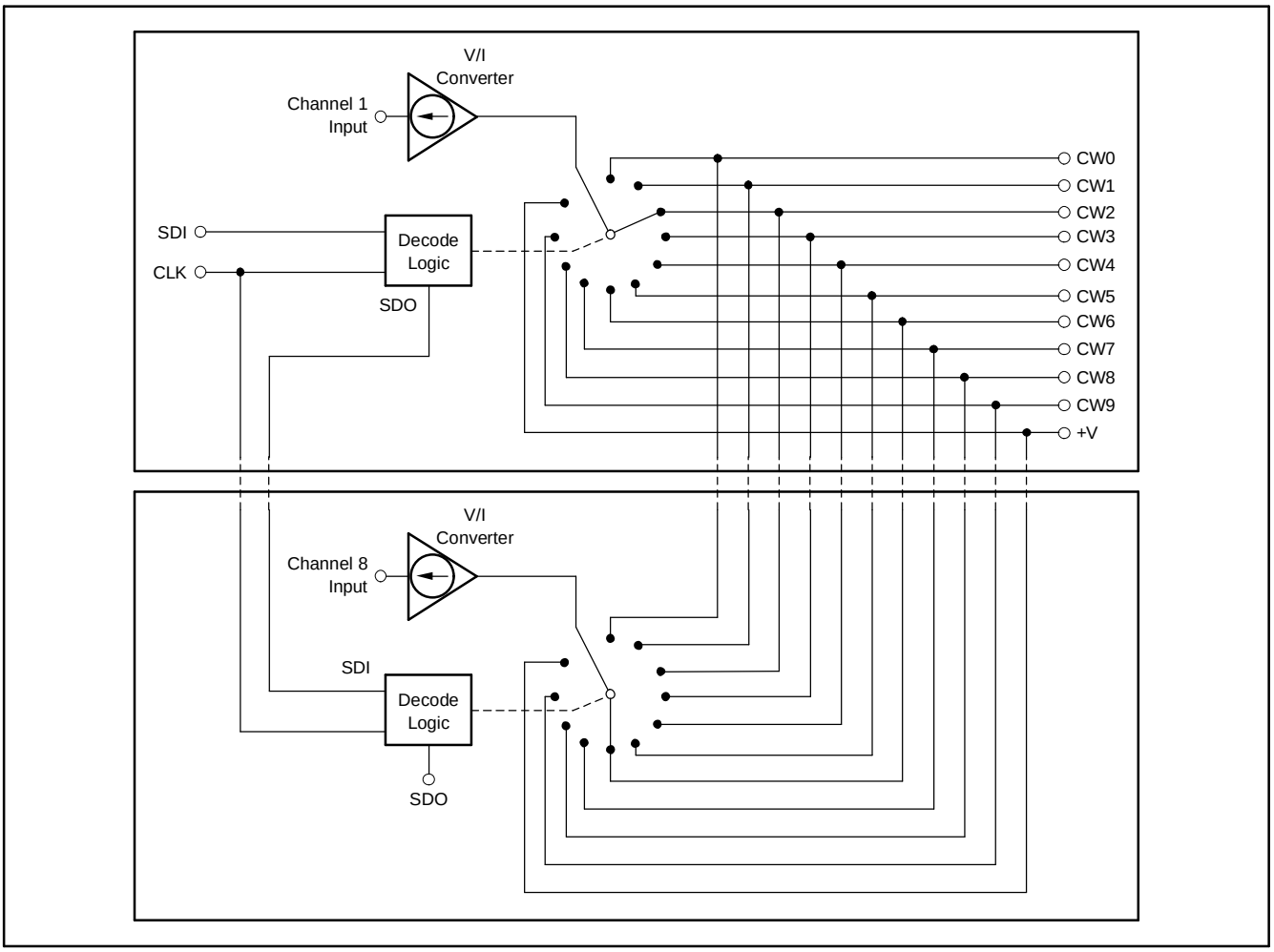


Figure 2. Basic CW Cross-Point Switch Matrix for All Eight Channels

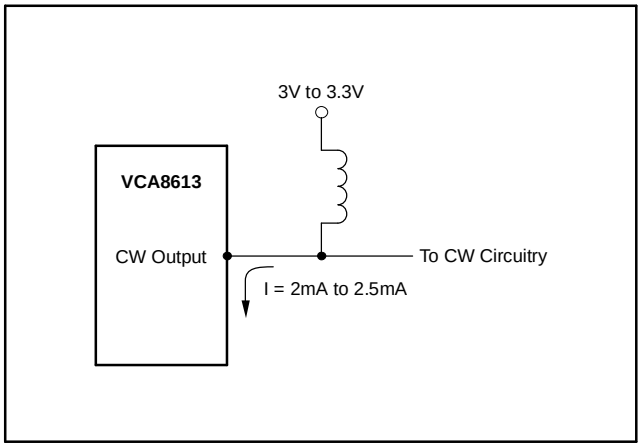


Figure 3. Inductor

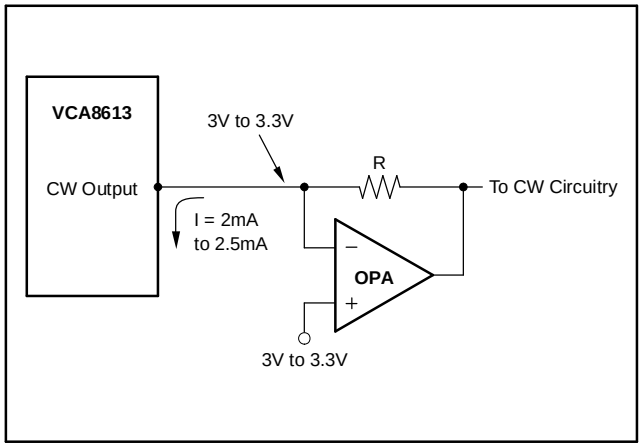


Figure 4. Operational Amplifier

VOLTAGE-CONTROLLED ATTENUATOR (VCA)—DETAIL

The VCA is designed to have a dB-linear attenuation characteristic; that is, the gain loss in dB is constant for each equal increment of the V_{CNTRL} control voltage. Figure 5 shows a block diagram of the VCA. The attenuator is essentially a variable voltage divider consisting of one series input resistor, R_S, and ten identical shunt FETs, placed in parallel and controlled by sequentially-activated clipping amplifiers. Each clipping amplifier can be thought of as a specialized voltage comparator with a soft transfer characteristic and well-controlled output limit voltages. The reference voltages V1 through V10 are equally spaced over the 0V to 2.0V control voltage range. As the control voltage rises through the input range of each clipping amplifier, the amplifier output will rise from 0V (FET completely ON) to V_{CM}– V_T (FET nearly OFF), where V_{CM} is the common source voltage and V_T is the threshold voltage of the FET. As each FET approaches its OFF state and the control voltage continues to rise, the next clipping amplifier/FET combination takes over for the next portion of the piecewise-linear attenuation characteristic. Thus, low control voltages have most of the FETs turned ON, while high control voltages have most turned OFF. Each FET acts to decrease the shunt resistance of the voltage divider formed by R_S and the parallel FET network.

The attenuator is comprised of two sections, with five parallel clipping amplifier/FET combinations in each. Special reference circuitry is provided so that the (V_{CM}– V_T) limit voltage will track temperature and IC process variations, minimizing the effects on the attenuator control characteristic.

In addition to the analog V_{CNTRL} gain setting input, the attenuator architecture provides digitally-programmable adjustment in four steps, via the two attenuation bits. These adjust the maximum achievable gain (corresponding to minimum attenuation in the VCA, with V_{CNTRL} = 2.0V). This function is accomplished by providing multiple FET sub-elements for each of the Q_1 to Q_{10} FET shunt elements (see Figure 6). In the simplified diagram of Figure 5, each shunt FET is shown as two sub-elements, Q_{NA} and Q_{NB}. Selector switches, controlled through the attenuator control bits (ATN [A1:A0]), activate either or both of the sub-element FETs to adjust the maximum R_{ON} and thus achieve the stepped attenuation options.

The input impedance of the VCA section will vary with gain setting, due to the changing resistances of the programmable voltage divider structure. At large attenuation factors (that is, low gain settings), the impedance will approach the series resistor value of approximately 120Ω.

As with the LNA stage, the VCA output is AC-coupled into the PGA. This means that the attenuation-dependent DC common-mode voltage will not propagate into the PGA, and so the PGA DC output level will remain constant.

Finally, note that the V_{CNTRL} input consists of FET gate inputs. This provides very high impedance and ensures that multiple VCA8613 devices may be connected in parallel with no significant loading effects. The nominal voltage range for the V_{CNTRL} input spans from 0V to 2.0V. Overdriving this input (> 3V) does not affect the performance; however, the Absolute Maximum ratings must be observed.

PGA POST-AMPLIFIER

Figure 7 shows a simplified circuit diagram of the PGA block. PGA gain is programmed through the serial port, and can be configured to two different gain settings of 21dB and 26dB, as shown in Table 10. A patented circuit has been implemented in the PGA that allows for fast overload signal recovery.

Table 10. PGA Gain Settings

PG1, PG0	GAIN
0, 0	21
0, 1	26

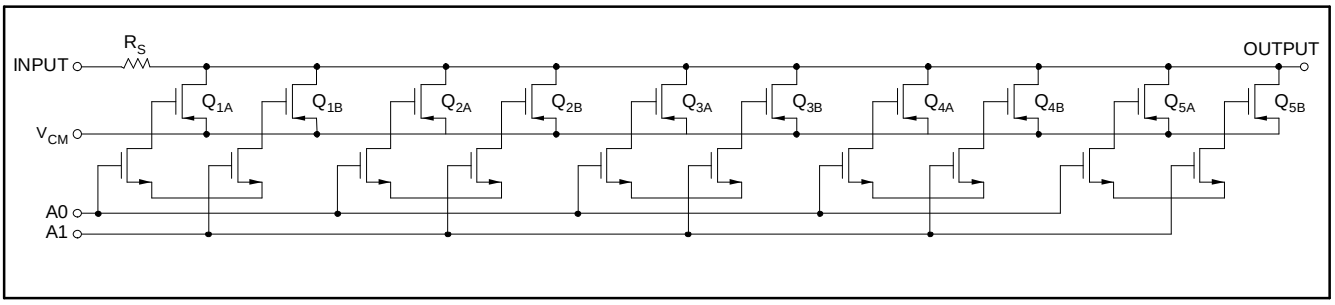


Figure 5. Programmable Attenuator Section

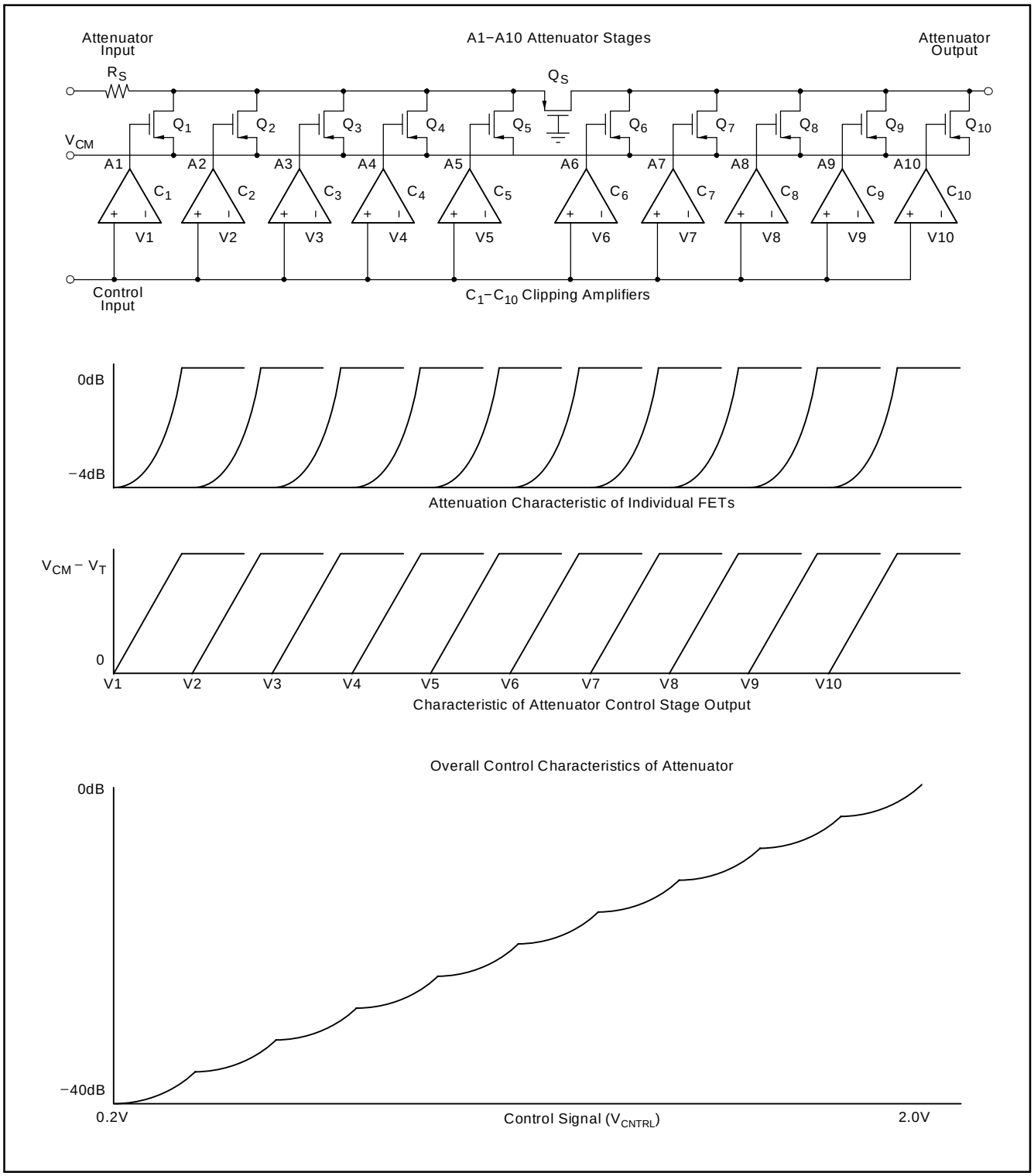


Figure 6. Piecewise Approximation to Logarithmic Control Characteristics

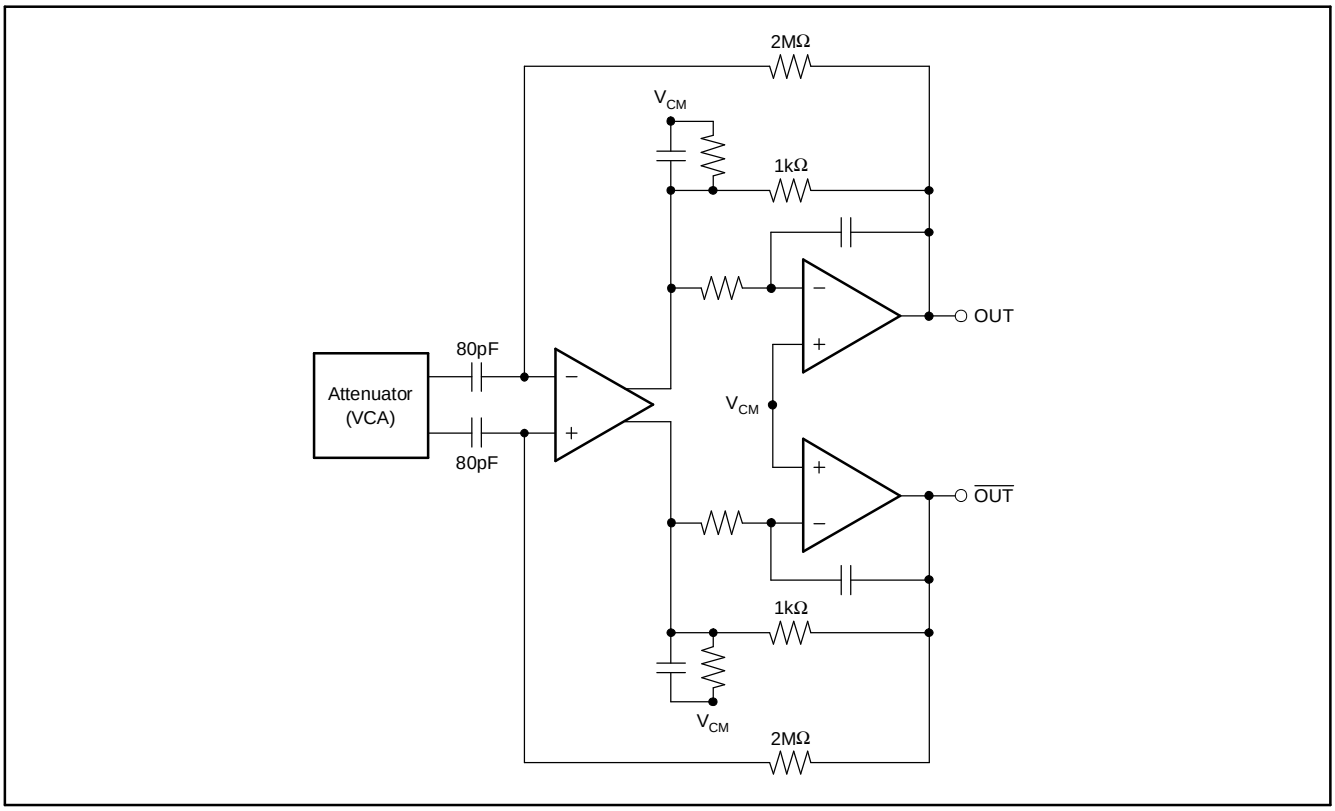


Figure 7. Simplified PGA and Output Filter Circuit

OUTPUT FILTER

The VCA8613 integrates a 2-pole, low-pass Butterworth filter in the output stage, as shown in Figure 7. The cutoff frequency is implemented with passive semiconductor elements and as such, the cutoff frequency will not be precise. Table 11 shows the cutoff frequency for the different PGA settings.

The variation shown in Table 11 reflects deviations as measured from chip to chip and over the specified temperature range.

Table 11. Cutoff Frequency for PGA Settings

PG1, PG0	BANDWIDTH
0, 0	13MHz to 14MHz
0, 1	11MHz to 12MHz

SERIAL INTERFACE

The serial interface of the VCA8613 allows flexibility in the use of the part. The following parameters are set from the serial control registers:

- Mode
  - TGC mode
  - CW mode
- Attenuation range
- PGA gain
- Power-down (this is the default state in which the VCA8613 initializes)
- CW output selection for each input channel

The serial interface uses an SPI style of interface format. The Input Register Bit Maps (see page 5) show the functionality of each control register.

LAYOUT CONSIDERATIONS

The VCA8613 is a multi-channel amplifier capable of high gains that has integrated digital controls. By connecting all of the grounds (including the digital grounds) to the analog ground, noise performance will help to be maintained. The analog ground should be a solid plane.

Power-supply decoupling and decoupling of the control voltage (V_{CNTRL}) pin are essential in order to ensure that the noise performance be maintained. For further help in determining basic values, please refer to Figure 8.

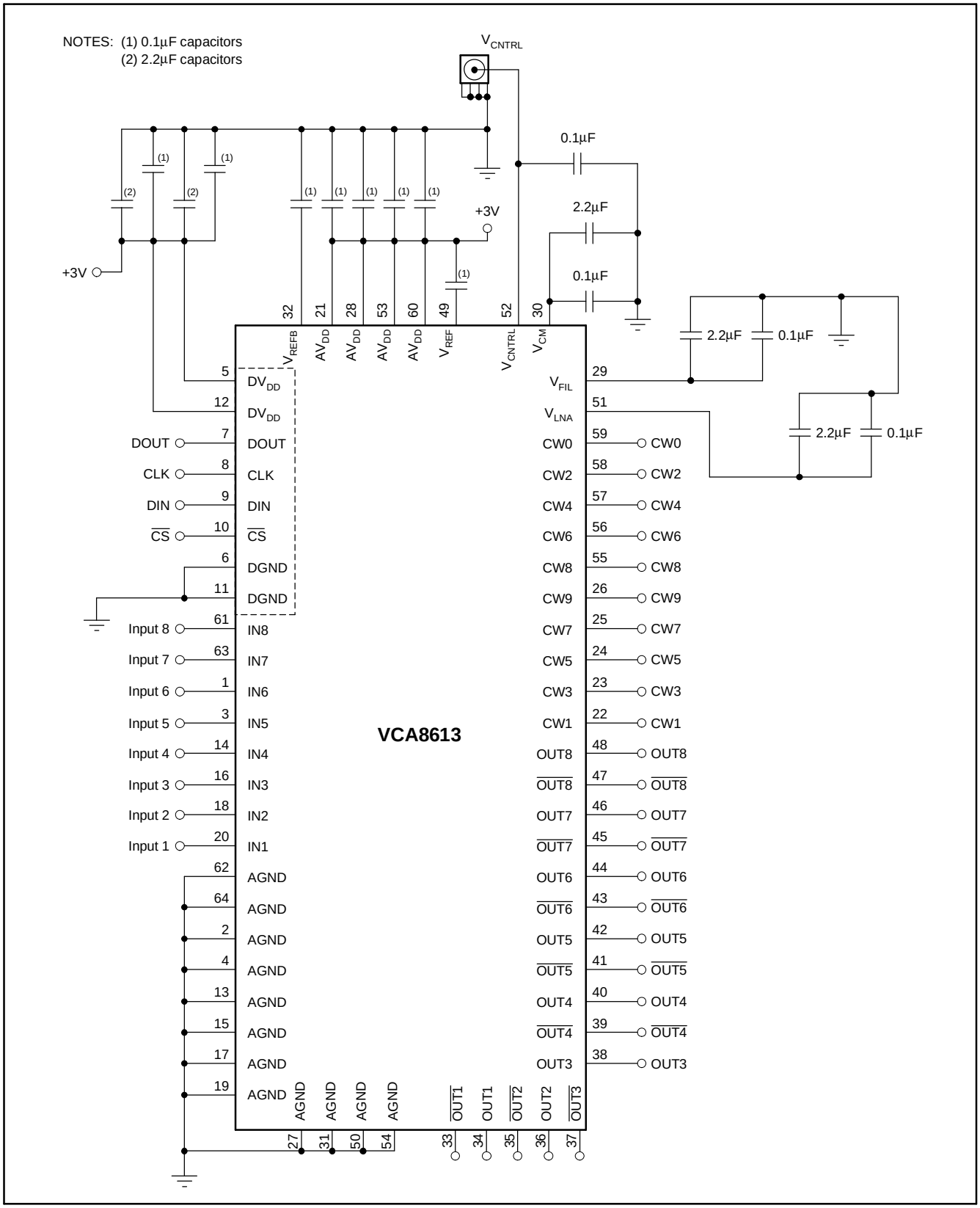


Figure 8. Basic Connection Diagram

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from E Revision (May 2005) to F Revision	Page
• Changed to 14MHz from 12MHz	3
• Changed line position with 3rd-harmonic distortion. Added condition of V_{OUT} = 500mV_{pp}. Changed typ and max values to -55dBc and -45dBc, respectively.	3
• Changed line position with 2nd-harmonic distortion. Added condition of V_{OUT} = 500mV_{pp}. Changed typ and max values to -50dBc and -40dBc, respectively.	3
• Changed Specified Operating Range to Supply Voltage	3
• Changed paragraph discussing attenuator architecture, digitally-programmable adjustments and maximum achievable gain	17

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from D Revision (April 2005) to E Revision	Page
• Changed 8 to 5 bytes at a time. Added 'Each byte consists of 8 bits' at end of first bullet.	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
VCA8613YT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples

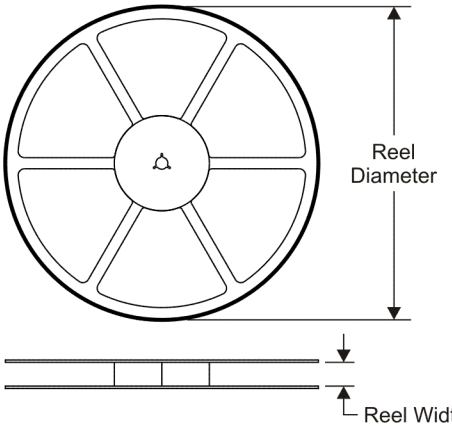
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

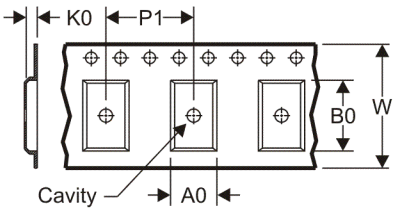
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

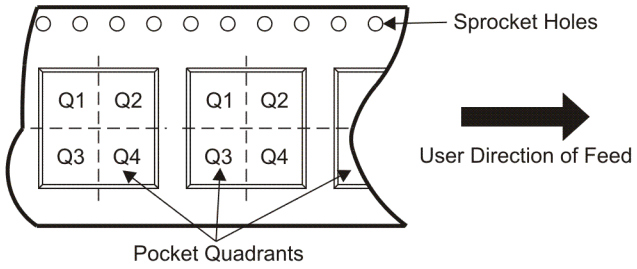


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

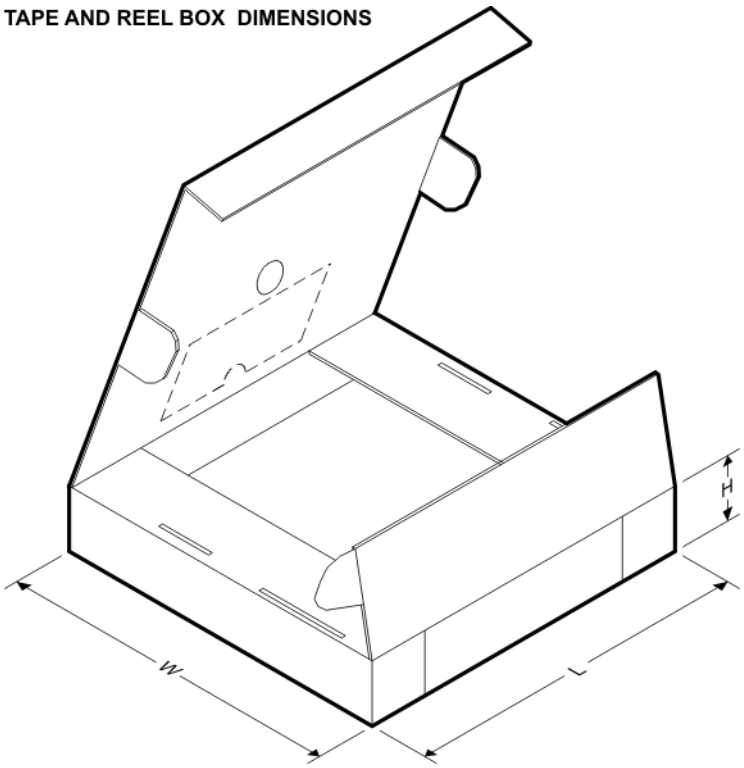
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VCA8613YT	TQFP	PAG	64	250	330.0	24.8	13.0	13.0	1.5	16.0	24.0	Q2

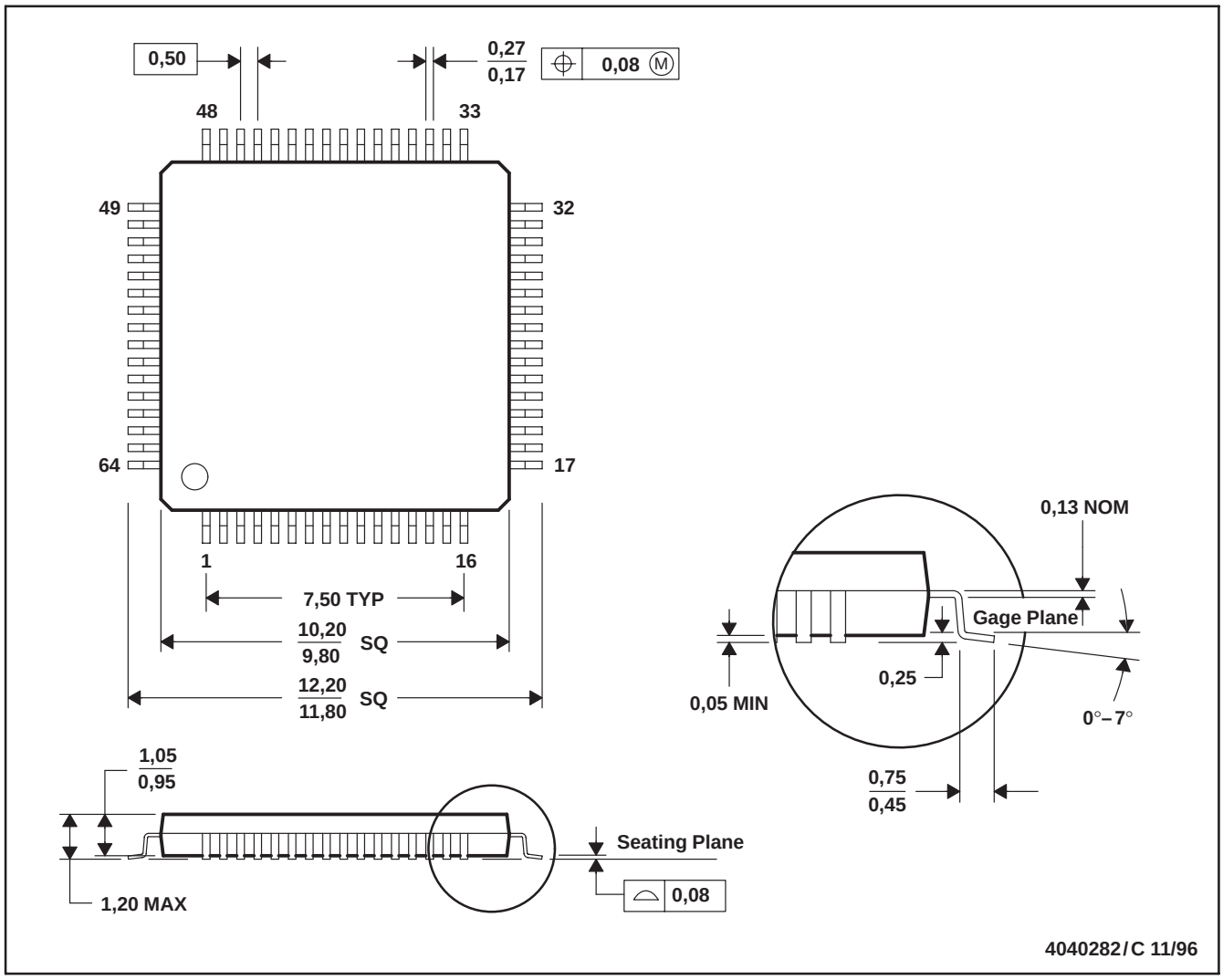
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

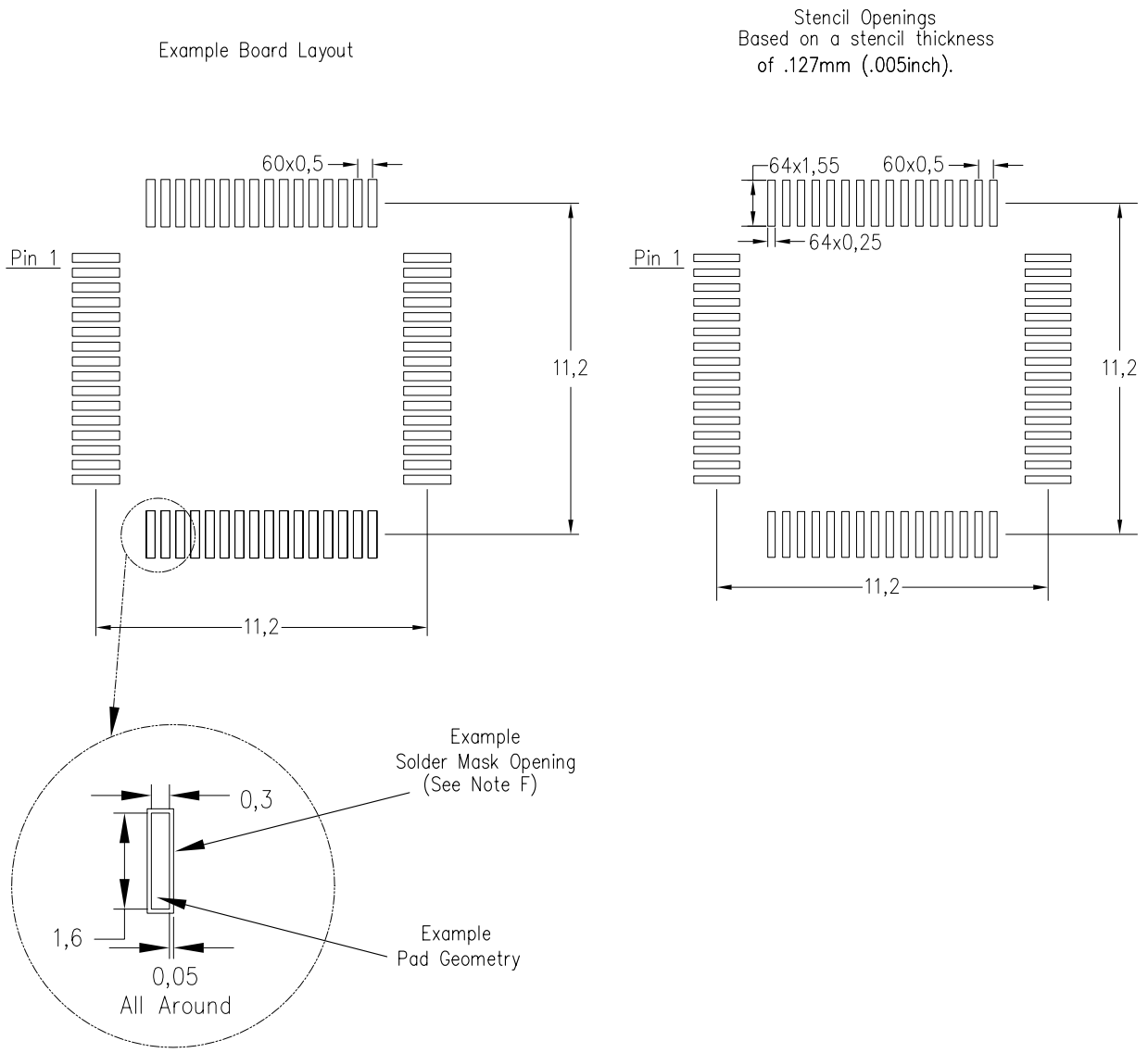
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VCA8613YT	TQFP	PAG	64	250	346.0	346.0	41.0

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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