FOUR-CHANNEL IMAGE SENSOR ANALOG FRONT-END

Check for Samples: VSP7502

FEATURES

- **Four-Channel Signal Paths**
- **Sample/Hold (S/H) Input**
- **Maximum Data Throughput: 50 MHz**
- **16-Bit A/D Conversion:**
  - **No Missing Codes Ensured**
- **Programmable Gain Amplifier (PGA):**
  - **Analog Front Gain: 0 dB to +15.4 dB**
  - **Digital Gain: 0 dB to +32 dB (0.032-dB Step)**
- **Wide Range of Input Common Voltage**
- **Operation Voltage and Power Consumption:**
  - **Voltage: 1.8 V and 3.3 V**
- **Power: 480 mW**
  (at VDD = 1.8 V, f_{MCLK} = 50 MHz)

DESCRIPTION

The VSP7502 is a four-channel analog front-end (AFE) for imaging signals. This device includes a programmable gain amplifier (PGA), analog-to-digital converter (ADC), input clamp, optical black (OB) level clamp loop, serial interface, and adjustable sampling timing control. The VSP7502 is offered in a BGA-159 package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VSP7502	BGA-159	ZWV	–25°C to +85°C	VSP7502ZWV	VSP7502ZWV	Tray, 360
					VSP7502ZWVR	Tape and Reel, 3000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	VSP7502	UNIT
Supply voltage (AVDD2, DLLVDD2, REFVDD, DRVDD2, DVDD2, DVDD2_SPI)	+2.4	V
Supply voltage (AVDD3, RGVDD3, H1VDD3, H2VDD3, DVDD3, DVDD3_SPI)	+4.0	V
Supply voltage differences (among power-supply pins)	±0.1	V
Ground voltage differences (among GND pins)	±0.1	V
Digital input voltage (ATPG, MN_DM, MN_KBLK, MN_OB, MN_PBLK)	–0.15 to (DVDD2 + 0.15)	V
Digital input voltage (HD, VD, MCLK, RST, SCLK, SCS, SDI)	–0.3 to (DVDD3 + 0.3)	V
Analog input voltage (IN_W, IN_X, IN_Y, IN_Z, IP_W, IP_X, IP_Y, IP_Z)	–0.3 to (AVDD3 + 0.3)	V
Input current (all pins except supplies)	±10	mA
Ambient temperature under bias	–40 to +125	°C
Storage temperature	–55 to +150	°C
Junction temperature	+150	°C
Package temperature (reflow, peak)	+260	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted

		MIN	TYP	MAX	UNIT
Analog supply voltage: AVDD2, DLLVDD2, REFVDD, LVAVDD, LVDLLVDD		1.65	1.8	1.95	V
Analog supply voltage: AVDD3		2.7	3.3	3.6	V
Digital supply voltage: DVDD2, DVDD2_SPI, LVDVDD, DRVDD2		1.65	1.8	1.95	V
Digital supply voltage: RGVDD3, H1VDD3, H2VDD3, DVDD3, DVDD3_SPI		2.7	3.3	3.6	V
Analog input voltage, full scale (0 dB)			1.0		V_{PP}
Digital input logic family			CMOS		
Digital input clock frequency	MCLK			50	MHz
	SCLK			25	MHz
Digital output load capacitance				10	pF
Operating free-air temperature, T_A		–25		+85	°C

ELECTRICAL CHARACTERISTICS(1)

All specifications at T_A = +25°C, all power-supply voltages = +3.0 V, and conversion rate = 36 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP2560PT MIN	VSP2560PT TYP	VSP2560PT MAX	UNIT
POWER SUPPLY						
Analog supply voltage	AVDD2		1.65	1.8	1.95	V
	REFVDD					
	DLLVDD2					
	LVAVDD					
	LVDLLVDD					
	AVDD3		2.7	3.0	3.6	V
Digital supply voltage	DVDD2		1.65	1.8	1.95	V
	DVDD2_SPI					
	DRVDD2					
	DVDD2_SPI					
	LVDVDD					
	DRVDD2					
	DVDD3		2.7	3.0	3.6	V
	DVDD3_SPI					
H-TG supply voltage	H1VDD3		2.7	3.0	3.6	V
	RGVDD3					
Power consumption		PT_SHAMP = 0		460		mW
		PT_SHAMP = 1		480		mW
		PT_SHAMP = 2		500		mW
		PT_SHAMP = 3		520		mW
		Standby mode		30		mW
		Sleep mode		0.7		mW
RESOLUTION						
Resolution				16		Bits
THROUGHPUT RATE						
Maximum data throughput rate				50	56	MHz
DIGITAL INPUTS						
Logic family				CMOS		
V_T	Input voltage (CMOS input)	Threshold voltage for MCLK		DVDD3/2		V
I_{IH}	Input current	Logic high, V_{IN} = +3.0 V			±20	µA
I_{IL}		Logic low, V_{IN} = 0 V			±20	µA
MCLK clock duty cycle			40	50	60	%
Input capacitance				5		pF
DIGITAL OUTPUT (CMOS Buffer)						
V_{OH}	Output voltage	Logic high, I_{OH} = –2 mA	DVDD × 0.8			V
V_{OL}		Logic low, I_{OL} = 2 mA			DVDD × 0.22	V

(1) All values listed are preliminary. Final values to be determined after evaluation.

ELECTRICAL CHARACTERISTICS [1] (continued)

All specifications at T_A = +25°C, all power-supply voltages = +3.0 V, and conversion rate = 36 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP2560PT MIN	VSP2560PT TYP	VSP2560PT MAX	UNIT
ANALOG INPUT						
Input signal level for full-scale out		Gain = 0 dB		1		V_{PP}
Input voltage	for INP pin				AVSS3	V
	for INN pin		AVSS3			V
Input capacitance			4.8	6.0	7.2	pF
Input limit			AVSS3 – 0.3		AVSS + 0.3	V
REFERENCE						
Positive reference voltage				1.25		V
Negative reference voltage				0.75		V
TRANSFER CHARACTERISTICS						
DNL	Differential nonlinearity			±1		LSB
INL	Integral nonlinearity	V_{IN} = 100 mV ramp		±8		LSB
		V_{IN} = 900 mV ramp		±32		LSB
	Integral nonlinearity channel mismatch	Among each channel (analog gain = 0 dB)				LSB
No missing codes				Ensured		
Step response settling time		Full-scale step input		1		Pixel
Overload recovery time		Step input from 1.8 V to 0 V		2		Pixels
Data latency					11	Clocks
Signal-to-noise ratio [2]		Grounded input capacitor		74	72	dB
Sensor offset correction range			–200		200	mV
Channel isolation		Among each channel (analog gain = 0 dB)		74		dB
PROGRAMMABLE GAIN (Analog)						
Analog gain programmable range			0		+15.40	dB
Analog gain setting		00 0000b		0		dB
		00 1100b		3.12		dB
		01 0011b		5.23		dB
		01 1010b		7.25		dB
		10 0010b		9.38		dB
		10 1010b		11.56		dB
		11 0001b		13.65		dB
		11 0111b		15.40		dB
Analog gain error		For setting gain		0.5		dB
PROGRAMMABLE GAIN (Digital)						
Digital gain programmable range			0		32	dB
Digital gain programmable step				0.032		dB
OPTICAL BLACK CLAMP (OBCLP) LOOP						
Optical black clamp level		Programmable range of clamp level	1024	2304	16383	LSB
		OB level program step		1		LSB
PRIMARY ANALOG OB CLAMP LOOP						
OB DAC resolution				7		Bits
OB DAC full-scale voltage		Negative side		–400		mV
		Positive side		+450		mV

(2) SNR = 20 log (full-scale voltage/rms noise).

ELECTRICAL CHARACTERISTICS [1] (continued)

All specifications at T_A = +25°C, all power-supply voltages = +3.0 V, and conversion rate = 36 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP2560PT			UNIT
			MIN	TYP	MAX	
LVDS BUFFER (D0, D1, CKS)						
R_L	Differential load impedance		90	100	110	Ω
$\|V_{OD}\|$	Differential steady-state output voltage magnitude	R_L = 100 Ω	90		110	mV
$\Delta\|V_{OD}\|$	Change in the steady-state differential output voltage magnitude between opposite binary states	R_L = 100 Ω			15	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	COM_SEL = 0 (0.9 V mode)	0.7		1.1	V
		COM_SEL = 1 (1.2 V mode)	1.0		1.4	V
$V_{OC(PP)}$	Peak-to-peak common-mode output			20	50	mV
I_{OS}	Short-circuit output current	Output = GND	–6		6	mA
I_{OZ}	High-impedance state output current	V_O = 0 V to VCC	–10		10	µA
TEMPERATURE RANGE						
Operating temperature			–25		+85	°C

TIMING CHARACTERISTICS

SERIAL INTERFACE TIMING SPECIFICATION (REGISTER AREA)

The serial interface command is composed of an 8-bit address, 14-bit data, and 2-bit dummy data. The 8-bit address should be sent primarily as LSB first; the following 14-bit data should also be sent as LSB first. The 2-bit dummy data is added after the 14-bit data. Figure 1 shows the standard write mode for serial interface timing.

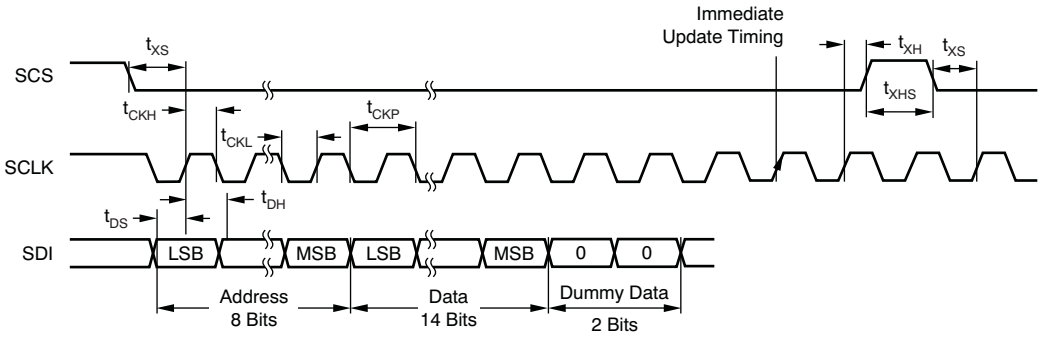
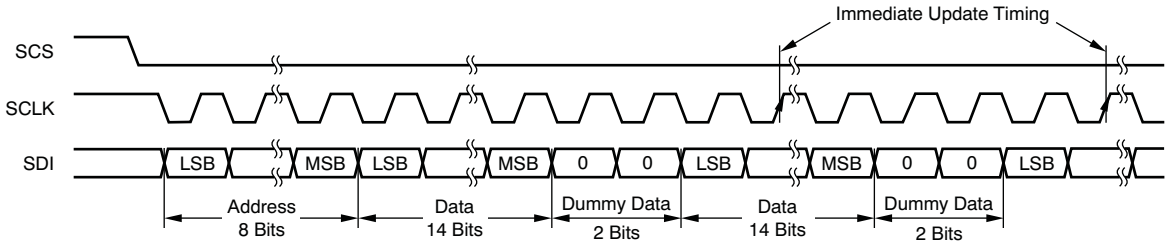


Figure 1. Standard Write Mode

Table 1. Timing Characteristics for Figure 1

PARAMETER		MIN	TYP	MAX	UNIT
t_{CKP}	Clock period	40.0			ns
t_{CKH}	Clock high pulse width	20.0			ns
t_{CKL}	Clock low pulse width	20.0			ns
t_{DS}	Data setup time	2.5			ns
t_{DH}	Data hold time	2.0			ns
t_{XS}	S_{LOAD} to SCLK setup time	2.5			ns
t_{XH}	SCLK to $\overline{CS}$ hold time	2.0			ns
t_{XHS}	$\overline{CS}$ width	40			ns

The VSP7502 also supports a continuous write mode, as shown in Figure 2.



NOTE: Continuous write mode is supported from address 1 to address 255; this mode is not supported in address 0.

Figure 2. Continuous Write Mode (Except Address 0)

The VSP7502 has two types of update timing (immediate and VD update) that are register dependent. The VD update timing is described in Figure 3.

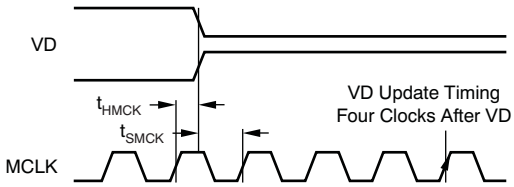


Figure 3. VD Update

Table 2. Timing Characteristics for Figure 3

PARAMETER		MIN	TYP	MAX	UNIT
t_{SMCK}	Setup time for MCLK to VD	6.0			ns
t_{HMCK}	Hold time for MCLK to VD	1.0			ns

POWER-ON/POWER-OFF SEQUENCE TIMING

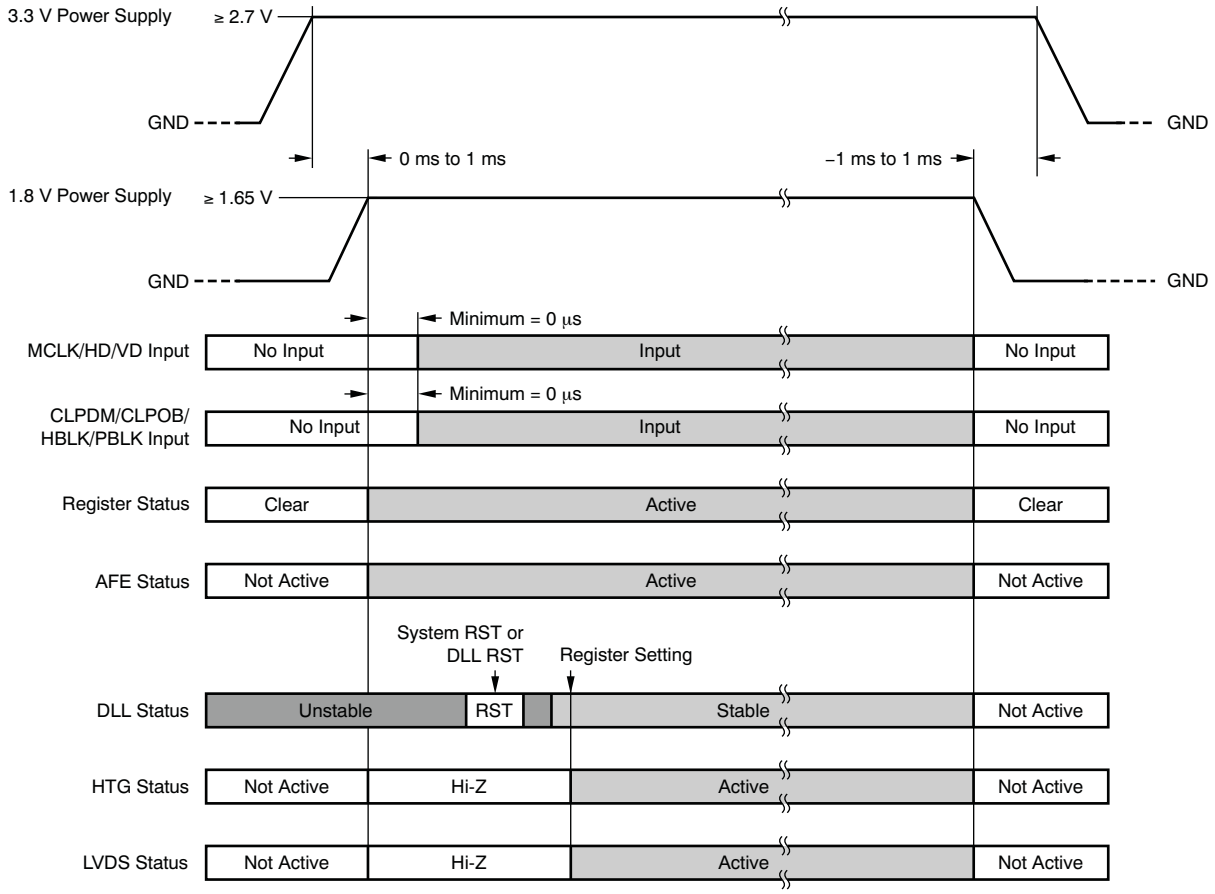


Figure 4. Power-On/Power-Off Reset Sequence

Table 3. Reset Standby Function

MODE	REGISTER	CDS	ADC	DLL	HTG	LVDS
Reset	Clear	Not active	Not active	Not active	Not active	High-Z
Standby	Active	Not active	Not active	Active	Low	High-Z
Sleep	Active(1)	Not active	Not active	Not active	Low	High-Z

(1) Enabled only by address 0.

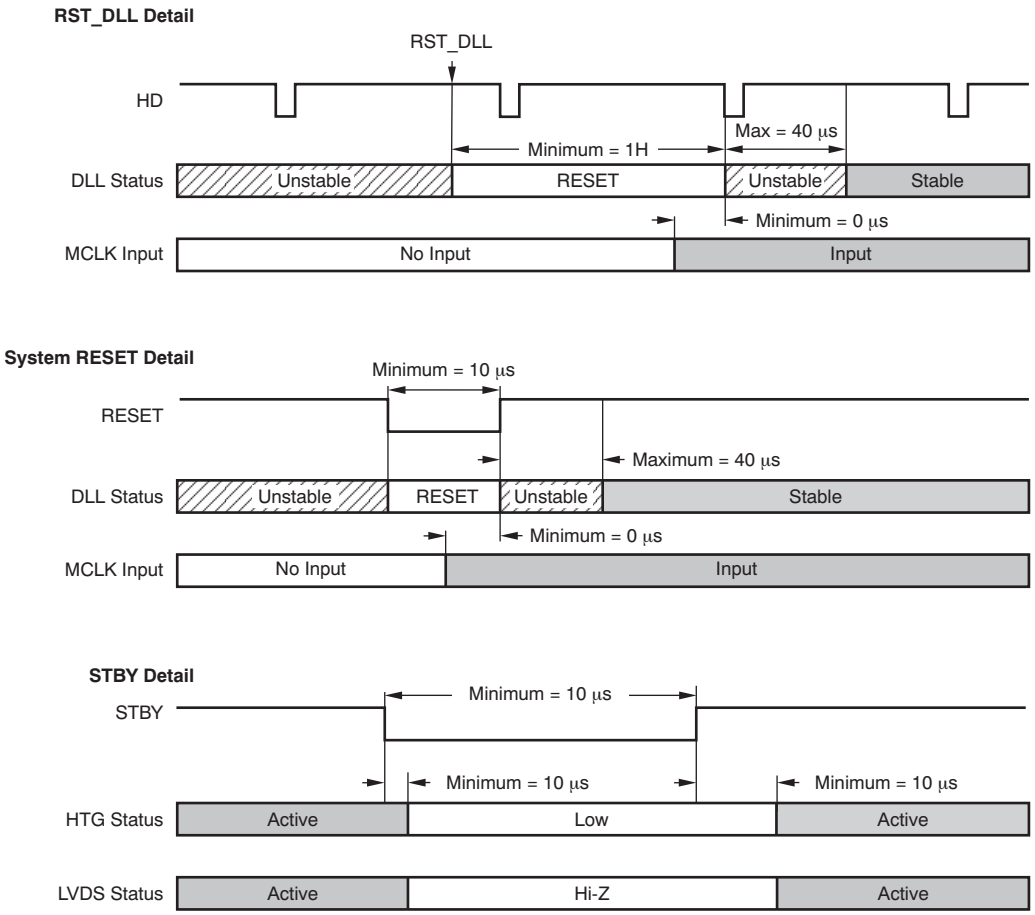


Figure 5. Detailed Power-On/Power-Off Timing

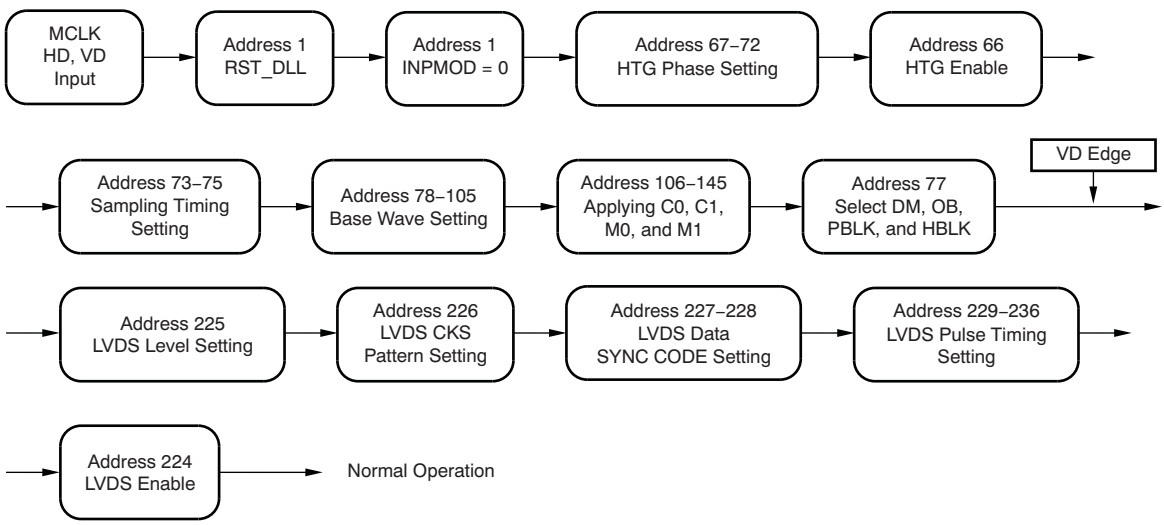


Figure 6. Register Setting Procedure

AFE BLOCK, S/H TIMING

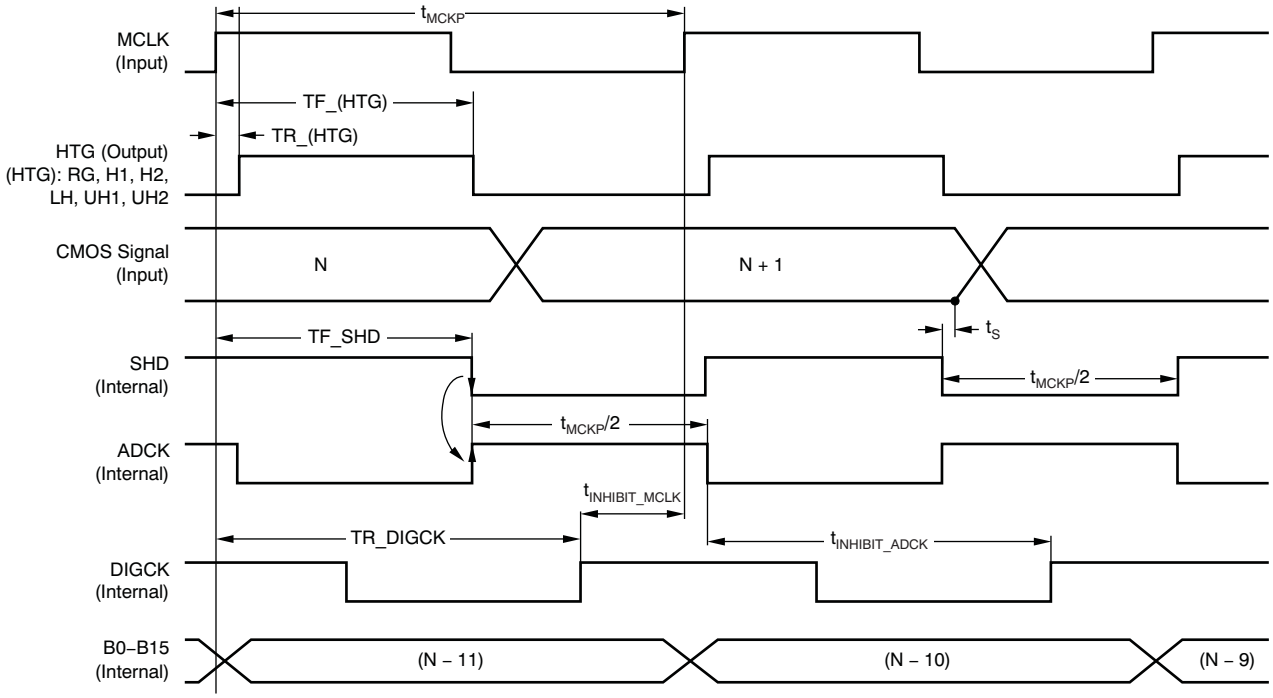


Figure 7. S/H Mode Timing Diagram for AFE Block

Table 4. S/H Mode Timing Characteristics for Figure 7

PARAMETER		MIN	TYP	MAX	UNIT
t_{MCKP}	Master clock period	20			ns
t_{WMCK}	MCLK clock duty	40	50	60	%
t_S	Sampling delay		2		ns
$t_{INHIBIT\_ADCK}$	Inhibit clock period from ADCK falling edge(1) to DIGCK rising edge		7		ns
$t_{INHIBIT\_MCLK}$	Inhibit clock period from DIGCK rising edge to MCLK rising edge		3		ns
t_{R_SHD}					
t_{F_SHD}					
t_{R_DIGCK}					

(1) ADCK falling edge = TF_SHD – t_{MCKP}/2.

Table 5. DLL-Generated Pulse Default Settings

ADDRESS	BITS	REGISTER NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION
67	5:0	TF_RG	RG fall tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 00 1101b
	13:8	TR_RG	RG rise tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 00 0001b
68	5:0	TF_H1	H1 fall tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 01 1111b
	13:8	TR_H1	H1 rise tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 00 0000b
69	5:0	TF_H2	H2 fall tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 00 00001b
	13:8	TR_H2	H2 rise tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 01 1111b
73	5:0	TF_SHD	SHD fall tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 10 0001b
	13:8	TR_SHD	SHD rise tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 11 1101b
74	5:0	TF_SHP	SHP fall tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 00 0100b
	13:8	TR_SHP	SHP rise tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 01 1110b
75	13:8	TR_DIGCK	DIGCK rise tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 11 0001b

LVDS BLOCK TIMING

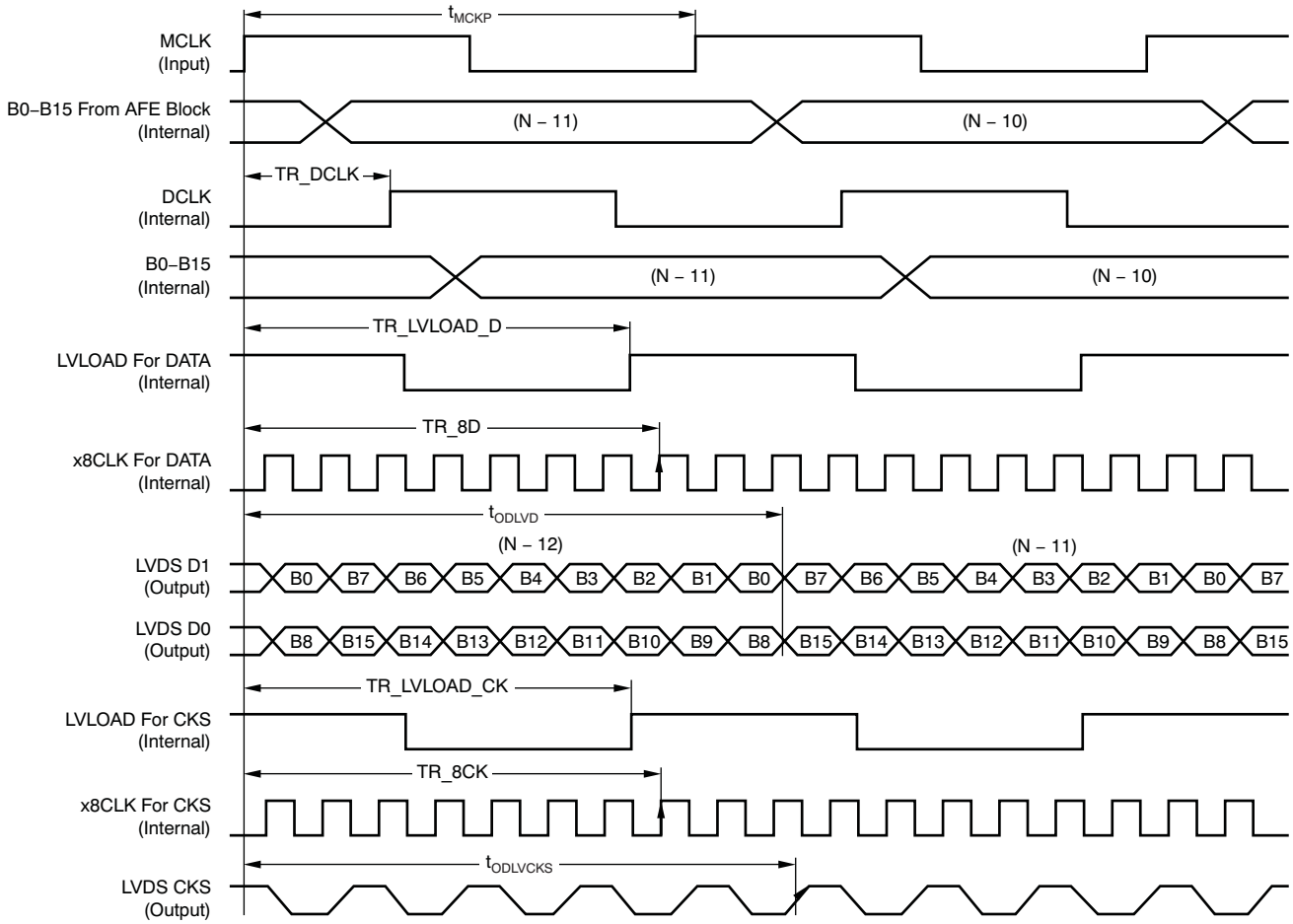


Figure 8. Timing Diagram for LVDS Block

Table 6. Timing Characteristics for Figure 8

PARAMETER		MIN	TYP	MAX	UNIT
t_{MCKP}	MCLK clock period	20			ns
t_{WMCK}	MCLK clock duty	40	50	60	%
t_{ODLVD}	LVDS data output delay		0		ns
$t_{ODLVCKS}$	LVDS data output delay		0		ns

Table 7. DLL-Generated Pulse Default Settings

ADDRESS	BITS	REGISTER NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION
229	5:0	TR_DCLK	DCLK rising edge (50% duty cycle)	Tap = D[5:0] × t_{MCKP}/64 Default = 01 0000b
230	5:0	TR_LVLOAD_CK	LVLOAD rising edge for CKSOUT (50% duty cycle)	Tap = D[5:0] × t_{MCKP}/64 Default = 11 0000b
231	5:0	TR_8CK	CLKx8 rising edge for CKSOUT (edge0)	Tap = D[5:0] × t_{MCKP}/64 Default = 11 0100b
235	5:0	TR_LVLOAD_D	LVLOAD rising edge for data (50% duty cycle)	Tap = D[5:0] × t_{MCKP}/64 Default = 11 0000b
236	5:0	TR_8D	CLKx8 rising edge for data (edge0)	Tap = D[5:0] × t_{MCKP}/64 Default = 11 0100b

INSERTED SYNC CODE TIMING

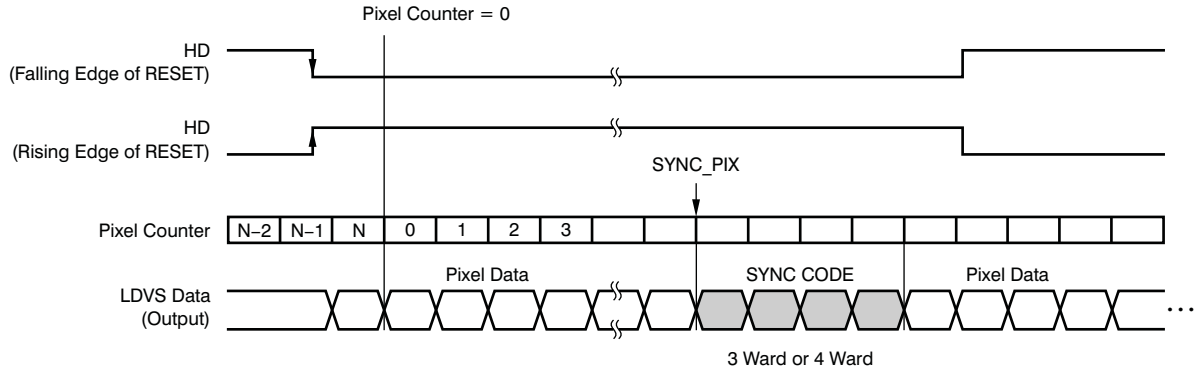


Figure 9. Inserted SYNC Code Timing

INSERTED SYNC CODE SETTING TIMING

The VSP7502 can generate a SYNC CODE that is inserted into LVDS data. Codes 0 and 65535 are applied for the SYNC CODE; therefore, pixel data are limited from 1 to 65534. Figure 10 illustrates the timing for the inserted SYNC CODE setting.

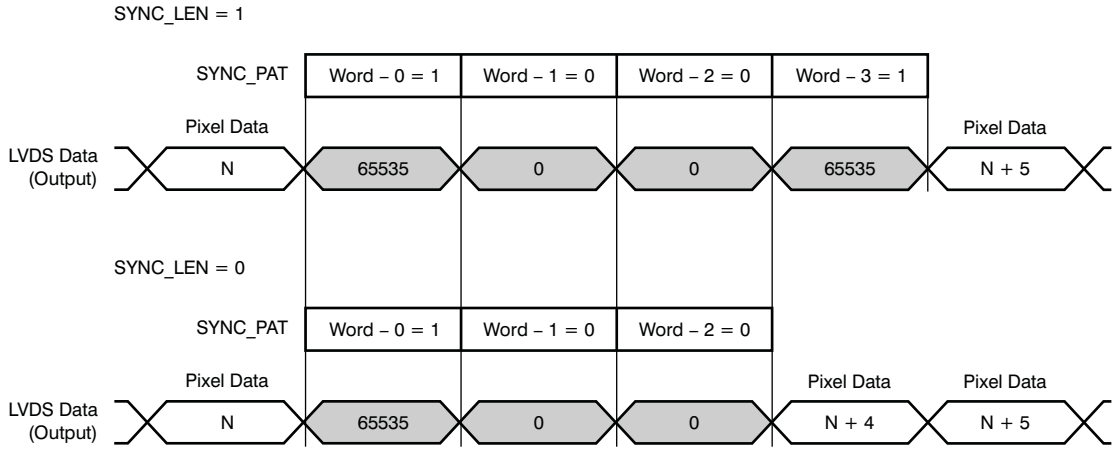


Figure 10. Inserted SYNC Code Setting Timing

Table 8. DLL-Generated Pulse Default Settings

ADDRESS	BITS	REGISTER NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION
227	12:0	SYNC_PIX	SYNC code start pixel	PIX number 0-8191
228	3:0	SYNC_PAT	SYNC code pattern setting	1 = FFFFh, 0 = 0000h [0] = word0, [1] = word1, [2] = word2, [3] = word3
	4	SYNC_LEN	Length of SYNC CODE	0 = 3-sync pattern 1 = 4-sync pattern

PIXEL COUNTER RESET TIMING

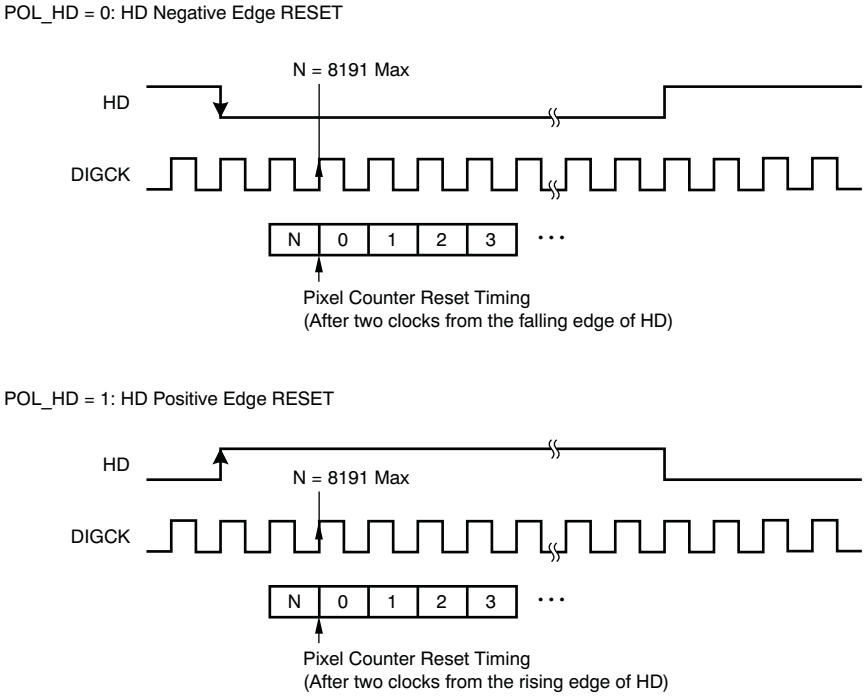


Figure 11. Pixel Counter Reset Timing

LINE COUNTER RESET TIMING

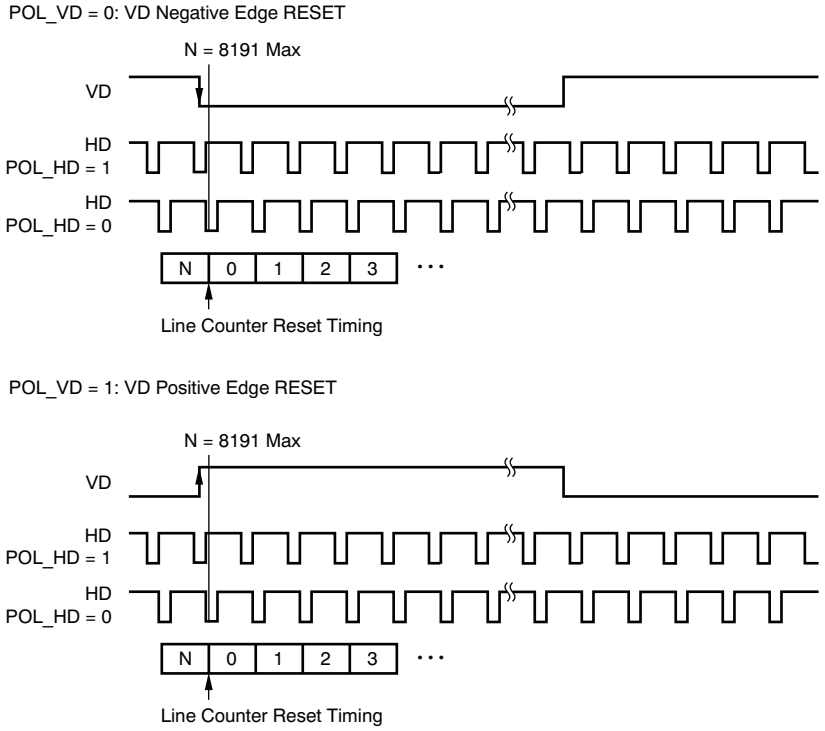


Figure 12. Inserted SYNC Code Setting Timing

Table 9. DLL-Generated Pulse Default Settings

ADDRESS	BITS	REGISTER NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION
65	1	POL_HD	$H_{COUNTER}$ reset timing	0 = HD negative edge reset 1 = HD positive edge reset
	2	POL_VD	$V_{COUNTER}$ reset timing	0 = VD negative edge reset 1 = VD positive edge reset

MCLK SETUP AND HOLD TIMING

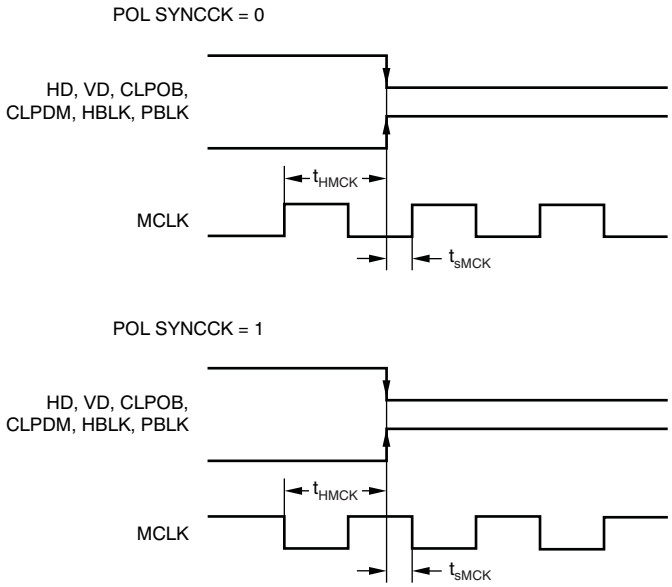


Figure 13. MCLK Setup and Hold Time

Table 10. Timing Characteristics for Figure 13

PARAMETER		MIN	TYP	MAX	UNIT
t_{SMCK}	MCLK setup time to HD	6.0			ns
t_{HMCK}	MCLK hold time to HD	1.0			ns

Table 11. DLL-Generated Pulse Default Settings

ADDRESS	BITS	REGISTER NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION
65	0	POL_SYNCCK	HD/VD/CLPOB/CLPDM/HBLK/PBLK latch timing	0 = Latch at positive edge of MCLK 1 = Latch at negative edge of MCLK

CLPDM, CLPOB, HBLK, AND PBLK PATTERN SETTING TIMING

The VSP7502 provides the functionality to generate CLPDM, CLPOB, HBLK, and PBLK pulses internally. This function has four different pattern combinations (C0, C1, M0, and M1), as shown in Figure 14. C0 and C1 can set six different signal patterns (Cx_SELx) within one frame. M0 and M1 can set four different signal patterns (Mx_SELx) within one frame. Cx_SELx and Mx_SELx are generated by base waves. The setting area of each pattern is specified by Cx_LINx and Mx_LINx.

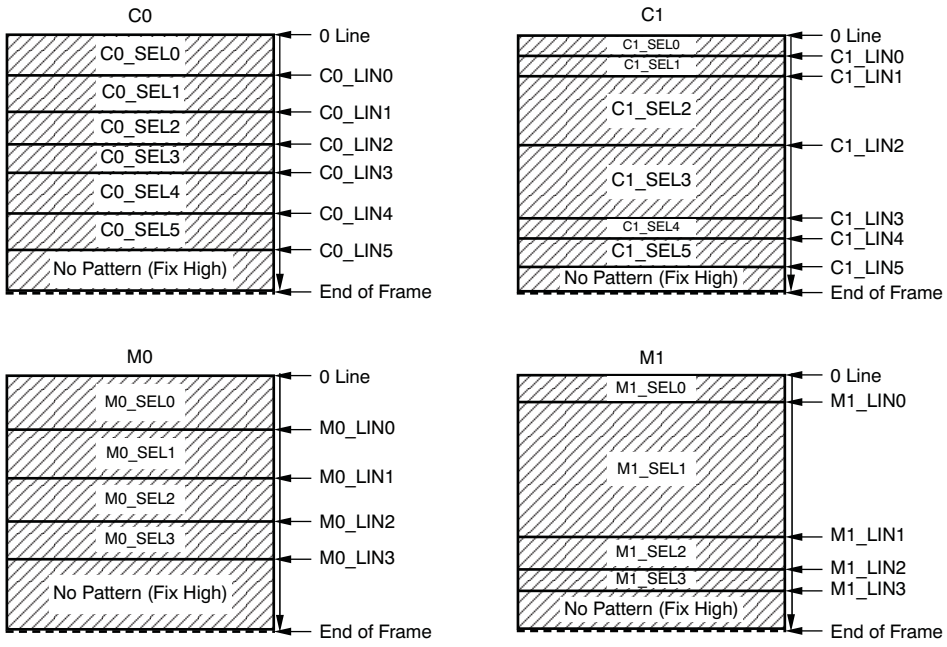


Figure 14. CLPD, CLPOB, HBLK, and PBLK Pulses

Step 1: Base Wave Setting (Address 78–105)

C_TPx and M_TPx are the base-wave toggling position setting registers. C_POLx and M_POLx are the polarity setting registers for the toggling position. Base wave C has six different patterns, and base wave M has eight different patterns, as Figure 15 shows.

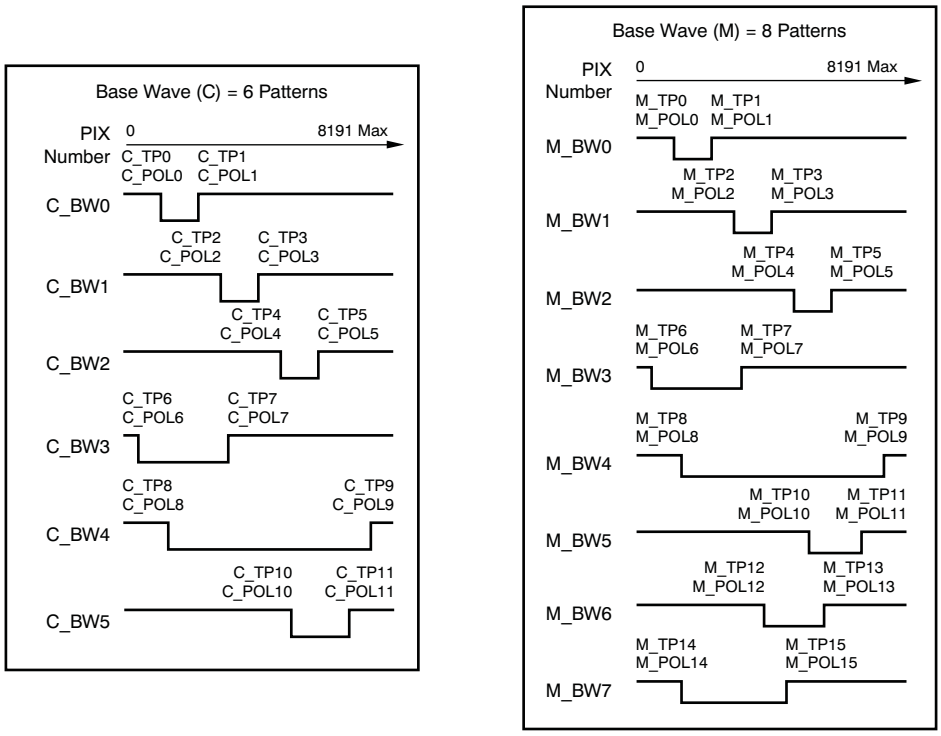


Figure 15. Base Wave Patterns

Step 2: Pattern Setting (Address 106–145)

The signal pattern is generated by using Cx_SELx and Mx_SELx, the base wave selection registers. These registers are shown in Figure 16. The signal pattern can generate not only single toggling patterns, but also two or more toggling patterns per line with a combination of base waves.

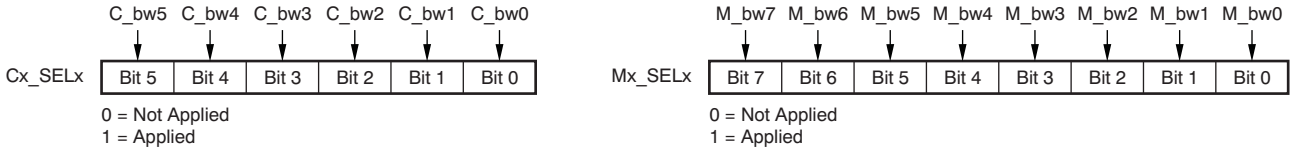


Figure 16. Base Wave Registers

Figure 17 describes the setting area of Cx_SELx and Mx_SELx, which are specified by Cx_LINx and Mx_LINx.

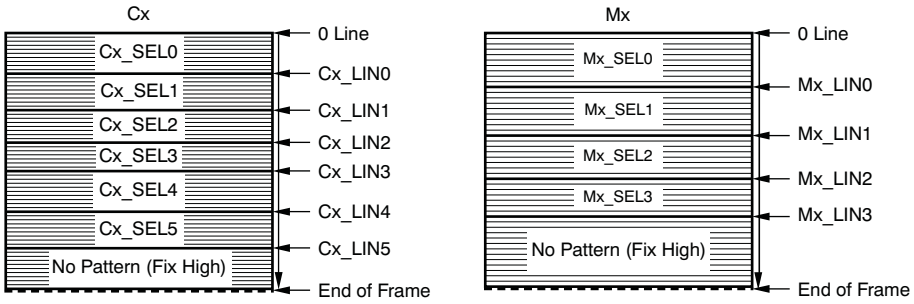


Figure 17. Cx, Mx Setting Area

Step 3: CLPDM, CLPOB, PBLK, and HBLK Pattern Selection (Address 77)

Apply C0, C1, M0, and M1 to CLPOB, CLPOB, PBLK, and HBLK with Address 77 (Table 12).

Table 12. Description of Address 77

ADDRESS	BITS	REGISTER NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION
77	2:0	SEL_DM	CLPOB pulse pattern selection	000b = Select C0 as CLPDM 001b = Select C1 as CLPDM 010b = Select M0 as CLPDM 011b = Select M1 as CLPDM 10xb = Fix low 11xb = Fix high Default = 000b
	5:3	SEL_OB	CLPOB pulse pattern selection	000b = Select C0 as CLPOB 001b = Select C1 as CLPOB 010b = Select M0 as CLPOB 011b = Select M1 as CLPOB 10xb = Fix low 11xb = Fix high Default = 000b
	8:6	SEL_HBLK	HBLK pulse pattern selection	000b = Select C0 as HBLK 001b = Select C1 as HBLK 010b = Select M0 as HBLK 011b = Select M1 as HBLK 10xb = Fix low 11xb = Fix high Default = 000b
	11:9	SEL_PBLK	PBLK pulse pattern selection	000b = Select C0 as PBLK 001b = Select C1 as PBLK 010b = Select M0 as PBLK 011b = Select M1 as PBLK 10xb = Fix low 11xb = Fix high Default = 000b
	13:12	—	—	Reserved Default = 00b

HTG MASK TIMING

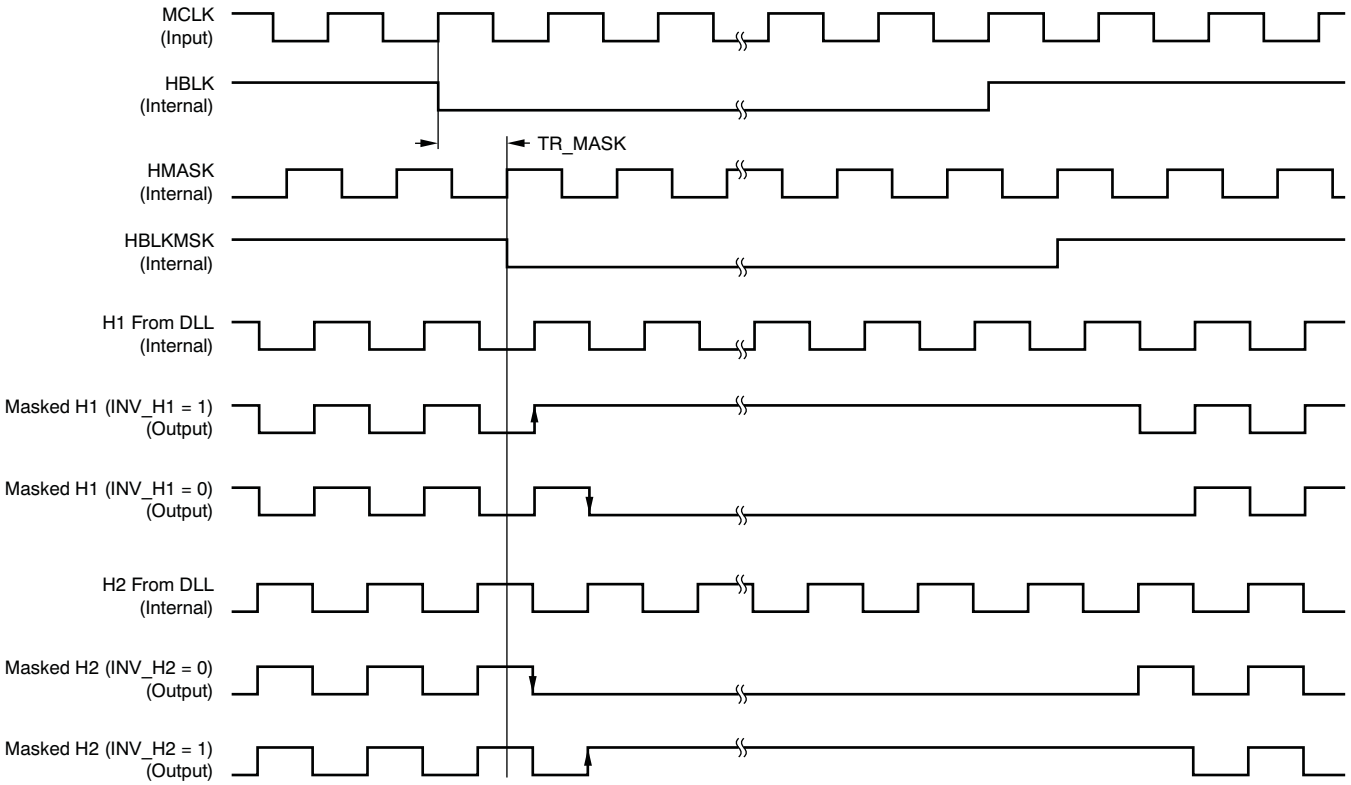


Figure 18. HTG Mask Timing

Table 13. Timing Characteristics for Figure 18

PARAMETER		MIN	TYP	MAX	UNIT
t_{R_MASK}					

Table 14. DLL-Generated Pulse Default Settings

ADDRESS	BITS	REGISTER NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION
75	5:0	TR_MASK	HMASK rise tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 11 0000b
76	8	INV_H1	Inverting H1 masked polarity	0 = Noninverting (default) 1 = Inverting
	9	INV_H2	Inverting H2 masked polarity	0 = Noninverting (default) 1 = Inverting
	10	INV_LH	Inverting LH masked polarity	0 = Noninverting (default) 1 = Inverting
	11	INV_UH1	Inverting UH1 masked polarity	0 = Noninverting (default) 1 = Inverting
	12	INV_UH2	Inverting UH2 masked polarity	0 = Noninverting (default) 1 = Inverting

PIN CONFIGURATION

BGA PACKAGE
VSP7502ZWV
(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	LVAVSS	LVBYPD	LVDLLVDD	DRVDD2	DVDD2_SPI	DVDD3_SPI	RST	SCK	AVSS2	L_W	RN_W	RP_W	NC	AVSS2
B	LVAVDD	LVAVSS	LVDLLVSS	DRVSS2	DVSS3_SPI	OUTMD	SCS	SDI	AVSS2	REFVSS_W	REFVSS_W	REFVDD_W	AVSS2	IN_W
C	LVDVDD	LVDVSS		DRVSS2	DVSS2_SPI	MN_HBLK	MN_DM	ATPG	AVSS2	AVSS2	AVSS2	REFVDD_W	AVSS2	IP_W
D	DW0–	DW1–	LVDVSS	GNDS	DVSS2_SPI	MN_PBLK	MN_OB	LVMON	AFEMON	NC	RP_X	REFVSS_X	AVSS2_W	AVSS2_W
E	DW0+	DW1+	GNDS	GNDS							RN_X	REFVSS_X	AVSS2	IP_X
F	DX0–	DX1–	CKS0–	GNDS							L_X	REFVDD_X	AVSS2	IN_X
G	DX0+	DX1+	CKS0+	GNDS							AVDD3	REFVDD_X	AVSS2_X	AVSS2_X
H	DY0–	DY1–	CKS1–	GNDS							AVSS3	REFVDD_Y	AVSS2_Y	AVSS2_Y
J	DY0+	DY1+	CKS1+	GNDS							L_Y	REFVDD_Y	AVSS2	IN_Y
K	DZ0–	DZ1–	GNDS	GNDS							RN_Y	REFVSS_Y	AVSS2	IP_Y
L	DZ0+	DZ1+	GNDS	RGVSS3	H2VSS3	H1VSS3	DVSS2	DVSS2	AVSS2	NC	RP_Y	REFVSS_Y	AVSS2_Z	AVSS2_Z
M	DLLVSS2	DLLVSS2	DRVSS2	RGVDD3	H2VDD3	H1VDD3	VD	DVSS2	AVSS2	AVSS2	AVSS2	REFVDD_Z	AVSS2	IP_Z
N	BYPD	DLLVDD2	DRVSS2	LH	UH2	UH1	DVSS3	HD	DVDD2	REFVSS_Z	REFVSS_Z	REFVDD_Z	AVSS2	IN_Z
P	DLLVSS2	DLLVDD2	DRVDD2	RG	H2	H1	DVDD3	MCK	DVDD2	L_Z	RN_Z	RP_Z	NC	AVSS2

TERMINAL FUNCTIONS

PIN NUMBER	NAME	VOLTAGE	TYPE (1)	DESCRIPTION
A1	LVAVSS	—	AGND	LVDS analog ground
B1	LVAVDD	1.8 V	A_Pow	LVDS analog power supply
C1	LVDVDD	1.8 V	D_Pow	LVDS power supply
D1	DW0–	—	LVO	LVDS data output MSB– (channel W)
E1	DW0+	—	LVO	LVDS data output MSB+ (channel W)
F1	DX0–	—	LVO	LVDS data output MSB– (channel X)
G1	DX0+	—	LVO	LVDS data output MSB+ (channel X)
H1	DY0–	—	LVO	LVDS data output MSB– (channel Y)
J1	DY0+	—	LVO	LVDS data output MSB+ (channel Y)
K1	DZ0–	—	LVO	LVDS data output MSB– (channel Z)
L1	DZ0+	—	LVO	LVDS data output MSB+ (channel Z)
M1	DLLVSS2	—	AGND	AFE DLL ground
N1	BYPD	—	AO	AFE DLL bypass; connected to DLLVDD with a 1000-pF capacitor
P1	DLLVSS2	—	AGND	AFE DLL ground
A2	LVBYPD	—	AO	LVDS DLL bypass; connected to DLLVDD with a 1000-pF capacitor
B2	LVAVSS	—	AGND	LVDS analog ground
C2	LVDVSS	—	DGND	LVDS ground
D2	DW1–	—	LVO	LVDS data output LSB– (channel W)
E2	DW1+	—	LVO	LVDS data output LSB+ (channel W)
F2	DX1–	—	LVO	LVDS data output LSB– (channel X)
G2	DX1+	—	LVO	LVDS data output LSB+ (channel X)
H2	DY1–	—	LVO	LVDS data output LSB– (channel Y)
J2	DY1+	—	LVO	LVDS data output LSB+ (channel Y)
K2	DZ1–	—	LVO	LVDS data output LSB– (channel Z)
L2	DZ1+	—	LVO	LVDS data output LSB+ (channel Z)
M2	DLLVSS2	—	AGND	AFE DLL ground
N2	DLLVDD2	1.8 V	A_Pow	AFE DLL power supply

(1) Designators in TYPE: AGND = analog ground pin; A_Pow = analog power supply pin; AI = analog signal input pin; AO = analog reference pin; DGND = digital ground pin; D_Pow = digital power supply pin; DI = digital signal input pin; DIO = digital signal bidirectional pin; DO = digital signal output pin; HTGGND = HTG ground pin; HTG_Pow = HTG power supply pin; HTG_O = HTG signal output pin; and LVO = LVDS signal output pin.

TERMINAL FUNCTIONS (continued)

PIN NUMBER	NAME	VOLTAGE	TYPE (1)	DESCRIPTION
P2	DLLVDD2	1.8 V	A_Pow	AFE DLL power supply
A3	LVDLLVDD	1.8 V	A_Pow	LVDS DLL power supply
B3	LVDLLVSS	—	AGND	LVDS DLL ground
D3	LVDVSS	—	DGND	LVDS ground
E3	GNDS	—	AGND	SUB ground
F3	CKS0–	—	LVO	Negative LVDS clock output (channel 0)
G3	CKS0+	—	LVO	Positive LVDS clock output (channel 0)
H3	CKS1–	—	LVO	Negative LVDS clock output (channel 1)
J3	CKS1+	—	LVO	Positive LVDS clock output (channel 1)
K3	GNDS	—	AGND	SUB ground
L3	GNDS	—	AGND	SUB ground
M3	DRVSS2	—	DGND	Internal parallel data output ground
N3	DRVSS2	—	DGND	Internal parallel data output ground
P3	DRVDD2	1.8 V	D_Pow	Internal parallel data output power supply
A4	DRVDD2	1.8 V	D_Pow	Internal parallel data output power supply
B4	DRVSS2	—	DGND	Internal parallel data output ground
C4	DRVSS2	—	DGND	Internal parallel data output ground
D4	GNDS	—	AGND	SUB ground
E4	GNDS	—	AGND	SUB ground
F4	GNDS	—	AGND	SUB ground
G4	GNDS	—	AGND	SUB ground
H4	GNDS	—	AGND	SUB ground
J4	GNDS	—	AGND	SUB ground
K4	GNDS	—	AGND	SUB ground
L4	RGVSS3	—	HTG_GND	HTG ground (RG, LH)
M4	RGVDD3	3 V	HTG_Pow	HTG power supply (RG, LH)
N4	LH	3 V	HTG_O	LH pulse output
P4	RG	3 V	HTG_O	RG pulse output
A5	DVDD2_SPI	1.8 V	D_Pow	Serial interface power supply
B5	DVSS3_SPI	—	DGND	Serial interface I/O power supply
C5	DVSS2_SPI	—	DGND	Serial interface ground
D5	DVSS2_SPI	—	DGND	Serial interface ground
L5	H2VSS3	—	HTG_GND	HTG ground (H2, UH2)
M5	H2VDD3	3 V	HTG_Pow	HTG power supply (H2, UH2)
N5	UH2	3 V	HTG_O	UH2 pulse output
P5	H2	3 V	HTG_O	H2 pulse output
A6	DVDD3_SPI	3 V	D_Pow	Serial interface I/O power supply
B6	OUTMD	3 V	DI	TEST setting pin; connected to DVDD3_SPI
C6	MN_HBLK	1.8 V	DIO	HBLK pulse input/output
D6	MN_PBLK	1.8 V	DIO	PBLK pulse input/output
L6	H1VSS3	—	HTG_GND	HTG ground (H1, UH1)
M6	H1VDD3	3 V	HTG_Pow	HTG power supply (H1, UH1)
N6	UH1	3 V	HTG_O	UH1 pulse output
P6	H1	3 V	HTG_O	H1 pulse output
A7	RST	3 V	DI	System reset; connected to DVDD when RESET is not used
B7	SCS	3 V	DI	Serial data enable (active low)
C7	MN_DM	1.8 V	DIO	CLPDM pulse input/output
D7	MN_OB	1.8 V	DIO	CLPOB pulse input/output
L7	DVSS2	—	DGND	Digital block ground
M7	VD	3 V	DI	Vertical sync pulse input
N7	DVSS3	—	DGND	Digital input ground

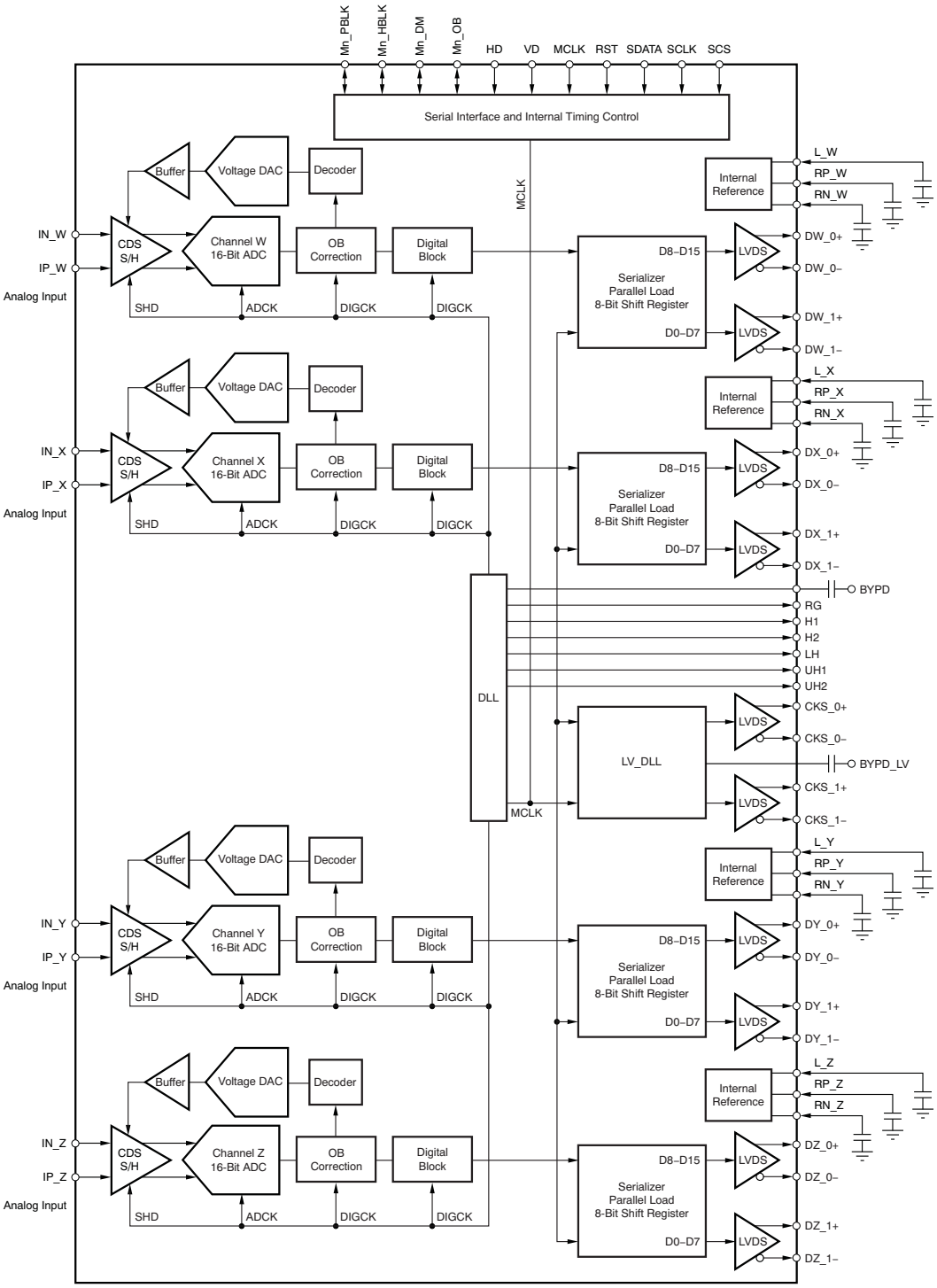
TERMINAL FUNCTIONS (continued)

PIN NUMBER	NAME	VOLTAGE	TYPE (1)	DESCRIPTION
P7	DVDD3	3 V	D_Pow	Digital input power supply
A8	SCLK	3 V	DI	Serial data clock
B8	SDI	3 V	DI	Serial data input/output
C8	ATPG	1.8 V	DI	TEST setting pin; connected to GND
D8	LVMON	1.8 V	DO	TEST signal output
L8	DVSS2	—	DGND	Digital block ground
M8	DVSS2	—	DGND	Digital block ground
N8	HD	3 V	DI	Horizontal sync pulse input
P8	MCLK	3 V	DI	Master clock input
A9	AVSS2	—	AGND	Analog ground
B9	AVSS2	—	AGND	Analog ground
C9	AVSS2	—	AGND	Analog ground
D9	AFEMON	1.8 V	DO	TEST signal output
L9	AVSS2	—	AGND	Analog ground
M9	AVSS2	—	AGND	Analog ground
N9	DVDD2	1.8 V	D_Pow	Digital block power supply
P9	DVDD2	1.8 V	D_Pow	Digital block power supply
A10	L_W	—	AO	Common reference, connected to GND with a 0.1-µF capacitor (channel W)
B10	REFVSS	—	AGND	Reference block ground
C10	AVSS2	—	AGND	Analog ground
D10	NC	—	—	No connection
L10	NC	—	—	No connection
M10	AVSS2	—	AGND	Analog ground
N10	REFVSS	—	AGND	Reference block ground
P10	L_Z	—	AO	Common reference, connected to GND with a 0.1-µF capacitor (channel Z)
A11	RN_W	—	AO	ADC negative reference, connected to GND with a 0.1-µF capacitor (channel W)
B11	REFVSS	—	AGND	Reference block ground
C11	AVSS2	—	AGND	Analog ground
D11	RP_X	—	AO	ADC positive reference, connected to GND with a 0.1-µF capacitor (channel X)
E11	RN_X	—	AO	ADC negative reference, connected to GND with a 0.1-µF capacitor (channel X)
F11	L_X	—	AO	Common reference, connected to GND with a 0.1-µF capacitor (channel X)
G11	AVDD3	3 V	A_Pow	Analog input power supply
H11	AVSS3	—	AGND	Analog input ground
J11	L_Y	—	AO	Common reference, connected to GND with a 0.1-µF capacitor (channel Y)
K11	RN_Y	—	AO	ADC negative reference, connected to GND with a 0.1-µF capacitor (channel Y)
L11	RP_Y	—	AO	ADC positive reference, connected to GND with a 0.1-µF capacitor (channel Y)
M11	AVSS2	—	AGND	Analog ground
N11	REFVSS	—	AGND	Reference block ground
P11	RN_Z	—	AO	ADC negative reference, connected to GND with a 0.1-µF capacitor (channel Z)
A12	RP_W	—	AO	ADC positive reference, connected to GND with a 0.1-µF capacitor (channel W)
B12	REFVDD_W	1.8 V	A_Pow	Reference block power supply (channel W)
C12	REFVDD_W	1.8 V	A_Pow	Reference block power supply (channel W)
D12	REFVSS	—	AGND	Reference block ground
E12	REFVSS	—	AGND	Reference block ground
F12	REFVDD_X	1.8 V	A_Pow	Reference block power supply (channel X)
G12	REFVDD_X	1.8 V	A_Pow	Reference block power supply (channel X)
H12	REFVDD_Y	1.8 V	A_Pow	Reference block power supply (channel Y)
J12	REFVDD_Y	1.8 V	A_Pow	Reference block power supply (channel Y)
K12	REFVSS	—	AGND	Reference block ground
L12	REFVSS	—	AGND	Reference block ground
M12	REFVDD_Z	1.8 V	A_Pow	Reference block power supply (channel Z)

TERMINAL FUNCTIONS (continued)

PIN NUMBER	NAME	VOLTAGE	TYPE (1)	DESCRIPTION
N12	REFVDD_Z	1.8 V	A_Pow	Reference block power supply (channel Z)
P12	RP_Z	—	AO	ADC positive reference, connected to GND with a 0.1-µF capacitor (channel Z)
A13	NC	—	—	No connection
B13	AVSS2	—	AGND	Analog ground
C13	AVSS2	—	AGND	Analog ground
D13	AVDD2_W	1.8 V	A_Pow	Analog power supply
E13	AVSS2	—	AGND	Analog ground
F13	AVSS2	—	AGND	Analog ground
G13	AVDD2_X	1.8 V	A_Pow	Analog power supply
H13	AVDD2_Y	1.8 V	A_Pow	Analog power supply
J13	AVSS2	—	AGND	Analog ground
K13	AVSS2	—	AGND	Analog ground
L13	AVDD2_Z	1.8 V	A_Pow	Analog power supply
M13	AVSS2	—	AGND	Analog ground
N13	AVSS2	—	AGND	Analog ground
P13	NC	—	—	No connection
A14	AVSS2	—	AGND	Analog ground
B14	IN_W	—	AI	Analog signal negative input (channel W)
C14	IP_W	—	AI	Analog signal positive input (channel W)
D14	AVDD2_W	1.8 V	A_Pow	Analog power supply
E14	IP_X	—	AI	Analog signal positive input (channel X)
F14	IN_X	—	AI	Analog signal negative input (channel X)
G14	AVDD2_X	1.8 V	A_Pow	Analog power supply
H14	AVDD2_Y	1.8 V	A_Pow	Analog power supply
J14	IN_Y	—	AI	Analog signal negative input (channel Y)
K14	IP_Y	—	AI	Analog signal positive input (channel Y)
L14	AVDD2_Z	1.8 V	A_Pow	Analog power supply
M14	IP_Z	—	AI	Analog signal positive input (channel Z)
N14	IN_Z	—	AI	Analog signal negative input (channel Z)
P14	AVSS2	—	AGND	Analog ground

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

SAMPLE-AND-HOLD (S/H) MODE

Figure 19 shows a simplified input circuit of the S/H mode. In this mode, the input signal is sampled by the SHD signal.

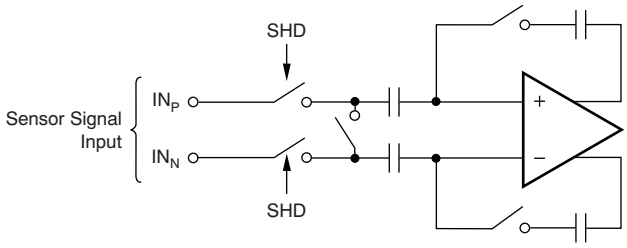


Figure 19. S/H Input Mode Block Diagram

16-BIT ADC

The VSP7502 also provides a high-speed, 16-bit ADC. This ADC uses a fully differential, pipelined architecture with a correction feature. This architecture achieves better linearity at lower signal levels because large linearity errors tend to occur at specific points in the full-scale range, and linearity improves for a signal level below that specific point. The ADC ensures 16-bit resolution for the entire full-scale range.

OPTICAL BLACK (OB) LOOP AND OB CLAMP LEVEL

The VSP7502 has a built-in optical black (OB) offset self-calibration circuit (OB loop) that compensates the OB level by using OB pixels that are output from the CCD image sensor. This device also provides a digital OB clamp loop. CCD offset is compensated by converging both OB loops while activating CLPOB during a period when OB pixels are output from the CCD. 20 pixels of the CLPOB period may be enough for stable OB loop operation.

CCD offset is compensated as a difference between the reference level and data level of the OB pixel. These compensated signal levels are recognized as actual *OB levels*, and all outputs are clamped to OB levels set by the register. These OB levels are the base of black for the effective pixel period thereafter.

The digital OB loop corrects the OB level with time constant control, as shown in Equation 1.

$$Err_{(N)} = Err_{(N-1)} - \frac{Err_{(N-1)} - \text{Target OB Level}}{2^{TCx}} \quad (1)$$

where:

TCX = TC1, TC2, TC3, and TC4

The OB-DAC update timing and TC application depend on the ADC code, OB error value, and frame as shown in Figure 20 through Figure 25. The VSP7502 provides four types of TC setting. TC1,TC2, and TC3 should set the short time constant for rapid OB convergence. TC4 should set the long time constant to prevent the sensitive OB convergence.

The first and second frames of operation are described in Figure 20 to Figure 25. Figure 20 and Figure 21 show the first frame. Figure 22 and Figure 23 illustrate the second frame. Figure 24 and Figure 25 depict the second frame with regards to address 4, bit 6 with OB_MODECTRL = 1.

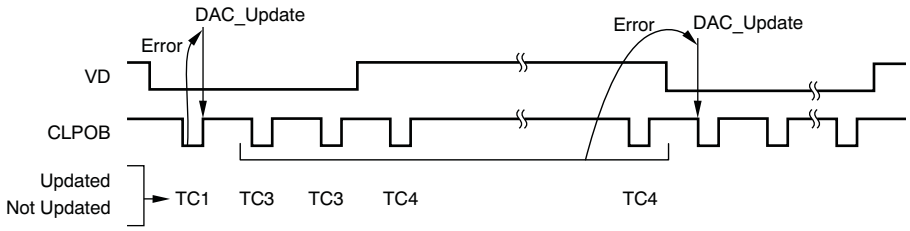


Figure 20. First Frame, Normal Operation (ADC[15:0] > 0)

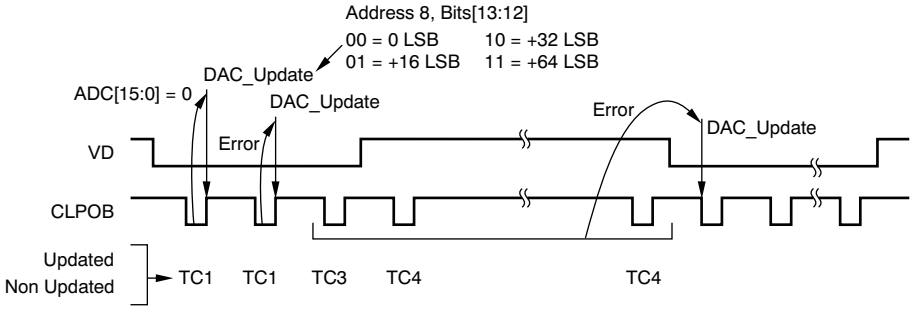


Figure 21. First Frame, Stuck Detection (ADC[15:0] = 0)

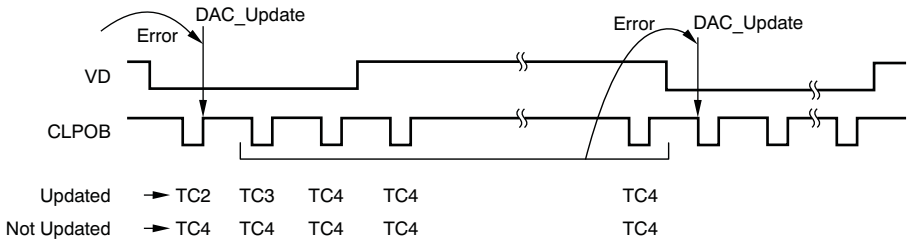


Figure 22. Second Frame, Normal Operation (ADC[15:0] > 0)

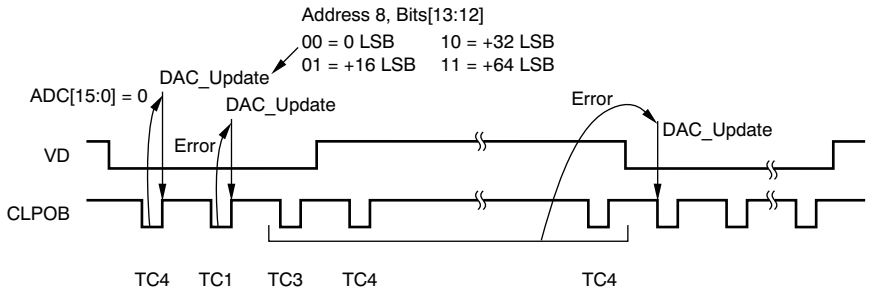


Figure 23. Second Frame, Stuck Detection (ADC[15:0] = 0)

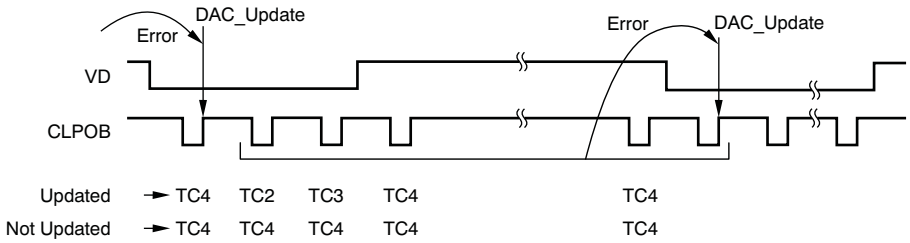


Figure 24. Second Frame, Normal Operation (ADC[15:0] > 0, OB_MODECTRL = 1)

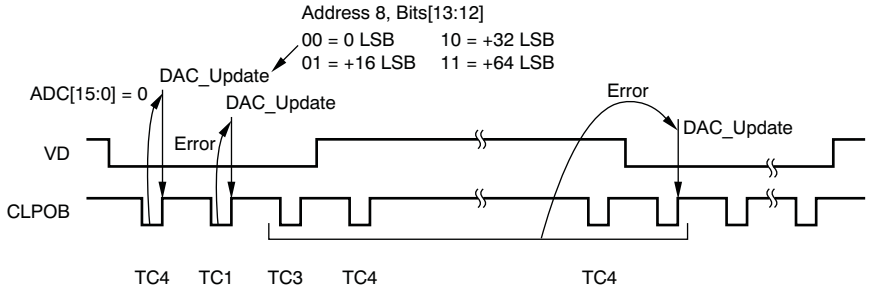


Figure 25. Second Frame, Stuck Detection (ADC[15:0] = 0, OB_MODECTRL = 1)

DAC Update Judgment

- DAC update | Error | ≥ DAC_THL, DAC_THU
- DAC not updated | Error | DAC_THL, DAC_THU

DAC update (stuck detection, DAC is under range error)

- ADC code of first CLPOB after VD edge = all '0'

DAC Update level (normal operation)

- Depends on Error value

DAC Update level (stuck detection, DAC is under range error)

- Depends on address 8, bits[13:12], STUCK_DACLEV

00b = 0 LSB at DAC; 01b = +16 LSB at DAC; 10b = +32 LSB at DAC; 11b = +64 LSB at DAC

(1 LSB at DAC = 512 LSB at 16-bit = 8 mV)

Table 15. DLL-Generated Pulse Default Settings

ADDRESS	BITS	REGISTER NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION
4	6	OB_MODECTRL	DAC update control	0 = Operation as usual (default) 1 = Stop DAC update at the negative edge of first CLPOB after VD
8	13:12	STUCK_DACLEV	DAC update code setting at stuck recovery mode	00b = +0 LSB at DAC CODE (no update) 01b = +16 LSB at DAC CODE (default) 10b = +32 LSB at DAC CODE 11b = +64 LSB at DAC CODE
9	2:0	DAC_THL	V_{DAC} lower update level (error register < 0)	|error reg| > 128 LSB at 14-bit + DAC_THL × 64 LSB at 14-bit Default = 000b
	6:4	DAC_THU	V_{DAC} upper update level (error register > 0)	|error reg| > 128 LSB at 14-bit + DAC_THU × 64 LSB at 14-bit Default = 000b

TC2 and TC3 are applicable to the plural lines of the OBLNTC register. This operation is shown in Figure 26.

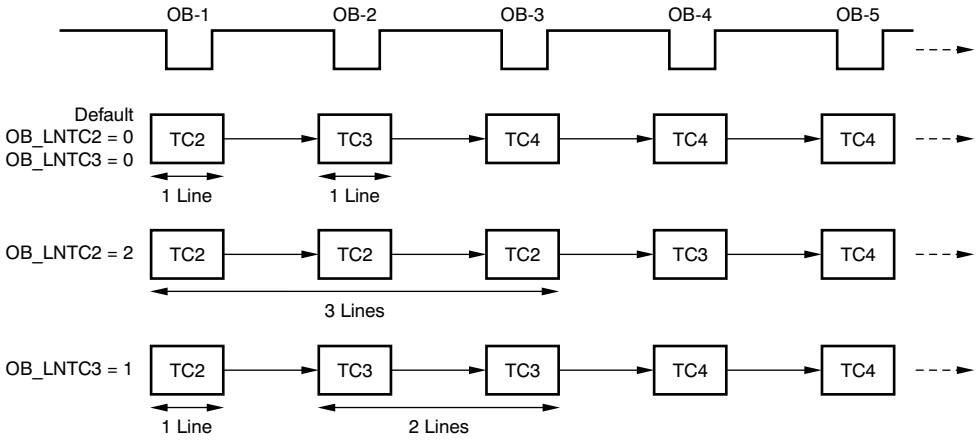


Figure 26. Need Title

Table 16. DLL-Generated Pulse Default Settings

ADDRESS	BITS	REGISTER NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION
5	3:0	OB_TC1	TC1 time constant	$TC1 = 2^{(OB\_TC1 + 1)}$ Default = 0100b
	7:4	OB_TC2	TC2 time constant	$TC2 = 2^{(OB\_TC2 + 1)}$ Default = 0100b
6	3:0	OB_TC3	TC3 time constant	$TC3 = 2^{(OB\_TC3 + 1)}$ Default = 1000b
	7:4	OB_TC4	TC4 time constant	$TC4 = 2^{(OB\_TC4 + 1)}$ Default = 1011b
7	5:0	OB_LNTC2	TC2 line length	Line length = OB_LNTC2 + 1 Default = 00 0000b
	11:6	OB_LNTC3	TC3 line length	Line length = OB_LNTC3 + 1 Default = 00 0000b

PROGRAMMABLE GAIN

The VSP7502 gain ranges from 0 dB to 47.4 dB. The desired gain is set through a combination of analog gain and the digital programmable gain amplifier (DPGA). Both gain settings are controlled through the serial interface.

Analog gain can be programmed from 0 dB to 15.4 dB in 8-dB steps. Digital gain can be programmed from 0 dB to 32 dB in 0.032-dB steps. The digital gain changes linearly in proportion to the setting code. The relationship between the input code and digital gain is shown in Figure 27.

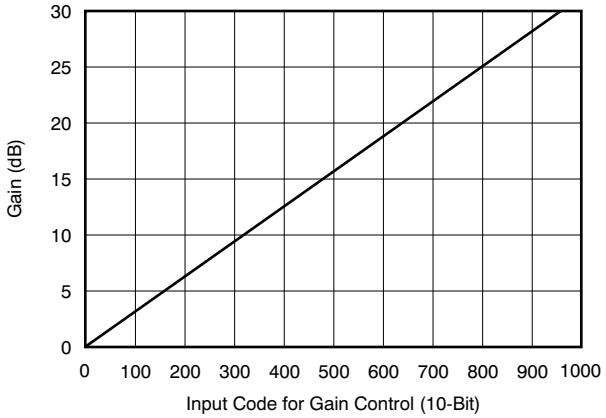


Figure 27. Setting Code versus Gain

Table 17. DLL-Generated Pulse Default Settings

ADDRESS	BITS	REGISTER NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION
36	5:0	AGAIN_W	Analog gain selection (channel W)	00 0000b = 0 dB 00 1100b = 3.1 dB 01 0011b = 5.2 dB 01 1010b = 7.3 dB 10 0010b = 9.4 dB 10 1010b = 11.6 dB 11 0001b = 13.7 dB 11 0111b = 15.4 dB Default = 00 0000b
37	5:0	AGAIN_X	Analog gain selection (channel X)	00 0000b = 0 dB 00 1100b = 3.1 dB 01 0011b = 5.2 dB 01 1010b = 7.3 dB 10 0010b = 9.4 dB 10 1010b = 11.6 dB 11 0001b = 13.7 dB 11 0111b = 15.4 dB Default = 00 0000b
38	5:0	AGAIN_Y	Analog gain selection (channel Y)	00 0000b = 0 dB 00 1100b = 3.1 dB 01 0011b = 5.2 dB 01 1010b = 7.3 dB 10 0010b = 9.4 dB 10 1010b = 11.6 dB 11 0001b = 13.7 dB 11 0111b = 15.4 dB Default = 00 0000b
39	5:0	AGAIN_Z	Analog gain selection (channel Z)	00 0000b = 0 dB 00 1100b = 3.1 dB 01 0011b = 5.2 dB 01 1010b = 7.3 dB 10 0010b = 9.4 dB 10 1010b = 11.6 dB 11 0001b = 13.7 dB 11 0111b = 15.4 dB Default = 00 0000b
40	9:0	DGAIN_W	Digital gain (channel W)	Digital gain (dB) = DGAIN/32 Default = 00 0000 0000b
41	9:0	DGAIN_X	Digital gain (channel X)	Digital gain (dB) = DGAIN/32 Default = 00 0000 0000b
42	9:0	DGAIN_Y	Digital gain (channel Y)	Digital gain (dB) = DGAIN/32 Default = 00 0000 0000b
43	9:0	DGAIN_Z	Digital gain (channel Z)	Digital gain (dB) = DGAIN/32 Default = 00 0000 0000b

CLOCKING AND DLL

The VSP7502 requires the following clocks for proper operation: MCLK, the system clock; CLPOB, the optical black level clamp; and CLPDM, the input clamp.

The HBLK timing signal transmits the horizontal blanking period timing. In this period, high-speed HTG pulses are masked. The PBLK timing signal transmits the data output blanking period timing. In this period, outputting the ADC data is masked.

The VSP7502 has built-in DLL circuits that enable the required sampling clocks and the horizontal timing pulse and logic clocks for outputting LVDS data to be generated.

VOLTAGE REFERENCE

All reference voltages and bias currents used on the VSP7502 are created from internal bandgap circuitry. The device has a symmetrically independent voltage reference for each channel.

Both channels of the S/H and the ADC use two primary reference voltages: REFP (1.25 V) and REFN (0.75 V) of individual references. REFP and REFN are buffered on-chip. The ADC full-scale range is determined by twice the difference voltage between REFP and REFN.

REFP and REFN should be heavily decoupled with appropriate capacitors.

HOT PIXEL REJECTION

Sometimes, OB pixel output signals from the CCD include unusual level signals that are caused by pixel defection. If this level reaches a full-scale level, it may affect OB level stability. The VSP7502 has a function that rejects the unusually large pixel levels (hot pixels) in the OB pixel. This function may contribute to CCD yield improvement that is caused by OB pixel failure.

The rejection level for hot pixels is set by HPIX_LEVEL. When hot pixels are detected, the VSP7502 rejects it and ignores the error value of hot pixels. Hot pixel rejection is only effective in TC4 (TC = OB time constant setting).

Table 18. DLL-Generated Pulse Default Settings

ADDRESS	BITS	REGISTER NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION
4	3:0	HPIX_LEVEL	Hot pixel reject level	(OB_HPLEV + 1) × 256 LSB at 16 bits Default = 1111b
	4	HPIX_ENABLE	Hot pixel rejection	0 = No rejection (default) 1 = Enable hot pixel rejection

REGISTER DEFINITIONS

Table 19. Register Definitions

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
0	1:0	STB	Standby, all circuits	X0b = Normal operation 01b = Standby 11b = Sleep Default = 00b	Immediate
	3:2	—	Reserved	Reserved Default = 00b	
	4	STB_CH_W	Channel W standby	0 = Normal operation 1 = Standby Default = 0	
	5	STB_CH_X	Channel X standby	0 = Normal operation 1 = Standby Default = 0	
	6	STB_CH_Y	Channel Y standby	0 = Normal operation 1 = Standby Default = 0	
	7	STB_CH_Z	Channel Z standby	0 = Normal operation 1 = Standby Default = 0	
	8	STB_HTG	HTG standby	0 = Normal operation 1 = HTG standby Default = 0	
	13:9	—	Reserved	Reserved Default = 00000b	
1	0	REG_RST	REG reset	0 = Normal operation 1 = Register reset Default = 0	Immediate
	1	RST_DLL	DLL reset	0 = Normal operation 1 = DLL reset Default = 0	
	2	INPMOD	Must be set to '0'	0 = Normal operation 1 = Inhibited Must be set to '0' before normal operation can begin. Default = 1	
	3	MCKSTPEN	MCLK stop detect	0 = Off 1 = MCK stop detection on Default = 1	
	13:8	—	Reserved	Reserved Default = 000 0000 0000b	
2	1:0	PT_SHAMP	SHAMP power trimming	00b = Power 0 10b = Power 2 01b = Power 1 11b = Power 3 Default = 01b	Immediate
	4:12	PT_RBIAS	RBIAS power trimming	001b = –10% mode 101b = +10% mode 010b = Normal operation Others = Null Default = 010b	
	13:5	—	Reserved	Reserved Default = 0 0000 0000b	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
3	3:0	—	Reserved	Reserved Default = 0000b	Immediate
	4	MSKBOUT_W	BOUT channel W mask	0 = Normal operation 1 = BOUT mask (fixed low) Default = 0	
	5	MSKBOUT_X	BOUT channel X mask	0 = Normal operation 1 = BOUT mask (fixed low) Default = 0	
	6	MSKBOUT_Y	BOUT channel Y mask	0 = Normal operation 1 = BOUT mask (fixed low) Default = 0	
	7	MSKBOUT_Z	BOUT channel Z mask	0 = Normal operation 1 = BOUT mask (fixed low) Default = 0	
	8	MASK_DATA	—	0 = Mask data when PBLK is '0' 1 = No mask Default = 0	
	13:9	—	Reserved	Reserved Default = 00000b	
4	3:0	HPIX_LEVEL	Hot pixel reject level	(HPIX_LEVEL + 1) × 256 LSB at 16 bits Default = 1111b	VD update
	4	HPIX_ENABLE	Hot pixel rejection	0 = No rejection 1 = Enable hot pixel rejection Default = 0	
	13:5	—	Reserved	Reserved Default = 0 0000 0000b	
5	3:0	OB_TC1	TC1 time constant	TC1 = $2^{(OB\_TC1 + 1)}$ Default = 0100b	VD update
	7:4	OB_TC2	TC2 time constant	TC2 = $2^{(OB\_TC2 + 1)}$ Default = 0100b	
	13:8	—	Reserved	Reserved Default = 00 0000b	
6	3:0	OB_TC3	TC3 time constant	TC3 = $2^{(OB\_TC3 + 1)}$ Default = 1000b	VD update
	7:4	OB_TC4	TC4 time constant	TC4 = $2^{(OB\_TC4 + 1)}$ Default = 1011b	
	13:8	—	Reserved	Reserved Default = 00 0000b	
7	5:0	OB_LNTC2	TC2 line length	Line length = OB_LNTC2 + 1 Default = 00 0000b	VD update
	11:6	OB_LNTC3	TC3 line length	Line length = OB_LNTC3 + 1 Default = 00 0000b	
	13:12	—	Reserved	Reserved Default = 00b	
8	11:0	—	Reserved	Reserved Default = 0000 0000 0000b	
	13:12	STUCK_ DACLEV	DAC update code setting at stuck recovery mode	00b = +0 LSB at DAC CODE (no update) 01b = +16 LSB at DAC CODE 10b = +32 LSB at DAC CODE 11b = +64 LSB at DAC CODE Default = 01b	
9	2:0	DAC_THL	V_{DAC} lower update level (error register < 0)	|error reg| > 128 LSB at 14-bit + DAC_THL × 64 LSB at 14-bit	Immediate
	3	—	Reserved	Reserved Default = 0	
	6:4	DAC_THU	V_{DAC} upper update level (error register > 0)	|error reg| > 128 LSB at 14-bit + DAC_THU × 64 LSB at 14-bit	
	13:7	—	Reserved	Reserved Default = 000 0000b	
10-31	—	—	Reserved	Reserved	—

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
32	2:0	DLY_SHD_W	SHD delay line control (channel W)	Delay (ns) = D[2:0] × 0.3 Default = 000b	Immediate
	13:3	—	Reserved	Reserved Default = 000 0000 0000b	
33	2:0	DLY_SHD_X	SHD delay line control (channel X)	Delay (ns) = D[2:0] × 0.3 Default = 000b	Immediate
	13:3	—	Reserved	Reserved Default = 000 0000 0000b	
34	2:0	DLY_SHD_Y	SHD delay line control (channel Y)	Delay (ns) = D[2:0] × 0.3 Default = 000b	Immediate
	13:3	—	Reserved	Reserved Default = 000 0000 0000b	
35	2:0	DLY_SHD_Z	SHD delay line control (channel X)	Delay (ns) = D[2:0] × 0.3 Default = 000b	Immediate
	13:3	—	Reserved	Reserved Default = 000 0000 0000b	
36	5:0	AGAIN_W	Analog gain selection (channel W)	00 0000b = 0 dB 00 1100b = 3.1 dB 01 0011b = 5.2 dB 01 1010b = 7.3 dB 10 0010b = 9.4 dB 10 1010b = 11.6 dB 11 0001b = 13.7 dB 11 0111b = 15.4 dB Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
37	5:0	AGAIN_X	Analog gain selection (channel X)	00 0000b = 0 dB 00 1100b = 3.1 dB 01 0011b = 5.2 dB 01 1010b = 7.3 dB 10 0010b = 9.4 dB 10 1010b = 11.6 dB 11 0001b = 13.7 dB 11 0111b = 15.4 dB Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
38	5:0	AGAIN_Y	Analog gain selection (channel Y)	00 0000b = 0 dB 00 1100b = 3.1 dB 01 0011b = 5.2 dB 01 1010b = 7.3 dB 10 0010b = 9.4 dB 10 1010b = 11.6 dB 11 0001b = 13.7 dB 11 0111b = 15.4 dB Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
39	5:0	AGAIN_Z	Analog gain selection (channel Z)	00 0000b = 0 dB 00 1100b = 3.1 dB 01 0011b = 5.2 dB 01 1010b = 7.3 dB 10 0010b = 9.4 dB 10 1010b = 11.6 dB 11 0001b = 13.7 dB 11 0111b = 15.4 dB Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
40	9:0	DGAIN_W	Digital gain (channel W)	Digital gain (dB) = DGAIN/32 Default = 00 0000 0000b	VD update
	13:10	—	Reserved	Reserved Default = 0000b	
41	9:0	DGAIN_X	Digital gain (channel X)	Digital gain (dB) = DGAIN/32 Default = 00 0000 0000b	VD update
	13:10	—	Reserved	Reserved Default = 0000b	
42	9:0	DGAIN_Y	Digital gain (channel Y)	Digital gain (dB) = DGAIN/32 Default = 00 0000 0000b	VD update
	13:10	—	Reserved	Reserved Default = 0000b	
43	9:0	DGAIN_Z	Digital gain (channel Z)	Digital gain (dB) = DGAIN/32 Default = 00 0000 0000b	VD update
	13:10	—	Reserved	Reserved Default = 0000b	
44	13:0	OBLEV_W	OB level (channel W)	OB level (LSB) = 1024 to 16383 Default = 00 1001 0000 0000b	VD update

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
45	13:0	OBLEV_X	OB level (channel X)	OB level (LSB) = 1024 to 16383 Default = 00 1001 0000 0000b	VD update
46	13:0	OBLEV_Y	OB level (channel Y)	OB level (LSB) = 1024 to 16383 Default = 00 1001 0000 0000b	VD update
47	13:0	OBLEV_Z	OB level (channel Z)	OB level (LSB) = 1024 to 16383 Default = 00 1001 0000 0000b	VD update
48-63	—	—	Reserved	Reserved	—
64	3:0	MON_SEL	Select monitor signal	0000b = No monitor (fixed low) 0010b = SHD_W 0100b = SHD_X 0110b = SHD_Y 1000b = SHD_Z 1001b = DIGCK 1010b = HMASK 1011b = SDO_TG 1100b = VR_{EVENT} 1101b = HR_{EVENT} Others = Fixed low Default = 0000b	Immediate
	4	MON_CLPDM	CLPDM monitor output	0 = No monitor (Hi-Z) 1 = Monitor (output) Default = 0	
	5	MON_CLPOB	CLPOB monitor output	0 = No monitor (Hi-Z) 1 = Monitor (output) Default = 0	
	6	MON_HBLK	HBLK monitor output	0 = No monitor (Hi-Z) 1 = Monitor (output) Default = 0	
	7	MON_PBLK	PBLK monitor output	0 = No monitor (Hi-Z) 1 = Monitor (output) Default = 0	
	8	EXT_CLPDM	CLPDM internal/external select	0 = Internal 1 = External Default = 0	
	9	EXT_CLPOB	CLPOB internal/external select	0 = Internal 1 = External Default = 0	
	10	EXT_HBLK	HBLK internal/external select	0 = Internal 1 = External Default = 0	
	11	EXT_PBLK	PBLK internal/external select	0 = Internal 1 = External Default = 0	
	13:12	—	Reserved	Reserved Default = 00b	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
65	0	POL_SYNCCK	HD/VD/CLPOB/CLPDM/ HBLK/PBLK latch timing	0 = Latch at positive edge of MCLK 1 = Latch at negative edge of MCLK Default = 0	Immediate
	1	POL_HD	$H_{COUNTER}$ reset timing	0 = HD negative edge reset 1 = HD positive edge reset Default = 0	
	2	POL_VD	$V_{COUNTER}$ reset timing	0 = VD negative edge reset 1 = VD positive edge reset Default = 0	
	3	—	Reserved	Reserved	
	4	POL_CLPDM	CLPDM polarity control (external)	0 = Active low 1 = Active high Default = 0	
	5	POL_CLPOB	CLPOB polarity control (external)	0 = Active low 1 = Active high Default = 0	
	6	POL_HBLK	HBLK polarity control (external)	0 = Active low 1 = Active high Default = 0	
	7	POL_PBLK	PBLK polarity control (external)	0 = Active low 1 = Active high Default = 0	
	8	OUTPOL_CLPDM	CLPDM output timing (internally generated)	0 = Output at positive edge of MCLK 1 = Output at negative edge of MCLK Default = 0	
	9	OUTPOL_CLPOB	CLPOB output timing (internally generated)	0 = Output at positive edge of MCLK 1 = Output at negative edge of MCLK Default = 0	
	10	OUTPOL_HBLK	HBLK output timing (internally generated)	0 = Output at positive edge of MCLK 1 = Output at negative edge of MCLK Default = 0	
	11	OUTPOL_PBLK	PBLK output timing (internally generated)	0 = Output at positive edge of MCLK 1 = Output at negative edge of MCLK Default = 0	
	13:12	—	Reserved	Reserved Default = 00000b	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
66	0	OUTEN_RG	RG output buffer control	0 = RG output 1 = High-Z Default = 1	Immediate
	1	OUTEN_H1	H1 output buffer control	0 = H1 output 1 = High-Z Default = 1	
	2	OUTEN_H2	H2 output buffer control	0 = H2 output 1 = High-Z Default = 1	
	3	OUTEN_LH	LH output buffer control	0 = LH output 1 = High-Z Default = 1	
	4	OUTEN_UH1	UH1 output buffer control	0 = UH1 output 1 = High-Z Default = 1	
	5	OUTEN_UH2	UH2 output buffer control	0 = UH2 output 1 = High-Z Default = 1	
	7:6	—	Reserved	Reserved Default = 00b	
	8	STBY_H1	H1 standby	0 = Active 1 = Standby Default = 1	
	9	STBY_H2	H2 standby	0 = Active 1 = Standby Default = 1	
	10	STBY_LH	LH standby	0 = Active 1 = Standby Default = 1	
	11	STBY_UH1	UH1 standby	0 = Active 1 = Standby Default = 1	
	12	STBY_UH2	UH2 standby	0 = Active 1 = Standby Default = 1	
	13	—	Reserved	Reserved Default = 0	
67	5:0	TF_RG	RG falling tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 00 1101b	VD update
	7:6	—	Reserved	Reserved Default = 00b	
	13:8	TR_RG	RG rising tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 00 0001b	
68	5:0	TF_H1	H1 falling tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 01 1111b	VD update
	7:6	—	Reserved	Reserved Default = 00b	
	13:8	TR_H1	H1 rising tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 00 0000b	
69	5:0	TF_H2	H2 falling tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 00 0000b	VD update
	7:6	—	Reserved	Reserved Default = 00b	
	13:8	TR_H2	H2 rising tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 01 1111b	
70	5:0	TF_LH	LH falling tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 00 0000b	VD update
	7:6	—	Reserved	Reserved Default = 00b	
	13:8	TR_LH	LH rising tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 00 0000b	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
71	5:0	TF_UH1	UH1 falling tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 00 0000b	VD update
	7:6	—	Reserved	Reserved Default = 00b	
	13:8	TR_UH1	UH1 rising tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 00 0000b	
72	5:0	TF_UH2	UH2 falling tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 00 0000b	VD update
	7:6	—	Reserved	Reserved Default = 00b	
	13:8	TR_UH2	UH2 rising tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 00 0000b	
73	5:0	TF_SHD	SHD falling tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 10 0001b	VD update
	7:6	—	Reserved	Reserved Default = 00b	
	13:8	TR_SHD	SHD rising tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 11 1101b	
74	—	—	Reserved	Reserved	VD update
75	5:0	TR_MASK	HMASK rising tap select	Tap = D[5:0] × t_{MCKP}/64 Default = 11 0000b	VD update
	7:6	—	Reserved	Reserved Default = 00b	
	13:8	TR_DIGCK	DIGCK rising tap select	Tap = D[13:8] × t_{MCKP}/64 Default = 11 0001b	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
76	0	OBSKIP	CLPOB skip mode	0 = Normal operation (CLPOB is effective for every line) 1 = Skip mode (CLPOB is effective at only the odd or even line) Default = 0	VD update
	1	SEL_OBSKIP	Skip select for even or odd line	0 = Skip odd lines 1 = Skip even lines Default = 0	
	3:2	—	Reserved	Reserved Default = 00b	
	4	INV_C0	C0 invert	0 = Noninverting 1 = Inverting Default = 0	
	5	INV_C1	C1 invert	0 = Noninverting 1 = Inverting Default = 0	
	6	INV_M0	M0 invert	0 = Noninverting 1 = Inverting Default = 0	
	7	INV_M1	M1 invert	0 = Noninverting 1 = Inverting Default = 0	
	8	INV_H1	Inverted H1 masked polarity	0 = Noninverting 1 = Inverting Default = 0	
	9	INV_H2	Inverted H2 masked polarity	0 = Noninverting 1 = Inverting Default = 0	
	10	INV_LH	Inverted LH masked polarity	0 = Noninverting 1 = Inverting Default = 0	
	11	INV_UH1	Inverted UH1 masked polarity	0 = Noninverting 1 = Inverting Default = 0	
	12	INV_UH2	Inverted UH2 masked polarity	0 = Noninverting 1 = Inverting Default = 0	
	13	—	Reserved	Reserved Default = 0000b	
77	2:0	SEL_DM	CLPDM pulse pattern selection	000b = Select C0 as CLPDM (default) 001b = Select C1 as CLPDM 010b = Select M0 as CLPDM 011b = Select M1 as CLPDM 10xb = Fixed low 11xb = Fixed high	VD update
	5:3	SEL_OB	CLPOB pulse pattern selection	000b = Select C0 as CLPOB (default) 001b = Select C1 as CLPOB 010b = Select M0 as CLPOB 011b = Select M1 as CLPOB 10xb = Fixed low 11xb = Fixed high	
	8:6	SEL_HBLK	HBLK pulse pattern selection	000b = Select C0 as HBLK (default) 001b = Select C1 as HBLK 010b = Select M0 as HBLK 011b = Select M1 as HBLK 10xb = Fixed low 11xb = Fixed high	
	11:9	SEL_PBLK	PBLK pulse pattern selection	000b = Select C0 as PBLK (default) 001b = Select C1 as PBLK 010b = Select M0 as PBLK 011b = Select M1 as PBLK 10xb = Fixed low 11xb = Fixed high	
	13:12	—	Reserved	Reserved Default = 00b	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
78	12:0	C_TP0	Pixel number setting (base wave 0, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL0	C_TP0 polarity	0 = Low 1 = High Default = 0	
79	12:0	C_TP1	Pixel number setting (base wave 0, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL1	C_TP1 polarity	0 = Low 1 = High Default = 0	
80	12:0	C_TP2	Pixel number setting (base wave 1, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL2	C_TP2 polarity	0 = Low 1 = High Default = 0	
81	12:0	C_TP3	Pixel number setting (base wave 1, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL3	C_TP3 polarity	0 = Low 1 = High Default = 0	
82	12:0	C_TP4	Pixel number setting (base wave 2, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL4	C_TP4 polarity	0 = Low 1 = High Default = 0	
83	12:0	C_TP5	Pixel number setting (base wave 2, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL5	C_TP5 polarity	0 = Low 1 = High Default = 0	
84	12:0	C_TP6	Pixel number setting (base wave 3, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL6	C_TP6 polarity	0 = Low 1 = High Default = 0	
85	12:0	C_TP7	Pixel number setting (base wave 3, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL7	C_TP7 polarity	0 = Low 1 = High Default = 0	
86	12:0	C_TP8	Pixel number setting (base wave 4, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL8	C_TP8 polarity	0 = Low 1 = High Default = 0	
87	12:0	C_TP9	Pixel number setting (base wave 4, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL9	C_TP9 polarity	0 = Low 1 = High Default = 0	
88	12:0	C_TP10	Pixel number setting (base wave 5, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL10	C_TP10 polarity	0 = Low 1 = High Default = 0	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
89	12:0	C_TP11	Pixel number setting (base wave 5, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C_POL11	C_TP11 polarity	0 = Low 1 = High Default = 0	
90	12:0	M_TP0	Pixel number setting (base wave 0, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL0	M_TP0 polarity	0 = Low 1 = High Default = 0	
91	12:0	M_TP1	Pixel number setting (base wave 0, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL1	M_TP1 polarity	0 = Low 1 = High Default = 0	
92	12:0	M_TP2	Pixel number setting (base wave 1, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL2	M_TP2 polarity	0 = Low 1 = High Default = 0	
93	12:0	M_TP3	Pixel number setting (base wave 1, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL3	M_TP3 polarity	0 = Low 1 = High Default = 0	
94	12:0	M_TP4	Pixel number setting (base wave 2, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL4	M_TP4 polarity	0 = Low 1 = High Default = 0	
95	12:0	M_TP5	Pixel number setting (base wave 2, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL5	M_TP5 polarity	0 = Low 1 = High Default = 0	
96	12:0	M_TP6	Pixel number setting (base wave 3, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL6	M_TP6 polarity	0 = Low 1 = High Default = 0	
97	12:0	M_TP7	Pixel number setting (base wave 3, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL7	M_TP7 polarity	0 = Low 1 = High Default = 0	
98	12:0	M_TP8	Pixel number setting (base wave 4, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL8	M_TP8 polarity	0 = Low 1 = High Default = 0	
99	12:0	M_TP9	Pixel number setting (base wave 4, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL9	M_TP9 polarity	0 = Low 1 = High Default = 0	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
100	12:0	M_TP10	Pixel number setting (base wave 5, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL10	M_TP10 polarity	0 = Low 1 = High Default = 0	
101	12:0	M_TP11	Pixel number setting (base wave 5, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL11	M_TP11 polarity	0 = Low 1 = High Default = 0	
102	12:0	M_TP12	Pixel number setting (base wave 6, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL12	M_TP12 polarity	0 = Low 1 = High Default = 0	
103	12:0	M_TP13	Pixel number setting (base wave 6, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL13	M_TP13 polarity	0 = Low 1 = High Default = 0	
104	12:0	M_TP14	Pixel number setting (base wave 7, first toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL14	M_TP14 polarity	0 = Low 1 = High Default = 0	
105	12:0	M_TP15	Pixel number setting (base wave 7, second toggle point)	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M_POL15	M_TP15 polarity	0 = Low 1 = High Default = 0	
106	12:0	C0_LIN0	Line number setting (C0, first pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C0_GEN0	C0 global enable	0 = Disabled 1 = Enabled Default = 0	
107	5:0	C0_SEL0	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
108	12:0	C0_LIN1	Line number setting (C0, second pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C0_EN1	C0_LIN1 enable	0 = Disabled 1 = Enabled Default = 0	
109	5:0	C0_SEL1	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
110	12:0	C0_LIN2	Line number setting (C0, third pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C0_EN2	C0_LIN2 enable	0 = Disabled 1 = Enabled Default = 0	
111	5:0	C0_SEL2	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
112	12:0	C0_LIN3	Line number setting (C0, fourth pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C0_EN3	C0_LIN3 enable	0 = Disabled 1 = Enabled Default = 0	
113	5:0	C0_SEL3	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
114	12:0	C0_LIN4	Line number setting (C0, fifth pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C0_EN4	C0_LIN4 enable	0 = Disabled 1 = Enabled Default = 0	
115	5:0	C0_SEL4	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
116	12:0	C0_LIN5	Line number setting (C0, sixth pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C0_EN5	C0_LIN5 enable	0 = Disabled 1 = Enabled Default = 0	
117	5:0	C0_SEL5	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
118	12:0	C1_LIN0	Line number setting (C1, first pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C1_GEN0	C1 global enable	0 = Disabled 1 = Enabled Default = 0	
119	5:0	C1_SEL0	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
120	12:0	C1_LIN1	Line number setting (C1, second pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C1_EN1	C1_LIN1 enable	0 = Disabled 1 = Enabled Default = 0	
121	5:0	C1_SEL1	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
122	12:0	C1_LIN2	Line number setting (C1, third pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C1_EN2	C1_LIN2 enable	0 = Disabled 1 = Enabled Default = 0	
123	5:0	C1_SEL2	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
124	12:0	C1_LIN3	Line number setting (C1, fourth pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C1_EN3	C1_LIN3 enable	0 = Disabled 1 = Enabled Default = 0	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
125	5:0	C1_SEL3	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
126	12:0	C1_LIN4	Line number setting (C1, fifth pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C1_EN4	C1_LIN4 enable	0 = Disabled 1 = Enabled Default = 0	
127	5:0	C1_SEL4	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
128	12:0	C1_LIN5	Line number setting (C1, sixth pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	C1_EN5	C1_LIN5 enable	0 = Disabled 1 = Enabled Default = 0	
129	5:0	C1_SEL5	Pattern select	Reserved Default = 00 0000b	VD update
	13:6	—	Reserved	Reserved Default = 0000 0000b	
130	12:0	M0_LIN0	Line number setting (M0, first pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M0_GEN0	M0 global enable	0 = Disabled 1 = Enabled Default = 0	
131	7:0	M0_SEL0	Pattern select	Reserved Default = 0000 0000b	VD update
	13:8	—	Reserved	Reserved Default = 00 0000b	
132	12:0	M0_LIN1	Line number setting (M0, second pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M0_EN1	M0_LIN1 enable	0 = Disabled 1 = Enabled Default = 0	
133	7:0	M0_SEL1	Pattern select	Reserved Default = 0000 0000b	VD update
	13:8	—	Reserved	Reserved Default = 00 0000b	
134	12:0	M0_LIN2	Line number setting (M0, third pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M0_EN2	M0_LIN2 enable	0 = Disabled 1 = Enabled Default = 0	
135	7:0	M0_SEL2	Pattern select	Reserved Default = 0000 0000b	VD update
	13:8	—	Reserved	Reserved Default = 00 0000b	
136	12:0	M0_LIN3	Line number setting (M0, fourth pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M0_EN3	M0_LIN3 enable	0 = Disabled 1 = Enabled Default = 0	
137	7:0	M0_SEL3	Pattern select	Reserved Default = 0000 0000b	VD update
	13:8	—	Reserved	Reserved Default = 00 0000b	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
138	12:0	M1_LIN0	Line number setting (M1, first pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M1_GEN0	M1 global enable	0 = Disabled 1 = Enabled Default = 0	
139	7:0	M1_SEL0	Pattern select	Reserved Default = 0000 0000b	VD update
	13:8	—	Reserved	Reserved Default = 00 0000b	
140	12:0	M1_LIN1	Line number setting (M1, second pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M1_EN1	M1_LIN1 enable	0 = Disabled 1 = Enabled Default = 0	
141	7:0	M1_SEL1	Pattern select	Reserved Default = 0000 0000b	VD update
	13:8	—	Reserved	Reserved Default = 00 0000b	
142	12:0	M1_LIN2	Line number setting (M1, third pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M1_EN2	M1_LIN2 enable	0 = Disabled 1 = Enabled Default = 0	
143	7:0	M1_SEL2	Pattern select	Reserved Default = 0000 0000b	VD update
	13:8	—	Reserved	Reserved Default = 00 0000b	
144	12:0	M1_LIN3	Line number setting (M1, fourth pattern change line)	Line number = 0 to 8191 Default = 0 0000 0000 0000b	VD update
	13	M1_EN3	M1_LIN3 enable	0 = Disabled 1 = Enabled Default = 0	
145	7:0	M1_SEL3	Pattern select	Reserved Default = 0000 0000b	VD update
	13:8	—	Reserved	Reserved Default = 00 0000b	
146	12:0	HCNT_STOP	$H_{COUNTER}$ stop pixel	HCNT_STOP = 0 to 8191 (pixels) Default = 1 1111 1111 1111b	VD update
	13	—	Reserved	Reserved Default = 0	
147	12:0	VCNT_STOP	$V_{COUNTER}$ stop line	VCNT_STOP = 0 to 8191 (lines) Default = 1 1111 1111 1111b	VD update
	13	—	Reserved	Reserved Default = 0	
148-223	—	—	Reserved	Reserved	—

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
224	0	STB_LVDSA_W	LVDS standby (channel W)	0 = Normal operation 1 = Standby Default = 1	Immediate
	1	STB_LVDSA_X	LVDS standby (channel X)	0 = Normal operation 1 = Standby Default = 1	
	2	STB_LVDSA_Y	LVDS standby (channel Y)	0 = Normal operation 1 = Standby Default = 1	
	3	STB_LVDSA_Z	LVDS standby (channel Z)	0 = Normal operation 1 = Standby Default = 1	
	7:4	—	Reserved	Reserved Default = 0000b	
	8	STB_CLKOA	LVDS CKS0 standby	0 = Normal operation 1 = Standby Default = 1	
	9	STB_CLKOB	LVDS CKS1 standby	0 = Normal operation 1 = Standby Default = 1	
	13:10	—	Reserved	Reserved Default = 0000b	
225	1:0	—	Reserved	Reserved	Immediate
	3:2	LEVL_SEL	Level selection	00b = 100 mV 10b = 200 mV 01b = 150 mV 11b = 250 mV Default = 00b	
	5:4	EMP_LVDS	Pre-emphasis on	00b = 100% 10b = 166% 01b = 133% 11b = 200% Default = 00b	
	6	COM_SEL	Common-mode voltage selection	0 = 0.9 V 1 = 1.2 V Default = 1	
	13:7	—	Reserved	Reserved Default = 00 0000b	
226	7:0	CKS_PAT	CKS pattern for CKSOUT	—	Immediate
	13:8	—	Reserved	Reserved Default = 00 0000b	
227	12:0	SYNC_PIX	SYNC CODE start pixel	Pixel number 0 to 8191 Default = 0 0000 0000 0000b	Immediate
	13	SYNC_EN	Enable sync pattern interpolation	0 = Enabled 1 = Disabled (allows code FFFFh or 0000h) Default = 0	
228	3:0	SYNC_PAT	SYNC CODE pattern setting	0 = 0000h [0] = Word 0 1 = FFFFh [1] = Word 1 [2] = Word 2 [3] = Word 3 Default = 0000b	Immediate
	4	SYNC_LEN	Sync code length	0 = Three-sync pattern 1 = Four-sync pattern Default = 0	
	7:5	—	Reserved	Reserved Default = 000b	
	10:8	MON_SEL	Monitor signal selection	000b = Fixed low 100b = LVLOAD_DATA 001b = SDO 101b = LVLOAD_CKS 010b = HR_{EVENT} Others = Fixed low 011b = DIGCK Default = 000b	
	13:11	—	Reserved	Reserved Default = 000b	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
229	5:0	TR _DCLK	DCLK rising edge (50% duty cycle)	Tap = D[5:0] × t_{MCKP}/64 Default = 01 0000b	Immediate
	13:6	—	Reserved	Reserved Default = 0000 0000b	
230	5:0	TR_LVLOAD_CK	LVLOAD rising edge (50% duty cycle) for CKSOUT	Tap = D[5:0] × t_{MCKP}/64 Default = 11 0000b	Immediate
	13:6	—	Reserved	Reserved Default = 0000 0000b	
231	5:0	TR_8CK	CLKx8 rising edge (edge 0) for CKSOUT	Tap = D[5:0] × t_{MCKP}/64 Default = 11 0100b	Immediate
	13:6	—	Reserved	Reserved Default = 0000 0000b	
232	1:0	TR_8CK0	Fine alignment for first CKSOUT rising edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	Immediate
	3:2	TF_8CK0	Fine alignment for first CKSOUT falling edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	5:4	TR_8CK1	Fine alignment for second CKSOUT rising edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	7:6	TF_8CK1	Fine alignment for second CKSOUT falling edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	9:8	TR_8CK2	Fine alignment for third CKSOUT rising edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	11:10	TF_8CK2	Fine alignment for third CKSOUT falling edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	13:12	—	Reserved	Reserved Default = 00b	—
233	1:0	TR_8CK3	Fine alignment for fourth CKSOUT rising edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	Immediate
	3:2	TF_8CK3	Fine alignment for fourth CKSOUT falling edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	5:4	TR_8CK4	Fine alignment for fifth CKSOUT rising edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	7:6	TF_8CK4	Fine alignment for fifth CKSOUT falling edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	9:8	TR_8CK5	Fine alignment for sixth CKSOUT rising edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	11:10	TF_8CK5	Fine alignment for sixth CKSOUT falling edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	13:12	—	Reserved	Reserved Default = 00b	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
234	1:0	TR_8CK6	Fine alignment for seventh CKSOUT rising edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	Immediate
	3:2	TF_8CK6	Fine alignment for seventh CKSOUT falling edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	—
	5:4	TR_8CK7	Fine alignment for eighth CKSOUT rising edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	7:6	TF_8CK7	Fine alignment for eighth CKSOUT falling edge	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	13:8	—	Reserved	Reserved Default = 00 0000b	
235	5:0	TR_LVLOAD_D	LVLOAD rising edge (50% duty cycle) for data	Tap = D[5:0] × t_{MCKP}/64 Default = 11 0000b	Immediate
	13:6	—	Reserved	Reserved Default = 0000 0000b	
236	5:0	TR_8D	CLKx8 rising edge (edge 0) for data	Tap = D[5:0] × t_{MCKP}/64 Default = 11 0100b	Immediate
	13:6	—	Reserved	Reserved Default = 0000 0000b	
237	1:0	TR_8D0	Fine alignment for first rising edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	Immediate
	3:2	TF_8D0	Fine alignment for first falling edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	5:4	TR_8D1	Fine alignment for second rising edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	7:6	TF_8D1	Fine alignment for second falling edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	9:8	TR_8D2	Fine alignment for third rising edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	11:10	TF_8D2	Fine alignment for third falling edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	—
	13:12	—	Reserved	Reserved Default = 00b	

Table 19. Register Definitions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
238	1:0	TR_8D3	Fine alignment for fourth rising edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	Immediate
	3:2	TF_8D3	Fine alignment for fourth falling edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	5:4	TR_8D4	Fine alignment for fifth rising edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	7:6	TF_8D4	Fine alignment for fifth falling edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	9:8	TR_8D5	Fine alignment for sixth rising edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	11:10	TF_8D5	Fine alignment for sixth falling edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	13:12	—	Reserved	Reserved Default = 00b	
239	1:0	TR_8D6	Fine alignment for seventh rising edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	Immediate
	3:2	TF_8D6	Fine alignment for seventh falling edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	5:4	TR_8D7	Fine alignment for eighth rising edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	7:6	TF_8D7	Fine alignment for eighth falling edge of data	00b-10b = Default 11b = Default – t_{MCKP}/64 01b = Default + t_{MCKP}/64 Default = 00b	
	13:8	—	Reserved	Reserved Default = 00 0000b	
240-254	—	—	Reserved	Reserved	—
255	7:0	RDADDR	—	Read back address	Immediate
	9:8	RDBACK	—	[8]: 0 = Serial out, 1 = Parallel out [9]: 0 = Disabled, 1 = Enable readout	
	13:10	—	Reserved	Reserved Default = 0000b	

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
VSP7502ZWV	PREVIEW	NFBGA	ZWV	159		TBD	Call TI	Call TI
VSP7502ZWVR	PREVIEW	NFBGA	ZWV	159		Pb-Free (RoHS)	SNAGCU	Level-2-260C-1 YEAR

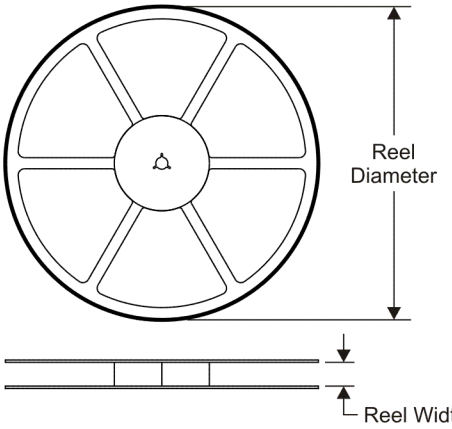
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

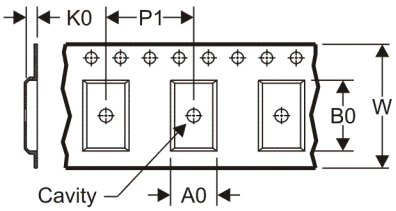
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

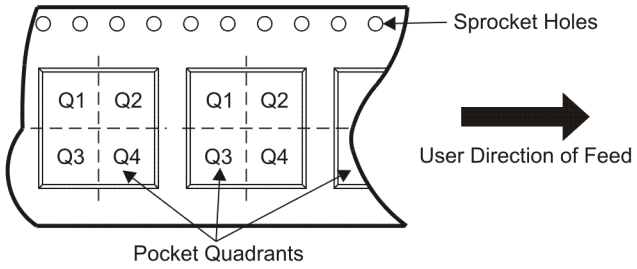


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

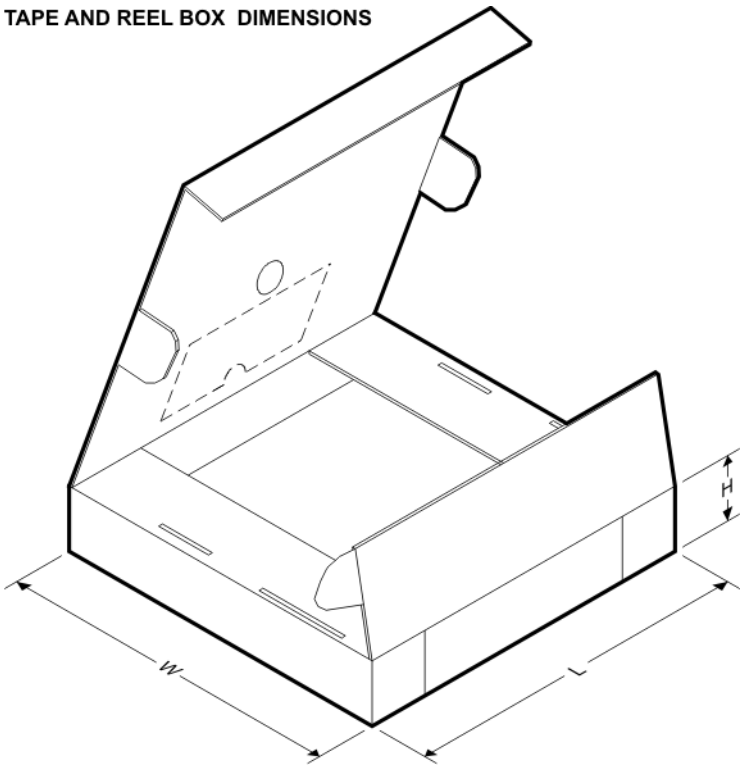
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP7502ZWVR	NFBGA	ZWV	159	0	330.0	16.4	7.3	7.3	2.2	12.0	16.0	Q1

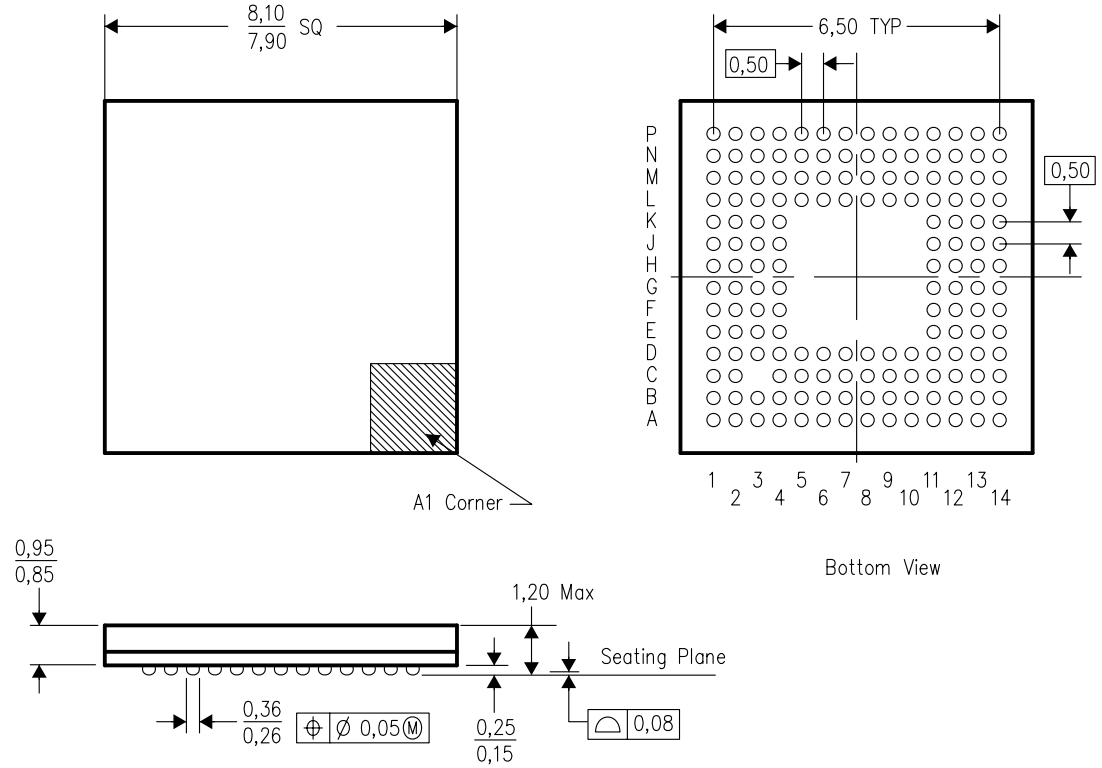
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP7502ZWVR	NFBGA	ZWV	159	0	342.0	336.0	34.0

ZWV (S–PBGA–N159) PLASTIC BALL GRID ARRAY



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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