Voltage Protection for 2-Series, 3-Series, or 4-Series Cell Li-Ion Batteries (Second-Level Protection)

Check for Samples: bq29440, bq2944L0, bq29449, bq2944L9

FEATURES

- **2-Series, 3-Series, or 4-Series Cell Secondary Protection**
- **External Capacitor-Controlled Delay Timer**
- **Low Power Consumption I_{CC} < 2 µA Typical [V_{CELL}(ALL) < $V_{PROTECT}$]**
- **High-Accuracy Overvoltage Protection: ±25 mV With T_A = 0°C to 60°C**
- **Fixed Overvoltage Protection Thresholds: 4.30 V, 4.35 V**
- **Small 8L QFN Package**

APPLICATIONS

- **Second-Level Protection in Li-Ion Battery Packs**
  - **Notebook Computers**
  - **Power Tools**
  - **Portable Equipment and Instrumentation**

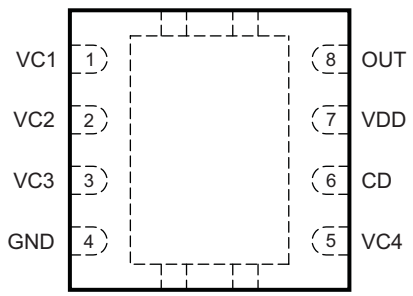
DESCRIPTION

The bq2944x is a secondary overvoltage protection IC for 2-series, 3-series, or 4-series cell lithium-ion battery packs that incorporates a high-accuracy precision overvoltage detection circuit.

FUNCTION

The voltage of each cell in a battery pack is compared to an internal reference voltage. If any cells reach an overvoltage condition, the bq2944x device starts a timer that provides a delay proportional to the capacitance on the CD pin. Upon expiration of the internal timer, the OUT pin changes from a low state to a high state. An optional latch configuration is available that holds the OUT pin in a high state indefinitely after an overvoltage condition has satisfied the specified delay timer period. The latch is released when the CD pin is shorted to GND.

DRB Package
(Top View)



P0012-02

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

TA	PART NUMBER	OUT PIN LATCH OPTION	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	OVP	ORDERING INFORMATION(2)	
							TAPE AND REEL (LARGE)(3)	TAPE AND REEL (SMALL)(4)
-40°C to +85°C	BQ29440	No	QFN-8	DRB	440	4.35 V	BQ29440DRBR	BQ29440DRBT
	BQ2944L0	Yes			44L0	4.35 V	BQ2944L0DRBR	BQ2944L0DRBT
	BQ29449	No			449	4.30 V	BQ29449DRBR	BQ29449DRBT
	BQ2944L9	Yes			44L9	4.30 V	BQ2944L9DRBR	BQ2944L9DRBT

(1) Example: bq2944L0DRBR is a device with the OUT latch option with a V_{OV} threshold of 4.35 V.
Contact Texas Instruments for other V_{OV} threshold options.
(2) For the most current package and ordering information, see the Package Addendum at the end of this document, or the TI website at www.ti.com.
(3) Large tape and reel quantity is 3,000 units.
(4) Small tape and reel quantity is 250 units.

THERMAL INFORMATION

THERMAL METRIC(1)		bq2944x DRB 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	50.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	25.1	
θ_{JB}	Junction-to-board thermal resistance (4)	19.3	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.7	
ψ_{JB}	Junction-to-board characterization parameter (6)	18.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	5.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

PIN FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
CD	6	Connection to external capacitor for programmable delay time
GND	4	Ground pin
OUT	8	Output
VC1	1	Sense voltage input for top cell
VC2	2	Sense voltage input for second-to-top cell
VC3	3	Sense voltage input for third-to-top cell
VC4	5	Sense voltage input for fourth-to-top cell (bottom cell)
VDD	7	Power supply

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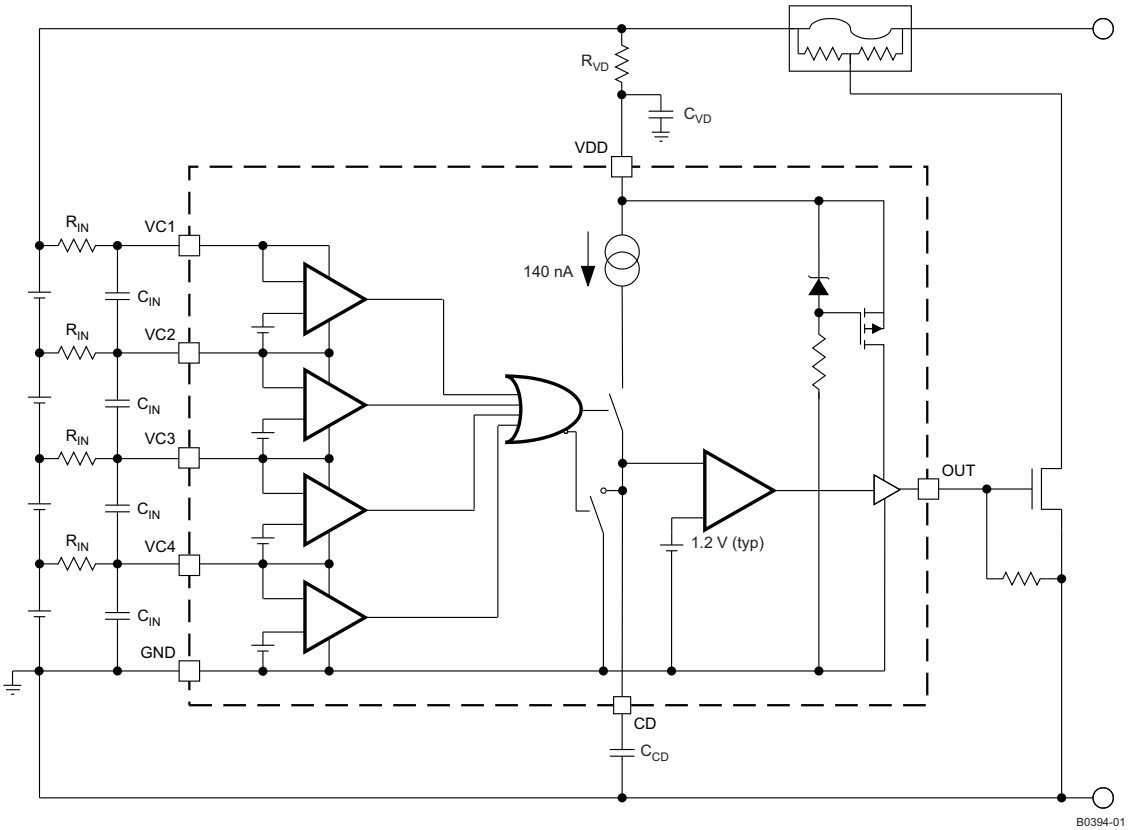
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE / UNITS
Supply voltage range, V_{MAX}	V_{DD}–GND	–0.3 to 28 V
Input voltage range, V_{IN}	VC1–GND, VC2–GND, VC3–GND	–0.3 to 28 V
	VC1–VC2, VC2–VC3, VC3–VC4, VC4–GND	–0.3 to 8 V
	CD–GND	–0.3 to 8 V
Output voltage range, V_{OUT}	OUT–GND	–0.3 to 28 V
Storage temperature range, T_{stg}		–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		25	V
Input voltage range	VC1–VC2, VC2–VC3, VC3–VC4, VC4–GND	0		5	V
$t_{d(CD)}$ delay-time capacitance	C_{CD} (See Figure 7.)		0.1		µF
Voltage monitor filter resistance	R_{IN} (See Figure 7.)	0.1	1		kΩ
Voltage monitor filter capacitance	C_{IN} (See Figure 7.)	0.01	0.1		µF
Supply voltage filter resistance	R_{VD} (See Figure 7.)	0.1		1	kΩ
Supply voltage filter capacitance	C_{VD} (See Figure 7.)		0.1		µF
Operating ambient temperature range, T_A		–40		110	°C

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ELECTRICAL CHARACTERISTICS

Typical values stated where T_A = 25°C and V_{DD} = 17 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 4 V to 25 V (unless otherwise noted).

PARAMETER			TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{PROTECT}$	Overvoltage detection voltage	bq29449			4.30		V
		bq29440			4.35		
V_{HYS}	Overvoltage detection hysteresis		For non-latch devices only	200	300	400	mV
V_{OA}	Overvoltage detection accuracy		T_A = 25°C	–10		10	mV
V_{OA_DRIFT} (1)	Overvoltage threshold temperature drift		T_A = 0°C to 60°C	–0.4		0.4	mV/°C
			T_A = –40°C to 110°C	–0.6		0.6	
X_{DELAY}	Overvoltage delay time scale factor		T_A = 0°C to 60°C Note: Does not include external capacitor variation	6.5	8.5	13	s/µF
			T_A = –40°C to 110°C Note: Does not include external capacitor variation	6.0	8.5	16	
X_{DELAY_CTM}	Overvoltage delay time scale factor in Customer Test Mode		See CUSTOMER TEST MODE.		0.08		s/µF
$I_{CD(CHG)}$	Overvoltage detection charging current		(See Figure 1.)		140		nA
$I_{CD(DSG)}$	Overvoltage detection discharging current		(See Figure 2.)		60		µA
V_{CD}	Overvoltage detection external capacitor comparator threshold				1.2		V
I_{CC}	Supply current		(VC1–VC2) = (VC2–VC3) = (VC3–VC4) = (VC4–GND) = 3.5 V (See Figure 3.)		2	3.5	µA
V_{OUT}	OUT pin drive voltage		(VC1–VC2), (VC2–VC3), (VC3–VC4) and (VC4–GND) = $V_{PROTECT}$MAX, V_{DD} = 20V, I_{OH} = 0 to -10 µA	6.5	8.0	9.5	V
			(VC1–VC2), (VC2–VC3), (VC3–VC4) and (VC4–GND) = $V_{PROTECT}$MAX, V_{DD} = 4V, I_{OL} = -10 µA, T_A = 0°C to 60°C	2.0	3.0	3.5	V
			(VC1–VC2), (VC2–VC3), (VC3–VC4) and (VC4–GND) = 4 V, I_{OL} = 0 µA			0.1	V
$I_{OUT(SHORT)}$	OUT short circuit current		OUT = 0 V, (VC1–VC2), (VC2–VC3), (VC3–VC4) or (VC4–GND) > $V_{PROTECT}$, V_{DD} = 18 V			4	mA
$t_{r(OUT)}$ (1)	OUT output rise time		C_L = 1 nF, V_{DD} = 4 V to 25 V, $V_{OH(OUT)}$ = 0 V to 5 V		5		µs
$Z_{O(OUT)}$ (1)	OUT output impedance				2		kΩ
I_{IN}	Input current at VCx pins		Measured at VC1, (VC1–VC2), (VC2–VC3), (VC3–VC4) and (VC4–GND) = 3.5 V, T_A = 0°C to 60°C (See Figure 3.)	–0.3		1.5	µA
			Measured at VC2, VC3 or VC4, (VC1–VC2), (VC2–VC3), (VC3–VC4) and (VC4–GND) = 3.5 V, T_A = 0°C to 60°C (See Figure 3.)	–0.3		0.3	µA

(1) Specified by design. Not 100% tested in production.

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TYPICAL CHARACTERISTICS

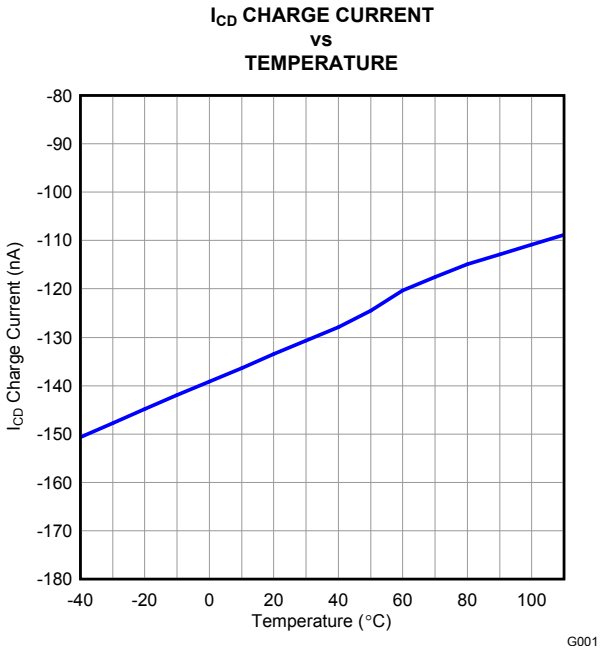

Figure 1. I_{CD} Charge Current

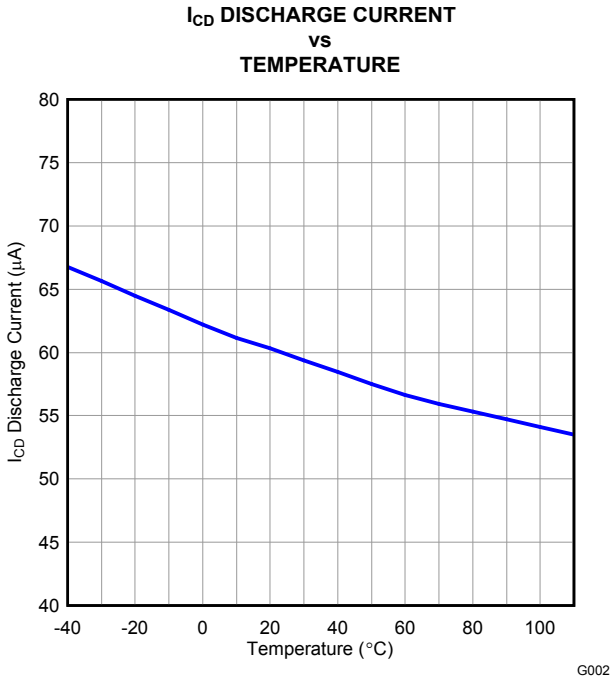

Figure 2. I_{CD} Discharge Current

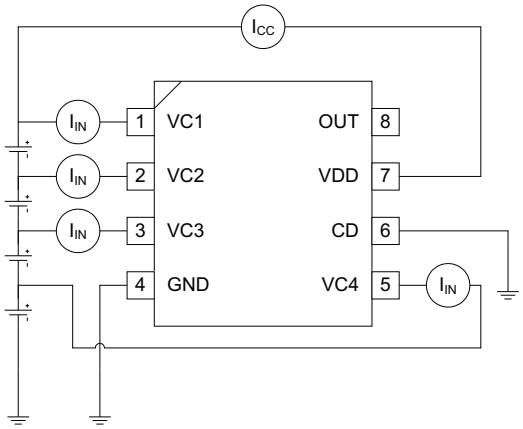

Figure 3. I_{CC}, I_{IN} Measurement

APPLICATIONS INFORMATION

PROTECTION (OUT) TIMING AND DELAY TIME CAPACITOR SIZING

The bq2944x uses an external capacitor to set delay timing during an overvoltage condition. When any of the cells exceed the overvoltage threshold, the bq2944x activates an internal current source of nominally 140 nA, which charges the external capacitor. When the external capacitor charges up to a voltage of nominally 1.2 V, the OUT pin transitions from a low state to a high state, by means of an internal pull-up network, to a regulated voltage of no more than 9.5 V when I_{OH} = 0 mA.

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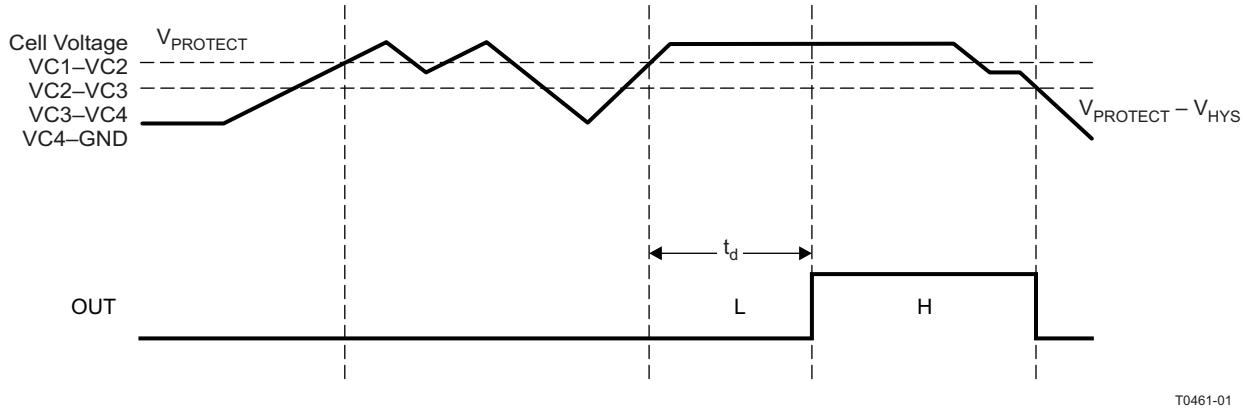

Figure 4. Timing for Overvoltage Sensing

Sizing the external capacitor is based on the desired delay time as follows:

$$c_{CD} = \frac{t_d}{x_{DELAY}}$$

Where t_d is the desired delay time and x_{DELAY} is the overvoltage delay time scale factor, expressed in seconds per microFarad. x_{DELAY} is nominally 8.5 s/µF. For example, if a nominal delay of 3 seconds is desired, the customer should use a CCD capacitor that is 3 s / 8.5 s/µF = 0.35 µF.

The delay time is calculated as follows:

$$t_d = \frac{[1.2\,V \times C_{CD}]}{I_{CD}}$$

If the cell overvoltage condition is removed before the external capacitor reaches the reference voltage, the internal current source is disabled and an internal discharge block is employed to discharge the external capacitor down to 0 V. In this instance, the OUT pin remains in a low state.

For latched versions of the bq2944x, if an overvoltage condition has caused the OUT pin to transition to a high state, the external capacitor remains charged even after the overvoltage condition has been removed. In this instance, the OUT pin remains in a high state.

For non-latched versions, the OUT pin is allowed to transition back from a high to low state when the overvoltage condition is no longer present, and the external capacitor is discharged down to 0 V.

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BATTERY CONNECTION FOR 2-SERIES, 3-SERIES, AND 4-SERIES CELL CONFIGURATIONS

Figure 5, Figure 6, and Figure 7 show the 2-series, 3-series, and 4-series cell configurations.

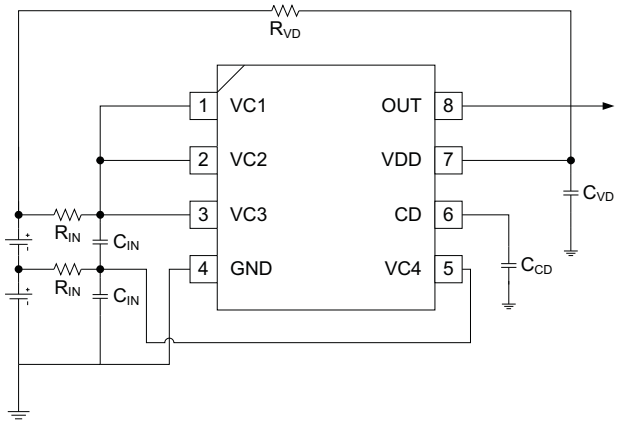

Figure 5. 2-Series Cell Configuration

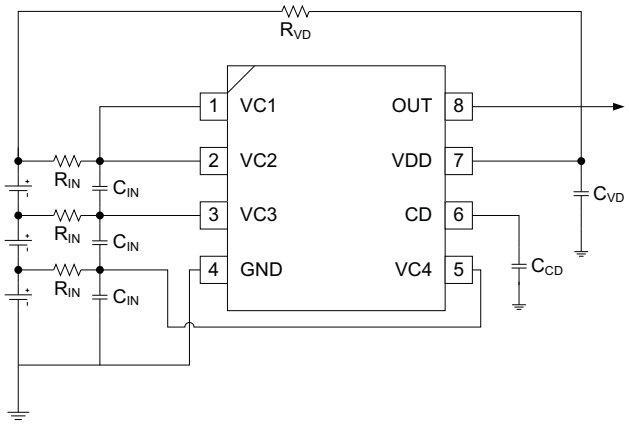

Figure 6. 3-Series Cell Configuration

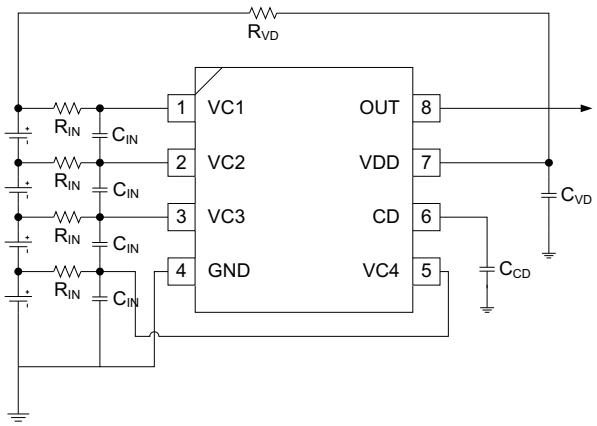

Figure 7. 4-Series Cell Configuration

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CELL CONNECTION SEQUENCE

The recommended cell connection sequence begins from the bottom of the stack, as follows:

1. GND
2. VC4
3. VC3
4. VC2
5. VC1

While not advised, connecting the cells in a sequence other than that described above does not result in errant activity on the OUT pin. For example:

1. GND
2. VC4, VC3, VC2, or VC1
3. Remaining VCx pin
4. Remaining VCx pin
5. Remaining VCx pin

It is also recommended that the overvoltage delay timing capacitor, C_{CD}, be propagated before connecting the cells.

CUSTOMER TEST MODE

Customer Test Mode (CTM) helps to greatly reduce the overvoltage detection delay time and enable quicker customer production testing. This mode is intended for quick-pass board-level verification tests, and, as such, individual cell overvoltage levels may deviate slightly from the specifications ($V_{PROTECT}$, V_{OA}). If accurate overvoltage thresholds are to be tested, use the standard delay settings that are intended for normal use.

To enter CTM, V_{DD} should be set to approximately 9.5 V higher than VC1. When CTM is entered, the device switches from the normal overvoltage delay time scale factor, x_{DELAY}, to a significantly reduced factor, x_{DELAY_CTM}, thereby reducing the delay time during an overvoltage condition. The CTM overvoltage delay time is similar to the equation presented in PROTECTION (OUT) TIMING AND DELAY TIME CAPACITOR SIZING with the substitution of x_{DELAY_CTM} in place of x_{DELAY}:

$$t_{d_CTM} = C_{CD} \times x_{DELAY_CTM}$$

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also, avoid exceeding Absolute Maximum Voltages for the individual cell voltages (VC1–VC2), (VC2–VC3), (VC3–VC4), and (VC4–GND). Stressing the pins beyond the rated limits may cause permanent damage to the device.

To exit CTM, the device should be powered off before being powered back on.

For latched versions of the bq2944x, the external C_{CD} capacitor must be externally discharged if any overvoltage functionality is exercised during protection testing. This can be accomplished by shorting the CD pin to GND. If the C_{CD} capacitor is not explicitly discharged, a residual charge may cause the overvoltage delay time to be inaccurate.

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REVISION HISTORY

Changes from Original (March 2010) to Revision A	Page
• Changed V_{OUT} first Test Condition - From: V_{DD} = 25V To: V_{DD} = 20V. MAX value From: 9.0 To 9.5	4

Changes from Revision A (March 2010) to Revision B	Page
• Changed the low power consumption value from 3 µA to 2 µA Typical	1
• Changed the Ordering Information	2
• Changed the Functional Block Diagram	3
• Changed the Electrical Characteristics	4
• Changed the Protection (Out) Timing Section to Protection (Out) Timing and Delay Time Capacitor Sizing	5
• Added the 2-series and 3-series cell configurations	7
• Added the Cell Connection Sequence Section	8
• Changed the Test Mode Section	8

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
BQ29440DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
BQ29440DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
BQ29449DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
BQ29449DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
BQ2944L0DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
BQ2944L0DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
BQ2944L9DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
BQ2944L9DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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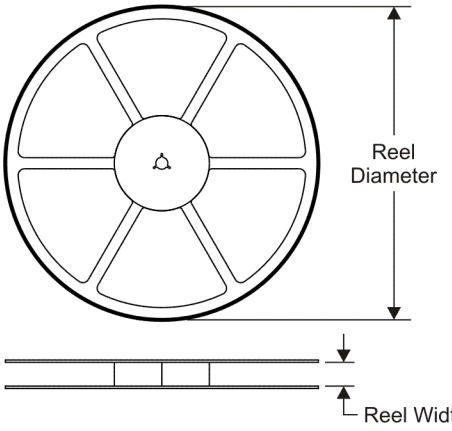
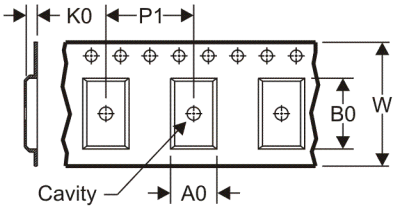
TAPE AND REEL INFORMATION

REEL DIMENSIONS

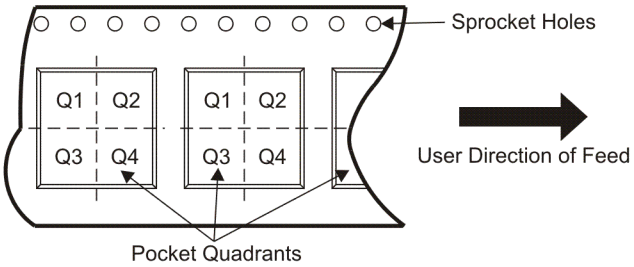


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29440DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29440DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29449DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29449DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ2944L0DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ2944L0DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ2944L9DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ2944L9DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

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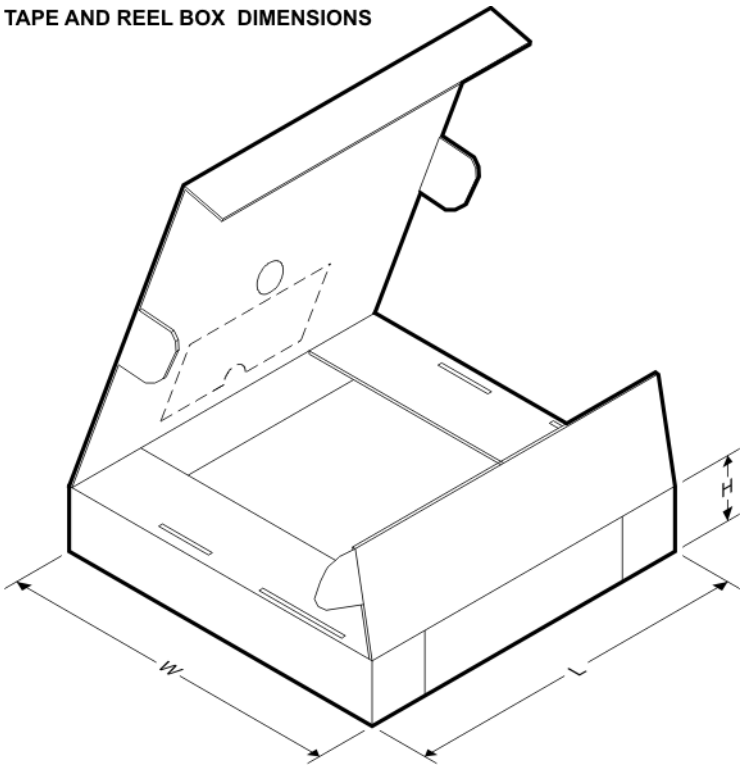
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29440DRBR	SON	DRB	8	3000	346.0	346.0	29.0
BQ29440DRBT	SON	DRB	8	250	190.5	212.7	31.8
BQ29449DRBR	SON	DRB	8	3000	346.0	346.0	29.0
BQ29449DRBT	SON	DRB	8	250	190.5	212.7	31.8
BQ2944L0DRBR	SON	DRB	8	3000	346.0	346.0	29.0
BQ2944L0DRBT	SON	DRB	8	250	190.5	212.7	31.8
BQ2944L9DRBR	SON	DRB	8	3000	346.0	346.0	29.0
BQ2944L9DRBT	SON	DRB	8	250	190.5	212.7	31.8

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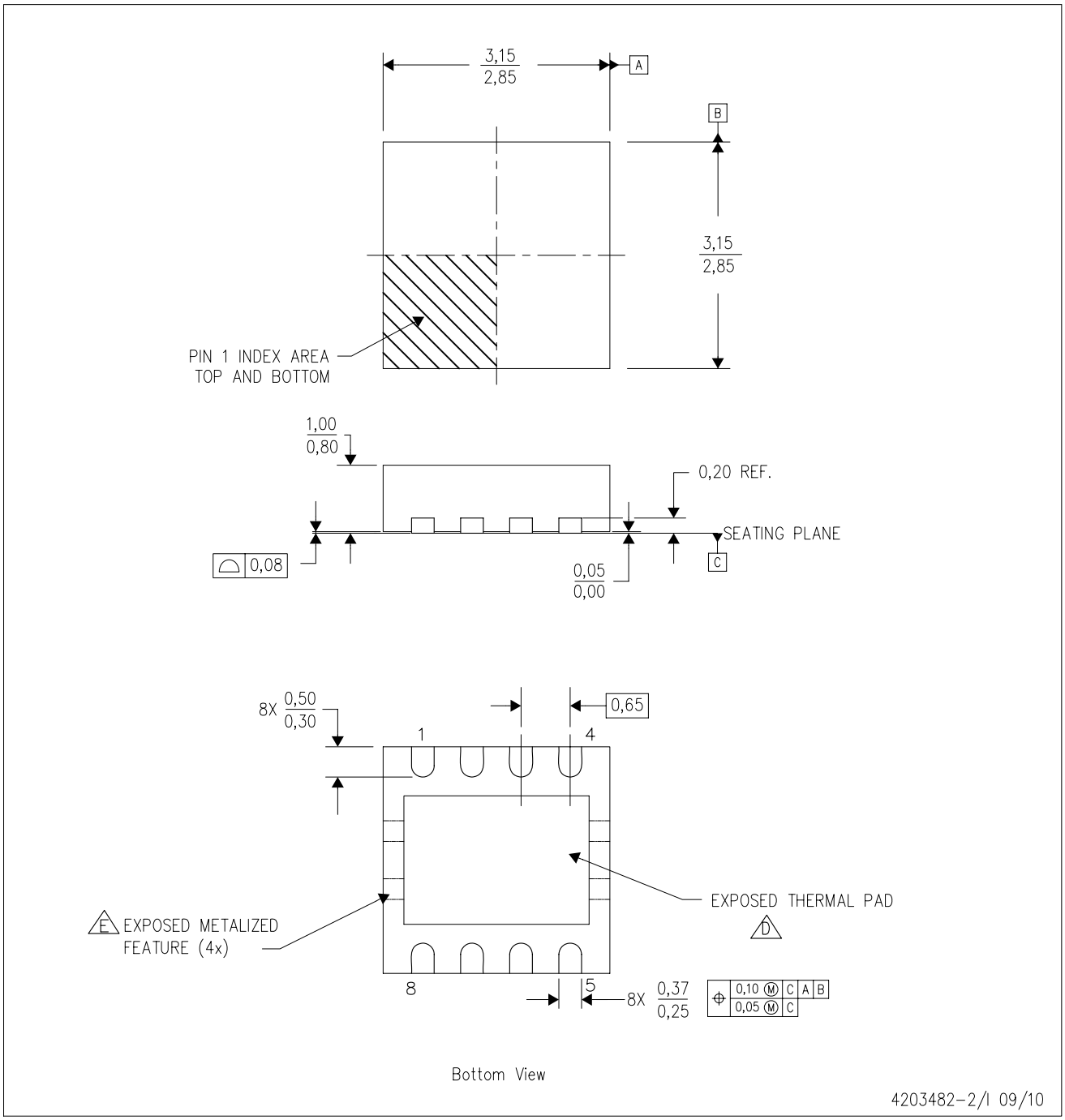
DRB (S-PVSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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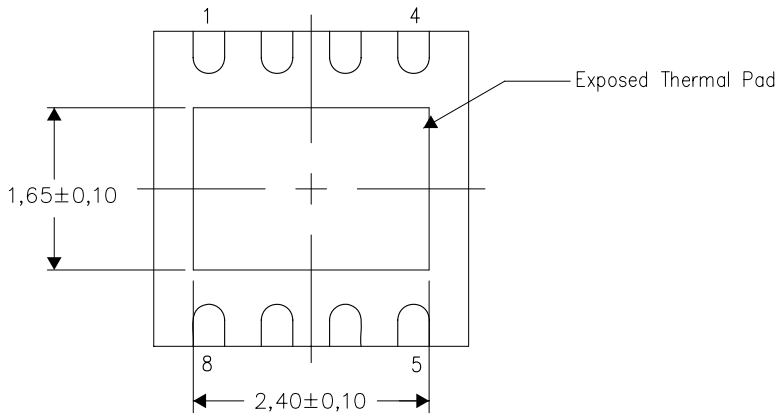
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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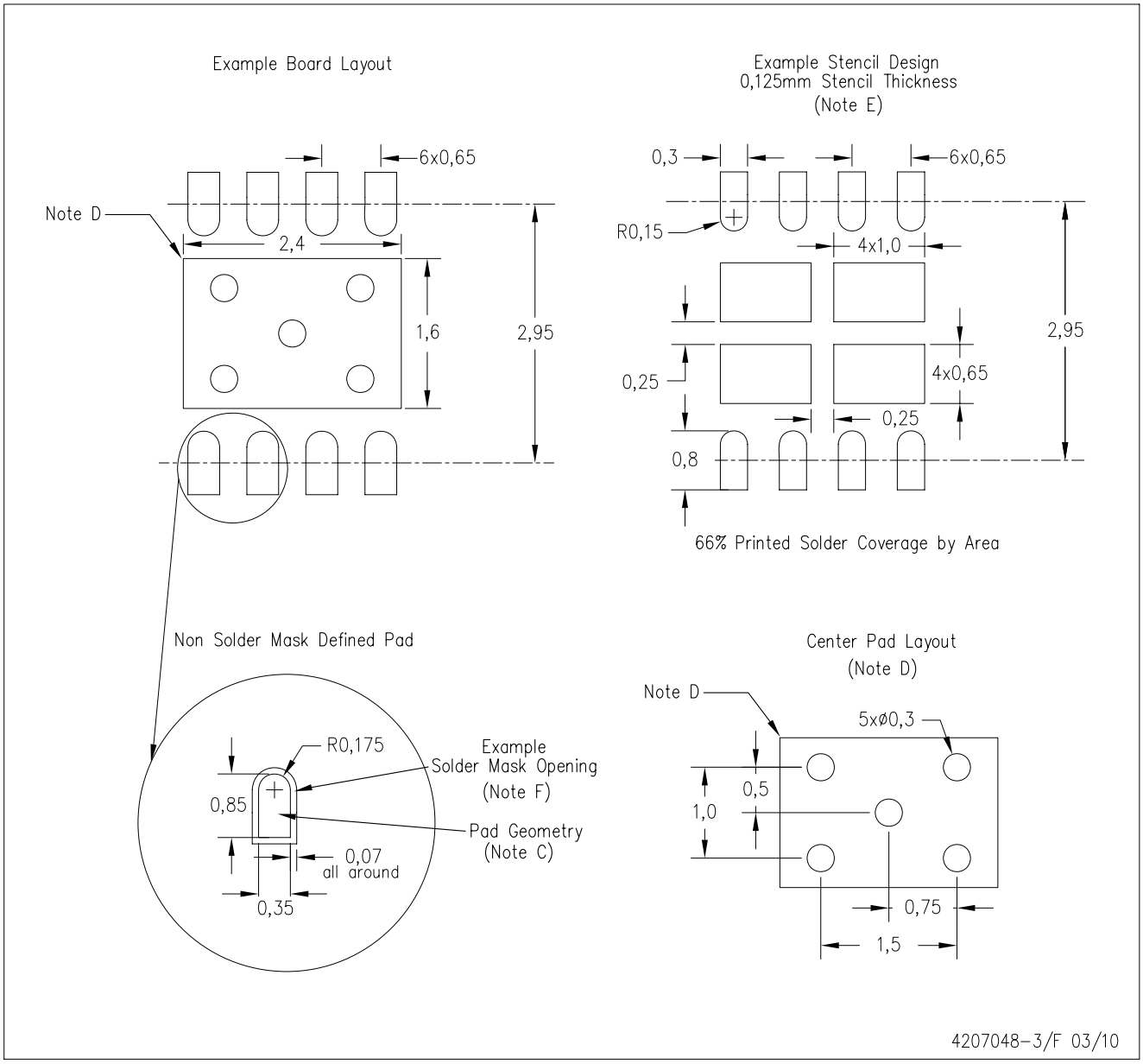
DRB (S-PVSON-N8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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