
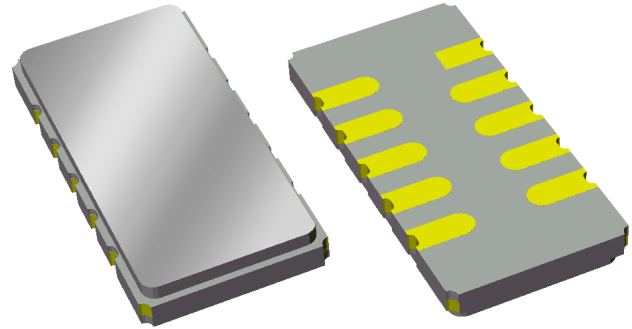


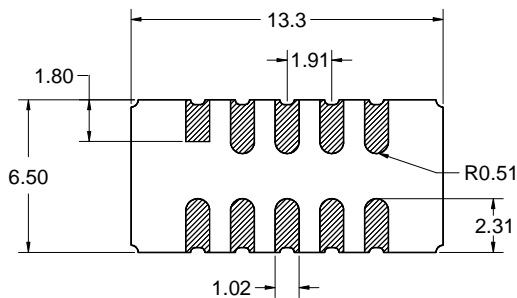
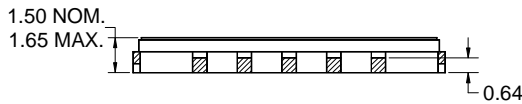
Features

- For broadband applications
- Typical 3 dB bandwidth of 8.2 MHz
- High attenuation
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Replaces Sawtek P/N 851917 (BW 3dB=8 MHz)
- Hermetic
- **RoHS** compliant (2002/95/EC), **Pb-free** 



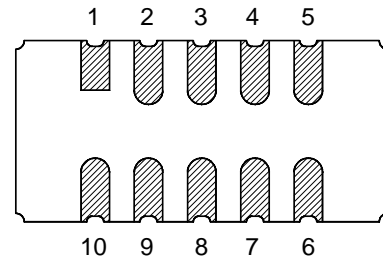
Package

Surface Mount 13.30 x 6.50 x 1.50 mm
SMP-53C



Pin Configuration

Bottom View



Single-ended Configuration

Pin No.	Description
10	RF Input
5	RF Output
1,6	Ground
2,3,4	Ground
7,8,9	Case Ground

Dimensions shown are nominal in millimeters
All tolerances are ± 0.15 mm except overall
length and width ± 0.10 mm

Body: Al_2O_3 ceramic
Lid: Kovar, Ni plated
Terminations: Au plating 0.5 - 1.0 μ m,
over a 2 - 6 μ m Ni plating

Electrical Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ 0 to +70 °C

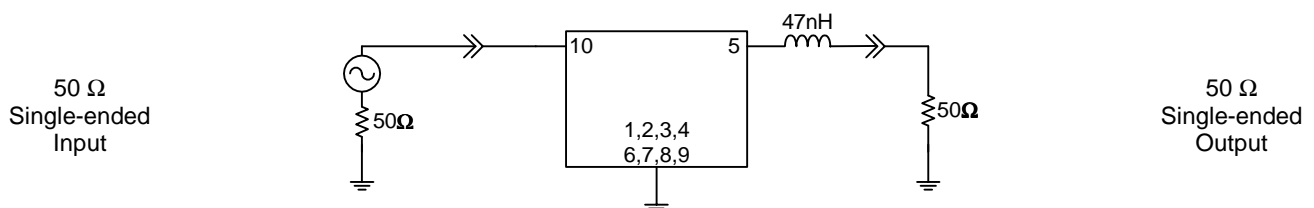
Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	140	-	MHz
Minimum Insertion Loss	-	23.4	24.6	dB
Lower 1 dB Bandedge ⁽⁵⁾	-	136.14	136.855	MHz
Upper 1 dB Bandedge	143.145	143.89	-	MHz
Lower 3 dB Bandedge ⁽⁵⁾	-	135.92	136.595	MHz
Upper 3 dB Bandedge	143.405	144.13	-	MHz
Lower 40 dB Bandedge ⁽⁵⁾	134.362	135.05	-	MHz
Upper 40 dB Bandedge	-	145.01	145.638	MHz
Amplitude Variation 136.855 - 143.145 MHz	-	0.44	0.83	dB
Phase Linearity 136.855 - 143.145 MHz	-	4	7.12	deg
Group Delay Variation 136.855 - 143.145 MHz	-	54	105	nsec
Absolute Delay	-	1.63	-	µsec
Relative Attenuation ⁽⁴⁾				
30 - 75 MHz	36.5	47	-	dB
75 - 130 MHz	43.5	50	-	dB
150 - 175 MHz	41.5	49	-	dB
175 - 275 MHz	49	55	-	dB
275 - 315 MHz	46.5	54	-	dB
315 - 350 MHz	48.5	57	-	dB
Substrate Material	-	YZ LiNbO ₃	-	-
Temperature Coefficient of Frequency	-	-94	-	ppm/°C
Source Impedance (single-ended) ⁽⁶⁾	-	50	-	Ω
Load Impedance (single-ended) ⁽⁶⁾	-	50	-	Ω

Notes:

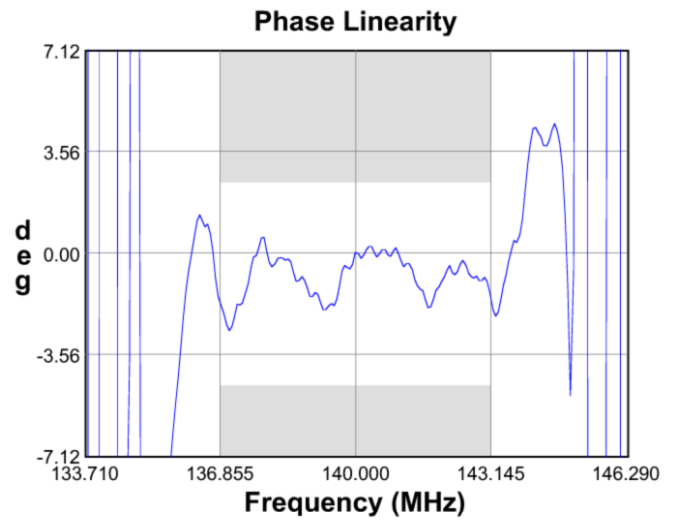
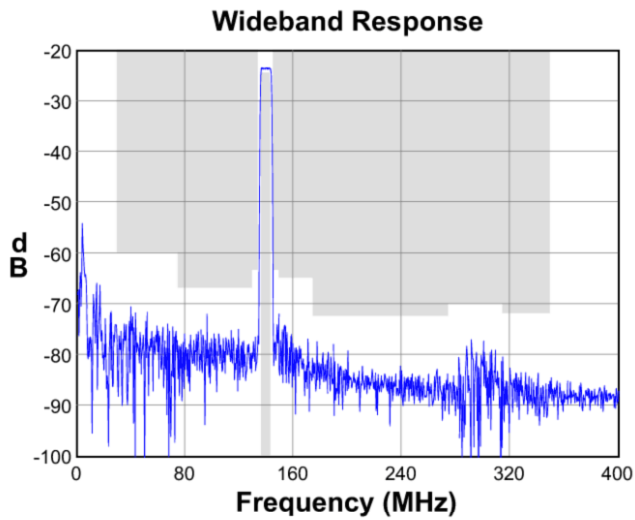
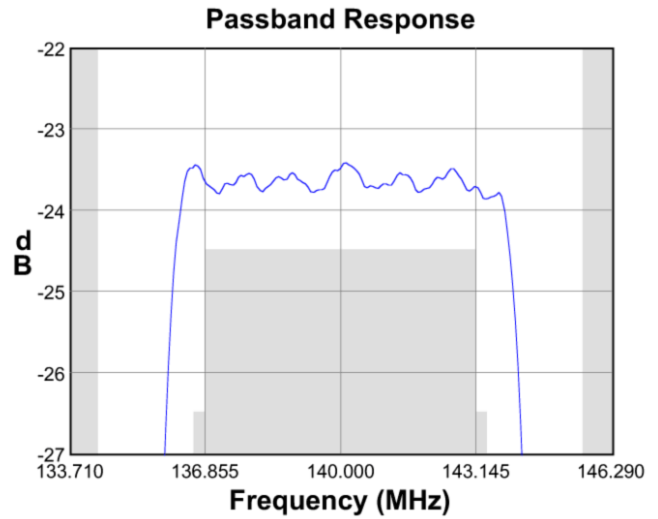
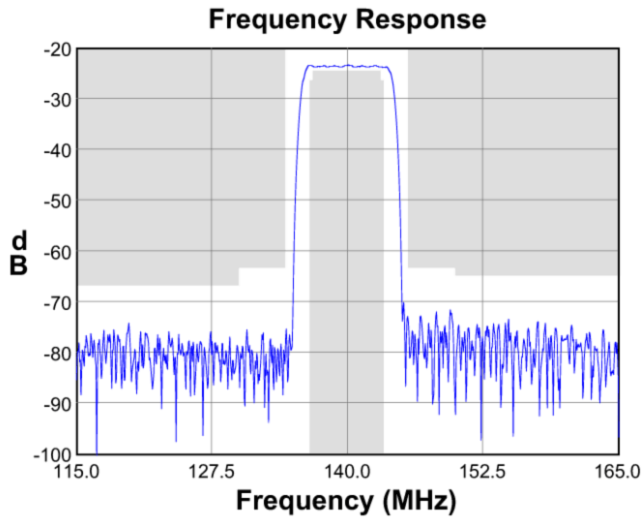
1. All specifications are based on the TriQuint test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. Relative to minimum insertion loss
6. This is the optimum impedance in order to achieve the performance shown

Test Circuit:

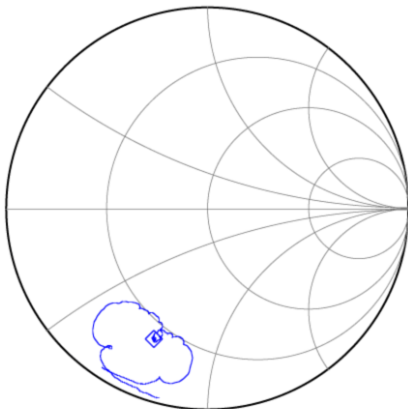
Actual matching values may vary due to PCB layout and parasitics



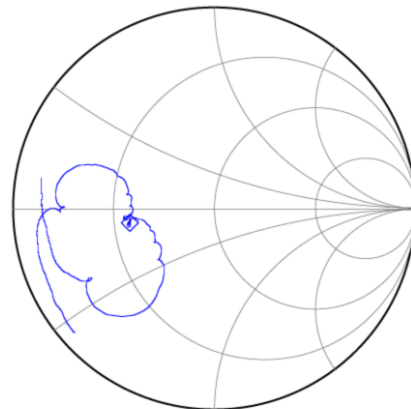
Typical Performance (at room temperature)



Input Smith Chart

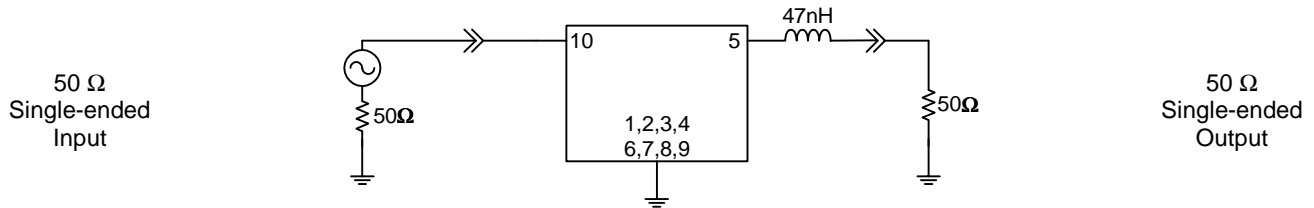


Output Smith Chart

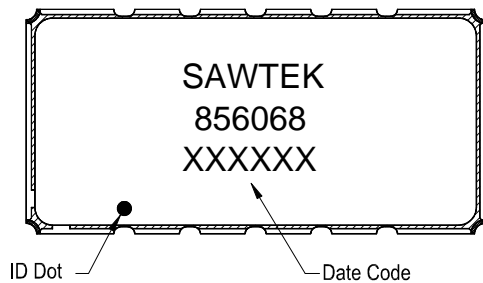


Matching Schematics

Actual matching values may vary due to PCB layout and parasitics

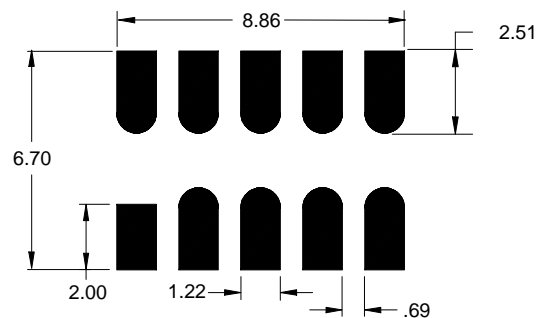


Marking



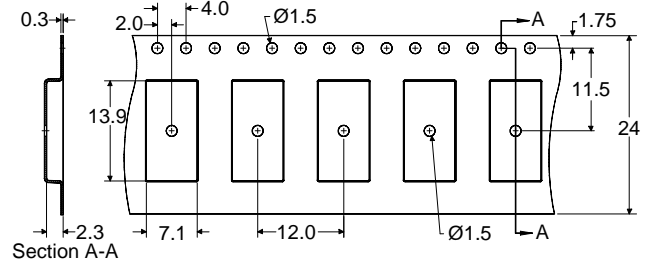
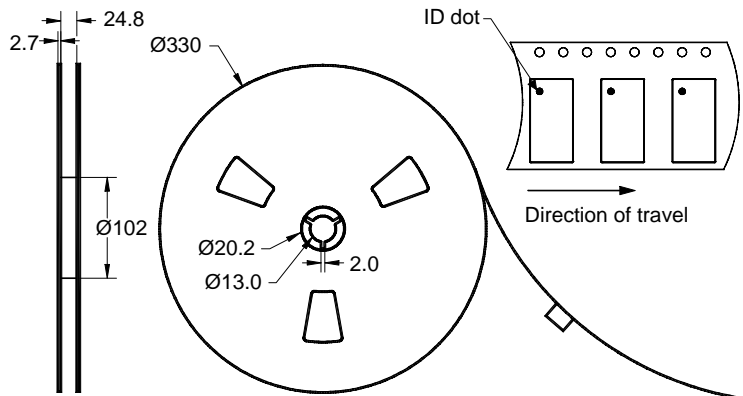
The date code consists of: day of the current year (Julian, 3 digits), last digit of the year (1 digit) and hour (2 digits)

PCB Footprint



This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel




Dimensions shown are nominal in millimeters
Packaging quantity: 2000 units/reel

Maximum Ratings


Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	0	+70	°C
Storage Temperature Range	T _{stg}	-40	+85	°C

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

Solderability

- Compatible with JESD22-B102, Pb-free process, 260C peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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