
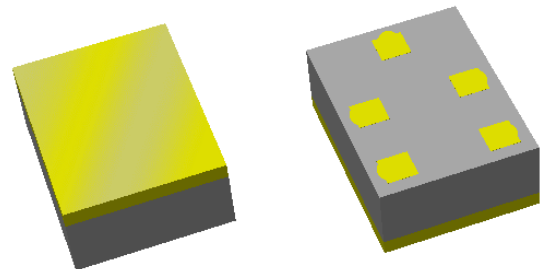


Preliminary Data Sheet

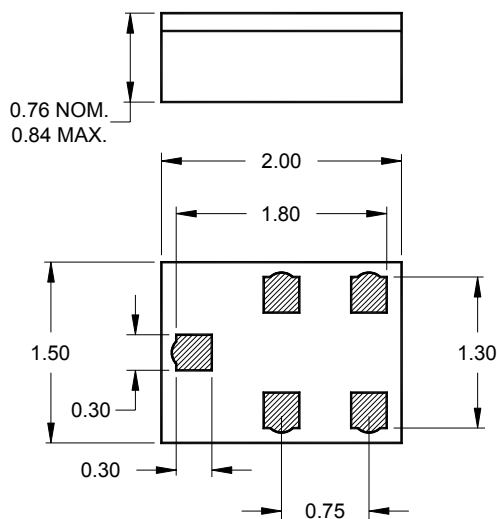
Features

- L2 filter for GPS applications
- Usable bandwidth of 20 MHz
- Low loss
- No impedance matching required for operation at 50Ω
- Ceramic Chip Scale Package (CSP)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



Package

Surface Mount 2.00 x 1.50 x 0.76 mm

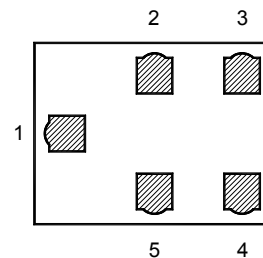


Dimensions shown are nominal in millimeters
All tolerances are ± 0.10 mm

Body: Al_2O_3 ceramic
Lid: Kovar or Alloy 42, Au over Ni plated
Terminations: Au plating 0.5 - 1.0μm,
over a 2 - 6μm Ni plating

Pin Configuration

Bottom View



Pin No.	Description
1	Input
4	Output
2,3,5	Case ground

Preliminary Data Sheet

Electrical Specifications ⁽¹⁾

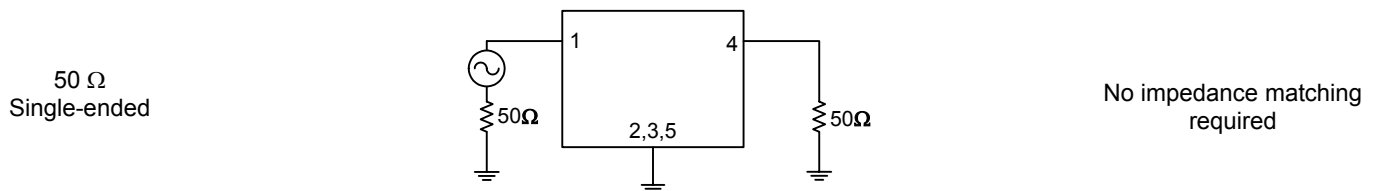
Operating Temperature Range: ⁽²⁾ -55 to +105 °C

Parameter ⁽³⁾	Minimum	Typical	Maximum	Unit
Center Frequency	-	1227.6	-	MHz
Minimum Insertion Loss	-	1.1	1.5	dB
3 dB Bandwidth	20	31	-	MHz
Absolute Attenuation				
300 - 1152 MHz	25	27	-	dB
1302 - 1900 MHz	25	33	-	dB
1900 - 3000 MHz	25	28	-	dB
Amplitude Ripple ⁽⁴⁾				
1217.6 - 1237.6 MHz	-	0.5	1.4	dB p-p
Absolute Group Delay				
1217.6 - 1237.6 MHz	16	21	26	ns
Group Delay Variation				
1217.6 - 1237.6 MHz	-	10	25	ns
Input/Output Return Loss				
1217.6 - 1237.6 MHz	9	10	-	dB
Source Impedance ⁽⁵⁾	-	50	-	Ω
Load Impedance ⁽⁵⁾	-	50	-	Ω

Notes:

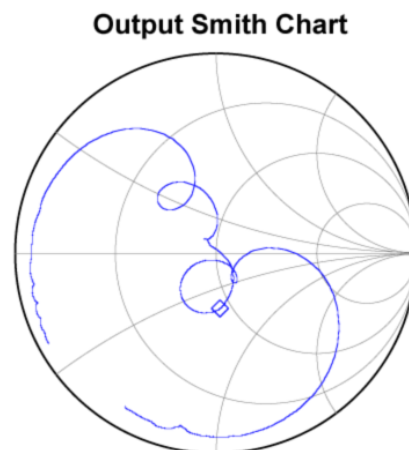
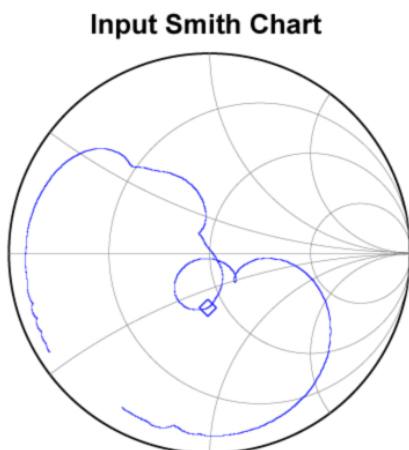
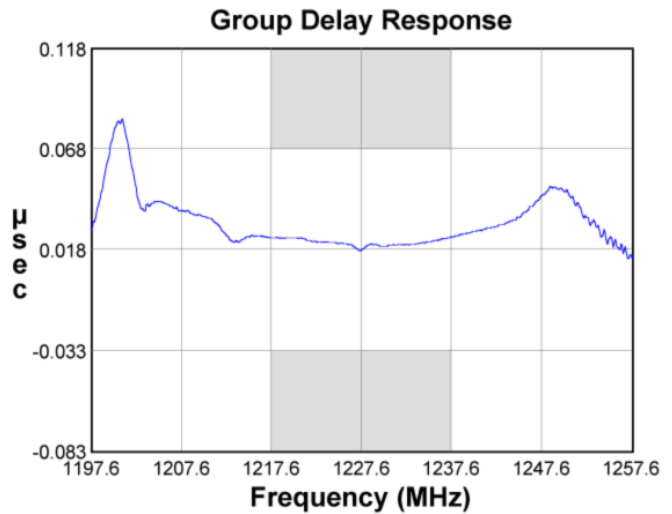
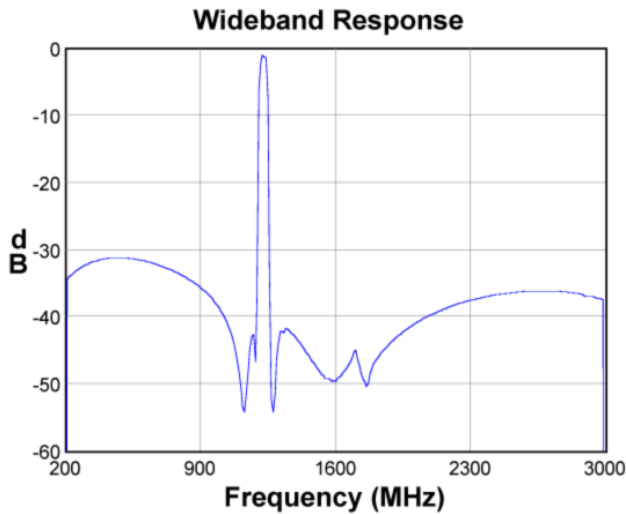
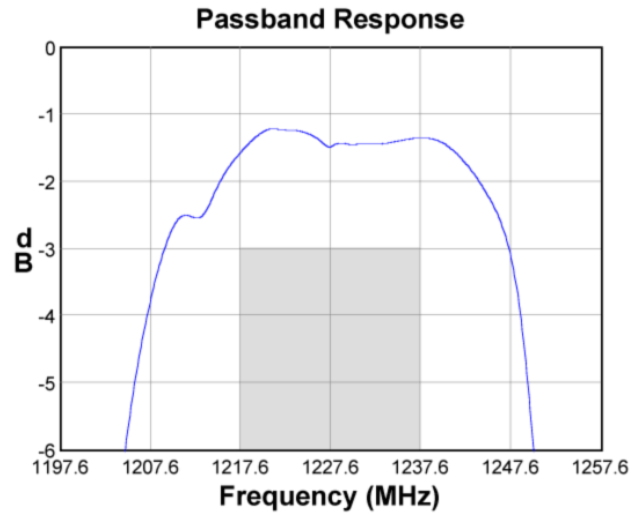
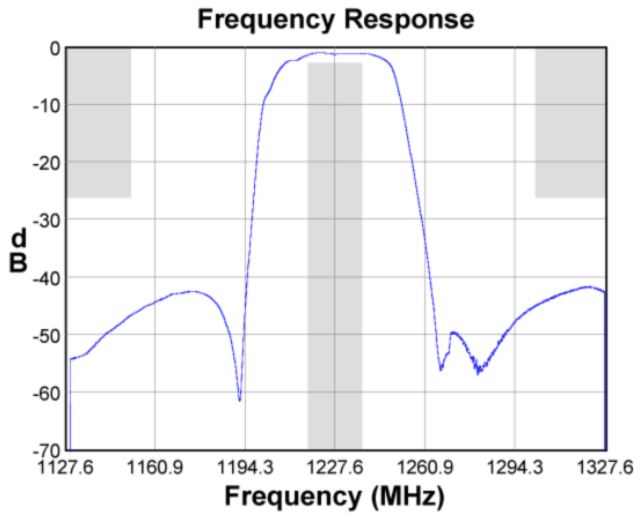
1. All specifications are based on the test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Maximum peak to adjacent valley measured over the indicated range
5. This is the optimum impedance in order to achieve the performance shown

Test Circuit:



Preliminary Data Sheet

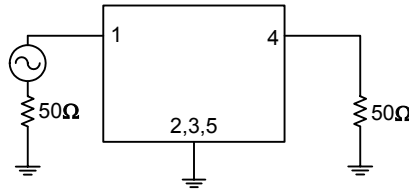
Typical Performance (at +25°C)



Preliminary Data Sheet

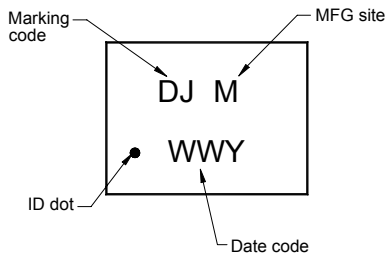
Matching Schematics

50 Ω
Single-ended

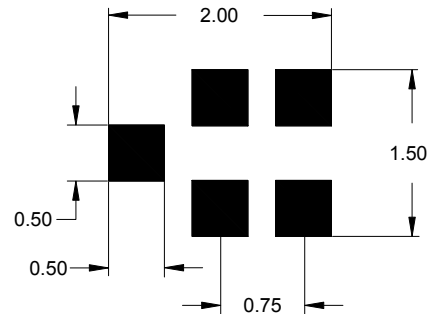


No impedance matching required

Marking **PCB Footprint**

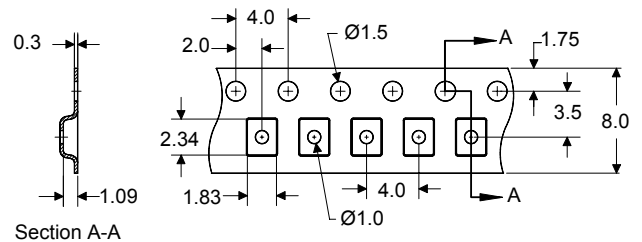
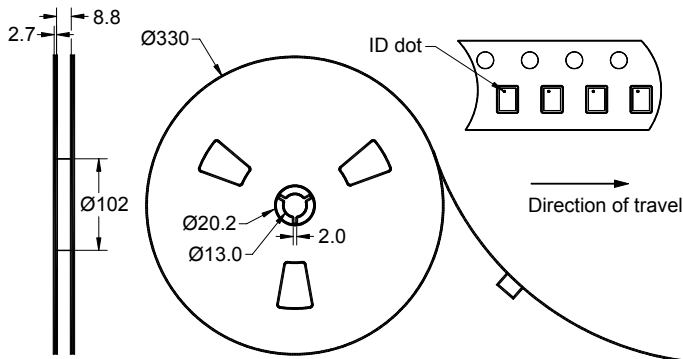


The date code consists of: WW = 2 digit week,
Y = last digit of year, M = manufacturing site code



This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel



Dimensions shown are nominal in millimeters
Packaging quantity: 10000 units/reel

Preliminary Data Sheet

Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-55	+105	°C
Storage Temperature Range	T _{stg}	-40	+85	°C

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD)
- Avoid ultrasonic exposure



RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS)



Solderability

- Compatible with JEDEC J-STD-020C **Pb-free** process, **260°C** peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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