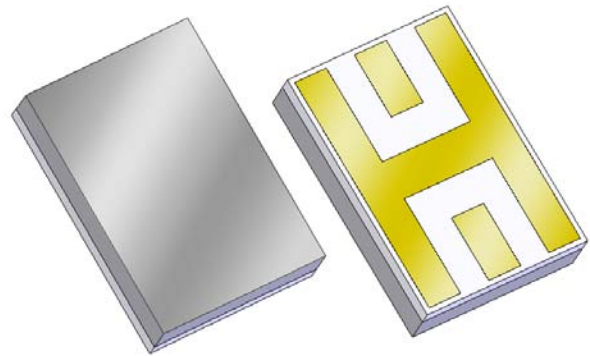


## Applications

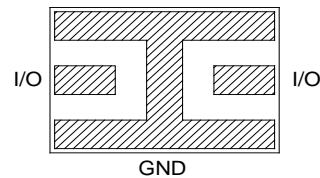
- For SSR/IFF Applications
- For high-selectivity applications



## Product Features

- Usable bandwidth 14.5 MHz
- Low loss
- High selectivity
- Single-ended operation
- Ceramic chip-scale Package (CSP)
- Small Size
- Hermetic **RoHS** compliant, **Pb-free**

## Functional Block Diagram



Overall width, length, and thickness are the only critical dimensions. All other dimensions are for reference only.

Dimensions shown are nominal in millimeters  
All tolerances are  $\pm 0.13\text{mm}$  except overall length and width  $\pm 0.25\text{mm}$

Body: *Sapphire*  
Package: *Alumina*

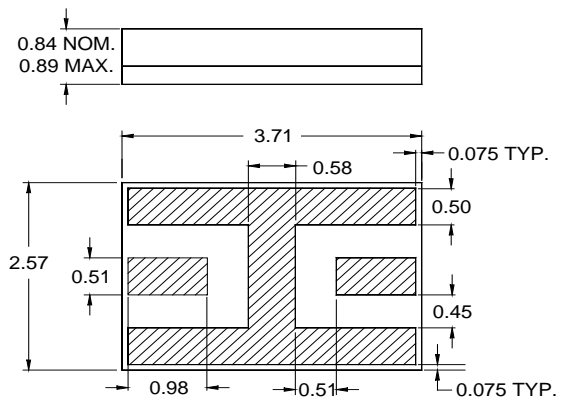
Terminations: *Au* plating 0.5 - 2.5 $\mu\text{m}$ , over a 2.0 - 6.0  $\mu\text{m}$  *Ni* plating

## Pin Configuration

Pin #	SE-Balanced	Description
I/O		Input/Output
GND		Ground

## Ordering Information

Part No.	Description
880367	packaged part
880367 Eval Board	evaluation board



## Specifications

### Electrical Specifications <sup>(1)</sup>

Specified Temperature Range: <sup>(2)</sup> -40 to +85 °C

Parameter <sup>(3)</sup>	Conditions	Min	Typical <sup>(4)</sup>	Max	Units
Center Frequency		-	1030	-	MHz
Maximum Insertion Loss	@ 1030 MHz	-	3.0	4.0	dB
3dB Bandwidth	Reference loss at 1030 MHz	14	20	-	MHz
40dB Lower Frequency Edge		1009	1013	-	MHz
40dB Upper Frequency Edge		-	1051	1046	MHz
VSWR	@ 1030 MHz	-	1.7	2.0	-
Source Impedance (single-ended) <sup>(5)</sup>		-	50	-	$\Omega$
Load Impedance (single-ended) <sup>(5)</sup>		-	50	-	$\Omega$

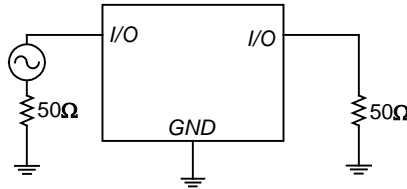
Notes:

1. All specifications are based on the TriQuint schematic for the main reference design shown on page 3
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. This is the optimum impedance in order to achieve the performance shown

## Reference Design

### Schematic

50  $\Omega$   
Single-ended  
Input

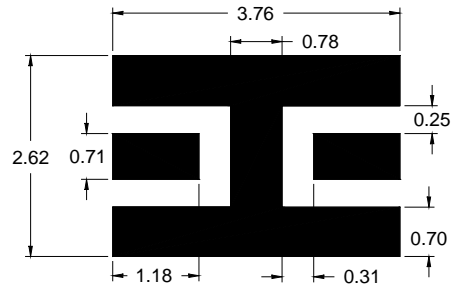


50  $\Omega$   
Single-ended  
Input

### PC Board

Refer to [PCB Layout](#) for more information.

### Mounting Configuration

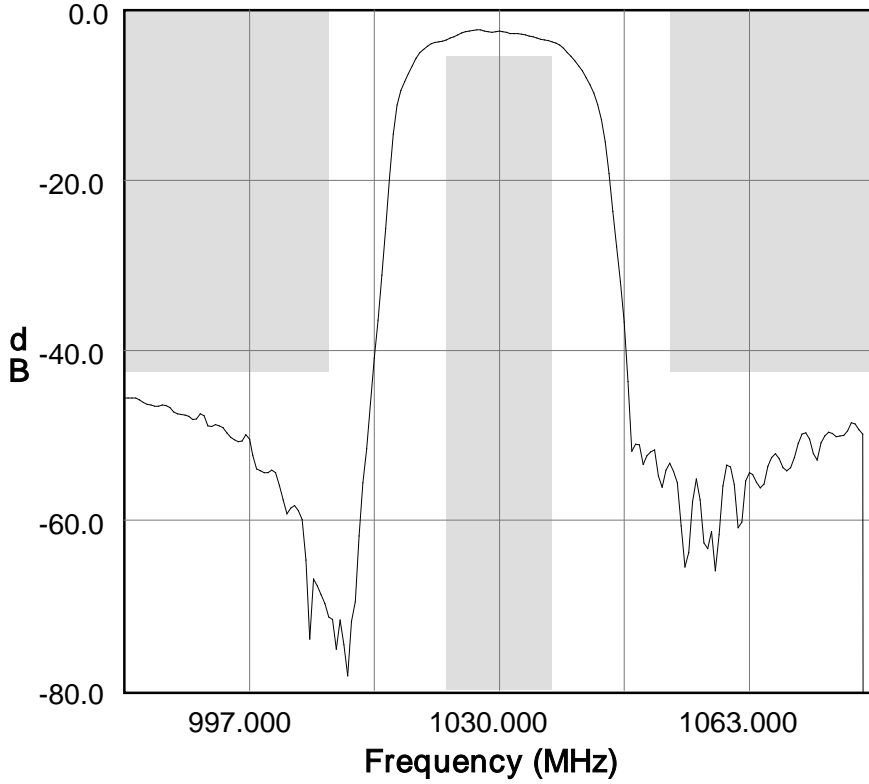


Notes:

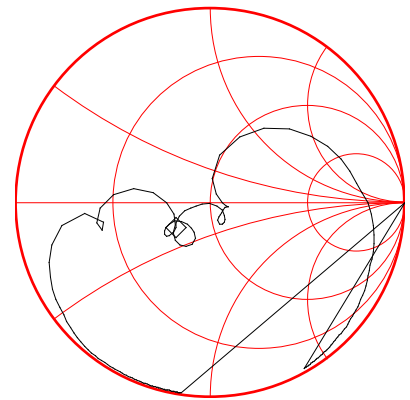
1. All dimensions are in millimeters.
2. This footprint represents a recommendation only.

**Typical Performance** (at room temperature)

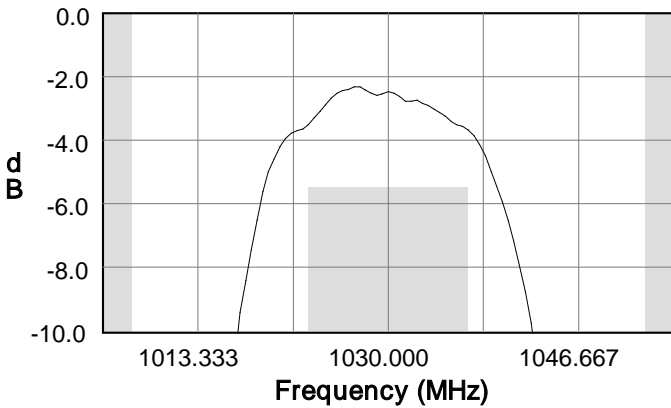
**S21 Amplitude Response**



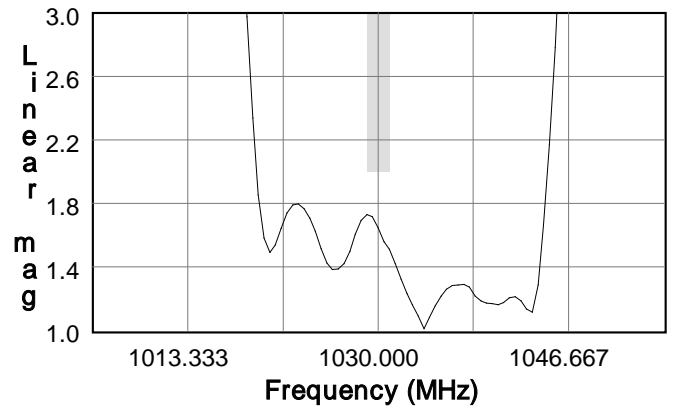
**S11 Smith Chart**



**S21 Amplitude Response**

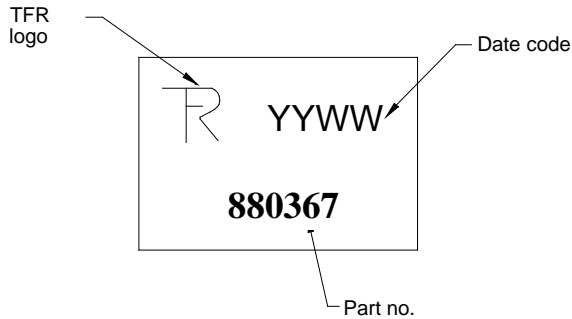


**S11 VSWR**



## Mechanical Information

### Marking



The date code consists of: YY = last digit of year,  
WW = 2 digit week

## Tape and Reel Information

Tape and Reel available upon request  
EIA-481

Tinning available per J-STD-001

### Absolute Maximum Ratings

Parameter	Rating
Operating Temperature	-40 to +85 °C
Storage Temperature	-55 to +100 °C
Maximum Input Power	+23 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

## Product Compliance Information

### ESD Information



#### Caution! ESD-Sensitive Device

Value: Passes  $\geq 8000$  V min.  
Test: Human Body Model (HBM)  
Standard: JEDEC Standard JESD22-A114

Value: Passes  $\geq 800$  V min.  
Test: Machine Model (MM)  
Standard: JEDEC Standard JESD22-A115

Refer to [ESD Sensitivity](#) for data

### Solderability

Compatible with the latest version of J-STD-020, lead free solder, 260°C

Refer to [Soldering Profile](#) for recommended guidelines.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free

## Contact Information

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