AH212

1 Watt High Linearity, High Gain InGaP HBT Amplifier

Product Features

- 1800 – 2400 MHz
- 24.7 dB Gain
- +30 dBm P1dB
- +46 dBm Output IP3
- +5V Single Positive Supply
- Internal Active Bias
- Lead-free/ RoHS-compliant SOIC-8 & 4x5mm DFN Package

Applications

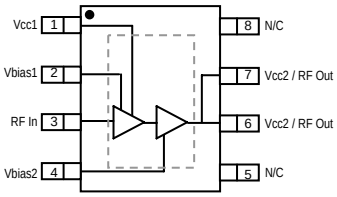
- Mobile Infrastructure
- WiBro Infrastructure
- TD-SCDMA

Product Description

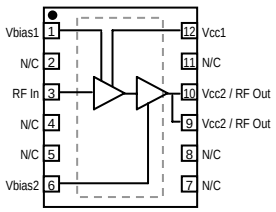
The AH212 is a high dynamic range two-stage driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve superior performance for various narrowband-tuned application circuits with up to +46 dBm OIP3 and +30 dBm of compressed 1-dB power. The amplifier is available in an industry-standard SMT lead-free/ RoHS-compliant SOIC-8 or 4x5mm DFN package. All devices are 100% RF and DC tested.

The product is targeted for use as linear driver amplifier for various current and next generation wireless technologies such as GPRS, GSM, CDMA, W-CDMA, TD-SCDMA, and WiBro, where high linearity and high power is required. The internal active bias allows the AH212 to maintain high linearity over temperature and operate directly off a +5 V supply.

Functional Diagram



AH212-S8G



AH212-EG

Specifications (1)

Parameters	Units	Min	Typ	Max
Operational Bandwidth	MHz	1800		2400
Test Frequency	MHz		2140	
Gain	dB	22.2	24.7	
Input Return Loss	dB		25	
Output Return Loss	dB		9	
Output P1dB	dBm	+29	+29.5	
Output IP3 (2)	dBm	+43.5	+46	
Noise Figure	dB		6.0	
W-CDMA Channel Power @ -45 dBc ACLR	dBm		+21	
Operating Current Range , Icc	mA	340	400	500
Stage 1 Amp Current, Icc1	mA		85	
Stage 2 Amp Current, Icc2	mA		315	
Device Voltage, Vcc	V		5	

1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. 3OIP measured with two tones at an output power of +15 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.

Typical Performance (1)

Parameters	Units	Typical	
Frequency	MHz	1960	2140
Gain (3)	dB	24.6	24.7
Input Return Loss	dB	12.5	25
Output Return Loss	dB	10	9
Output P1dB (3)	dBm	+30	+29.5
Output IP3	dBm	+48.0	+46
IS-95A Channel Power @ -45 dBc ACPR	dBm	+23.0	
W-CDMA Channel Power @ -45 dBc ACLR	dBm		+21
Noise Figure	dB	5.5	6.0
Supply Bias		+5 V @ 400 mA	

3. The performance is shown for the AH212-S8G (SOIC-8 package) at 25ºC. The AH212-EG in a 4x5 mm DFN package offers approximately 0.5dB more gain and 0.5 dB higher P1dB.

Absolute Maximum Rating

Parameter	Rating
Storage Temperature	-65 to +150 °C
RF Input Power (continuous)	+26 dBm
Device Voltage	+7 V
Device Current	900 mA
Device Power	5 W
Thermal Resistance, Rth	33 °C/W
Junction Temperature	+200 °C

Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

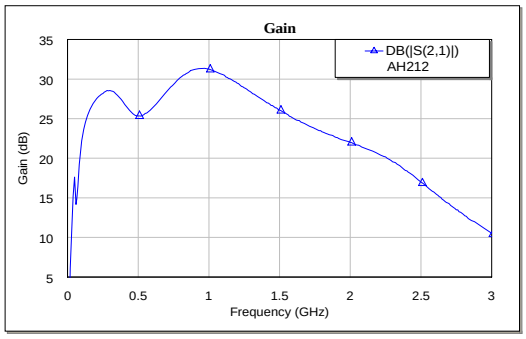
Part No.	Description
AH212-S8G	1 Watt, High Gain InGaP HBT Amplifier (lead-free/ RoHS-compliant SOIC-8 package)
AH212-EG	1 Watt, High Gain InGaP HBT Amplifier (lead-free/ RoHS-compliant 12-pin 4x5mm DFN package)
AH212-S8PCB1960	1960 MHz Evaluation Board
AH212-S8PCB2140	2140 MHz Evaluation Board
AH212-EPCB1960	1960 MHz Evaluation Board
AH212-EPCB2140	2140 MHz Evaluation Board

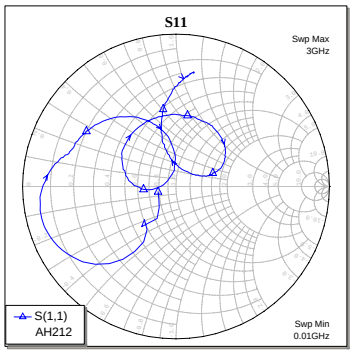
Standard tape / reel size = 500 pieces for SOIC-8 package on a 7" reel

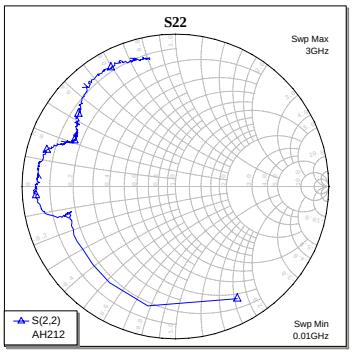
Standard tape / reel size = 1000 pieces for DFN package on a 7" reel.

Typical Device Data (SOIC-8)

S-Parameters (V_{CC} = +5 V, I_{CC} = 400 mA, T = 25 °C, calibrated to device leads)







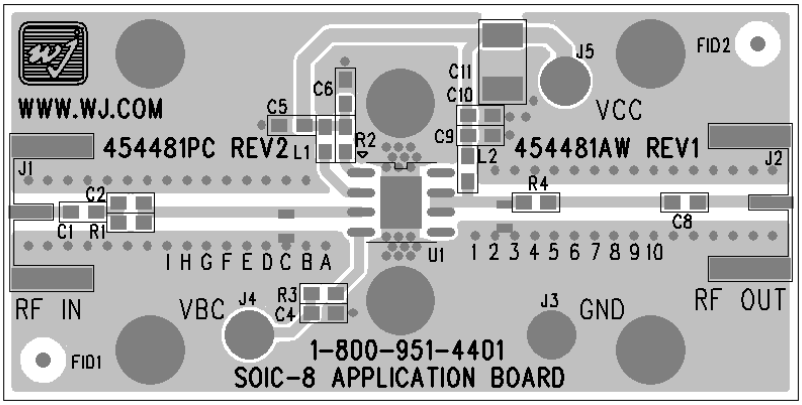
Notes:
The gain for the unmatched device in 50-ohm system is shown as the trace in blue color. For a band specific tuned circuit, it is expected that actual gain will be higher. The impedance plots are shown from 50 – 3000 MHz, with markers placed at 0.5 – 3.0 GHz in 0.5 GHz increment.

S-Parameters for AH212-S8G (V_{CC} = +5 V, I_{CC} = 400 mA, T = 25 °C, unmatched 50 ohm system, calibrated to device leads)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-9.19	-130.35	17.61	65.80	-64.44	122.93	-2.71	-145.39
100	-4.58	-125.96	21.86	69.36	-58.42	-135.96	-2.92	-160.72
200	-0.92	-169.81	27.39	14.98	-55.39	49.47	-3.04	-166.12
400	-2.81	160.59	26.96	-55.64	-50.75	78.75	-1.13	-169.23
600	-4.10	134.99	26.35	-69.83	-49.90	59.30	-0.86	-179.36
800	-10.08	97.76	30.19	-108.08	-46.20	44.46	-0.93	172.84
1000	-14.20	-174.16	31.30	-167.40	-49.63	25.99	-1.05	164.98
1200	-7.51	146.36	29.49	141.86	-44.88	48.15	-1.97	159.52
1400	-6.58	101.88	27.14	99.61	-45.19	29.86	-2.76	156.95
1600	-6.67	65.24	25.02	63.05	-46.75	33.97	-2.82	154.08
1800	-7.87	37.31	23.35	28.87	-47.96	24.08	-2.53	150.05
2000	-11.42	19.84	22.01	-5.81	-44.88	70.88	-2.08	143.86
2200	-18.51	69.85	20.56	-44.21	-40.54	52.01	-1.45	134.91
2400	-8.70	105.38	18.40	-84.80	-38.49	31.21	-1.02	123.57
2600	-4.43	93.47	15.61	-122.39	-38.94	23.84	-0.89	113.66
2800	-2.78	84.89	12.91	-156.41	-39.25	-2.01	-1.16	106.71
3000	-2.44	81.11	10.51	167.98	-38.27	0.70	-1.34	101.38

Device S-parameters are available for download from the website at: http://www.wj.com

Application Circuit PC Board Layout

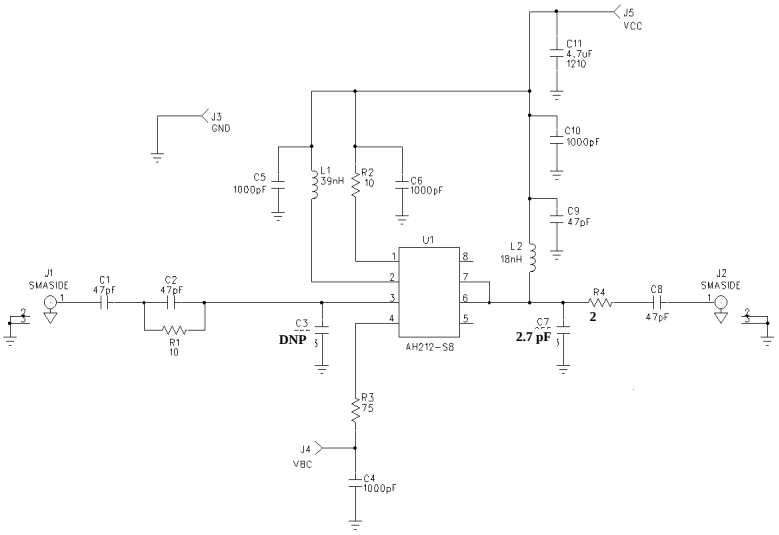


Circuit Board Material: .014” FR4, four layer, 1 oz copper, Microstrip line details: width = .026”, spacing = .026”
The silk screen markers ‘A’, ‘B’, ‘C’, etc. and ‘1’, ‘2’, ‘3’, etc. are used as placemarkers for the input and output tuning shunt capacitor – C7. The markers and vias are spaced in 0.050” increments.

AH212-S8 1850 MHz Reference Design

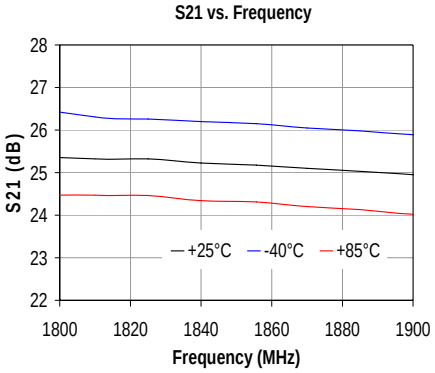
Typical RF Performance at 25 °C

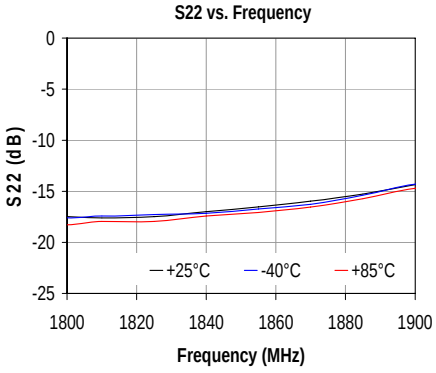
Frequency (MHz)	1800	1850	1900
Gain (dB)	25.4	25.1	25
Input Return Loss (dB)	10.5	12	12.5
Output Return Loss (dB)	15.5	15	13
Output P1dB (dBm)	+30.5	+30.5	+30
Output IP3 (dBm) (+15 dBm / tone, 1 MHz spacing)	+47	+47	+47.5
Noise Figure (dB)	5.8	5.8	5.9
Device / Supply Voltage	+5 V		
Quiescent Current	400 mA		

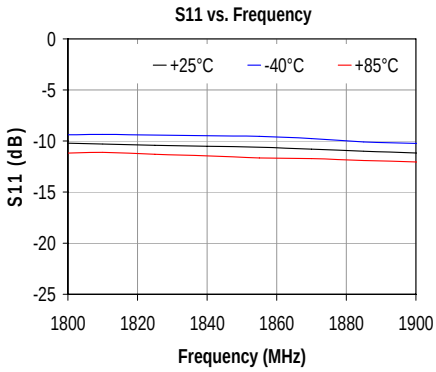


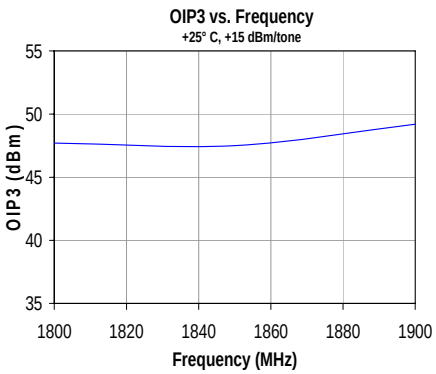
Notes:

1. C7 is placed at silkscreen marker '2' and '3' on tqs evalboard or @ 10 deg at 1.85 GHz away from pins 6 and 7.
2. All passive components are of size 0603 unless otherwise noted.





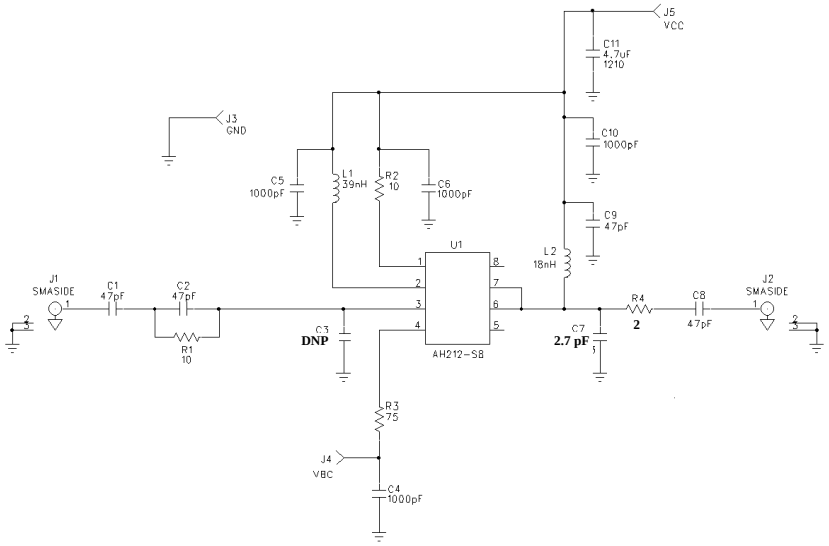




1960 MHz Application Circuit (AH212-S8PCB1960)

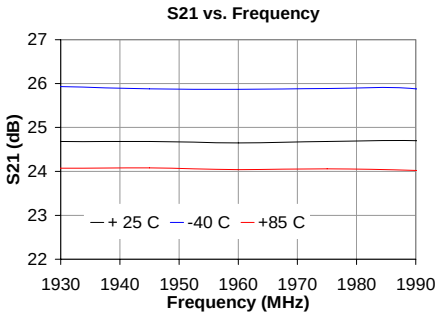
Typical RF Performance at 25 °C

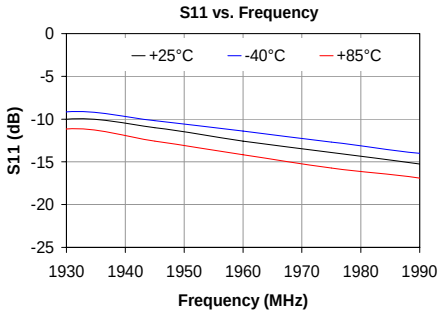
Frequency	1960 MHz
Gain	24.6 dB
Input Return Loss	12.5 dB
Output Return Loss	10 dB
Output P1dB	+30 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+48 dBm
Channel Power (@-45 dBc ACPR, IS-95, 9 channels fwd)	23 dBm
Noise Figure	5.5 dB
Device / Supply Voltage	+5 V
Quiescent Current	400 mA

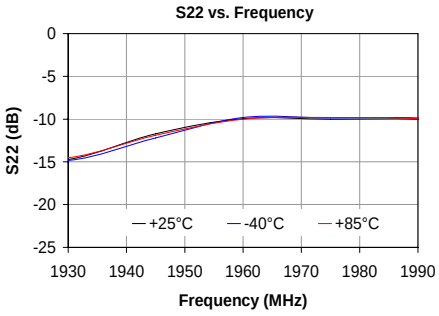


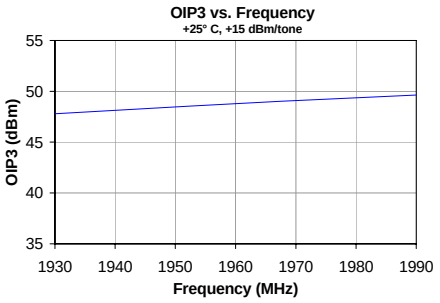
Notes:

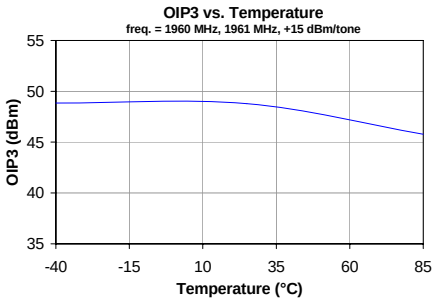
1. C7 is placed at silkscreen marker '2' and '3' on tqs evalboard or @14 deg at 1.96 GHz away from pins 6 and 7.
2. All passive components are of size 0603 unless otherwise noted.

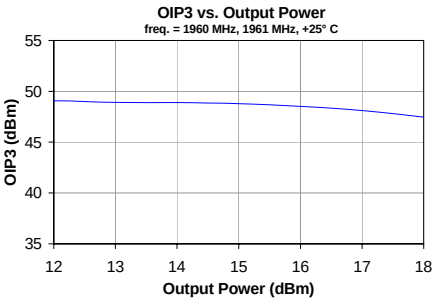


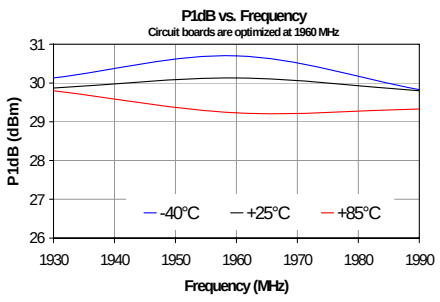


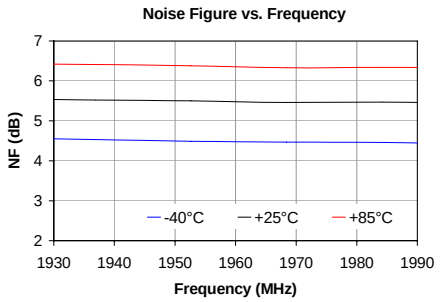


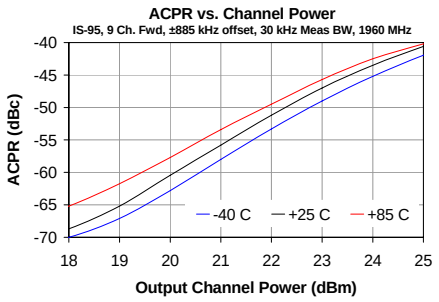








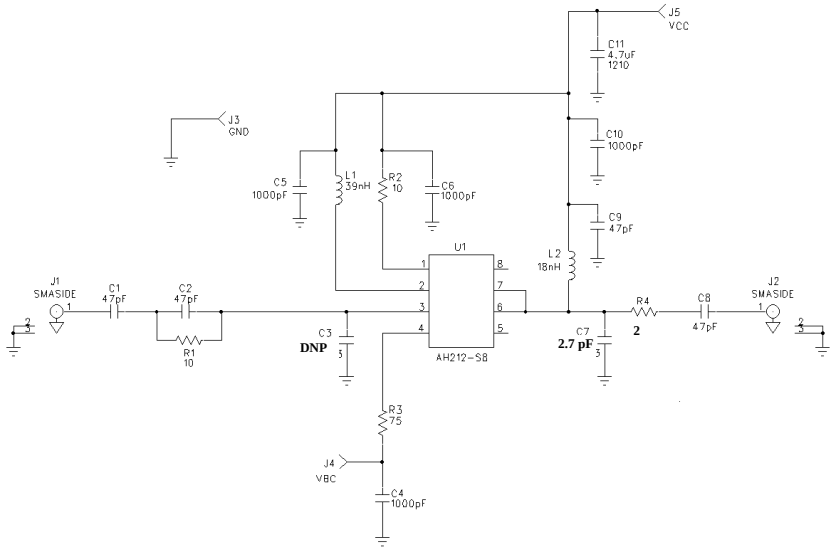




AH212-S8 2015 MHz Reference Design for TD-SCDMA Applications

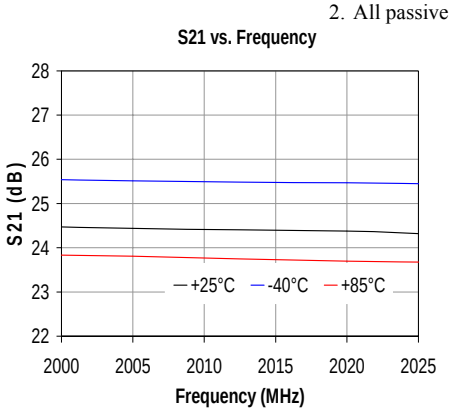
Typical RF Performance at 25 °C

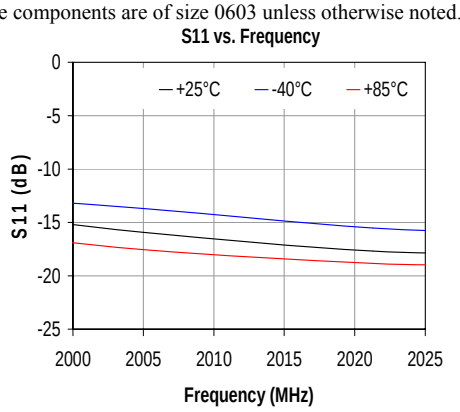
Frequency (MHz)	2010	2025
Gain (dB)	24.6	24.3
Input Return Loss (dB)	16	18
Output Return Loss (dB)	9.5	9
Output P1dB (dBm)	+30	+30
Output IP3 (dBm) (+15 dBm / tone, 1 MHz spacing)	+47	46.6
Channel Power (dBm) (@-45 dBc ACPR, IS-95, 9 channels fwd)	23	23
Noise Figure (dB)	6	6
Device / Supply Voltage	+5 V	
Quiescent Current	400 mA	

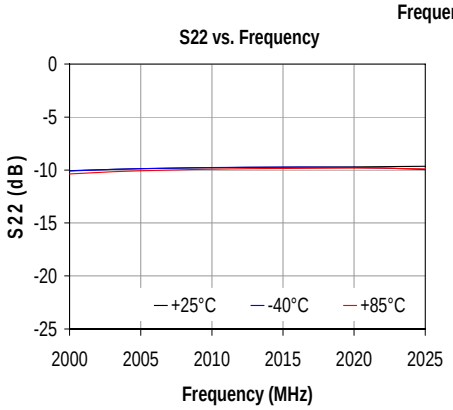


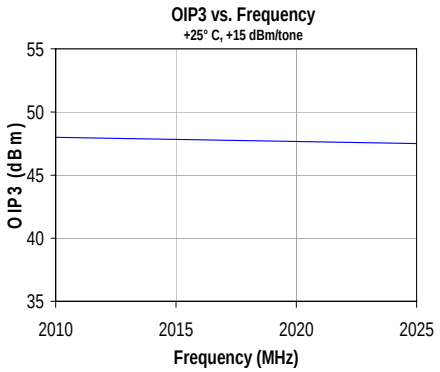
Note:

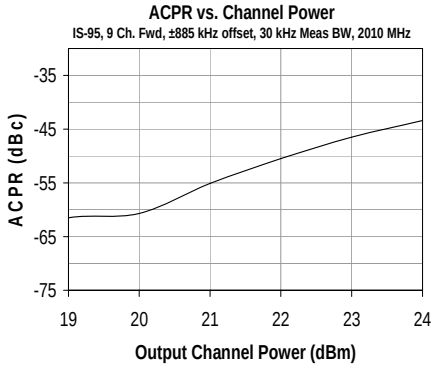
1. C7 is placed at silkscreen marker '2' and '3' on tqs evalboard or @17 deg at 2.015 GHz away from pins 6 and 7.
2. All passive components are of size 0603 unless otherwise noted.







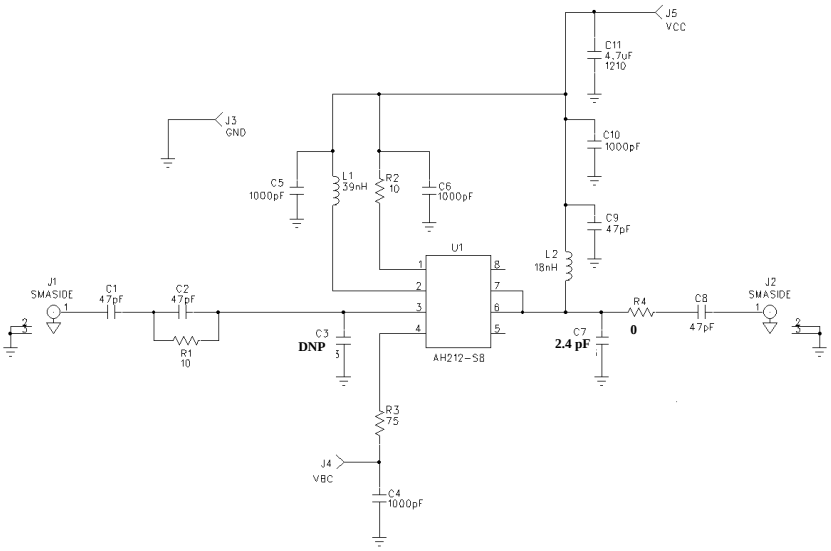




2140 MHz Application Circuit (AH212-S8PCB2140)

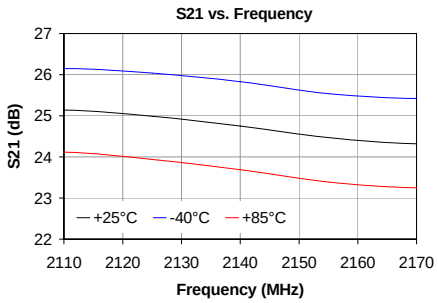
Typical RF Performance at 25 °C

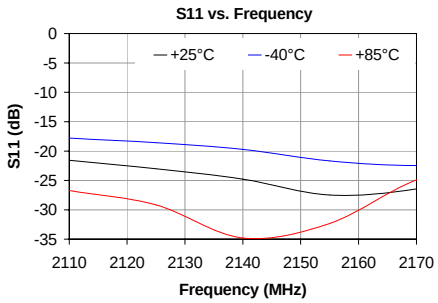
Frequency	2140 MHz
Gain	24.7 dB
Input Return Loss	25 dB
Output Return Loss	9 dB
Output P1dB	+29.5 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+46 dBm
Channel Power (@-45 dBc ACLR, W-CDMA, TM64 DPCH)	+21 dBm
Noise Figure	6 dB
Device / Supply Voltage	+5 V
Quiescent Current	400 mA

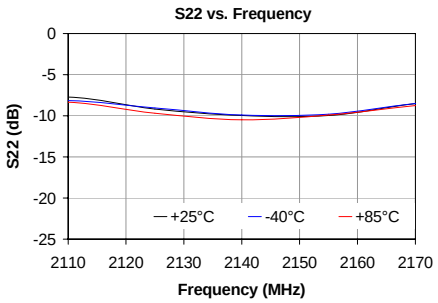


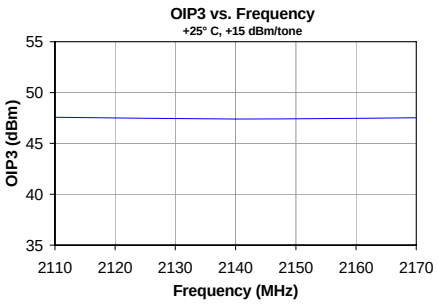
Notes:

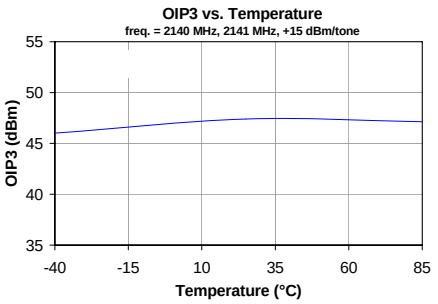
1. C7 is placed at silkscreen marker '2' on tqs evalboard or @12.2 deg at 2.14 GHz away from pins 6 and 7. DNP C3.
2. All passive components are of size 0603 unless otherwise noted.

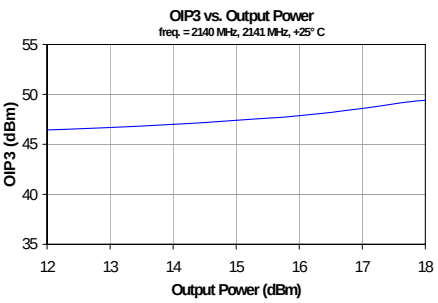


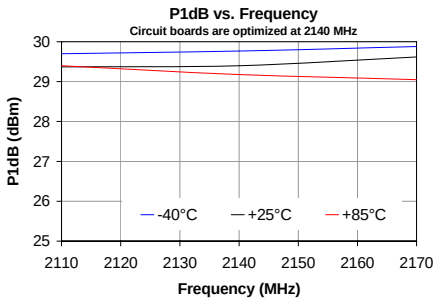


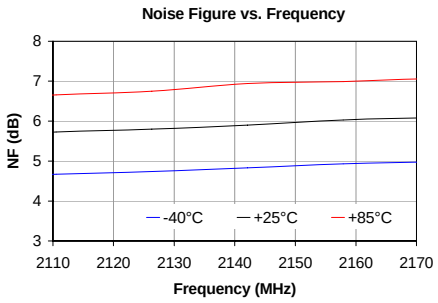


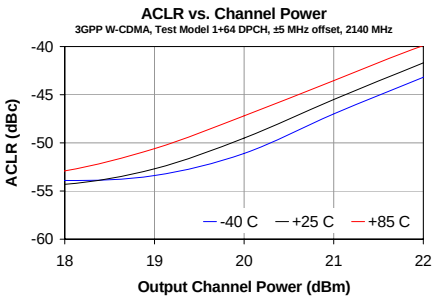








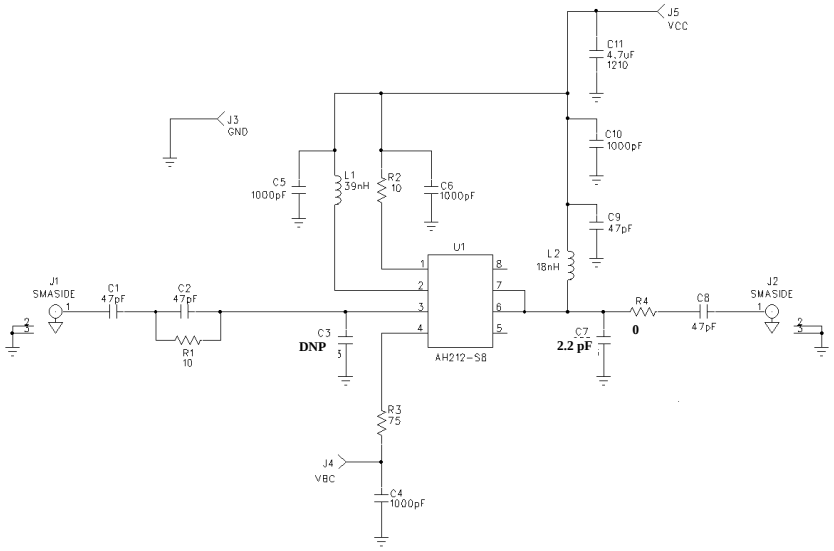




AH212-S8 2350 MHz Reference Design for WiBro Applications

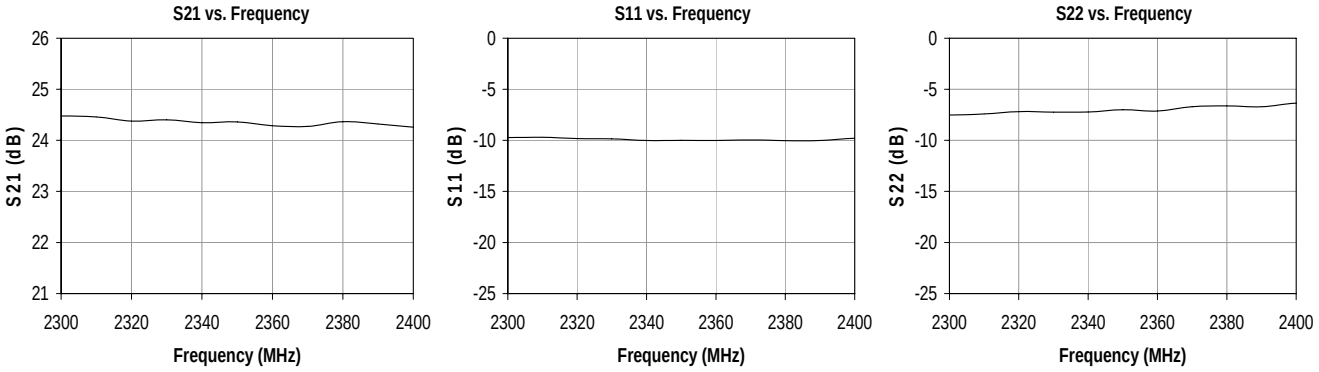
Typical RF Performance at 25 °C

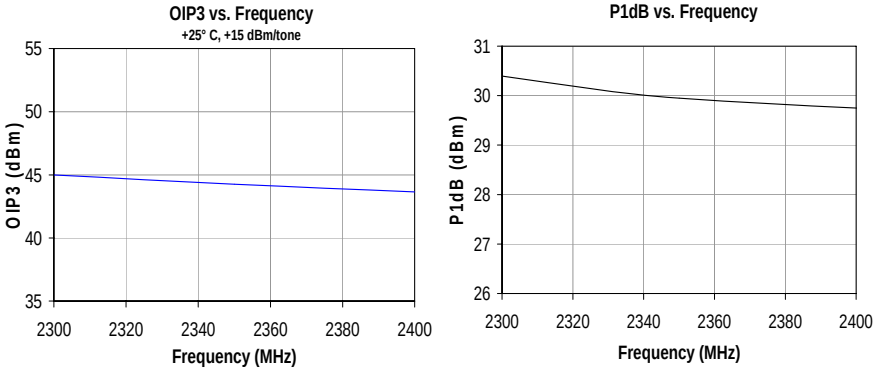
Frequency (MHz)	2300	2350	2400
Gain (dB)	24.5	24.4	24.3
Input Return Loss (dB)	10	10	10
Output Return Loss (dB)	7.5	7	6.5
Output P1dB (dBm)	+30.4	+30	+29.6
Output IP3 (dBm) (+15 dBm / tone, 1 MHz spacing)	+45	+44.3	+43.7
Device / Supply Voltage	+5 V		
Quiescent Current	400 mA		



Notes:

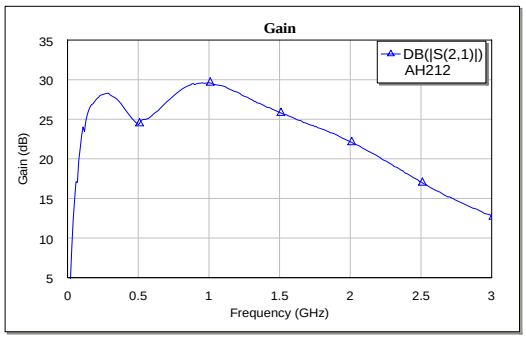
1. C7 is placed at the silkscreen marker '1' on tqs evalboard or @ 4.2 degrees at 2.35 GHz away from pin 6 and 7. C3 is placed at silkscreen marker 'A' or@ 4.2 degrees at 2.35 GHz away from pin 3.
2. All passive components are of size 0603 unless otherwise noted.

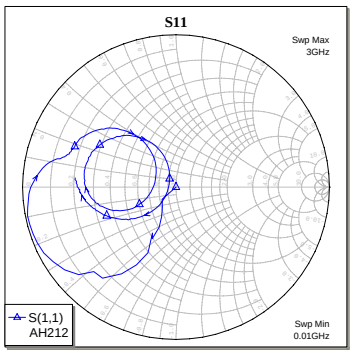


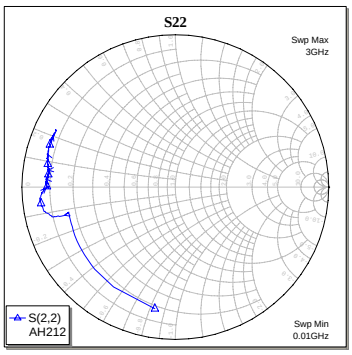


Typical Device Data (DFN 4x5 mm)

S-Parameters (V_{CC} = +5 V, I_{CC} = 400 mA, T = 25 °C, calibrated to device leads)







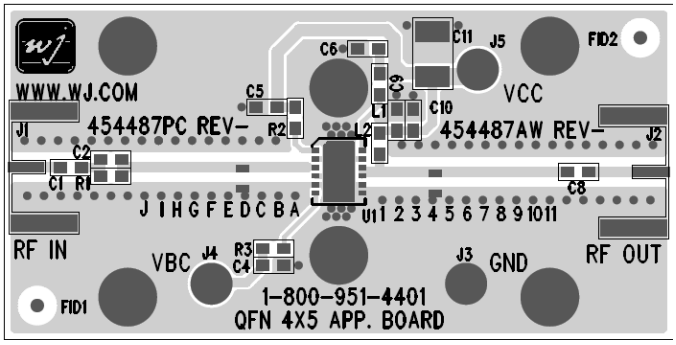
Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in blue color. For a band specific tuned circuit, it is expected that actual gain will be higher. The impedance plots are shown from 50 – 3000 MHz, with markers placed at 0.5 – 3.0 GHz in 0.5 GHz increment.

S-Parameters for AH212-EG (V_{CC} = +5 V, I_{CC} = 400 mA, T = 25 °C, unmatched 50 ohm system, calibrated to device leads)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-10.92	-112.71	14.75	95.57	-73.98	47.38	-2.62	-143.22
100	-3.48	-121.92	22.90	70.25	-70.46	9.54	-2.87	-160.44
200	-0.12	-168.99	27.45	14.93	-67.96	94.09	-2.87	-166.36
400	-2.58	163.93	26.41	-53.73	-60.92	47.82	-1.39	-168.43
600	-3.56	147.73	25.52	-62.82	-59.17	67.34	-1.19	-177.07
800	-8.55	125.39	28.69	-95.79	-54.90	49.69	-1.51	179.99
1000	-12.30	-155.14	29.61	-147.37	-55.92	32.50	-1.54	179.91
1200	-5.21	-171.47	28.43	167.21	-55.39	23.93	-1.50	177.74
1400	-4.42	164.06	26.63	132.05	-56.48	3.83	-1.61	175.61
1600	-5.81	140.51	25.16	99.97	-57.72	-6.10	-1.61	173.57
1800	-9.68	118.60	23.77	67.69	-60.00	-86.34	-1.58	171.97
2000	-22.03	121.72	22.15	34.69	-60.00	-166.62	-1.43	169.44
2200	-13.88	-133.74	20.27	2.51	-55.39	157.88	-1.39	166.52
2400	-7.86	-148.71	18.12	-28.03	-50.75	130.86	-1.27	162.89
2600	-5.27	-164.02	16.09	-56.46	-48.64	115.31	-1.27	159.59
2800	-4.10	-176.86	14.35	-85.23	-47.96	96.72	-1.27	156.84
3000	-3.60	174.71	12.79	-117.50	-47.13	90.37	-1.24	154.34

Device S-parameters are available for download from the website at: http://www.wj.com

Application Circuit PC Board Layout

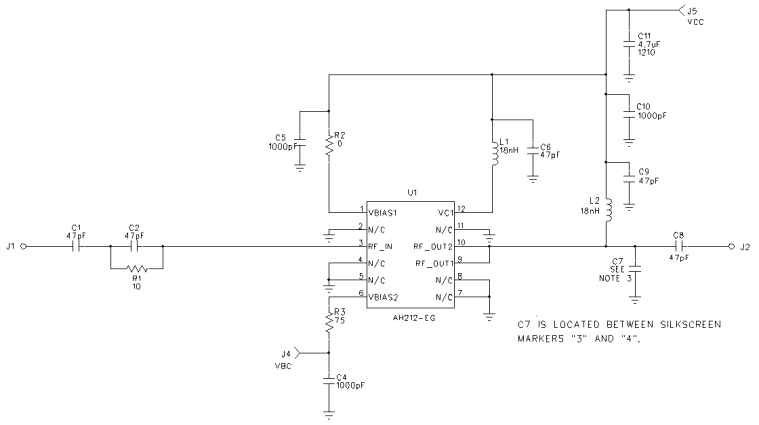


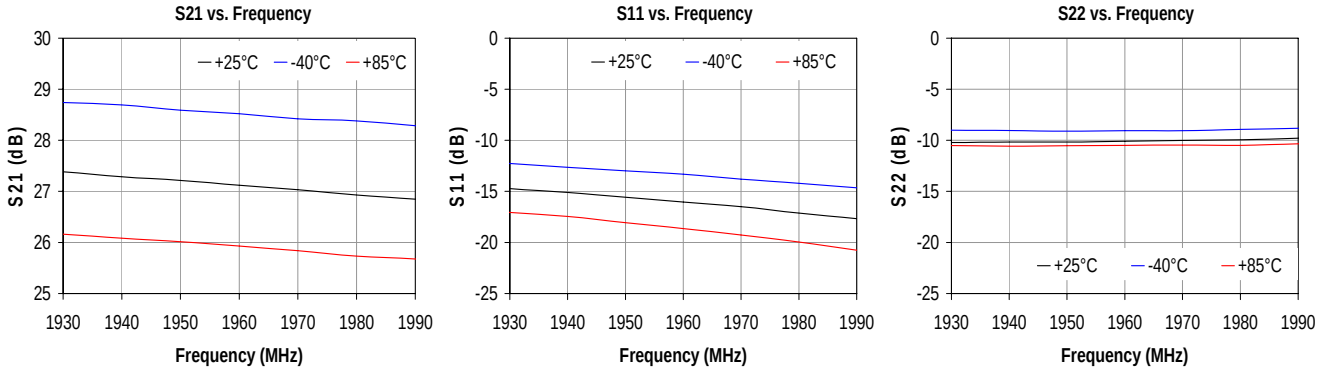
Circuit Board Material: .014" FR4, four layer, 1 oz copper, Microstrip line details: width = .026", spacing = .026"
The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as placemarkers for the input and output tuning shunt capacitor – C7. The markers and vias are spaced in 0.050" increments.

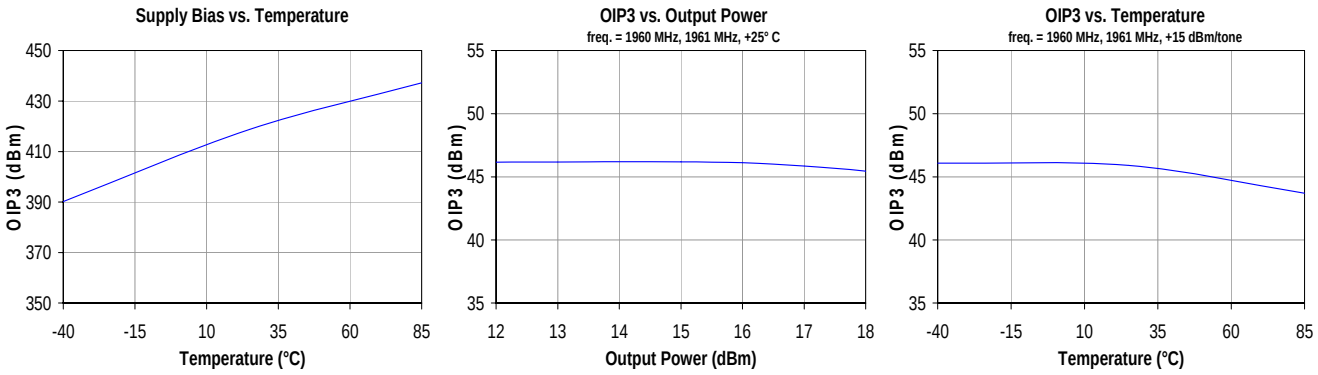
1960 MHz Application Circuit (AH212-EPCB1960)

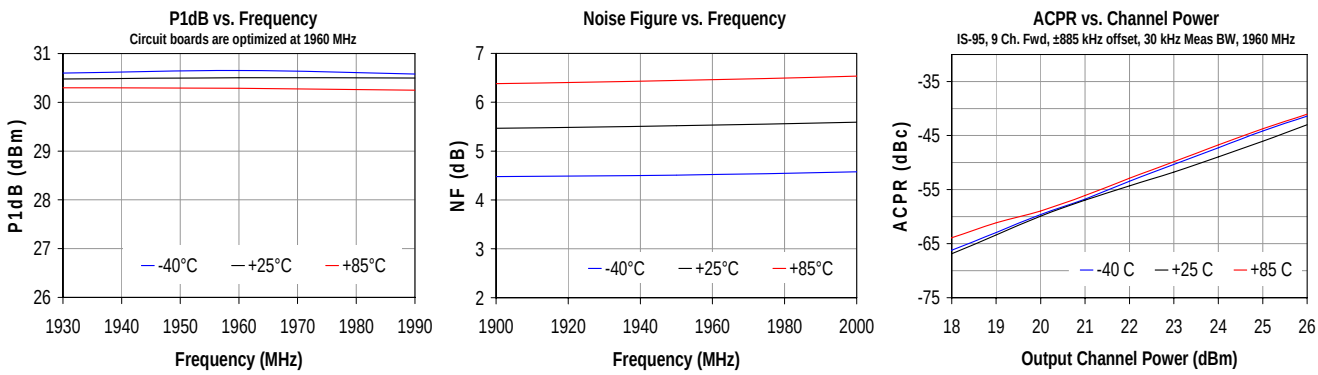
Typical RF Performance at 25 °C

Frequency	1960 MHz
Gain	27 dB
Input Return Loss	16 dB
Output Return Loss	10 dB
Output P1dB	+30.5 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+46.5 dBm
Channel Power (@-45 dBc ACPR, IS-95, 9 channels fwd)	+24.5 dBm
Noise Figure	5.5 dB
Device / Supply Voltage	+5 V
Quiescent Current	400 mA





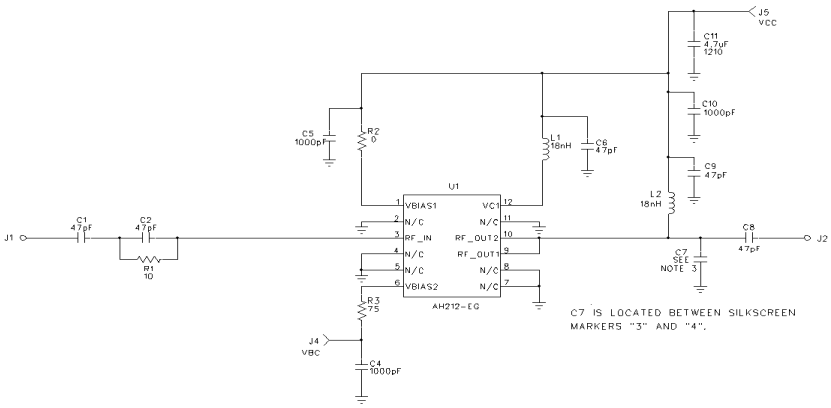


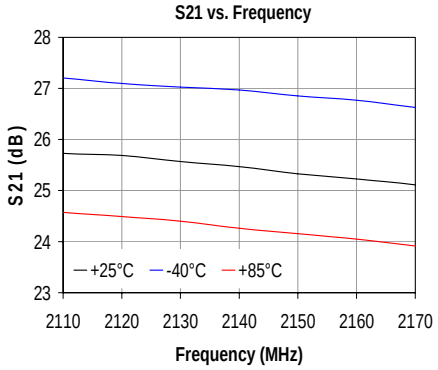


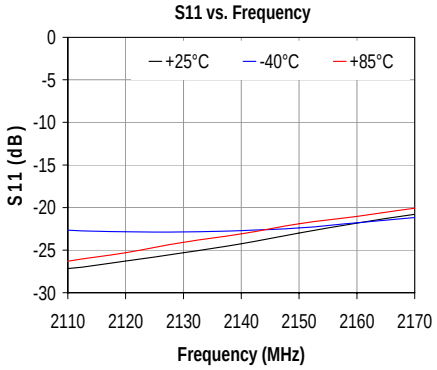
2140 MHz Application Circuit (AH212-EPCB2140)

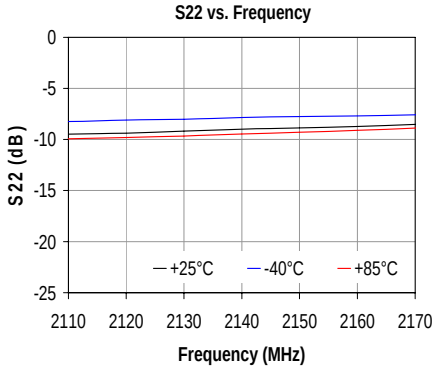
Typical RF Performance at 25 °C

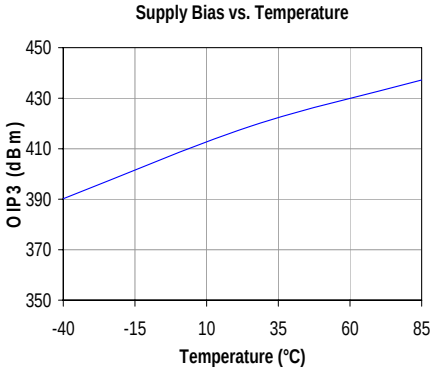
Frequency	2140 MHz
Gain	25.5 dB
Input Return Loss	24 dB
Output Return Loss	9 dB
Output P1dB	+30.5 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+46 dBm
Channel Power (@-45 dBc ACPR, IS-95, 9 channels fwd)	+22 dBm
Noise Figure	6 dB
Device / Supply Voltage	+5 V
Quiescent Current	400 mA

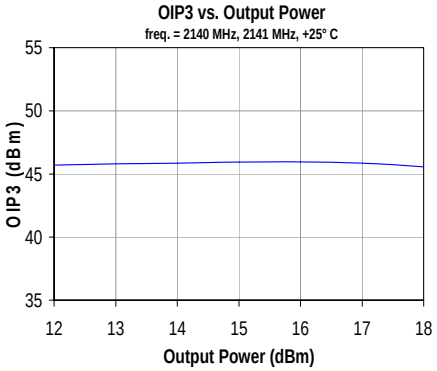


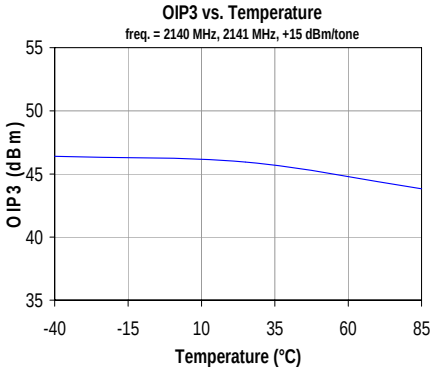


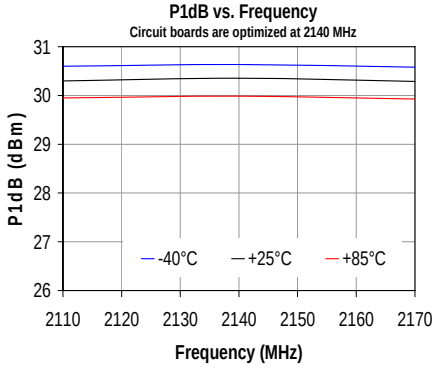


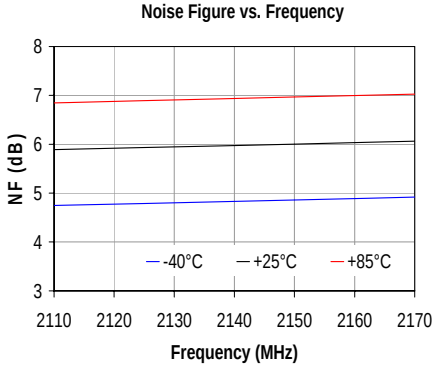


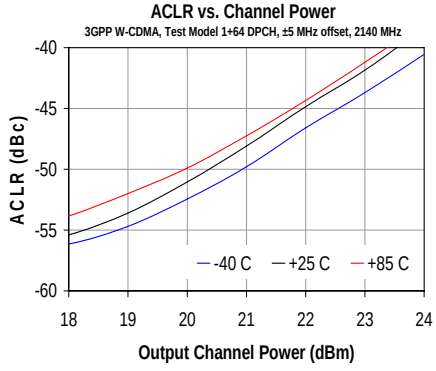








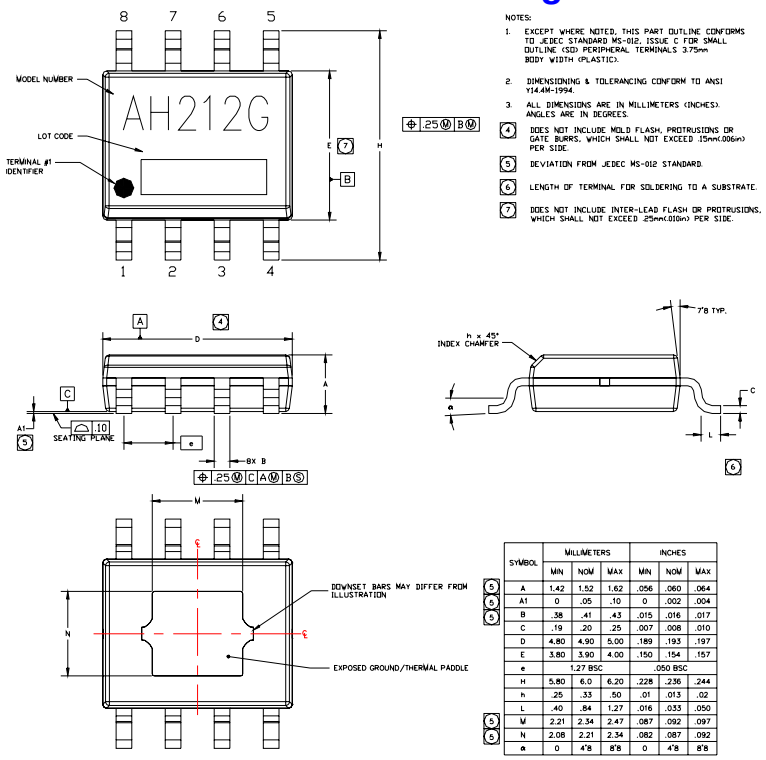




AH212-S8G (Lead-Free SOIC-8 Package) Mechanical Information

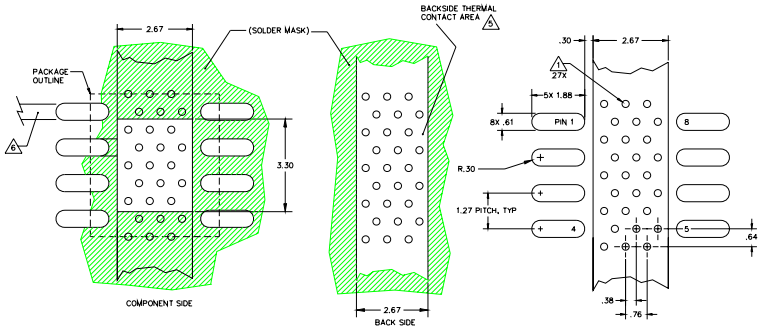
This package is lead-free/ RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

Outline Drawing



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.42	1.52	1.62	.056	.060	.064
A1	0	.05	.10	0	.002	.004
B	.38	.41	.43	.015	.016	.017
C	.19	.20	.25	.007	.008	.010
D	4.80	4.90	5.00	.189	.193	.197
E	3.80	3.90	4.00	.150	.154	.157
e	1.27 BSC			.050 BSC		
H	5.80	6.0	6.20	.228	.236	.244
h	.25	.33	.50	.01	.013	.02
L	.40	.84	1.27	.016	.033	.050
M	2.21	2.34	2.47	.087	.092	.097
N	2.08	2.21	2.34	.082	.087	.092
α	0	4°8	8°8	0	4°8	8°8

Mounting Configuration / Land Pattern



Product Marking

The component will be marked with an "AH212G" designator with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

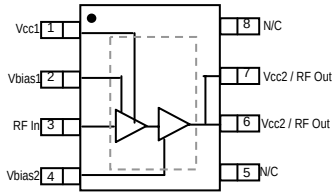
Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes ⩾ 500V to <1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
ESD Rating:	Class IV
Value:	Passes ≥ 2000V min.
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101
MSL Rating:	Level 2 at +260 °C convection reflow
Standard:	JEDEC Standard J-STD-020

Mounting Config. Notes

1. A heatsink underneath the area of the PCB for the mounted device is recommended for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters

Functional Pin Layout

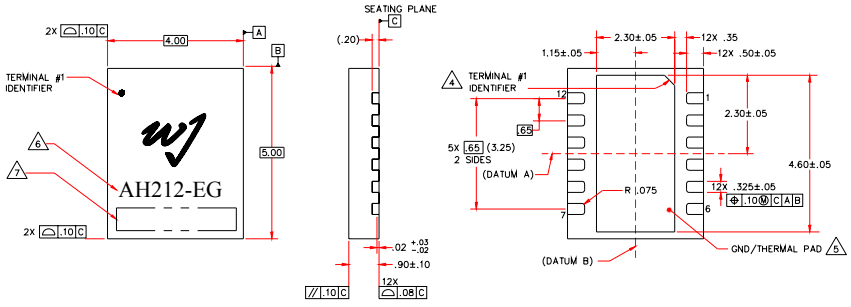


Function	Pin No.
Vcc1	1
Input	3
Output/ Vcc2	6, 7
Vbias1	2
Vbias2	4
GND	Backside Paddle
N/C or GND	5, 8

AH212-EG (Lead-Free DFN 4x5 mm Package) Mechanical Information

This package is lead-free/ RoHS-compliant. The plating material on the leads is Matte Tin. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

Outline Drawing

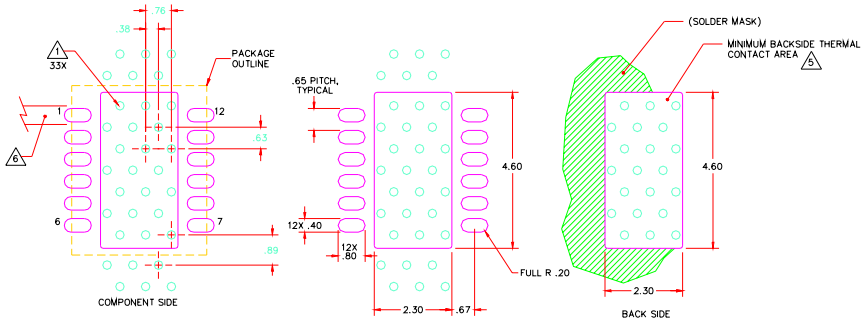


NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-229, ISSUE C (VARIATION VJGC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. PART NUMBER
7. ALPHA-NUMERIC LOT CODE.

Mounting Configuration / Land Pattern



Product Marking

The component will be marked with an "AH212-EG" designator with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes ≥ 500V to <1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

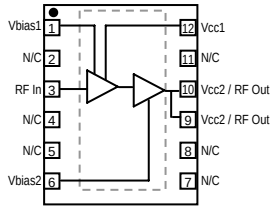
ESD Rating:	Class IV
Value:	Passes ≥ 2000V min.
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating:	Level 2 at +260 °C convection reflow
Standard:	JEDEC Standard J-STD-020

Mounting Config. Notes

1. A heatsink underneath the area of the PCB for the mounted device is recommended for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters

Functional Pin Layout



Function	Pin No.
Vcc1	12
Input	3
Output /Vcc2	9, 10
Vbias1	1
Vbias2	6
GND	Backside Paddle
N/C or GND	2, 4, 5, 7, 8, 11