ECP200D

2 Watt, High Linearity InGaP HBT Amplifier

Product Features

- 400 – 2300 MHz
- 18 dB Gain @ 900 MHz
- +33 dBm P1dB
- +51 dBm Output IP3
- +5V Single Positive Supply
- Lead-free/green/RoHS-compliant 16pin 4mm QFN package

Applications

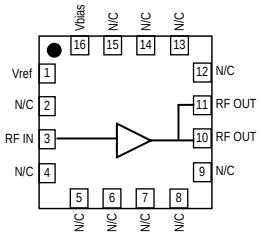
- Final stage amplifiers for Repeaters
- Mobile Infrastructure

Product Description

The ECP200D is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve high performance for various narrowband-tuned application circuits with up to +51 dBm OIP3 and +33 dBm of compressed 1dB power. It is housed in an industry standard in a lead-free/ green/RoHS-compliant 16-pin 4x4mm QFN surface-mount package. All devices are 100% RF and DC tested.

The ECP200D is targeted for use as a driver amplifier in wireless infrastructure where high linearity and medium power is required. An internal active bias allows the ECP200D to maintain high linearity over temperature and operate directly off a single +5V supply. This combination makes the device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G base stations.

Functional Diagram



Function	Pin No.
Vref	1
RF Input	3
RF Output	10, 11
Vbias	16
GND	Backside Paddle
N/C or GND	2, 4-9, 12-15

Specifications (1)

Parameter	Units	Min	Typ	Max
Operational Bandwidth	MHz	400		2300
Test Frequency	MHz		2140	
Gain	dB	9	10	
Input Return Loss	dB		20	
Output Return Loss	dB		6.8	
P1dB	dBm	+32	+33.2	
Output IP3 (2)	dBm	+47	+48	
IS-95A Channel Power @ -45 dBc ACPR, 1960 MHz	dBm		+27.5	
wCDMA Channel Power @ -45 dBc ACLR, 2140 MHz	dBm		+25.3	
Noise Figure	dB		7.7	
Operating Current Range, Icc (3)	mA	700	800	900
Device Voltage, Vcc	V		+5	

1. Test conditions unless otherwise noted: 25 ºC, +5V Vsupply, 2140 MHz, in tuned application circuit.
2. 3OIP measured with two tones at an output power of +17 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
3. This corresponds to the quiescent current or operating current under small-signal conditions into pins 6, 7, and 8. It is expected that the current can increase by an additional 200 mA at P1dB. Pin 1 is used as a reference voltage for the internal biasing circuitry. It is expected that Pin 1 will pull 22mA of current when used with a series bias resistor of R1=15Ω. (ie. total device current typically will be 822 mA.)

Typical Performance (4)

Parameter	Units	Typical		
Frequency	MHz	900	1960	2140
S21 – Gain	dB	18	11	10
S11 – Input R.L.	dB	-18	-19	-20
S22 – Output R.L.	dB	-11	-6.8	-6.8
P1dB	dBm	+33	+33.4	+33.2
Output IP3	dBm	+49	+51	+48
IS-95A Channel Power @ -45 dBc ACPR	dBm	+27	+27.5	
wCDMA Channel Power @ -45 dBc ACLR	dBm			+25.3
Noise Figure	dB	8.0	7.3	7.7
Device Bias (3)		+5 V @ 800 mA		

4. Typical parameters reflect performance in a tuned application circuit at +25 °C.

Absolute Maximum Rating

Parameter	Rating
Storage Temperature	-65 to +150 °C
RF Input Power (continuous)	+28 dBm
Device Voltage	+8 V
Device Current	1400 mA
Device Power	8 W
Thermal Resistance, Rth	17.5°C/W
Junction Temperature	+200°C

Operation of this device above any of these parameters may cause permanent damage.

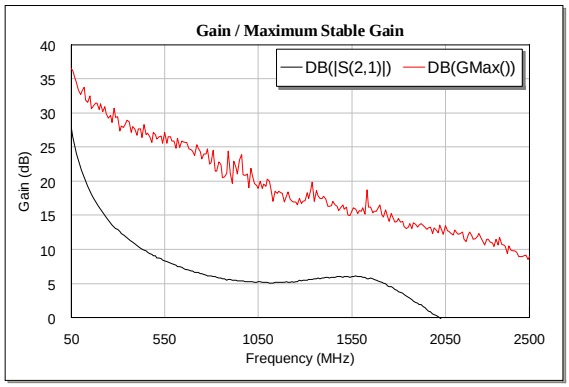
Ordering Information

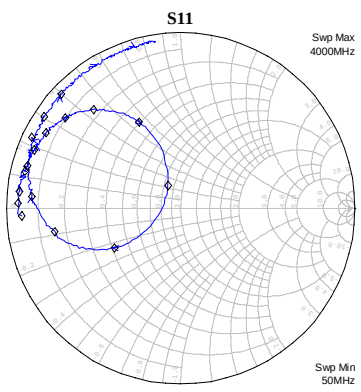
Part No.	Description
ECP200D-G	2 Watt, High Linearity InGaP HBT Amplifier (lead-free/green/RoHS-compliant 16-pin 4x4mm QFN package)
ECP200D-PCB900	900 MHz Evaluation Board
ECP200D-PCB1960	1960 MHz Evaluation Board
ECP200D-PCB2140	2140 MHz Evaluation Board

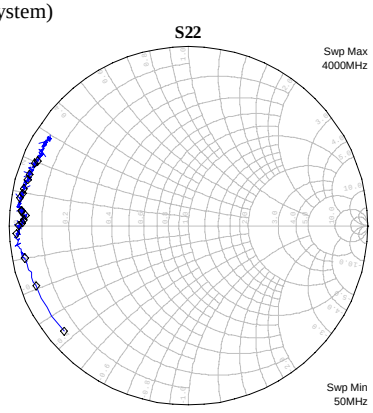
Standard tape / reel size = 1000 pieces on a 7” reel

Typical Device Data

S-Parameters (V_{CC} = +5 V, I_{CC} = 800 mA, T = 25 °C, unmatched 50 ohm system)







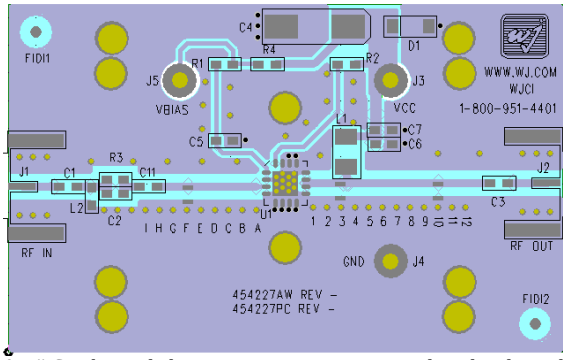
Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the dashed red line. The impedance plots are shown from 50 – 3000 MHz, with markers placed at 0.5 – 3.0 GHz in 0.5 GHz increments.

S-Parameters (V_{CC} = +5 V, I_{CC} = 800 mA, T = 25 °C, unmatched 50 ohm system, calibrated to device leads)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-0.80	-177.34	27.72	107.79	-45.30	19.06	-0.81	-139.65
100	-0.60	178.13	22.13	96.85	-43.21	11.92	-0.79	-158.43
200	-0.64	174.02	16.20	89.13	-44.86	-4.05	-0.62	-168.80
400	-0.76	166.66	10.54	80.79	-42.84	6.99	-0.35	-177.29
600	-0.89	158.43	7.75	72.52	-44.05	2.89	-0.47	179.92
800	-1.08	150.86	6.09	64.42	-43.61	-7.72	-0.66	179.00
1000	-1.54	141.98	5.29	54.50	-42.64	-4.97	-0.73	177.98
1200	-2.48	131.55	5.24	41.62	-39.25	-33.49	-0.82	176.35
1400	-5.25	115.96	5.83	20.85	-39.43	-52.73	-0.58	175.10
1600	-16.57	118.86	6.03	-9.41	-37.39	-100.38	-0.58	174.84
1800	-7.12	-149.33	3.81	-47.41	-39.26	-126.48	-0.42	170.66
2000	-2.68	-169.62	0.37	-72.56	-40.69	-169.19	-0.52	169.04
2200	-1.34	175.50	-3.32	-89.96	-45.63	-163.76	-0.53	167.35
2400	-0.80	164.47	-6.81	-102.05	-50.41	149.05	-0.61	164.01
2600	-0.49	154.67	-9.46	-112.59	-48.80	157.02	-0.62	162.14
2800	-0.53	146.29	-12.22	-121.23	-50.62	69.74	-0.68	157.85
3000	-0.50	136.44	-14.55	-128.37	-49.46	79.86	-0.77	156.81

Device S-parameters are available for download from the website at: http://www.wj.com

Application Circuit PC Board Layout



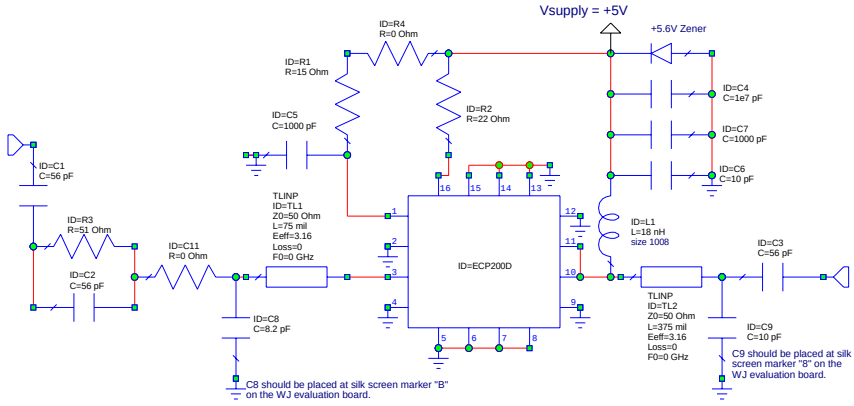
Circuit Board Material: .014” Getek, single layer, 1 oz copper, Microstrip line details: width = .026”, spacing = .026”
The silk screen markers ‘A’, ‘B’, ‘C’, etc. and ‘1’, ‘2’, ‘3’, etc. are used as placemarkers for the input and output tuning shunt capacitors – C8 and C9. The markers and vias are spaced in .050” increments.

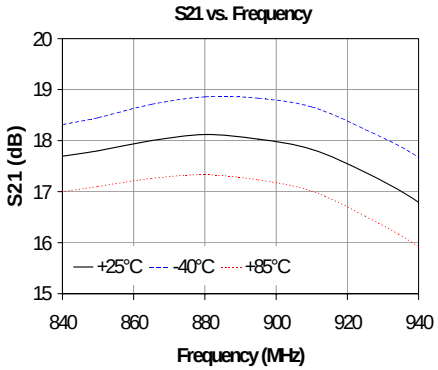
900 MHz Application Circuit (ECP200D-PCB900)

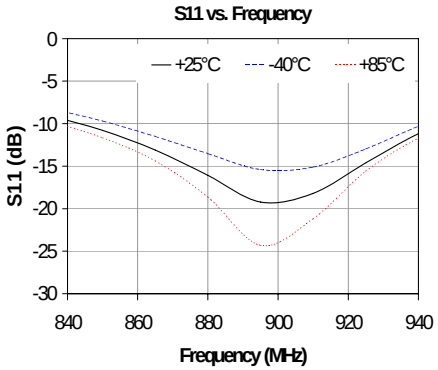
Typical RF Performance at 25 °C

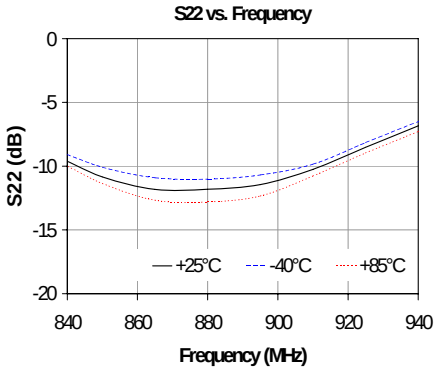
Frequency	900 MHz
S21 – Gain	18 dB
S11 – Input Return Loss	-18 dB
S22 – Output Return Loss	-11 dB
Output P1dB	+33 dBm
Output IP3 (+17 dBm / tone, 1 MHz spacing)	+49 dBm
Channel Power (@-45 dBc ACPR, IS-95 9 channels fwd)	+27 dBm
Noise Figure	8.0 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	800 mA

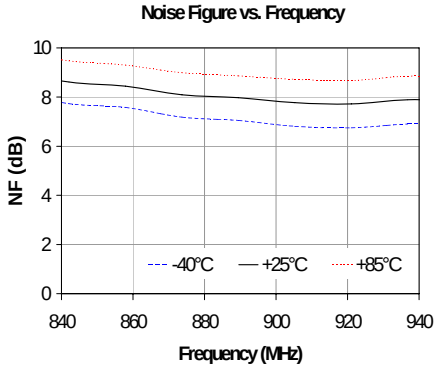
1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 10, 11, and 16.

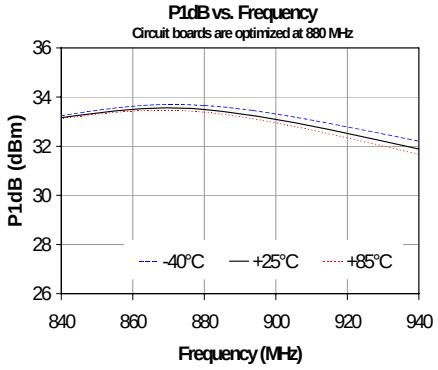


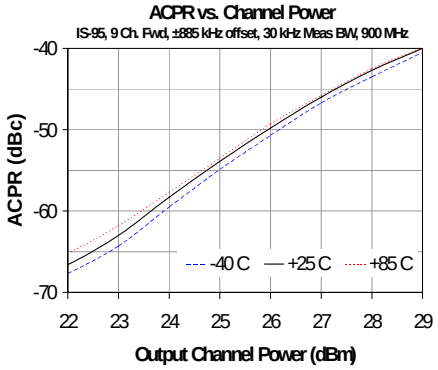


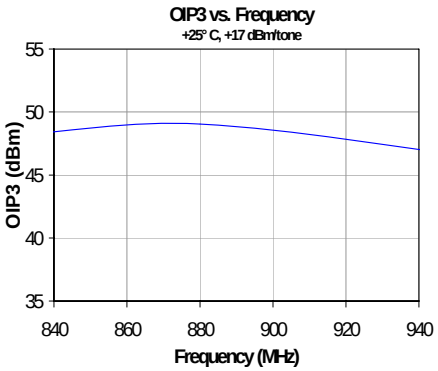


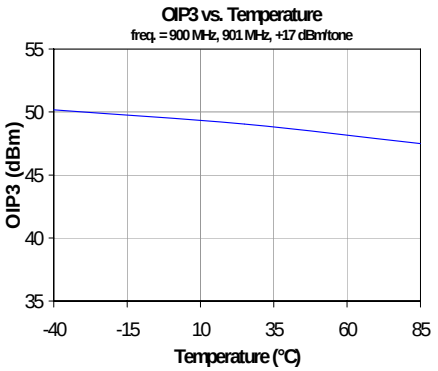


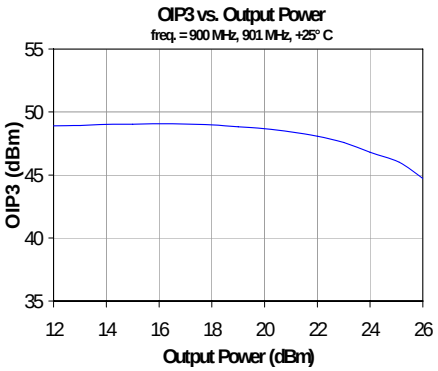










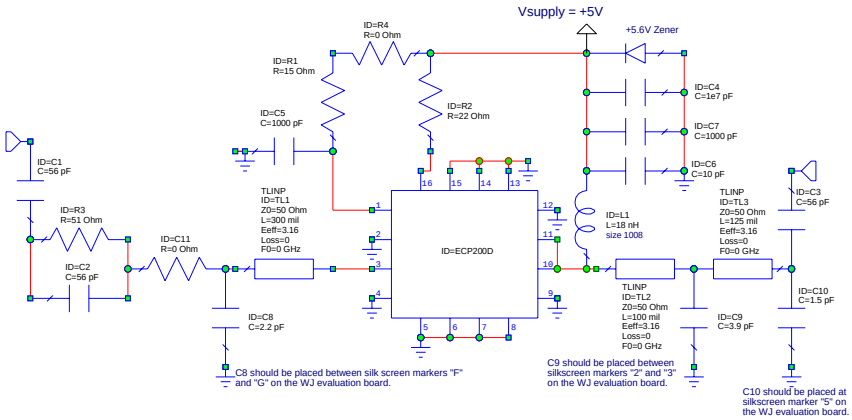


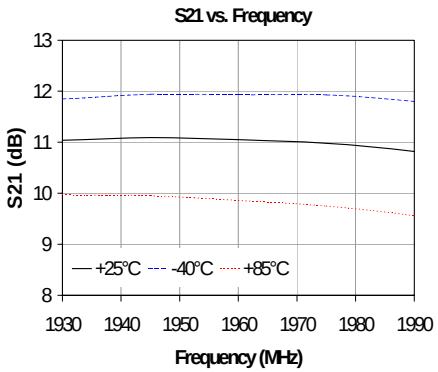
1960 MHz Application Circuit (ECP200D-PCB1960)

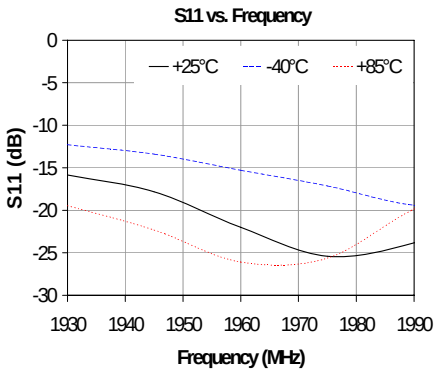
Typical RF Performance at 25 °C

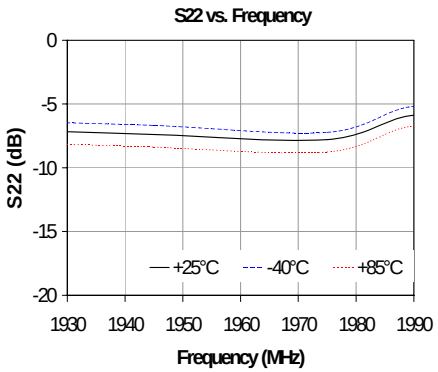
Frequency	1960 MHz
S21 – Gain	11 dB
S11 – Input Return Loss	-20 dB
S22 – Output Return Loss	-6.8 dB
Output P1dB	+33.4 dBm
Output IP3 (+17 dBm / tone, 1 MHz spacing)	+51 dBm
Channel Power (@-45 dBc ACPR, IS-95 9 channels fwd)	+27.5 dB
Noise Figure	7.3 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	800 mA

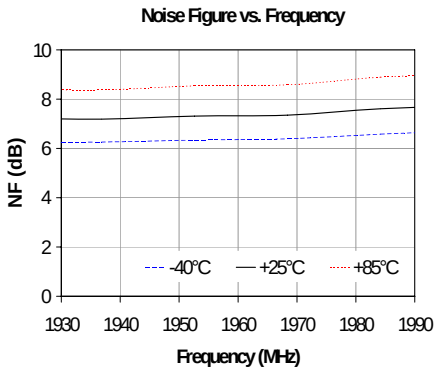
1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 10, 11, and 16.

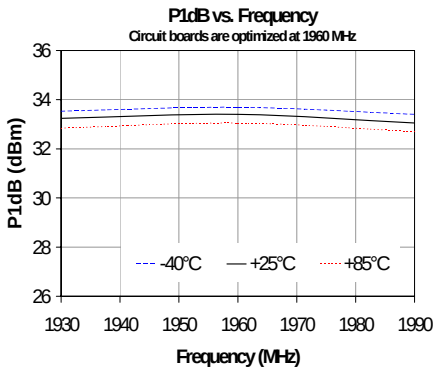


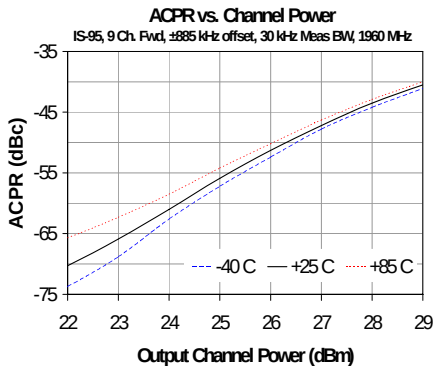


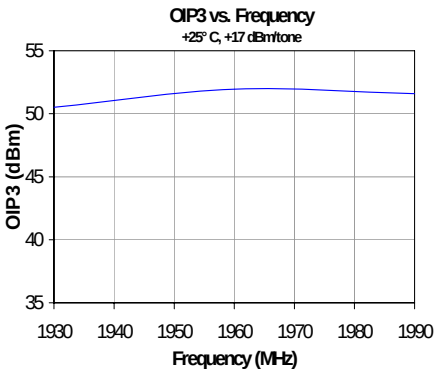


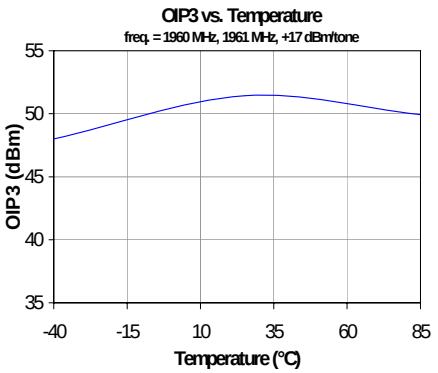


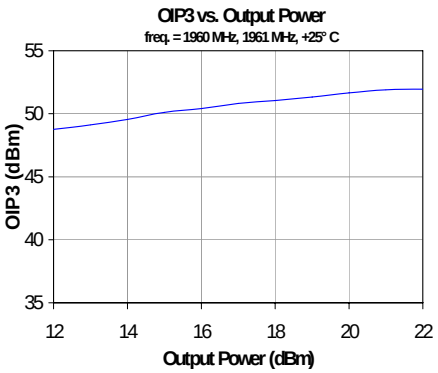










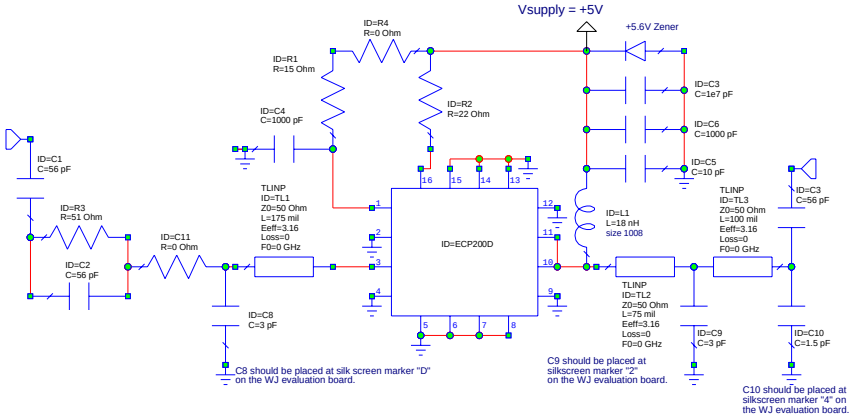


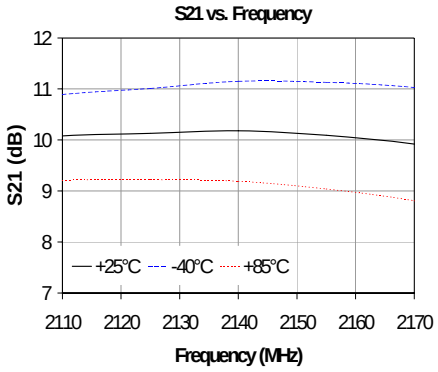
2140 MHz Application Circuit (ECP200D-PCB2140)

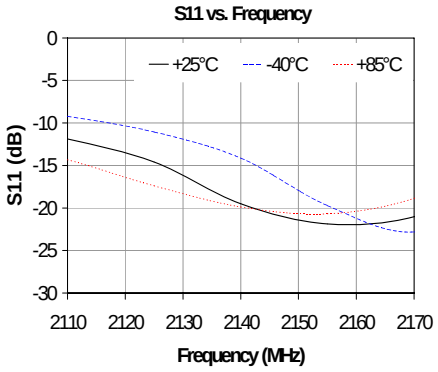
Typical RF Performance at 25 °C

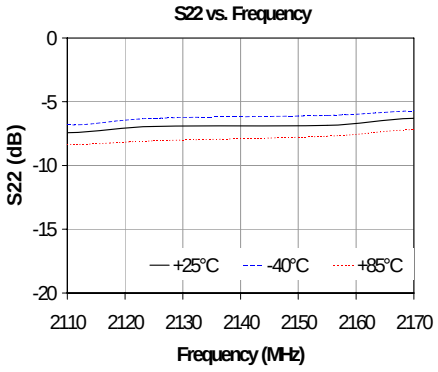
Frequency	2140 MHz
S21 – Gain	10 dB
S11 – Input Return Loss	-20 dB
S22 – Output Return Loss	-6.8 dB
Output P1dB	+33.2 dBm
Output IP3 (+17 dBm / tone, 1 MHz spacing)	+48 dBm
W-CDMA Channel Power (@ -45 dBc ACLR)	+25.3 dBm
Noise Figure	7.7 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	800 mA

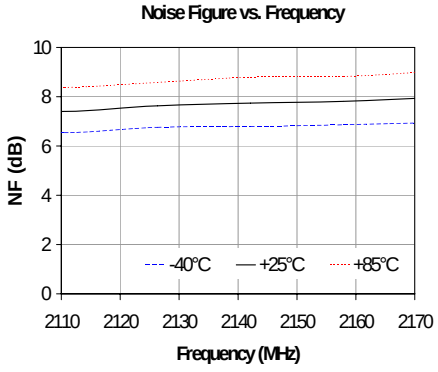
1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 10, 11, and 16.

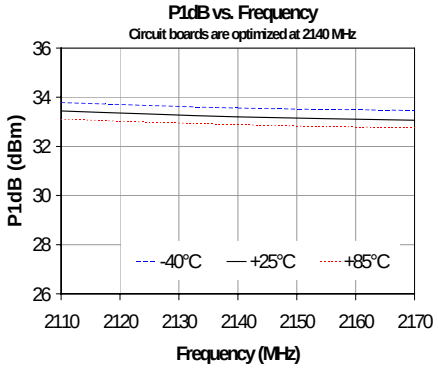


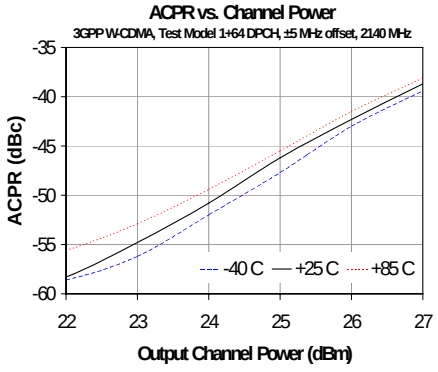


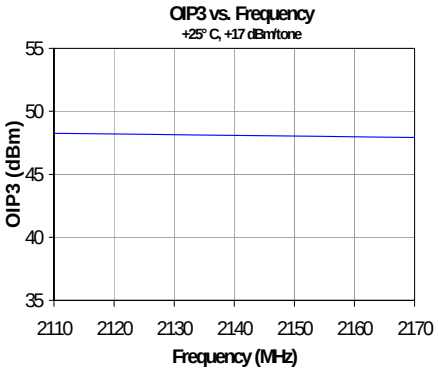


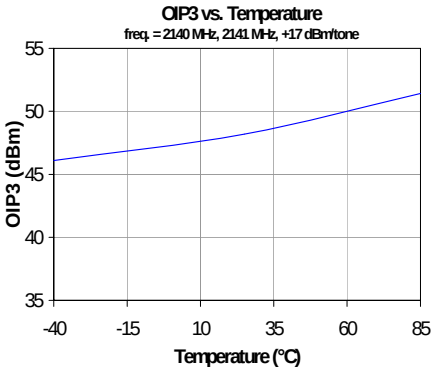


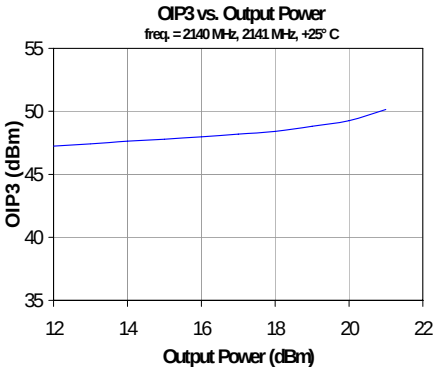








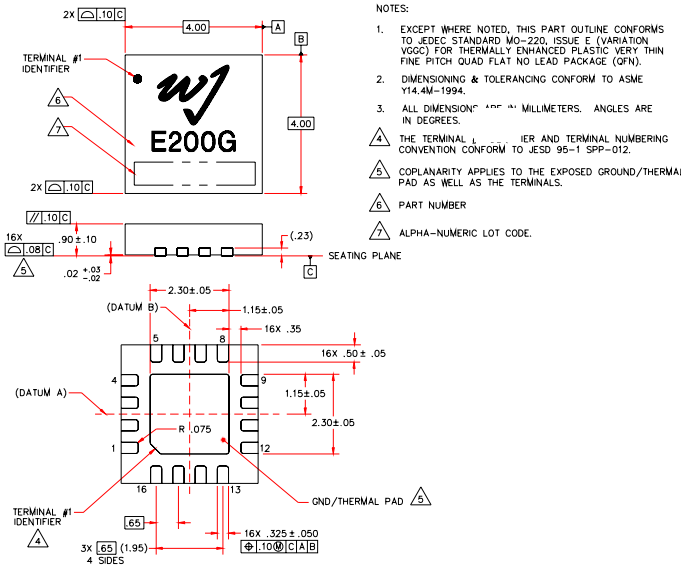




ECP200D-G Mechanical Information

This package is lead-free/RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes. The plating material on the pins is annealed matte tin over copper.

Outline Drawing



NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-220, ISSUE E (VARIATION VGGC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. THE TERMINAL [illegible]IER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. PART NUMBER
7. ALPHA-NUMERIC LOT CODE.

Land Pattern

NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

Product Marking

The component will be marked with an "E200G" designator with an alphanumeric lot code on the top surface of the package. The obsolete tin-lead package is marked with an "ECP200D" designator followed by an alphanumeric lot code.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes between 500 and 1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
MSL Rating:	Level 2 at +260 °C convection reflow
Standard:	JEDEC Standard J-STD-020

Mounting Config. Notes

1. A heatsink underneath the area of the PCB for the mounted device is highly recommended for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters (inches). Angles are in degrees.