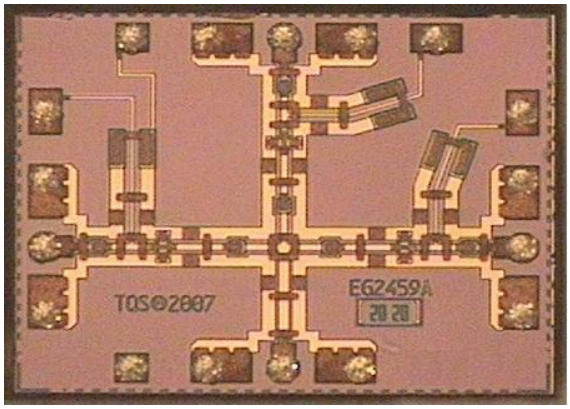
# TGS4305-FC

## 60-90 GHz SP3T Switch Flip Chip

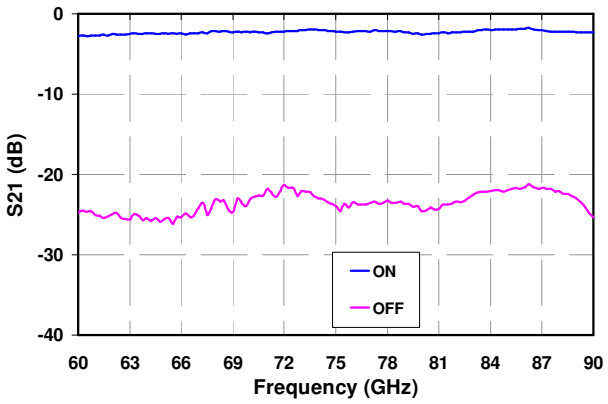


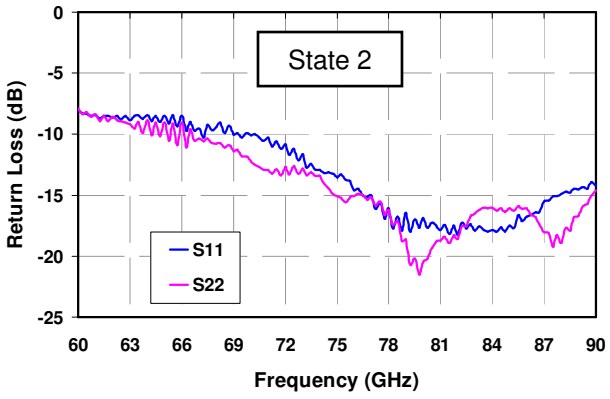

## Measured Performance

Bias conditions OFF: Vd = 1.35 V, Id = ~10 mA, State 4

ON: Vd = -5V, Id = 0 mA, State 2

RF IN to RF OUT 2




## Key Features

- Frequency Range: 60-90 GHz
- 2.3 dB Typical Flipped Insertion Loss
- 20 dB Nominal Isolation
- > 13 dB Typical Thru State Return Loss
- < 5 nsec Switching Speed
- Integrated DC blocking at RF ports
- Chip dimensions: 1.69 x 1.37 x 0.38 mm (0.067 x 0.054 x 0.015 in)

## Primary Applications

- Automotive Transceivers
- E-Band Transceivers

## Product Description

The TriQuint TGS4305-FC is a 60-90 GHz SP3T Switch. This part is designed using TriQuint's proven standard VPIN production process. The switching speed for TGS4305-FC is < 5 nsec typically.

The TGS4305-FC, when flipped, provides a nominal 2.3 dB insertion loss, > 13 dB Thru State return loss, and 20 dB isolation in the automotive band.

The TGS4305-FC integrates DC blocking capacitors on all output ports to reduce the number of off-chip components.

The TGS4305-FC has a protective surface passivation layer providing environmental robustness.

Lead-free and RoHS compliant



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## Table I
## Absolute Maximum Ratings 1/

| SYMBOL | PARAMETER | VALUES | NOTES |
|---|---|---|---|
| Vd1,2,3 | Maximum Supply Voltage | -15 V to 2 V | |
| Id1,2,3 | Maximum Supply Current | 15 mA | |
| Pin | Maximum Input Power | 27 dBm | |
| Tstg | Storage Temperature | -65 to 150 $^{0}$C | |

1/ These ratings represent the maximum operating values for this device.

## Table II
## Recommended Operating Conditions
## Truth Table

| State | RF IN to RF OUT 1 | RF IN to RF OUT 2 | RF IN To RF OUT 3 | Vd1 | Vd2 | Vd3 |
|---|---|---|---|---|---|---|
| 1 | ON | OFF | OFF | -5 V @ 0 mA | 1.35 V @ 10 mA | 1.35 V @ 10 mA |
| 2 | OFF | ON | OFF | 1.35 V @ 10 mA | -5 V @ 0 mA | 1.35 V @ 10 mA |
| 3 | OFF | OFF | ON | 1.35 V @ 10 mA | 1.35 V @ 10 mA | -5 V @ 0 mA |
| 4 | OFF | OFF | OFF | 1.35 V @ 10 mA | 1.35 V @ 10 mA | 1.35 V @ 10 mA |



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# Table III
# RF Characterization Table

(TA = 25 °C, Nominal)
Probe Tip Calibration
Id = 6 mA, typical

| PARAMETER | THROUGH PATH IDENTIFICATION | TEST CONDITIONS | MINIMUM | NOMINAL | MAXIMUM | UNITS |
|---|---|---|---|---|---|---|
| Insertion Loss (State 2) | RF Input to RF Output 1<br>RF Input to RF Output 2<br>RF Input to RF Output 3 | F = 76 – 77 GHz | | 1.6 | 3.75 | dB |
| Isolation<br>On/off ratio<br>(State 2 / 4 ) | RF Input to RF Output 1<br>RF Input to RF Output 2<br>RF Input to RF Output 3 | F = 76 – 77 GHz | 16 | 20 | | dB |
| Input Return Loss (State 2) | RF Input to RF Output 1<br>RF Input to RF Output 2<br>RF Input to RF Output 3 | F = 76 – 77 GHz | 8 | 10 | | dB |
| Output Return Loss (State 2) | RF Input to RF Output 1<br>RF Input to RF Output 2<br>RF Input to RF Output 3 | F = 76 – 77 GHz | 8 | 10 | | dB |



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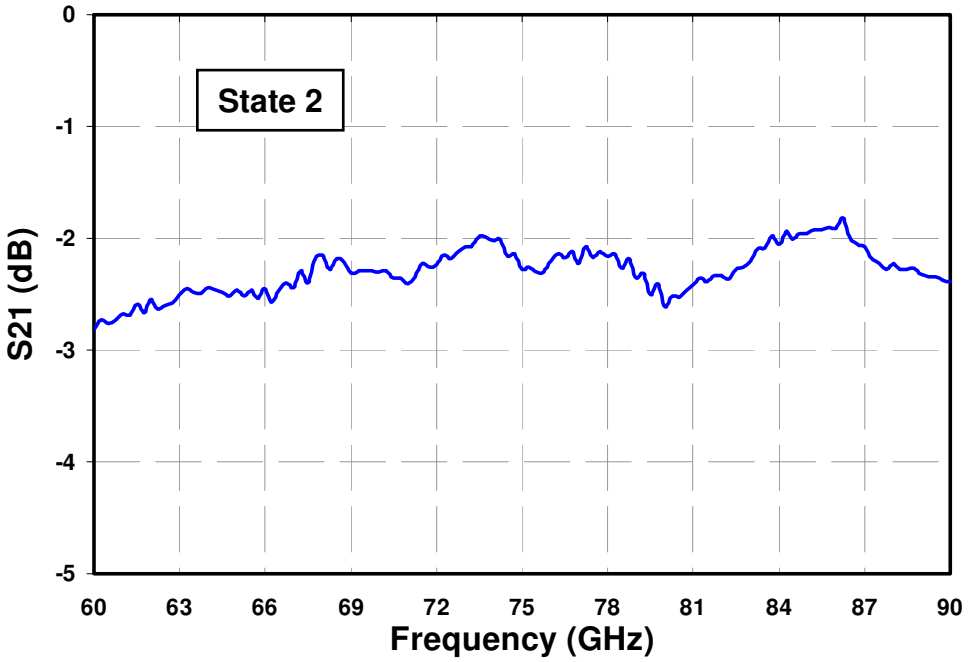
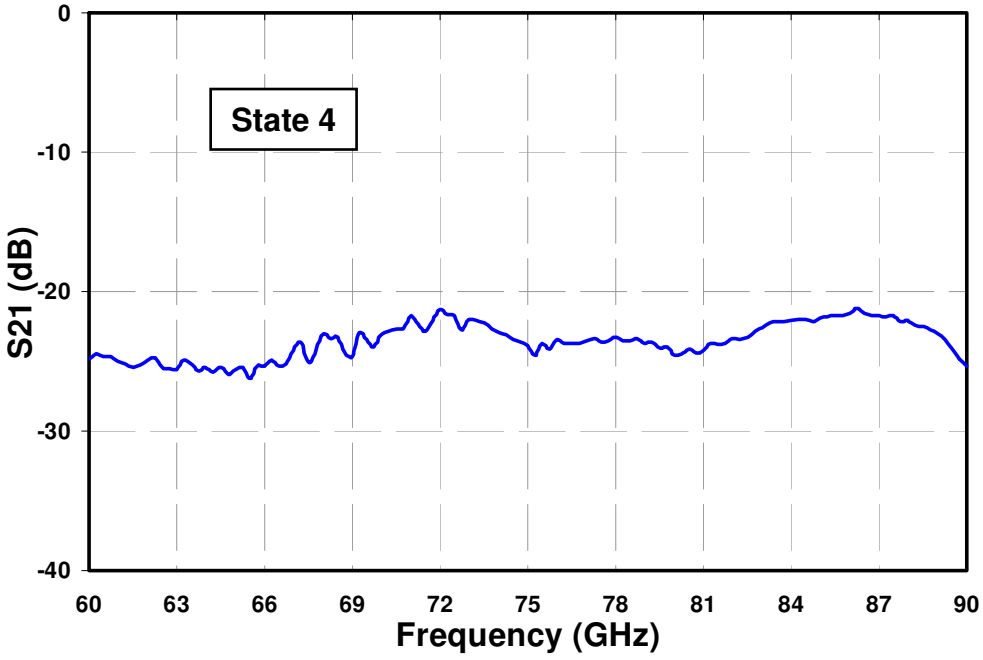
## Measured Data

### Insertion Loss

RF IN to RF OUT 2




RF IN to RF OUT 2



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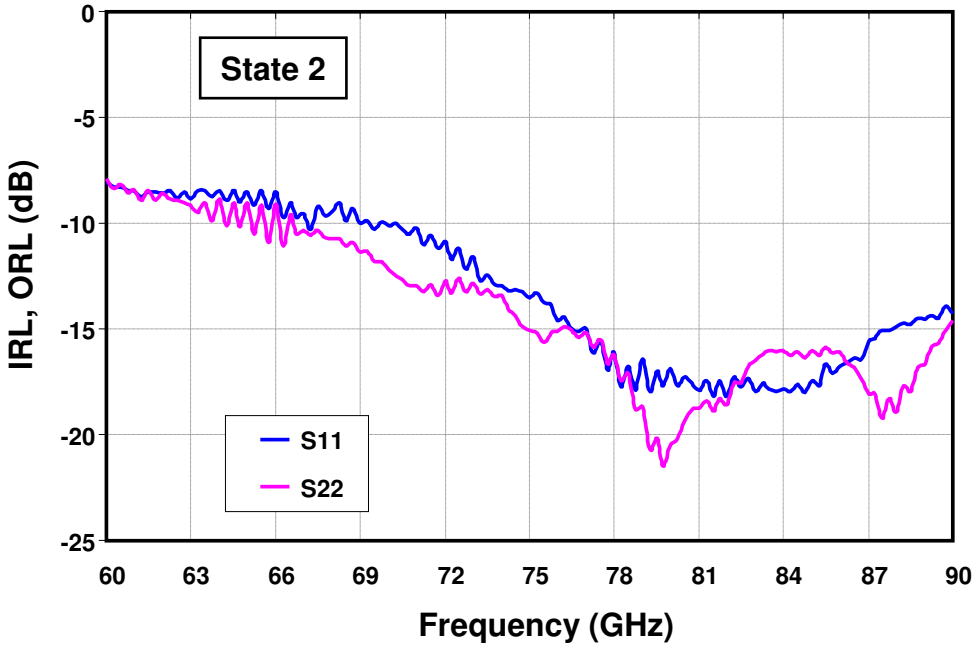
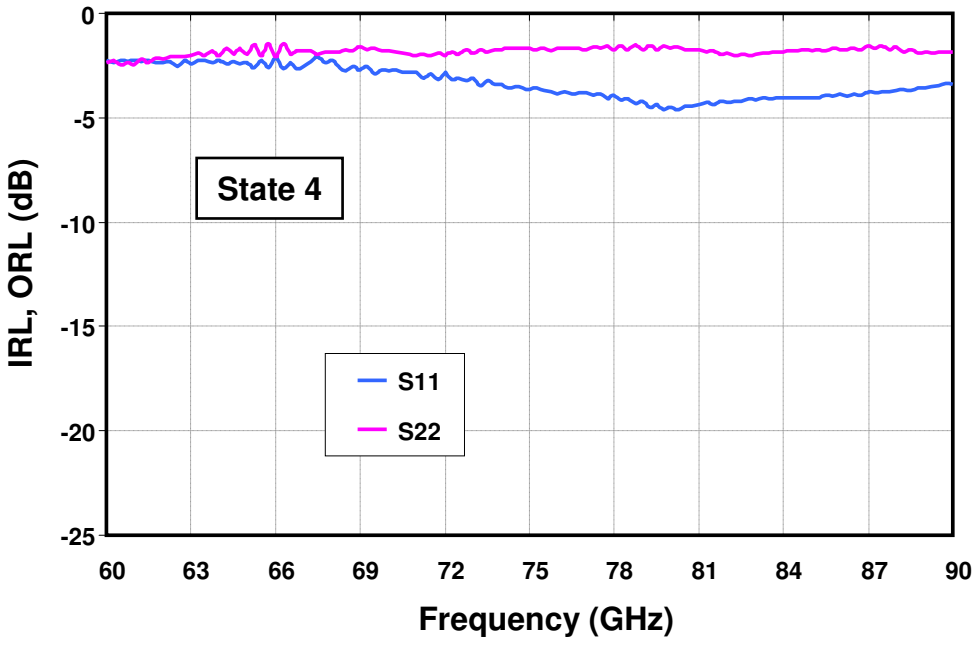
## Measured Data

### Return Loss

RF IN to RF OUT 2




RF IN to RF OUT 2



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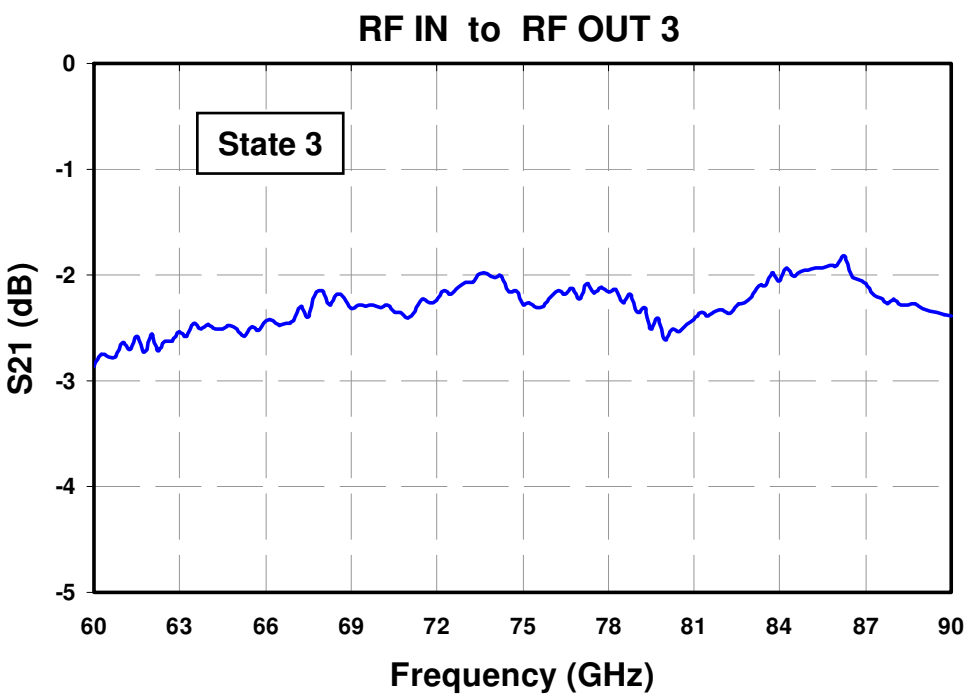
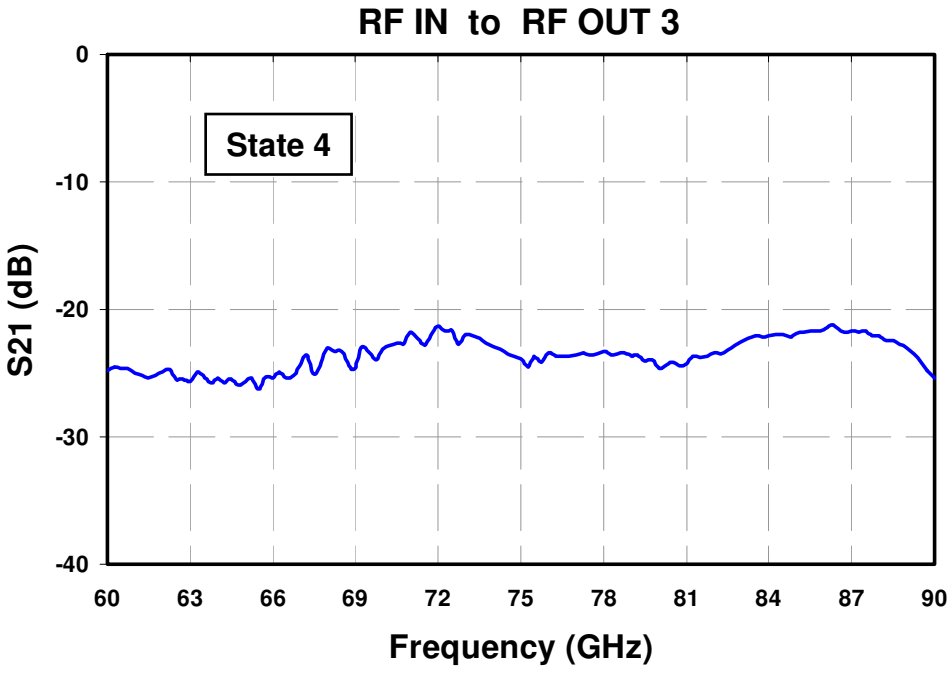
## Measured Data

### Insertion Loss



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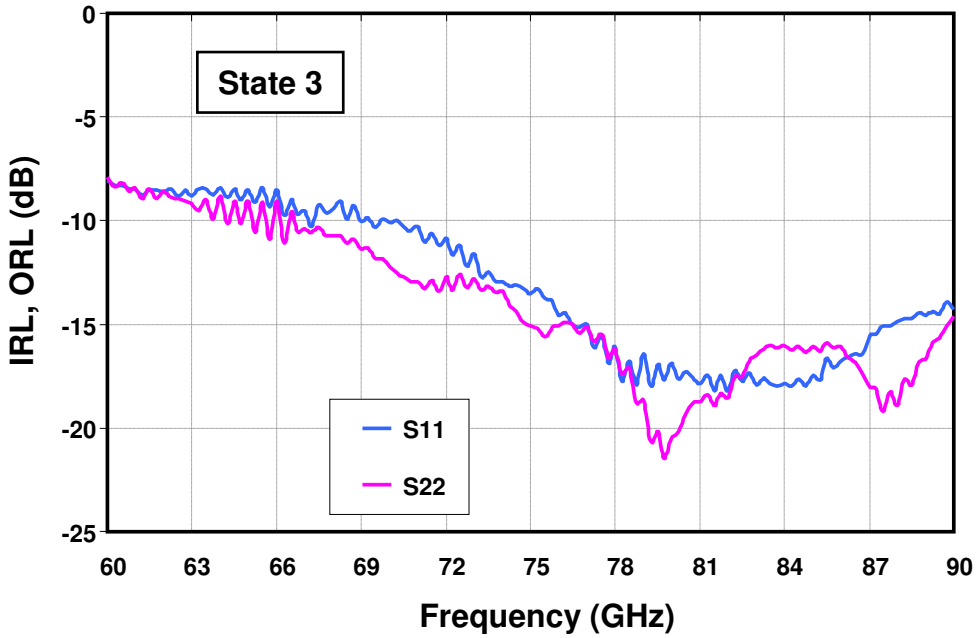
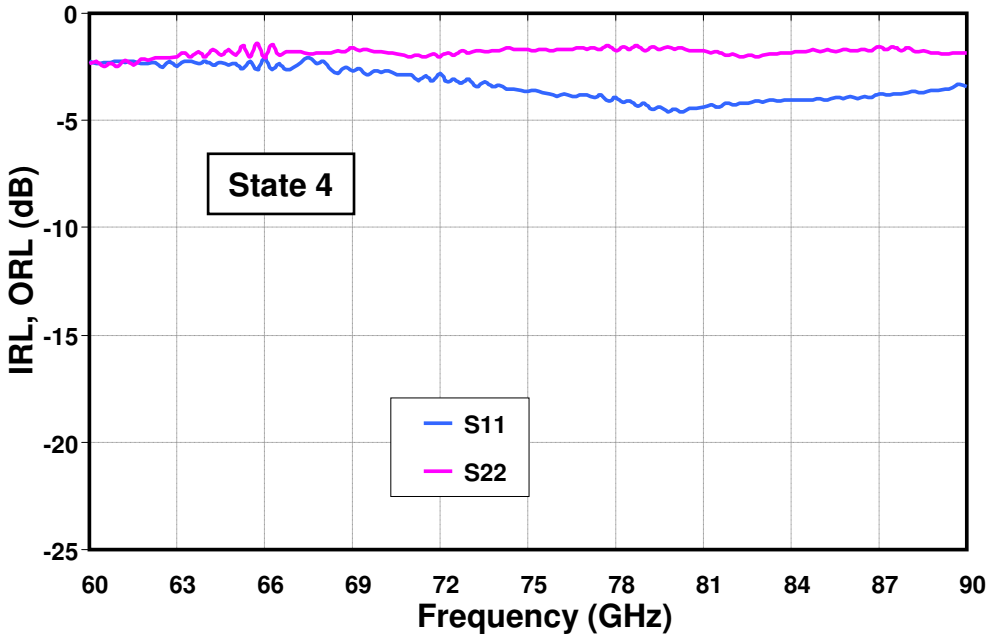
## Measured Data

### Return Loss

RF IN to RF OUT 3




RF IN to RF OUT 3



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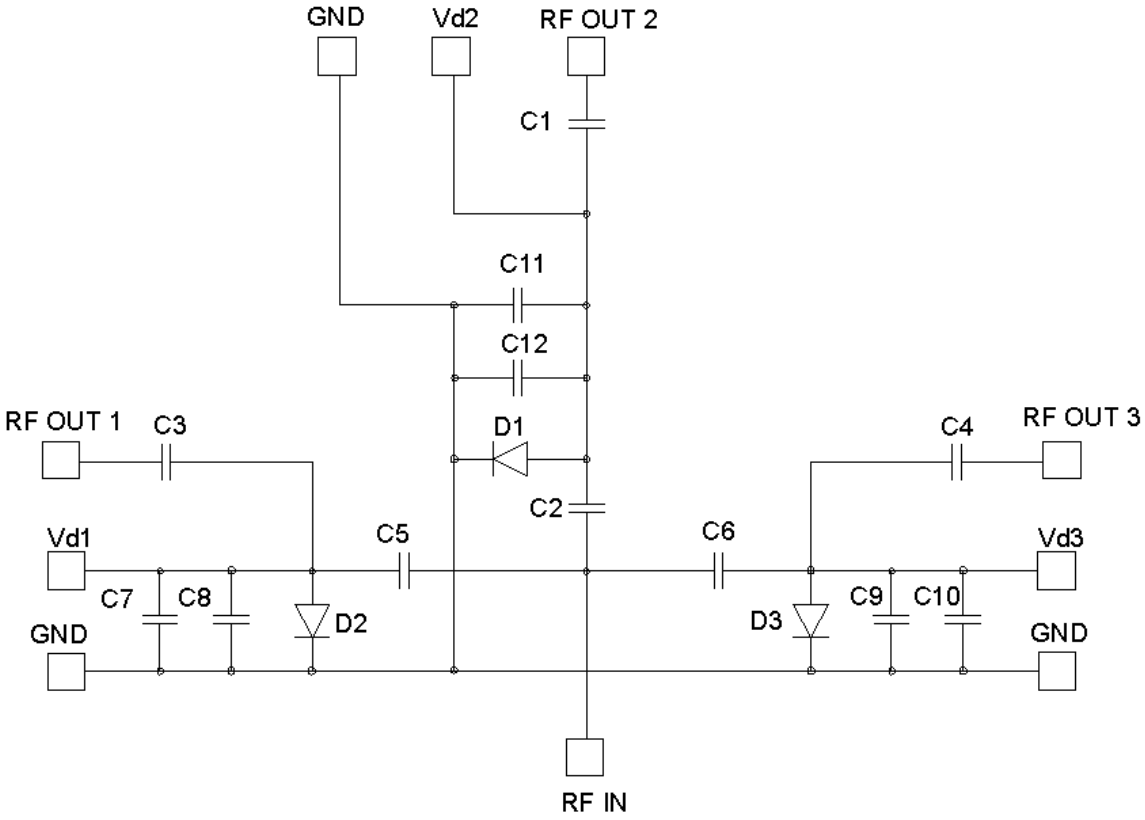
## Electrical Schematic



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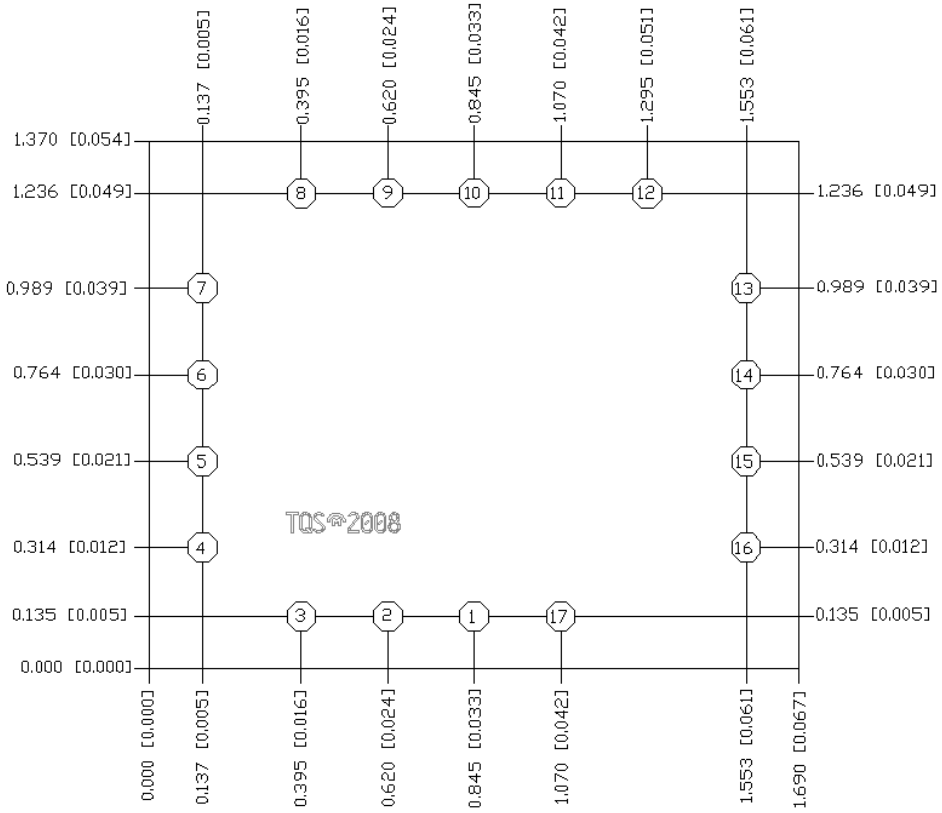
# Mechanical Drawing

## Drawing is for chip face up




Units: millimeters (inches)

Thickness: 0.380 (0.015). Die x,y size tolerance: +/- 0.050 (0.002)

Chip edge to pillar dimensions are shown to center of pillar

| | | |
|---|---|---|
| Pillar # 1 | RF IN | 0.075 Φ |
| Pillar # 5 | RF OUT 1 | 0.075 Φ |
| Pillar # 10 | RF OUT 2 | 0.075 Φ |
| Pillar # 15 | RF OUT 3 | 0.075 Φ |
| Pillar # 7 | Vd1 | 0.075 Φ |
| Pillar # 12 | Vd2 | 0.075 Φ |
| Pillar # 13 | Vd3 | 0.075 Φ |
| Pillar # 8 | DC Ground | 0.075 Φ |
| Pillar # 2, 4, 6, 9, 11, 14, 16, 17 | RF CPW Ground | 0.075 Φ |
| Pillar # 3 | Mechanical Support Only | 0.075 Φ |

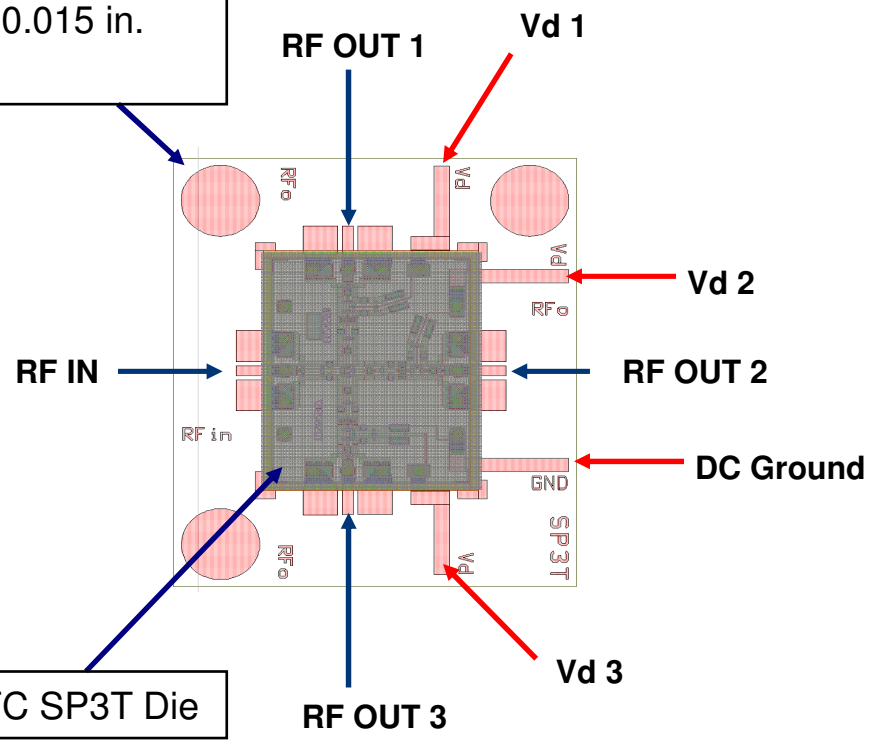
***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***

## Recommended Assembly Diagram

TGS4305-FC SP3T data represented in this datasheet was taken using co-planar waveguide (CPW) transition on the shown substrate and ground-signal-ground probes.

Bypass capacitors not required.

Alumina substrate board
Thickness: 0.015 in.
$\varepsilon_r$ = 9.9




Die is flip-chip soldered to substrate

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# Assembly Notes

Component placement and die attach assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- Cu pillars on die are 65 um tall with a 22 um tall Sn solder cap.
- Recommended board metallization is evaporated TiW followed by nickel/gold at pillar attach interface. Ni is the adhesion layer for the solder and the gold keeps the Ni from oxidizing. The Au should be kept to a minimum to avoid embrittlement; suggested Au / Sn mass ratio must not exceed 8%.
- Au metallization is not recommended on traces due to solder wicking and consumption concerns. If Au traces are used, a physical solder barrier must be applied or designed into the pad area of the board. The barrier must be sufficient to keep the solder from undercutting the barrier.

Reflow process assembly notes:

- Minimum alloying temperatures 245 ˚C.
- Repeating reflow cycles is not recommended due to Sn consumption on the first reflow cycle.
- An alloy station or conveyor furnace with an inert atmosphere such as N2 should be used.
- Dip copper pillars in “no-clean flip chip” flux prior to solder attach. Suggest using a high temperature flux. Avoid exposing entire die to flux.
- If screen printing flux, use small apertures and minimize volume of flux applied.
- Coefficient of thermal expansion matching between the MMIC and the substrate/board is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.
- Suggested reflow will depend on board material and density.

See Triquint Application Note for flip-chip soldering process: TBD

# Typical Reflow Profiles for TriQuint Cu / Sn Pillars

| Process | Sn Reflow |
|---|---|
| Ramp-up Rate | 3 ˚C/sec |
| Flux Activation Time and Temperature | 60 – 120 sec @ 140 – 160 ˚C |
| Time above Melting Point (245 ˚C) | 60 – 150 sec |
| Max Peak Temperature | 300 ˚C |
| Time within 5 ˚C of Peak Temperature | 10 – 20 sec |
| Ramp-down Rate | 4 – 6 ˚C/sec |

# Ordering Information

| Part | Package Style |
|---|---|
| TGA4305-FC | GaAs MMIC Die |

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