

FEATURES

Single-supply operation: 3 V to 36 V
Wide input voltage range
Rail-to-rail output swing
Low supply current: 250 μ A/amp
Wide bandwidth: 1.2 MHz
Slew rate: 0.46 V/ μ s
Low offset voltage: 500 μ V maximum
No phase reversal

APPLICATIONS

Industrial process control
Battery-powered instrumentation
Power supply control and protection
Telecommunications
Remote sensors
Low voltage strain gage amplifiers
DAC output amplifiers

GENERAL DESCRIPTION

The ADA4091-2 is a dual, micropower, single-supply, 1.2 MHz bandwidth amplifier featuring rail-to-rail inputs and outputs. It is guaranteed to operate from a +3 V single supply as well as from ± 15 V dual supplies.

The ADA4091 family of op amps features a unique input stage that allows the input voltage to safely exceed either supply without any phase inversion or latch-up. The output voltage swings to within 10 mV of the supplies.

Applications for these amplifiers include portable telecommunications equipment, power supply control and protection, and interface for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezo-electric, and resistive transducers.

PIN CONFIGURATION

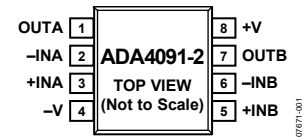


Figure 1. 8-Lead, Narrow Body SOIC

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios.

The ADA4091 family of op amps is specified over the extended industrial temperature range of -40°C to $+125^{\circ}\text{C}$. The ADA4091-2 is part of a growing family of 36 V, low power op amps from Analog Devices, Inc. (see Table 1).

The ADA4091-2 is available in an 8-lead plastic SOIC surface-mount package.

Table 1. Low Power, 36 V Operational Amplifiers

Family	Rail-to-Rail I/O	PJFET	Low Noise
Single			OP1177
Dual	ADA4091-2	AD8682	OP2177
Quad		AD8684	OP4177

Rev. 0

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REVISION HISTORY

10/08—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

$V_{SY} = \pm 1.5\text{ V}$, $V_{CM} = 0.15\text{ V}$, $V_O = 1.4\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-500	+45	+500	μV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-1.0		+1.0	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-50		+50	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-55		+55	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-275		+275	nA
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-5		+5	nA
Input Voltage Range	Common-Mode Rejection Ratio	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-5		+5	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-75		+75	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-1.5		+1.5	V
Large Signal Voltage Gain	A_{VO}	$\pm 1.5\text{ V} < V_{SY} \pm 18\text{ V}$	76			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	70			dB
		$R_L = 100\text{ k}\Omega$, $V_O = 0.3\text{ V}$ to 2.7 V	106			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$R_L = 10\text{ k}\Omega$, $V_O = 0.3\text{ V}$ to 2.7 V	93			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	85			dB
				2.5		$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to GND	1.495			V
		-40°C to $+125^\circ\text{C}$	1.490			V
		$R_L = 10\text{ k}\Omega$ to GND	1.475			V
		-40°C to $+125^\circ\text{C}$	1.455			V
Output Voltage Low	V_{OL}	$R_L = 100\text{ k}\Omega$ to GND			-1.498	V
		-40°C to $+125^\circ\text{C}$			-1.498	V
		$R_L = 10\text{ k}\Omega$ to GND			-1.495	V
		-40°C to $+125^\circ\text{C}$			-1.491	V
Short-Circuit Limit	I_{SC}	Sink/source = -40°C to $+125^\circ\text{C}$		± 31		mA
Open-Loop Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = 1$		102		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V}$ to 36 V	100			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100			dB
Supply Current per Amplifier	I_{SY}	$I_O = 0\text{ mA}$			200	μA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			300	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 100\text{ k}\Omega$, $C_L = 30\text{ pF}$		0.46		$\text{V}/\mu\text{s}$
Settling Time	t_s	To 0.01%		22		μs
Gain Bandwidth Product	GBP			1.22		MHz
Phase Margin	Φ_M			69		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		24		$\text{nV}/\sqrt{\text{Hz}}$

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$V_O = \pm 5.0\text{ V}$, $-4.9\text{ V} \leq V_{CM} \leq +4.9\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-500 -1.0	+141	+500 +1.00	μV mV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		30	60	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			2	nA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			30	nA
Common-Mode Rejection Ratio	CMRR	$\pm 1.5\text{ V} < V_{SY} \pm 18\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-5 88		+5	V dB
Large Signal Voltage Gain	A_{VO}	$R_L = 100\text{ k}\Omega$, $V_O = \pm 4.7\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $R_L = 10\text{ k}\Omega$, $V_O = \pm 4.7\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	113 103 98 87			dB dB dB dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to GND -40°C to $+125^\circ\text{C}$	4.980 4.980	4.990		V V
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $R_L = 100\text{ k}\Omega$ to GND -40°C to $+125^\circ\text{C}$ $R_L = 10\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.950 4.900	4.970	-4.990 -4.980 -4.980 -4.975	V V V V V
Short-Circuit Limit	I_{SC}	Sink/source = -40°C to $+125^\circ\text{C}$		± 20		mA
Open-Loop Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = 1$		77		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V}$ to 36 V $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100 100			dB dB
Supply Current per Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		180	225 300	μA μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 100\text{ k}\Omega$, $C_L = 30\text{ pF}$		0.46		V/ μs
Gain Bandwidth Product	GBP			1.22		MHz
Phase Margin	Φ_M			70		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		μV p-p
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		24		nV/ $\sqrt{\text{Hz}}$

$V_{SY} = \pm 15.0\text{ V}$, $-14.9\text{ V} \leq V_{CM} \leq +14.9\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-500		+500	μV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-1.2		+1.20	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-55		+55	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-80		+80	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-510		+510	nA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-2		+2	nA
Common-Mode Rejection Ratio	CMRR	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-10		+10	nA
		$\pm 1.5\text{ V} < V_{SY} < \pm 18\text{ V}$	-140		+140	nA
Large Signal Voltage Gain	A_{VO}	$R_L = 100\text{ k}\Omega$, $V_O = \pm 14.7\text{ V}$	-5		+5	V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	95			dB
		$R_L = 10\text{ k}\Omega$, $V_O = \pm 14.7\text{ V}$	90			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	116			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	106			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	102			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	92			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to GND	14.975			V
		-40°C to $+125^\circ\text{C}$	14.950			V
		$R_L = 10\text{ k}\Omega$ to GND	14.900			V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	14.800			V
Output Voltage Low	V_{OL}	$R_L = 100\text{ k}\Omega$ to GND			-14.990	V
		-40°C to $+125^\circ\text{C}$			-1.4990	V
		$R_L = 10\text{ k}\Omega$ to GND			-14.950	V
		-40°C to $+125^\circ\text{C}$			-14.940	V
Short-Circuit Limit	I_{SC}	Sink/source = -40°C to 125°C		± 20		mA
Open-Loop Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = 1$		71		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V}$ to 36 V	100			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100			dB
Supply Current per Amplifier	I_{SY}	$I_O = 0\text{ mA}$			250	μA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			350	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 100\text{ k}\Omega$, $C_L = 30\text{ pF}$		0.46		V/ μs
Gain Bandwidth Product	GBP			1.27		MHz
Phase Margin	Φ_M			72		Degrees
Channel Separation	CS	$f = 1\text{ kHz}$		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		25		nV/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	Refer to the Input Overvoltage Protection section
Differential Input Voltage ¹	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

¹ Input current should be limited to ± 5 mA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device soldered on a 4-layer JEDEC standard PCB with zero air flow.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC (R-8)	155	45	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

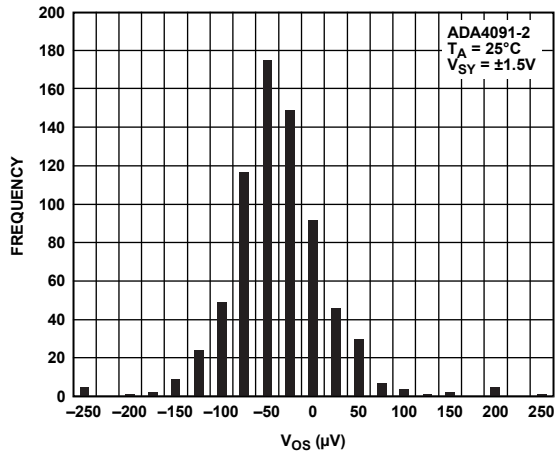


Figure 2. Input Offset Voltage Distribution

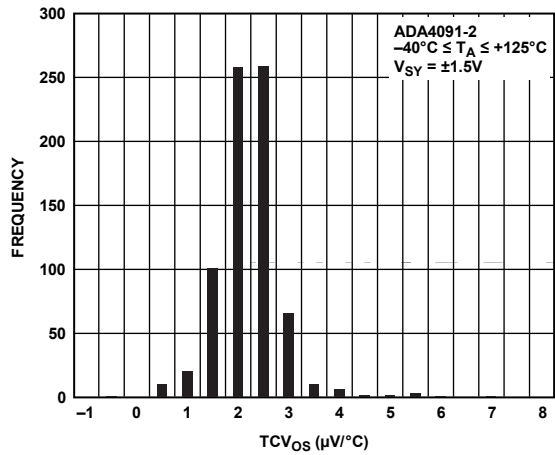


Figure 3. Input Offset Voltage vs. Temperature

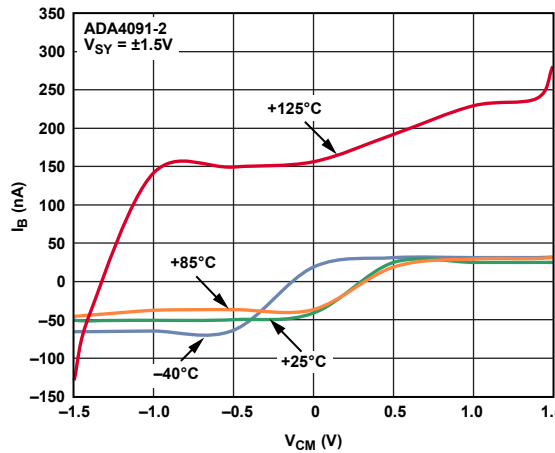


Figure 4. Input Bias Current vs. Input Common-Mode Voltage

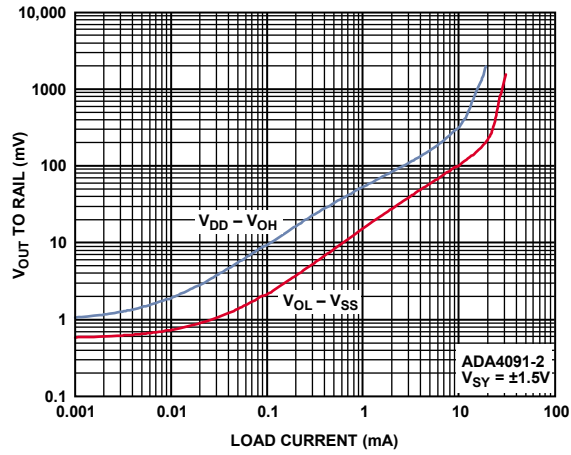


Figure 5. Dropout Voltage vs. Load Current

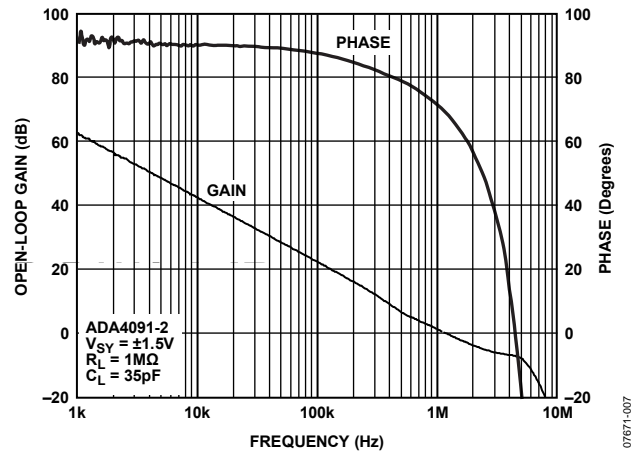


Figure 6. Open-Loop Gain and Phase vs. Frequency

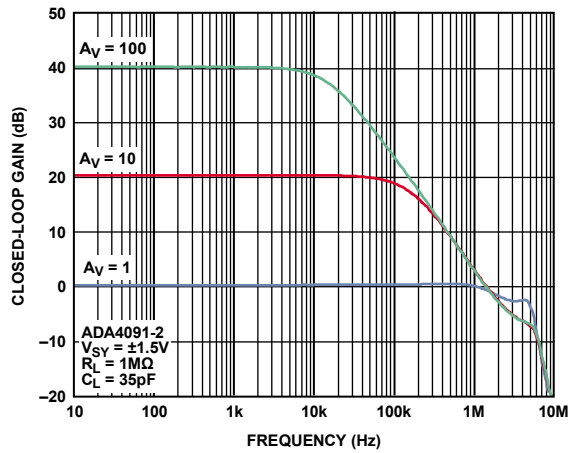


Figure 7. Closed-Loop Gain vs. Frequency

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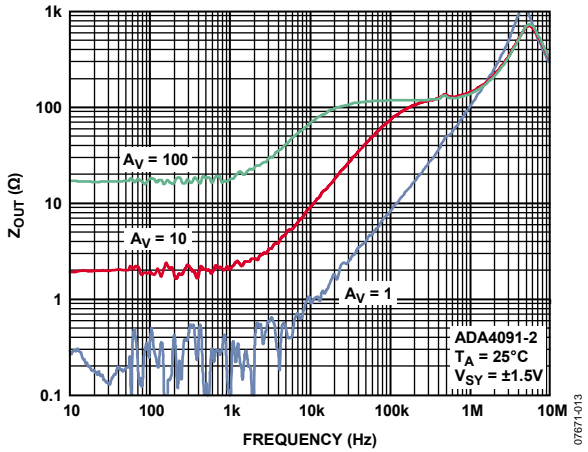


Figure 8. Output Impedance vs. Frequency

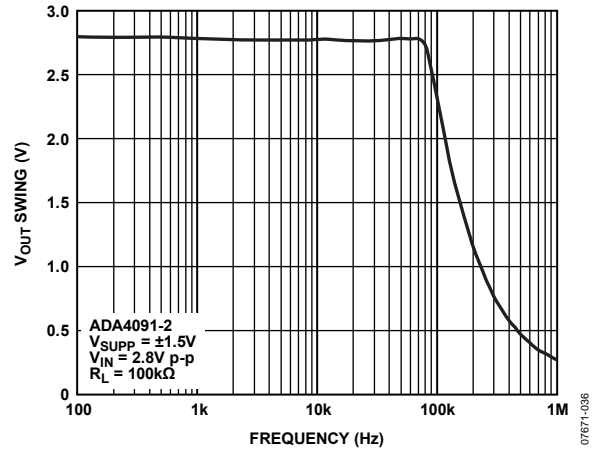


Figure 11. Output Swing vs. Frequency

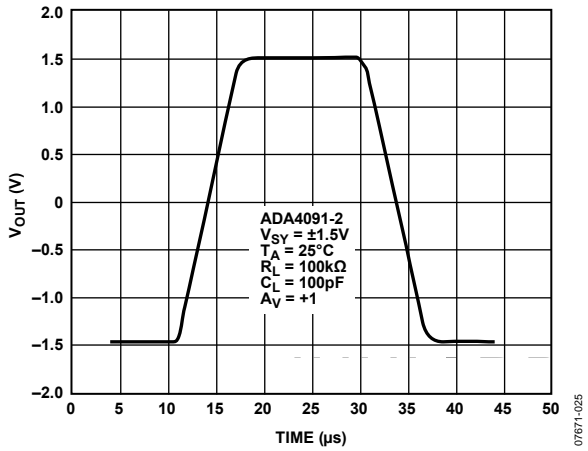


Figure 9. Large Signal Transient Response

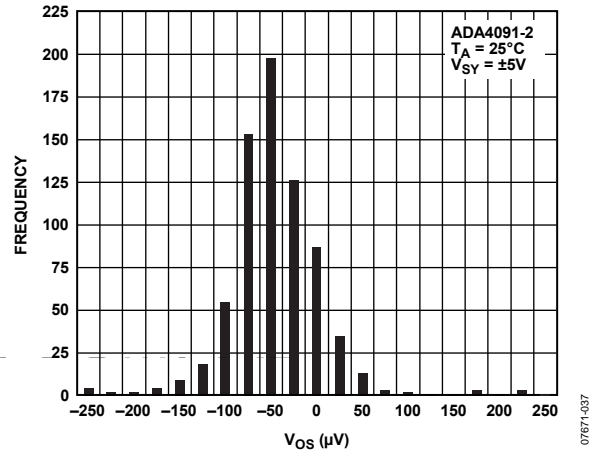


Figure 12. Input Offset Voltage Distribution

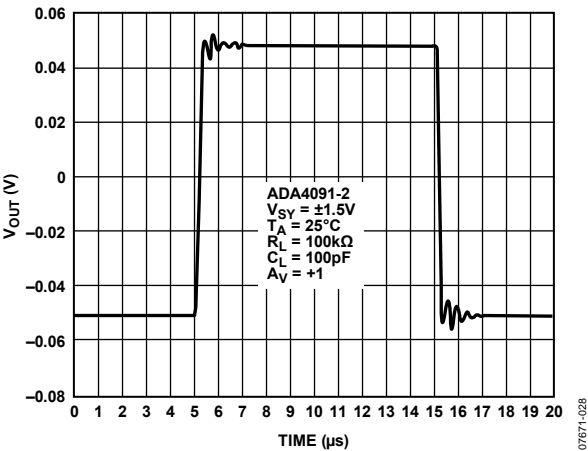


Figure 10. Small Signal Transient Response

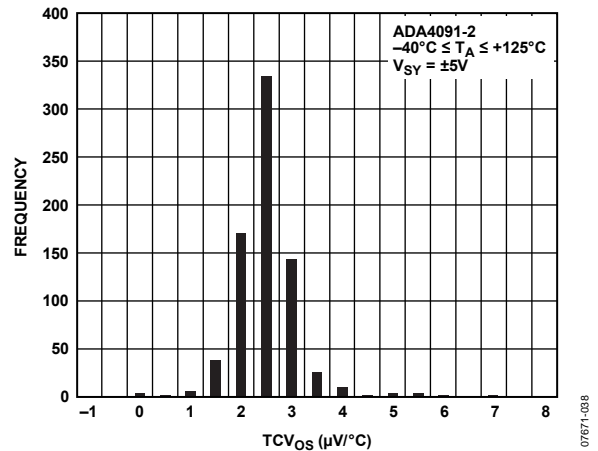


Figure 13. Input Offset Voltage vs. Temperature

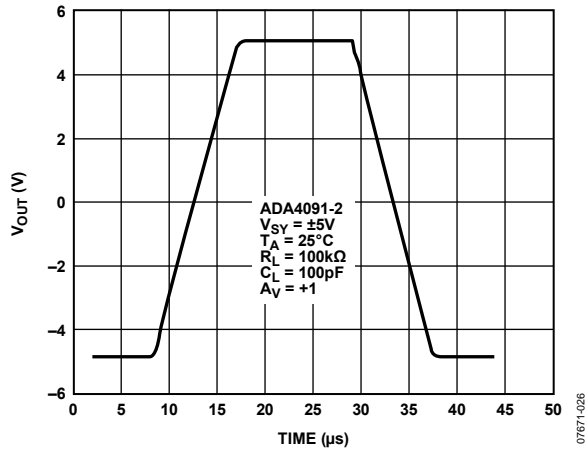


Figure 14. Large Signal Transient Response

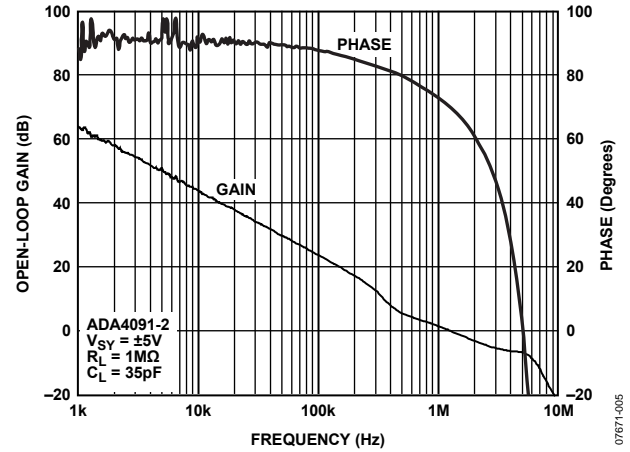


Figure 17. Open-Loop Gain and Phase vs. Frequency

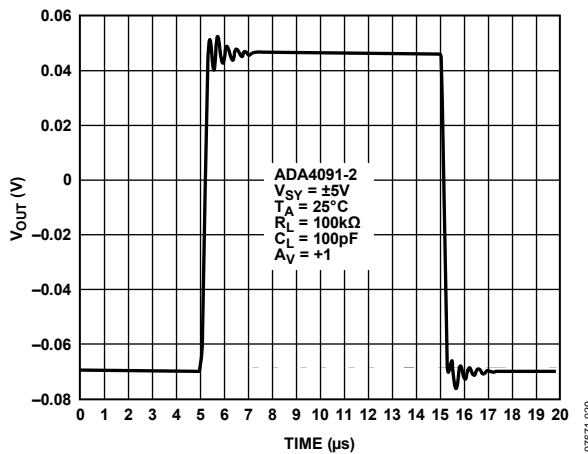


Figure 15. Small Signal Transient Response

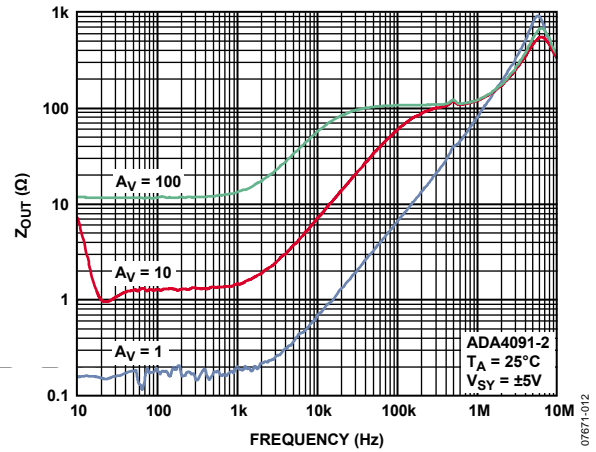


Figure 18. Output Impedance vs. Frequency

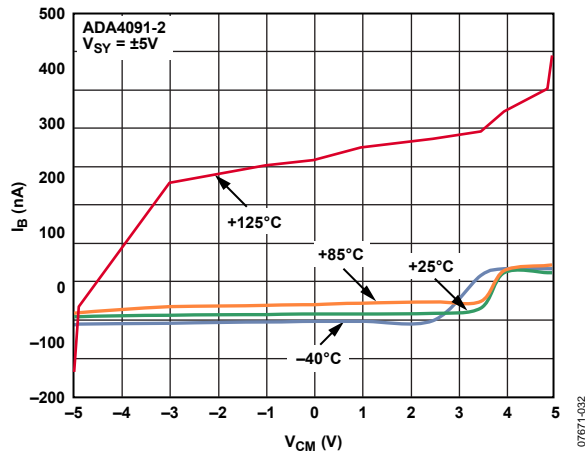


Figure 16. Input Bias Current vs. Common-Mode Voltage

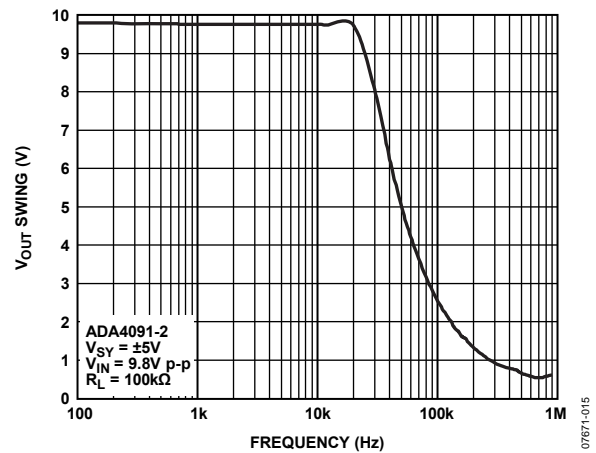


Figure 19. Output Voltage Swing vs. Frequency

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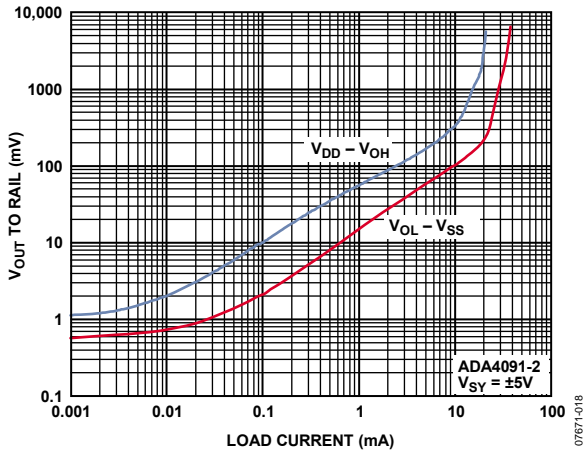


Figure 20. Dropout Voltage vs. Load Current

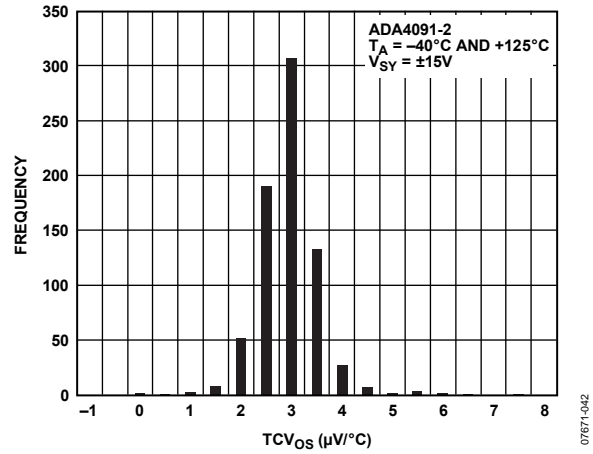


Figure 23. Offset Voltage TC

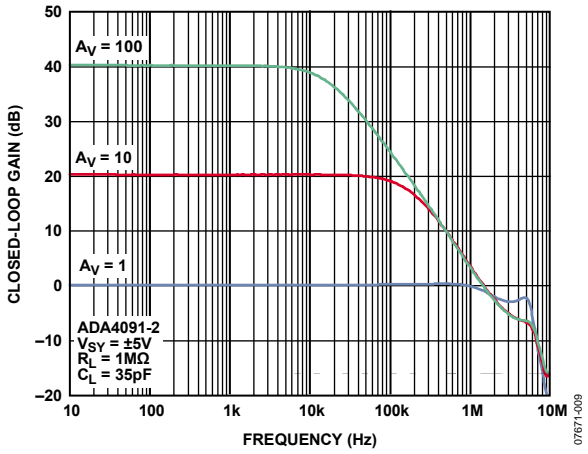


Figure 21. Closed-Loop Gain vs. Frequency

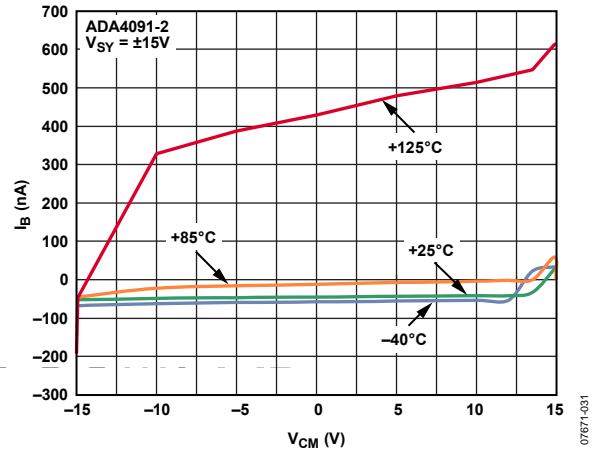


Figure 24. Input Bias Current vs. Common-Mode Voltage

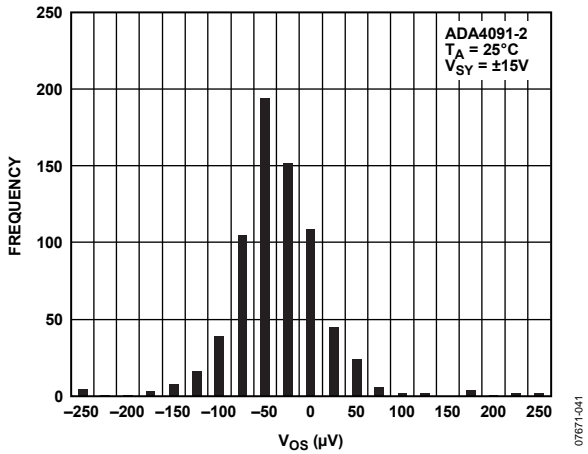


Figure 22. Input Offset Voltage Distribution

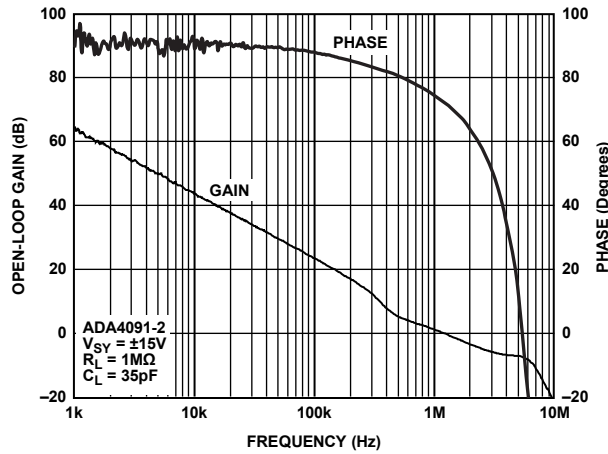


Figure 25. Open-Loop Gain and Phase vs. Frequency

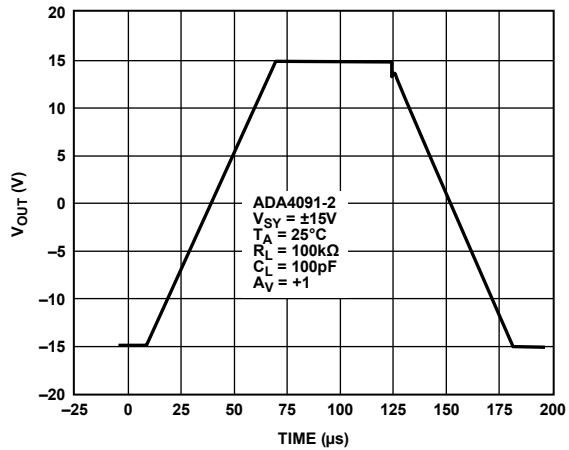


Figure 26. Large Signal Transient Response

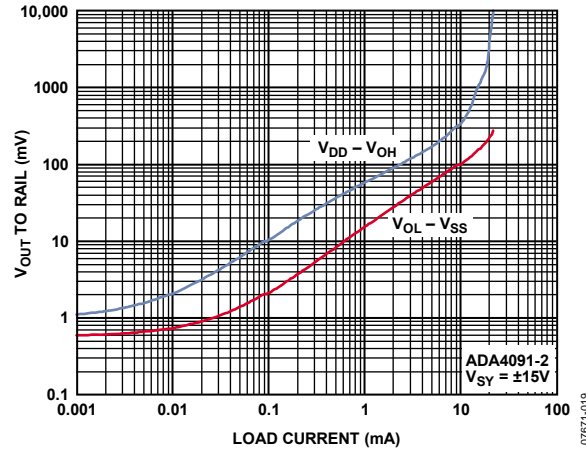


Figure 29. Dropout Voltage vs. Load Current

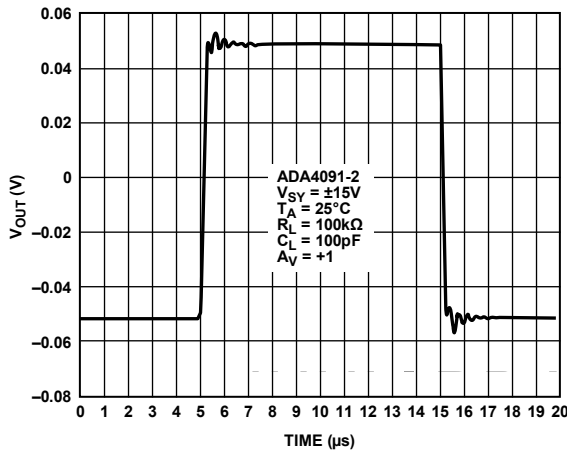


Figure 27. Small Signal Transient Response

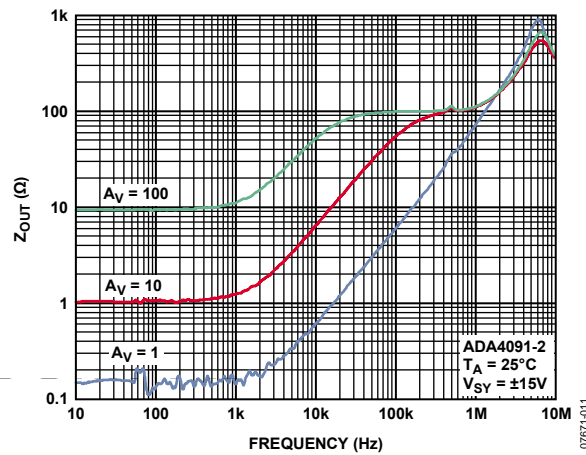


Figure 30. Output Impedance vs. Frequency

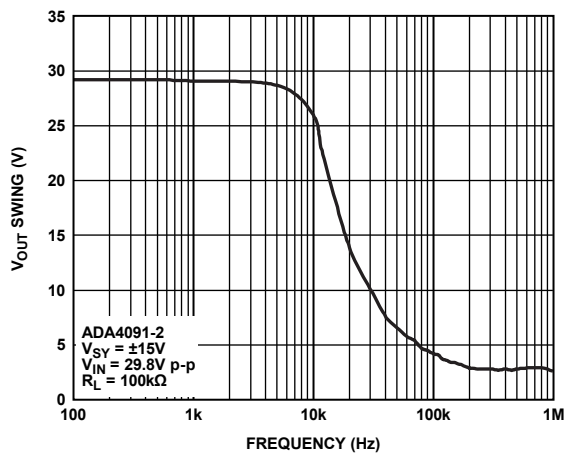


Figure 28. Output Voltage Swing vs. Frequency

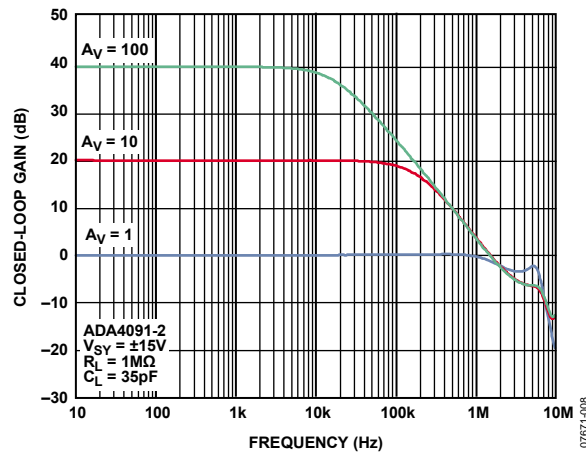


Figure 31. Closed-Loop Gain vs. Frequency

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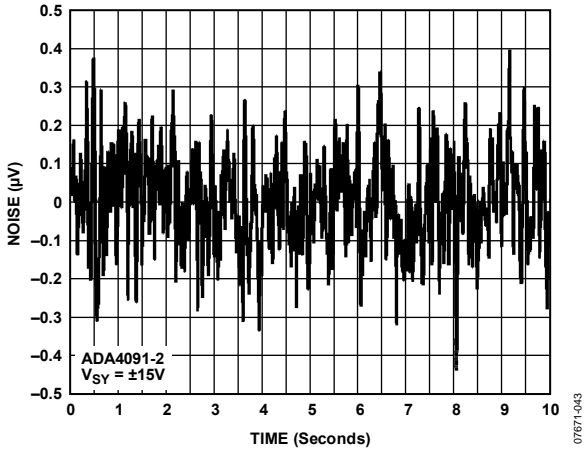


Figure 32. Voltage Noise, V_{p-p}

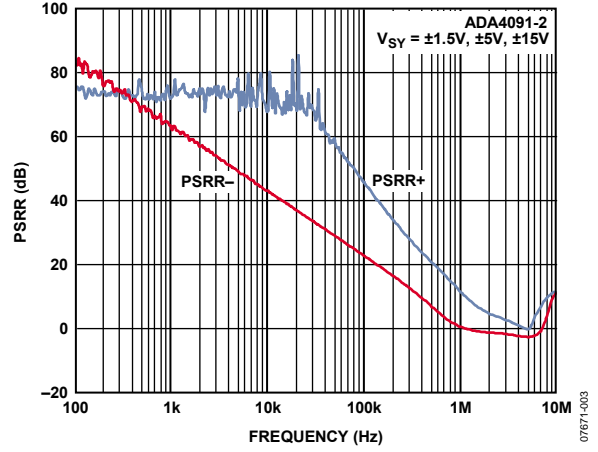


Figure 35. PSRR vs. Frequency

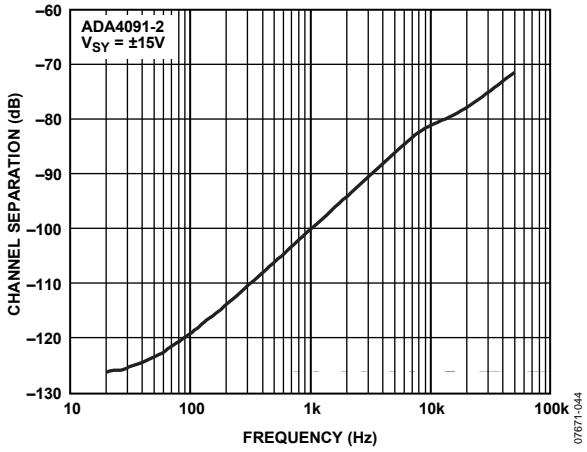


Figure 33. Channel Separation vs. Frequency

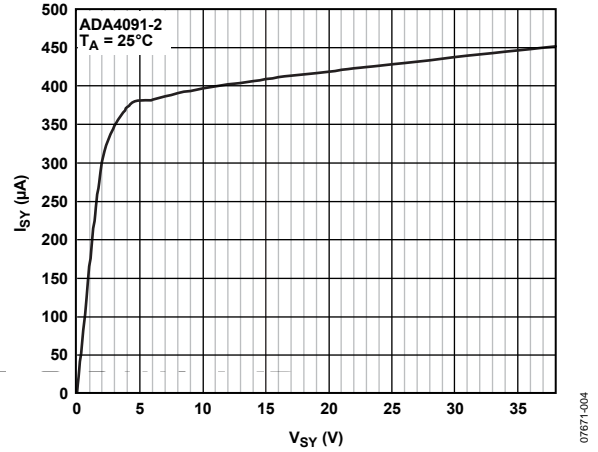


Figure 36. Supply Current vs. Supply Voltage

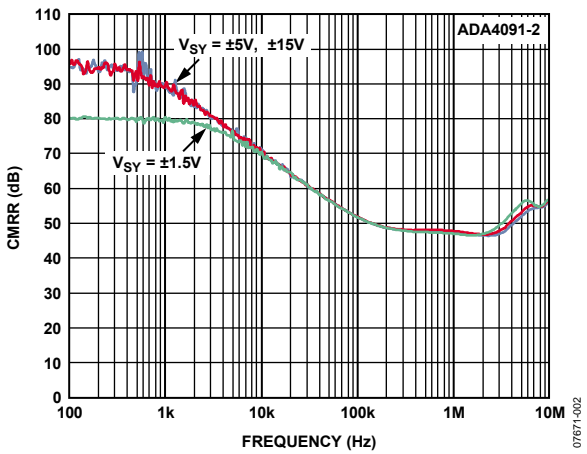


Figure 34. CMRR vs. Frequency

THEORY OF OPERATION

The ADA4091-2 is a single-supply, micropower amplifier featuring rail-to-rail inputs and outputs. To achieve wide input and output ranges, this amplifier employs unique input and output stages. In Figure 37, the input stage comprises two differential pairs, a PNP pair and an NPN pair. These two stages do not work in parallel. Instead, only one stage is on for any given input signal level. The PNP stage (Transistor Q1 and Transistor Q2) is required to ensure that the amplifier remains in the linear region when the input voltage approaches and reaches the negative rail. Alternatively, the NPN stage (Transistor Q5 and Transistor Q6) is needed for input voltages up to and including the positive rail.

For the majority of the input common-mode range, the PNP stage is active, as shown in Figure 4. Notice that the bias current switches direction at approximately 1.5 V below the positive rail. At voltages below this level, the bias current flows out of the ADA4091-2, from the PNP input stage. Above this voltage, however, the bias current enters the device, due to the NPN stage. The actual mechanism within the amplifier for switching between the input stages comprises Transistor Q3, Transistor Q4, and Transistor Q7. As the input common-mode voltage increases, the emitters of Q1 and Q2 follow that voltage plus a diode drop. Eventually, the emitters of Q1 and Q2 are high enough to turn on Q3, which diverts the tail current away from the PNP input stage, turning it off. Instead, the current is mirrored through Q4 and Q7 to activate the NPN input stage.

A common practice in bipolar amplifiers to protect the input transistors from large differential voltages is to include series resistors and differential diodes. (See Figure 39 for the full input protection circuitry.) These diodes turn on whenever the differential voltage exceeds approximately 0.6 V. In this condition, current flows between the input pins, limited only by the two 5 kΩ resistors. Evaluate each circuit carefully to make sure that the increase in current does not affect performance.

The output stage in the ADA4091-2 device uses a PNP and an NPN transistor, as do most output stages. However, Q32 and Q33, the output transistors, are actually connected with their collectors to the output pin to achieve the rail-to-rail output swing.

As the output voltage approaches either the positive or negative rail, these transistors begin to saturate. Thus, the final limit on output voltage is the saturation voltage of these transistors, which is about 50 mV. The output stage does have inherent gain arising from the collectors and any external load impedance. Because of this, the open-loop gain of the op amp is dependent on the load resistance.

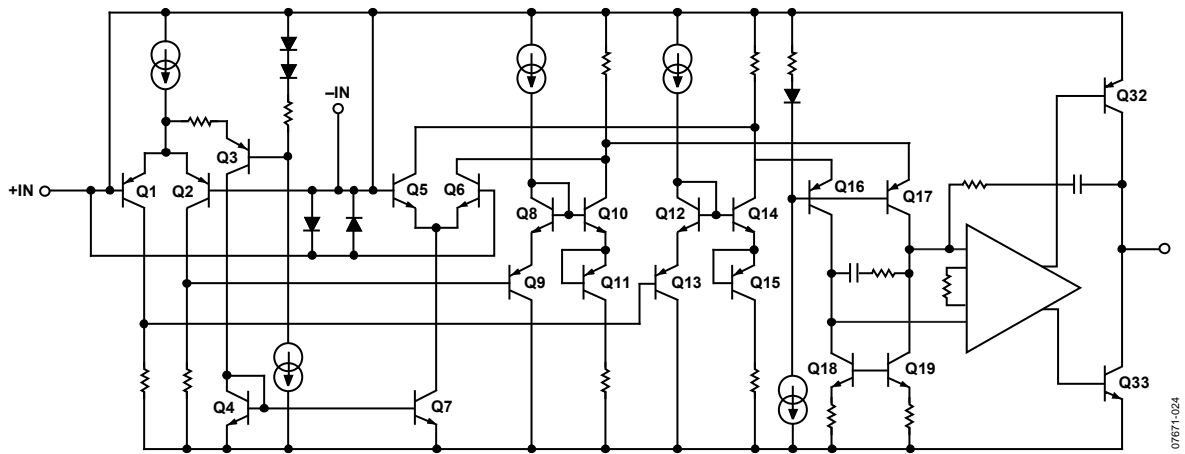


Figure 37. Simplified Schematic without Input Protection (see Figure 39)

ADA4091-2

INPUT OVERVOLTAGE PROTECTION

The ADA4091-2 has two different ESD circuits for enhanced protection as shown in Figure 39. One circuit is a series resistor of 5 k Ω to the internal inputs and diodes (D1 and D2 or D5 and D6) from the internal inputs to the supply rails. The other protection circuit is a circuit with two DIACs (D3 and D4 or D7 and D8) to the supply rails. A DIAC can be considered a bidirectional Zener diode with a transfer characteristic as shown in Figure 39.

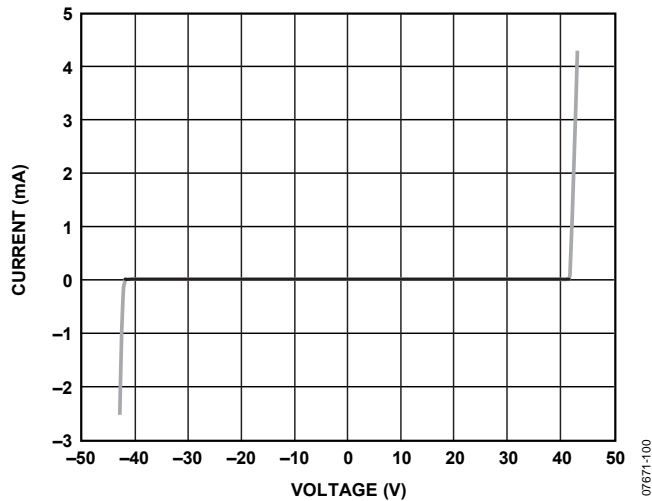


Figure 38. DIAC Transfer Characteristic

For a worst-case design analysis, consider two cases. The ADA4091-2 has the normal ESD structure from the internal op amp inputs to the supply rails. In addition, it has 42 V DIACs from the external inputs to the rails as shown in Figure 37.

Therefore, two conditions have to be considered to determine which one is the limiting factor.

- Condition 1. Consider, for example, that when operating on ± 15 V, the inputs can go +42 V above the negative supply rail. With the -V pin equal to -15 V, +42 V above this supply (the negative supply) is +27 V,
- Condition 2. There is also a restriction on the input current of 5 mA through a 5 k Ω resistor to the ESD structure to the positive rail. In Condition 1, +27 V through the 5 k Ω resistor to +15 V gives a current of 2.4 mA. Thus, the DIAC is the limiting factor. If the ADA4091-2 supply voltages are changed to ± 5 V, then -5 V + 42 V = 37 V. However, $+5$ V + (5 k Ω \times 5 mA) = 30 V. Thus, the normal resistor-diode structure is the limitation when running on lower supply voltages.

Additional resistance can be added externally in series with each input to protect against higher peak voltages, however the additional thermal noise of the resistors must be considered.

The flatband voltage noise of the ADA4091-2 is approximately 24 nV/ $\sqrt{\text{Hz}}$, and a 5 k Ω resistor has a noise of 9 nV/ $\sqrt{\text{Hz}}$. Adding an additional 5 k Ω resistor increases the total noise by less than 15% root-sum-square (RSS). Therefore, resistor values should be kept below this value if overall noise performance is critical.

Note that this is input protection under abnormal conditions only. The correct amplifier operation is only specified with an input voltage range as shown in the Specifications section of this data sheet.

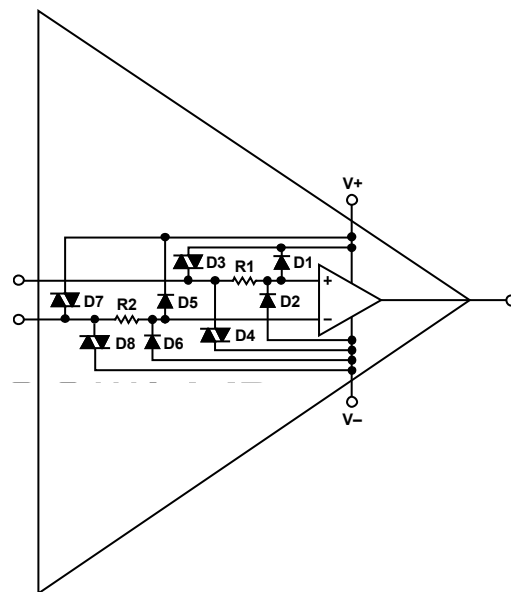
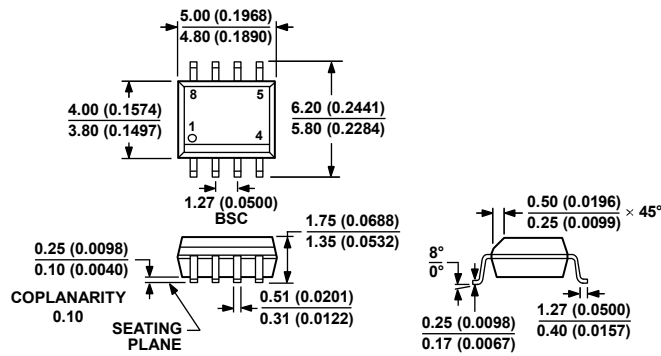


Figure 39. Complete Input Protection Network

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 40. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-8)

Dimensions shown in millimeters and (inches)

012407-A

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADA4091-2ARZ-R2 ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADA4091-2ARZ-R7 ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADA4091-2ARZ-RL ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

¹ Z = RoHS Compliant Part.

NOTES