



### FEATURES

- Serial data input: 12.3 Mb/s to 2.7 Gb/s
- Exceeds ITU-T Jitter Specifications
- Integrated Limiting Amp: 6mV sensitivity
- Adjustable slice level:  $\pm 100$  mV
- Patented dual-loop clock recovery architecture
- Programmable LOS detect and Slice Level
- Integrated PRBS Generator and Detector
- No reference clock required
- Loss of lock indicator
- Rate Selectivity without the use of a reference clock
- I<sup>2</sup>C™ interface to access optional features
- Single-supply operation: 3.3 V
- Low power: 1.0W
- 8 mm × 8 mm 56-lead LFCSP

### APPLICATIONS

- Passive Optical Network s
- SONET OC-1/3/12/48 and all associated FEC rates
- Fibre Channel, 2× Fibre Channel , GbE, HDTV, etc.
- WDM transponders
- Test equipment

### PRODUCT DESCRIPTION

The ADN2865 provides the receiver functions of quantization, signal level detect, and clock and data recovery for continuous data rates from 12.3 Mb/s to 2.7 Gb/s. An integrated deserialiser supports 8 bit parallel transfer to an FPGA or digital ASIC. The recovered clock can simultaneously serialize data supplied in an 8 bit parallel format.

The ADN2865 automatically locks to all data rates without the need for an external reference clock or programming. All SONET jitter requirements are exceeded, including jitter transfer, jitter generation, and jitter tolerance. All specifications are quoted for  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  ambient temperature, unless otherwise noted.

This device, together with a PIN diode and a TIA preamplifier, can implement a highly integrated, low cost, low power fiber optic receiver.

The ADN2865 have many optional features available via an I<sup>2</sup>C interface, e.g. the user can read back the data rate that the ADN2865 is locked on to, or the user can set the device to only lock to one particular data rate if provisioning of data rates is required.

### FUNCTIONAL BLOCK DIAGRAM

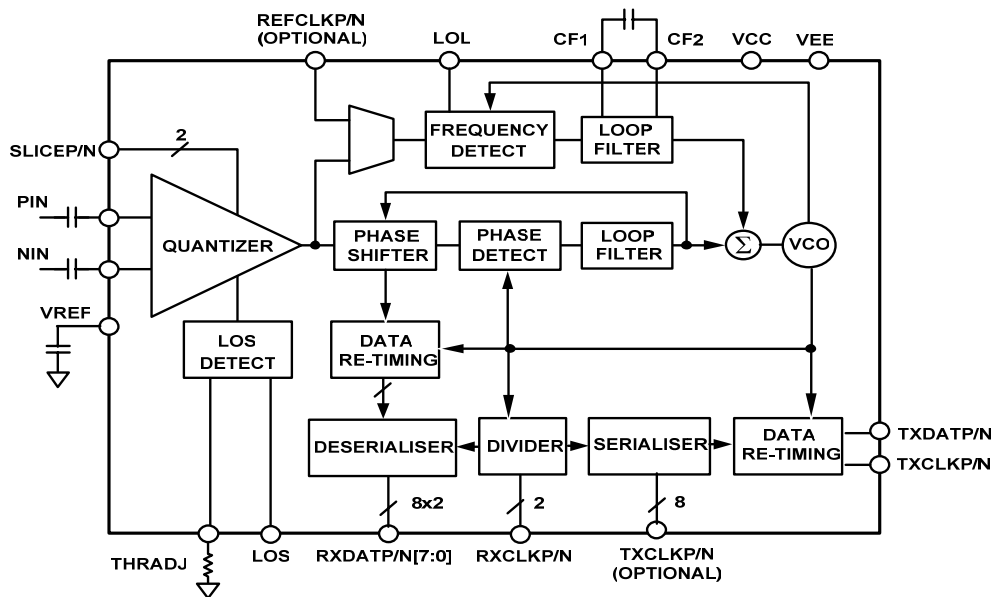


Figure 1 ADN2865 Functional Block Diagram

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### Rev.PrA

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### REVISION HISTORY

Revision 0: Initial Version

Revision A: Remove Minimum Supply Current Spec

Revision B: Update spec table

## SPECIFICATIONS

$T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = V_{MIN}$  to  $V_{MAX}$ ,  $V_{EE} = 0$  V,  $C_F = 0.47$   $\mu$ F, SLICEP = SLICEN = VEE, Input Data Pattern: PRBS  $2^{23} - 1$ , unless otherwise noted.

**Table 1.**

Parameter	Conditions	Min	Typ	Max	Unit
<b>QUANTIZER—DC CHARACTERISTICS</b>					
Input Voltage Range	@ PIN or NIN, dc-coupled	1.8		2.8	V
Peak-to-Peak Differential Input	PIN – NIN			2.0	V
Input Common Mode Level	DC-coupled (see Figure , Figure , and Figure )	2.3	2.5	2.8	V
Differential Input Sensitivity	$2^{23} - 1$ PRBS, ac-coupled, <sup>1</sup> BER = $1 \times 10^{-10}$	TBD	TBD		mV p-p
Input Overdrive	(see Figure )	TBD	TBD		mV p-p
Input Offset			TBD		$\mu$ V
Input RMS Noise	BER = $1 \times 10^{-10}$		TBD		$\mu$ V rms
<b>QUANTIZER—AC CHARACTERISTICS</b>					
Data Rate		12.3		2700	Mb/s
S11	@ 2.5 GHz		-15		dB
Input Resistance	Differential		100		$\Omega$
Input Capacitance			0.65		pF
<b>QUANTIZER—SLICE ADJUSTMENT</b>					
Gain	SLICEP – SLICEN = $\pm 0.5$ V	TBD	0.1	TBD	V/V
Differential Control Voltage Input	SLICEP – SLICEN			TBD	V
Control Voltage Range	DC level @ SLICEP or SLICEN	VEE		0.95	V
Slice Threshold Offset			1		mV
<b>LOSS OF SIGNAL DETECT (LOS)</b>					
Loss of Signal Detect Range (see Figure 2)	$R_{Thresh} = 0 \Omega$	TBD		TBD	mV
	$R_{Thresh} = 100 \text{ k}\Omega$	TBD		TBD	mV
Hysteresis (Electrical)	OC-48 $R_{Thresh} = 0 \Omega$	TBD		TBD	dB
	$R_{Thresh} = 100 \text{ k}\Omega$	TBD		TBD	dB
	OC-1 $R_{Thresh} = 0 \Omega$	TBD		TBD	dB
	$R_{Thresh} = 10 \text{ k}\Omega$	TBD		TBD	dB
LOS Assert Time	DC-coupled <sup>2</sup>		TBD		ns
LOS De-Assert Time	DC-coupled <sup>2</sup>		TBD		ns
<b>LOSS OF LOCK DETECT (LOL)</b>					
VCO Frequency Error for LOL Assert	With respect to nominal		1000		ppm
VCO Frequency Error for LOL De-Assert	With respect to nominal		250		ppm
LOL Response Time	12.3 Mb/s		4		ms
	OC-12		1.0		$\mu$ s
	OC-48		1.0		$\mu$ s
<b>ACQUISITION TIME</b>					
Lock to Data Mode	OC-48		1.3		ms
	OC-12		2.0		ms
	OC-3		3.4		ms
	OC-1		9.8		ms
	12.3 Mb/s		40.0		ms
Optional Lock to REFCLK Mode			10.0		ms

<sup>1</sup> PIN and NIN should be differentially driven and ac-coupled for optimum sensitivity.

<sup>2</sup> When ac-coupled, the LOS assert and de-assert time is dominated by the RC time constant of the ac coupling capacitor and the 50  $\Omega$  input termination of the ADN2865 input stage.

Parameter	Conditions	Min	Typ	Max	Unit
DATA RATE READBACK ACCURACY					
Coarse Readback	(See Table )		10		%
Fine Readback	In addition to REFCLK accuracy			200	ppm
	Data rate $\leq$ 20 Mb/s			100	ppm
	Data rate $>$ 20 Mb/s				
POWER SUPPLY VOLTAGE		3.0	3.3	3.6	V
POWER SUPPLY CURRENT			300	350	mA
OPERATING TEMPERATURE RANGE		-40		+85	°C

## JITTER SPECIFICATIONS

$T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = V_{MIN}$  to  $V_{MAX}$ ,  $V_{EE} = 0$  V,  $C_F = 0.47$  uF, SLICEP = SLICEN = VEE, Input Data Pattern: PRBS  $2^{23} - 1$ , unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
PHASE-LOCKED LOOP CHARACTERISTICS					
Jitter Transfer BW	OC-48			2000	kHz
	OC-12			500	kHz
	OC-3			130	kHz
Jitter Peaking	OC-48		0	0.1	dB
	OC-12		0	0.1	dB
	OC-3		0	0.1	dB
Jitter Generation	OC-48, 12 kHz to 20 MHz		TBD	TBD	UI rms
			TBD	0.33	UI p-p
	OC-12, 12 kHz to 5 MHz		TBD	TBD	UI rms
			TBD	0.2	UI p-p
	OC-3, 12 kHz to 1.3 MHz		TBD	TBD	UI rms
			TBD	0.2	UI p-p
Jitter Tolerance	OC-48, $2^{23} - 1$ PRBS				
	100 kHz	0.75			UI p-p
	1 MHz	0.075			UI p-p
	20 MHz	0.075			UI p-p
	OC-12, $2^{23} - 1$ PRBS				
	25 kHz	0.75			UI p-p
	250 kHz <small>Error! Bookmark not defined.</small>	0.075			UI p-p
	OC-3, $2^{23} - 1$ PRBS				
	6500 Hz	0.75			UI p-p
	65 kHz	0.075			UI p-p
Power Supply Rejection	See Figure XX.		TBD		dB

**OUTPUT AND TIMING SPECIFICATIONS**

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
<b>CML OUPUT CHARACTERISTICS</b>					
Single-Ended Output Swing	V <sub>SE</sub> (see Figure 75)	300	350	600	mV
Differential Output Swing	V <sub>DIFF</sub> (see Figure 75)	600	700	1200	mV
Output High Voltage	V <sub>OH</sub>			VCC	V
Output Low Voltage	V <sub>OL</sub>	VCC – 0.6	VCC – 0.35	VCC – 0.3	V
<b>CML Ouput Timing</b>					
Rise Time	20% to 80%			TBD	ps
Fall Time	80% to 20%			TBD	ps
<b>LVDS OUPUT CHARACTERISTICS (RXCLKP/N, RXDATP/N)</b>					
Differential Output Swing	V <sub>DIFF</sub> (see Figure 4)	250	320	400	mV
Output High Voltage	V <sub>OH</sub>			1475	mV
Output Low Voltage	V <sub>OL</sub>	925			V
Output Offset Voltage	V <sub>OS</sub>	1125	1200	1275	V
Output Impedance Differential			100		Ω
<b>LVDS Ouputs Timing</b>					
Rise Time	20% to 80%		115	220	ps
Fall Time	80% to 20%		115	220	ps
Setup Time	T <sub>S</sub> (see Figure 4), OC-48	2.61			ns
Hold Time	T <sub>H</sub> (see Figure 4), OC-48	-1.70			ns
<b>I<sup>2</sup>C INTERFACE DC CHARACTERISTICS</b>					
Input High Voltage	V <sub>IH</sub>	0.7 VCC			V
Input Low Voltage	V <sub>IL</sub>			0.3 VCC	V
Input Current	V <sub>IN</sub> = 0.1 VCC or V <sub>IN</sub> = 0.9 VCC	-10.0		+10.0	μA
Output Low Voltage	V <sub>OL</sub> , I <sub>OL</sub> = 3.0 mA			0.4	V
<b>I<sup>2</sup>C INTERFACE TIMING (See Figure )</b>					
SCK Clock Frequency				400	kHz
SCK Pulse Width High	t <sub>HIGH</sub>	600			ns
SCK Pulse Width Low	t <sub>LOW</sub>	1300			ns
Start Condition Hold Time	t <sub>HD;STA</sub>	600			ns
Start Condition Setup Time	t <sub>SU;STA</sub>	600			ns
Data Setup Time	t <sub>SU;DAT</sub>	100			ns
Data Hold Time	t <sub>HD;DAT</sub>	300			ns
SCK/SDA Rise/Fall Time	T <sub>R</sub> /T <sub>F</sub>	20 + 0.1 Cb <sup>1</sup>		300	ns
Stop Condition Setup Time	t <sub>SU;STO</sub>	600			ns
Bus Free Time between a Stop and a Start	t <sub>BUF</sub>	1300			ns
<b>REFCLK CHARACTERISTICS</b>					
Input Voltage Range	Optional lock to REFCLK mode @ REFCLKP or REFCLKN				
	V <sub>IL</sub>		0		V
	V <sub>IH</sub>		VCC		V
Minimum Differential Input Drive			100		mV p-p
Reference Frequency		12.3		200	MHz
Required Accuracy			100		ppm
<b>LVTTTL DC INPUT CHARACTERISTICS</b>					
Input High Voltage	V <sub>IH</sub>	2.0			V
Input Low Voltage	V <sub>IL</sub>			0.8	V
Input High Current	I <sub>IH</sub> , V <sub>IN</sub> = 2.4 V			5	μA

<sup>1</sup> Cb = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times are allowed (see Table 6).

Parameter	Conditions	Min	Typ	Max	Unit
Input Low Current	$I_{IL}, V_{IN} = 0.4\text{ V}$	-5			$\mu\text{A}$
LVTTTL INPUT TIMING					
Setup Time (Sync Mode)	$T_{SSU}$ (see Figure 3), 1.25Gb/s	3.60			ns
Hold Time (Sync Mode)	$T_{SH}$ (see Figure 3), 1.25Gb/s	0.70			ns
Setup Time (Align Mode)	$T_{ASU}$ (see Figure 4), 1.25Gb/s	TBD			ns
Hold Time (Align Mode)	$T_{AH}$ (see Figure 4), 1.25Gb/s	TBD			ns
LVTTTL DC OUTPUT CHARACTERISTICS					
Output High Voltage	$V_{OH}, I_{OH} = -2.0\text{ mA}$	2.4			V
Output Low Voltage	$V_{OL}, I_{OL} = 2.0\text{ mA}$			0.4	V

## ABSOLUTE MAXIMUM RATINGS

$T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = V_{MIN}$  to  $V_{MAX}$ ,  $V_{EE} = 0$  V,  $C_F = 0.47$   $\mu$ F,  $SLICEP = SLICEN = V_{EE}$ , unless otherwise noted.

Table 4.

Parameter	Rating
Supply Voltage (VCC)	4.2 V
Minimum Input Voltage (All Inputs)	$V_{EE} - 0.4$ V
Maximum Input Voltage (All Inputs)	$V_{CC} + 0.4$ V
Maximum Junction Temperature	125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering 10 s)	300°C

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL CHARACTERISTICS

### Thermal Resistance

56-LFCSP, 4-layer board with exposed paddle soldered to VEE  
 $\theta_{JA} = 28^\circ\text{C/W}$

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

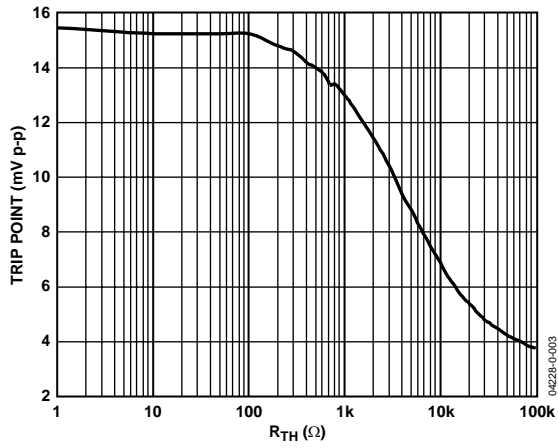


Figure 2. LOS Comparator Trip Point Programming

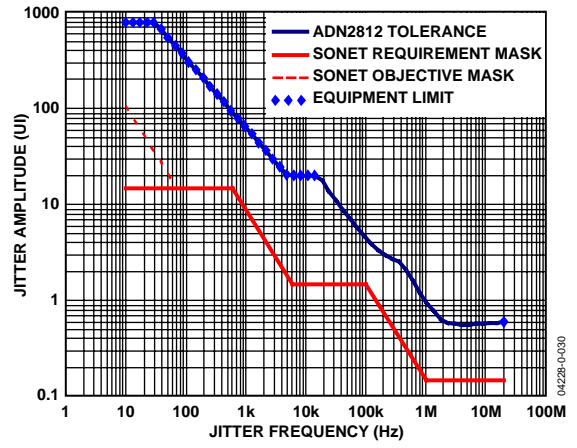


Figure 3. Typical Measured Jitter Tolerance OC-48



# TIMING CHARACTERISTICS

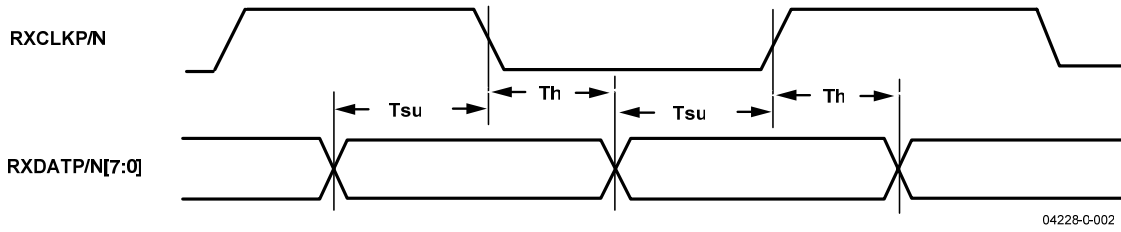


Figure 4. Rx Output Timing

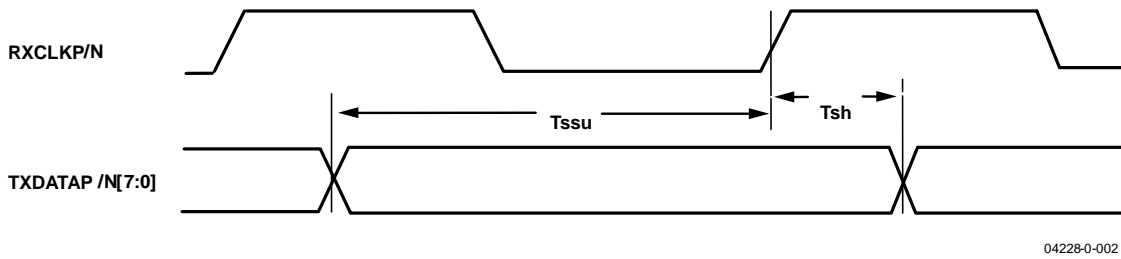


Figure 5. Tx Input Timing (Sync Mode)

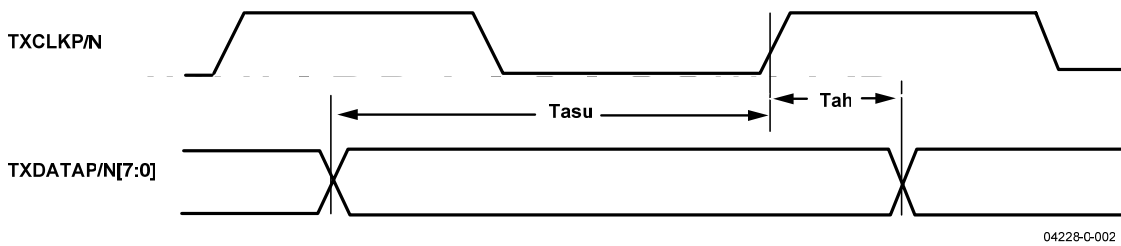


Figure 6. Tx Input Timing (Align Mode)

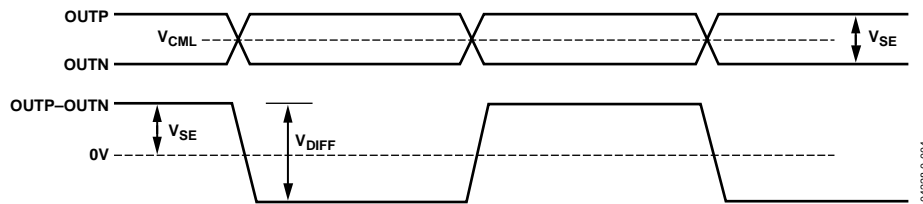


Figure 75. Single-Ended vs. Differential Output Specifications

**PIN CONFIGURATION AND FUNCTION DESCRIPTIONS**

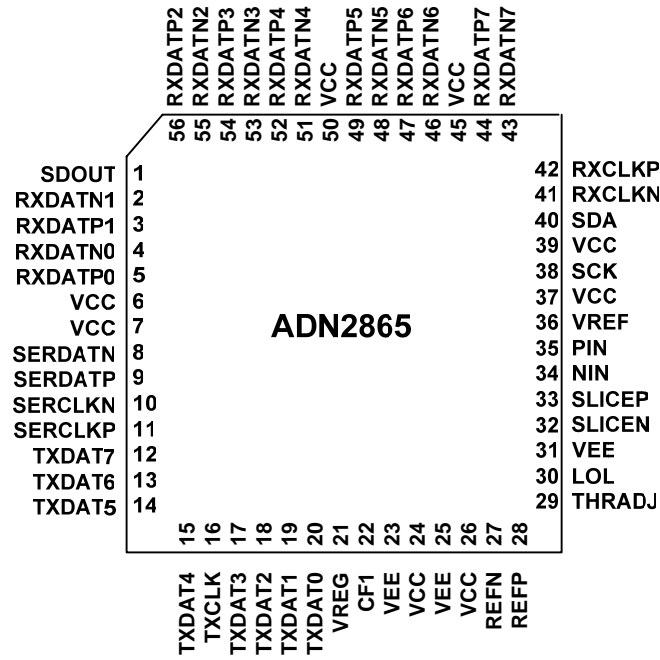


Figure 86. Pin Configuration

Table 5. Pin Function Descriptions

Pin #	Mnemonic	Type	Description
1	SDOUT	DO	Active high, Loss of signal indicator. (LVTTTL)
2	RXDATN1	DO	Differential receive data output. (LVDS)
3	RXDATP1	DO	Differential receive data output. (LVDS)
4	RXDATN0	DO	Differential receive data output. <b>Last bit received.</b> (LVDS)
5	RXDATP0	DO	Differential receive data output. <b>Last bit received.</b> (LVDS)
6	VCC3	PWR	Power for CDR & Serialiser
7	VCC7	PWR	Power for CML drivers
8	SERDATN	DO	Differential serialized data output to LDD. (CML)
9	SERDATP	DO	Differential serialized data output to LDD. (CML)
10	SERCLKN	DO	Differential clock for serialized Tx data. (CML)
11	SERCLKP	DO	Differential clock for serialized Tx data. (CML)
12	TXDAT7	DI	Transmit data input. <b>First bit sent.</b> (LVTTTL)
13	TXDAT6	DI	Transmit data input. (LVTTTL)
14	TXDAT5	DI	Transmit data input. (LVTTTL)
15	TXDAT4	DI	Transmit data input. (LVTTTL)
16	TXCLK	DI	Qualifying clock for transmit data input. (LVTTTL)
17	TXDAT3	DI	Transmit data input. (LVTTTL)
18	TXDAT2	DI	Transmit data input. (LVTTTL)
19	TXDAT1	DI	Transmit data input. (LVTTTL)
20	TXDAT0	DI	Transmit data input. <b>Last bit sent.</b> (LVTTTL)
21	VREG	AO	Decoupling node for VCO power.
22	CF1	AO	PLL loop filter capacitor.
23	VEE2	PWR	Ground for VCO / PLL / Gm
24	VCC2	PWR	Power for VCO / PLL / Gm
25	VEE4	PWR	Ground for FLL
26	VCC4	PWR	Power for FLL
27	REFN	DI	Reference clock input. (LVDS/LVTTTL)
28	REFP	DI	Reference clock input. (LVDS/LVTTTL)
29	THRADJ	AO	LOS Threshold Setting Resistor.
30	LOL	DO	Active high, Loss-of-Lock Indicator. (LVTTTL)
31	VEE1	PWR	Ground for Limamp / LOS
32	SLICEN	AI	Differential Slice Level Adjust Input.
33	SLICEP	AI	Differential Slice Level Adjust Input.
34	NIN	AI	Differential serial input to Limiting Amp. (CML)
35	PIN	AI	Differential serial input to Limiting Amp. (CML)
36	VREF	AO	Decoupling node for internal voltage reference.
37	VCC1	PWR	Power for Limamp / LOS
38	SCK	DI	I2C Serial Clock Input.
39	VCC6	PWR	Power for Deserialiser, LVDS pre-drivers
40	SDA	DI	I2C Serial Data Input.
41	RXCLKN	DO	Qualifying clock for Rx Data Outputs. (LVDS)
42	RXCLKP	DO	Qualifying clock for Rx Data Outputs. (LVDS)
43	RXDATN7	DO	Differential receive data output. <b>Last bit received.</b> (LVDS)
44	RXDATP7	DO	Differential receive data output. <b>Last bit received.</b> (LVDS)
45	VCC5	PWR	Power for LVDS drivers
46	RXDATN6	DO	Differential receive data output. (LVDS)
47	RXDATP6	DO	Differential receive data output. (LVDS)
48	RXDATN5	DO	Differential receive data output. (LVDS)
49	RXDATP5	DO	Differential receive data output. (LVDS)
50	VCC5	PWR	Power for LVDS Drivers
51	RXDATN4	DO	Differential receive data output. (LVDS)
52	RXDATP4	DO	Differential receive data output. (LVDS)
53	RXDATN3	DO	Differential receive data output. (LVDS)
54	RXDATP3	DO	Differential receive data output. (LVDS)
55	RXDATN2	DO	Differential receive data output. (LVDS)
56	RXDATP2	DO	Differential receive data output. (LVDS)

<sup>1</sup>Type: P = power, AI = analog input, AO = analog output, DI = digital input, DO = digital output.



Table 6. Internal Register Map<sup>1</sup>

Reg Name	R/W	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0	
FREQ0	R	0x0	MSB							LSB	
FREQ1	R	0x1	MSB							LSB	
FREQ2	R	0x2	0	MSB						LSB	
RATE	R	0x3	COARSE_RD[8] Coarse Data Readback							COARSE_RD[1]	
MISC	R	0x4	X	X	Los Status	Static LOL	LOL Status	Datarate meas complete	X	COARSE_RD[0] LSB	
CTRLA	W	0x8	Fref Range		Data Rate/DIV FREF Ratio				Measure Data Rate	Lock to Reference	
CTRLA_RD	R	0x5	Readback CTRLA								
CTRLB	W	0x9	Config LOL	Reset MISC[4]	System Reset	0	Reset MISC[2]	0	0	0	
CTRLB_RD	R	0x6	Readback CTRLB								
CTRLC	W	0x11	0	0	Set Signal Degrade Threshold	Enable Signal Degrade	LOS forces acquisition	Config LOS	Squelch Mode	Boost Output	
CTRLD	W	0x22	CDR Bypass	Power Down LVDS Drivers	Power Down GML Drivers	Squelch Output Buffers	Initiate PBS Sequence	PRBS Mode[2:0]			
CTRL E	W	0x27	RXCLK Alignment			Align	TX Mode	Reverse RX Bus	Reverse TX Bus	0	
FDDI_MODE	W	0x0D	FDDI Mode Enable	Subharmonic Ratio					0	0	
SEL_MODE	W	0x34	0	0	Acq Mode	Cont Rate / Single Rate	Datarate Range	CLK Holdover Mode 2A	CLK Holdover Mode 2B	0	
HI_CODE	W	0x35	HI_CODE[8]							HI_CODE[1]	
LO_CODE	W	0x36	LO_CODE[8]							LO_CODE[1]	
CODE_LSB	W	0x39	0	0	0	0	0	0	HI_CODE[0]	LO_CODE[0]	

<sup>1</sup> All writeable registers default to 0x00.

Table 7. Miscellaneous Register, MISC

		LOS Status	Static LOL	LOL Status	Datarate Measurement Complete	Coarse Rate Readback LSB	
D7	D6	D5	D4	D3	D2	D1	D0
x	x	0 = No loss of signal 1 = Loss of signal	0 = Waiting for next LOL 1 = Static LOL until reset	0 = Locked 1 = Acquiring	0 = Measuring datarate 1 = Measurement complete	x	COARSE_RD[0]

Table 8. Control Register, CTRLA<sup>1</sup>

F <sub>REF</sub> Range		Datarate/Div_F <sub>REF</sub> Ratio	Measure Datarate	Lock to Reference
D7	D6	D5 D4 D3 D2	D1	D0
0	0	12.3 MHz to 25 MHz	0 0 0 0 1	0 = Lock to input data 1 = Lock to reference clock
0	1	25 MHz to 50 MHz	0 0 0 1 2	
1	0	50 MHz to 100 MHz	0 0 1 0 4	
1	1	100 MHz to 200 MHz	n 2 <sup>n</sup>	
			1 0 0 0 256	

<sup>1</sup>Where DIV\_F<sub>REF</sub> is the divided down reference referred to the 12.3 MHz to 25 MHz band (see the Reference Clock (Optional) section).

Table 9. Control Register, CTRLB

Config LOL	Reset MISC[4]	System Reset		Reset MISC[2]			
D7	D6	D5	D4	D3	D2	D1	D0
0 = LOL pin normal operation 1 = LOL pin is static LOL	Write a 1 followed by 0 to reset MISC[4]	Write a 1 followed by 0 to reset ADN2865	Set to 0	Write a 1 followed by 0 to reset MISC[2]	Set to 0	Set to 0	Set to 0

Table 10. Control Register, CTRLC

Signal Degrade Threshold		Signal Degrade Mode		Config LOS	SERCLK		
D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Set to 0	0=Set SD Threshold to 9mV 1=Set SD Threshold to 1.9x LOS Threshold	0= Disable Signal Degrade Mode 1= Enable Signal Degrade Mode	Set to 0	0 = Active high LOS 1 = Active low LOS	0 = Power Down SERCLK buffer 1 = Enable SERCLK buffer	Set to 0

Table 11. Control Register, CTRLD

CDR Bypass	Buffer Control				Initiate PRBS	PRBS Mode		
D7	D6	D5	D4	D3	D2	D1	D0	
0=CDR Enabled 1=CDR Disabled	0=Normal operation 1=Power Down LVDS drivers	0=Normal operation 1=Power Down CML drivers	0	Write a 1 followed by 0 to initiate PRBS Generate Sequence	0 0 0	0 0 1	0 1 0	Power Down Generate Mode Detect Mode, compares errors

Table 12. Control Register, CTRL E

RXCLK Alignment to RXDATA				Tx Mode		Bus Reversal		
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0=Sync Mode	0=Enable align	RXDATA[7:0]	TXDATA[7:0]	Set
0	0	1	+1 UI	1=Align	1=Disable align	0=Bit 0 is last received 1=Bit 7 is last received	0=Bit 0 is last sent 1=Bit 7 is last sent	To 0
0	1	0	0					
0	1	1	-3 UI					
1	0	0	+4 UI					
1	0	1	+2 UI					
1	1	0	+4 UI					
1	1	1	-2 UI					

Table 13. FDDI\_MODE

FDDI Enable	Subharmonic Ratio [6..2]					D1	D0
D7	D6	D5	D4	D3	D2		
0= FDDI Mode Disabled	0	0	0	0	1 = 1	Set to 0	Set to 0
1= FDDI Mode Enabled	0	0	0	1	0 = 2		
	0	0	0	1	1 = 3		
	1	1	1	1	1 = 31		

Table 14. SEL\_MODE

		Mode Control 2	Mode Control 1	Mode Control 0	Clock Holdover Mode 2A	Clock Holdover Mode 2B	
D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Set to 0	0=LTD/LTR Mode 1=LTR Mode Only	0= Continuous Rate 1= Single Rate	0= Full Range (12.3M-2.7G) 1= Limited Range	Set to 1 for Clock Holdover Mode 2A	Set to 1 for Clock Holdover Mode 2B	Set to 0

Table 15. CTLF

					CDR Mode		
D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	0	0	0= NDC -> OB
					1	0	1= NDC -> PRBS

## TERMINOLOGY

### Input Sensitivity and Input Overdrive

Sensitivity and overdrive specifications for the quantizer involve offset voltage, gain, and noise. The relationship between the logic output of the quantizer and the analog voltage input is shown in Figure 14. For sufficiently large positive input voltage, the output is always Logic 1 and, similarly for negative inputs, the output is always Logic 0. However, the transitions between output Logic Levels 1 and 0 are not at precisely defined input voltage levels, but occur over a range of input voltages. Within this range of input voltages, the output might be either 1 or 0, or it might even fail to attain a valid logic state. The width of this zone is determined by the input voltage noise of the quantizer. The center of the zone is the quantizer input offset voltage. Input overdrive is the magnitude of signal required to guarantee the correct logic level with  $1 \times 10^{-10}$  confidence level.

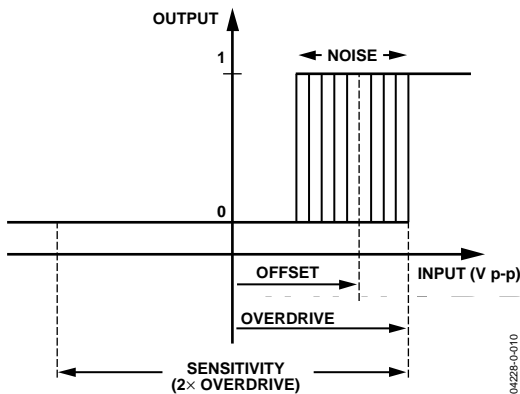


Figure 14. Input Sensitivity and Input Overdrive

### Single-Ended vs. Differential

AC coupling is typically used to drive the inputs to the quantizer. The inputs are internally dc biased to a common-mode potential of  $\sim 2.5$  V. Driving the ADN2865 single-ended and observing the quantizer input with an oscilloscope probe at the point indicated in Figure 15 shows a binary signal with an average value equal to the common-mode potential and instantaneous values both above and below the average value. It is convenient to measure the peak-to-peak amplitude of this signal and call the minimum required value the quantizer sensitivity. Referring to Figure 14, because both positive and negative offsets need to be accommodated, the sensitivity is twice the overdrive. The ADN2865 quantizer typically has 6 mV p-p sensitivity.

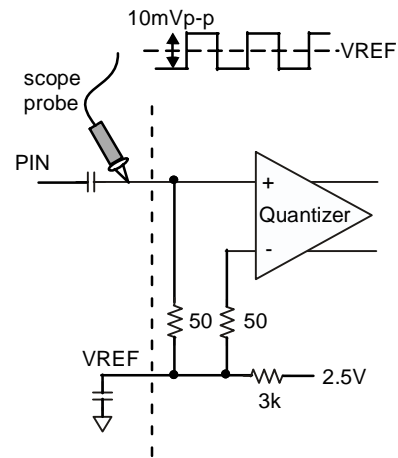


Figure 15. Single-Ended Sensitivity Measurement

Driving the ADN2865 differentially (see Figure 16), sensitivity seems to improve from observing the quantizer input with an oscilloscope probe. This is an illusion caused by the use of a single-ended probe. A 5 mV p-p signal appears to drive the ADN2865 quantizer. However, the single-ended probe measures only half the signal. The true quantizer input signal is twice this value, because the other quantizer input is a complementary signal to the signal being observed.

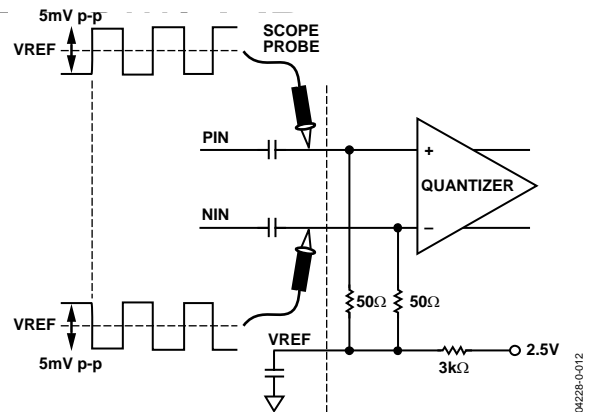


Figure 16. Differential Sensitivity Measurement

### LOS Response Time

LOS response time is the delay between removal of the input signal and indication of loss of signal (LOS) at the LOS output, Pin 22. When the inputs are dc-coupled, the LOS assert time of the AD2817 is 500 ns typically and the de-assert time is 400 ns typically. In practice, the time constant produced by the ac coupling at the quantizer input and the 50  $\Omega$  on-chip input termination determines the LOS response time.



## JITTER SPECIFICATIONS

The ADN2865 CDR is designed to achieve the best bit-error-rate (BER) performance and exceeds the jitter transfer, generation, and tolerance specifications proposed for SONET/SDH equipment defined in the Telcordia Technologies specification.

Jitter is the dynamic displacement of digital signal edges from their long-term average positions, measured in unit intervals (UI), where 1 UI = 1 bit period. Jitter on the input data can cause dynamic phase errors on the recovered clock sampling edge. Jitter on the recovered clock causes jitter on the retimed data.

The following sections briefly summarize the specifications of jitter generation, transfer, and tolerance in accordance with the Telcordia document (GR-253-CORE, Issue 3, September 2000) for the optical interface at the equipment level and the ADN2865 performance with respect to those specifications.

### JITTER GENERATION

The jitter generation specification limits the amount of jitter that can be generated by the device with no jitter and wander applied at the input. For OC-48 devices, the band-pass filter has a 12 kHz high-pass cutoff frequency with a roll-off of 20 dB/decade, and a low-pass cutoff frequency of at least 20 MHz. The jitter generated must be less than 0.01 UI rms, and must be less than 0.1 UI p-p.

### JITTER TRANSFER

The jitter transfer function is the ratio of the jitter on the output signal to the jitter applied on the input signal versus the frequency. This parameter measures the limited amount of the jitter on an input signal that can be transferred to the output signal (see Figure ).

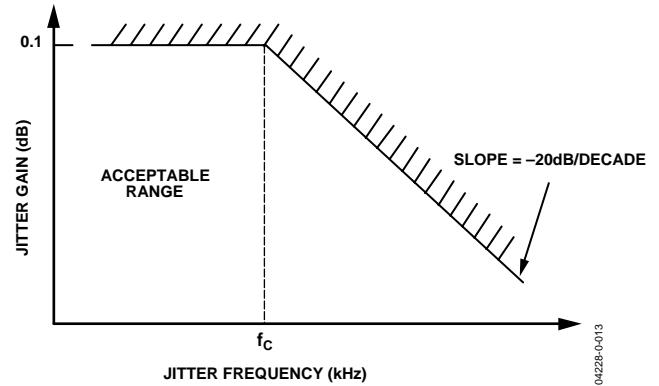


Figure 17. Jitter Transfer Curve

### JITTER TOLERANCE

The jitter tolerance is defined as the peak-to-peak amplitude of the sinusoidal jitter applied on the input signal, which causes a 1 dB power penalty. This is a stress test intended to ensure that no additional penalty is incurred under the operating conditions (see Figure ).

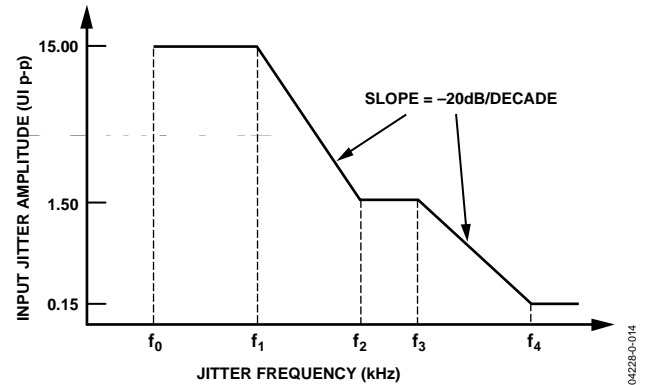


Figure 18. SONET Jitter Tolerance Mask

## THEORY OF OPERATION

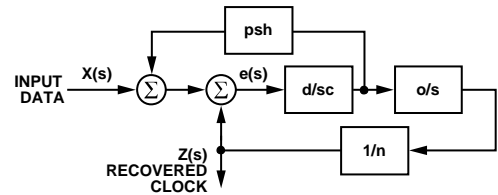
The ADN2865 is a delay- and phase-locked loop circuit for clock recovery and data retiming from an NRZ encoded data stream. The phase of the input data signal is tracked by two separate feedback loops, which share a common control voltage. A high speed delay-locked loop path uses a voltage controlled phase shifter to track the high frequency components of input jitter. A separate phase control loop, comprised of the VCO, tracks the low frequency components of input jitter. The initial frequency of the VCO is set by yet a third loop, which compares the VCO frequency with the input data frequency and sets the coarse tuning voltage. The jitter tracking phase-locked loop controls the VCO by the fine-tuning control.

The delay- and phase-loops together track the phase of the input data signal. For example, when the clock lags input data, the phase detector drives the VCO to higher frequency, and also increases the delay through the phase shifter; both these actions serve to reduce the phase error between the clock and data. The faster clock picks up phase, while the delayed data loses phase. Because the loop filter is an integrator, the static phase error is driven to zero.

Another view of the circuit is that the phase shifter implements the zero required for frequency compensation of a second-order phase-locked loop, and this zero is placed in the feedback path and, thus, does not appear in the closed-loop transfer function. Jitter peaking in a conventional second-order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Because this circuit has no zero in the closed-loop transfer, jitter peaking is minimized.

The delay- and phase-loops together simultaneously provide wide-band jitter accommodation and narrow-band jitter filtering. The linearized block diagram in Figure 19 shows that the jitter transfer function,  $Z(s)/X(s)$ , is a second-order low-pass providing excellent filtering. Note that the jitter transfer has no zero, unlike an ordinary second-order phase-locked loop. This means that the main PLL loop has virtually zero jitter peaking (see Figure 20). This makes this circuit ideal for signal regenerator applications, where jitter peaking in a cascade of regenerators can contribute to hazardous jitter accumulation.

The error transfer,  $e(s)/X(s)$ , has the same high-pass form as an ordinary phase-locked loop. This transfer function is free to be optimized to give excellent wide-band jitter accommodation, because the jitter transfer function,  $Z(s)/X(s)$ , provides the narrow-band jitter filtering.



$d$  = PHASE DETECTOR GAIN  
 $o$  = VCO GAIN  
 $c$  = LOOP INTEGRATOR  
 $psh$  = PHASE SHIFTER GAIN  
 $n$  = DIVIDE RATIO

**JITTER TRANSFER FUNCTION**

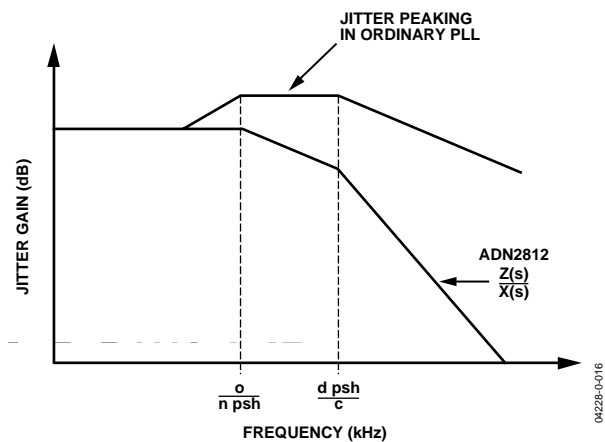
$$\frac{Z(s)}{X(s)} = \frac{1}{s^2 \frac{cn}{do} + s \frac{n psh}{o} + 1}$$

**TRACKING ERROR TRANSFER FUNCTION**

$$\frac{e(s)}{X(s)} = \frac{s^2}{s^2 + s \frac{d psh}{c} + \frac{do}{cn}}$$

04228-0-015

Figure 19. ADN2865 PLL/DLL Architecture



04228-0-016

Figure 20. ADN2865 Jitter Response vs. Conventional PLL

The delay- and phase-loops contribute to overall jitter accommodation. At low frequencies of input jitter on the data signal, the integrator in the loop filter provides high gain to track large jitter amplitudes with small phase error. In this case, the VCO is frequency modulated and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the VCO tuning range. A wider tuning range gives larger accommodation of low frequency jitter. The internal loop control voltage remains small for small phase errors, so the phase shifter remains close to the center of its range and thus contributes little to the low frequency jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the VCO are not large enough to track input jitter. In this case, the VCO control voltage becomes large and saturates, and the VCO frequency dwells at one extreme of its tuning range or the other. The size of the VCO tuning range, therefore, has only a small effect on the jitter accommodation. The delay-locked loop control voltage is now larger, and so the phase shifter takes on the burden of tracking the input jitter. The phase shifter range, in UI, can be seen as a broad plateau on the jitter tolerance curve. The phase shifter has a minimum range of 2 UI at all data rates.

The gain of the loop integrator is small for high jitter frequencies, so that larger phase differences are needed to make the loop control voltage big enough to tune the range of the phase shifter. Large phase errors at high jitter frequencies

cannot be tolerated. In this region, the gain of the integrator determines the jitter accommodation. Because the gain of the loop integrator declines linearly with frequency, jitter accommodation is lower with higher jitter frequency. At the highest frequencies, the loop gain is very small, and little tuning of the phase shifter can be expected. In this case, jitter accommodation is determined by the eye opening of the input data, the static phase error, and the residual loop jitter generation. The jitter accommodation is roughly 0.5 UI in this region. The corner frequency between the declining slope and the flat region is the closed loop bandwidth of the delay-locked loop, which is roughly 3 MHz at OC-48.

## FUNCTIONAL DESCRIPTION

### SERDES

The ADN2865 has an integrated serializer / deserializer and clock divider which allows the continuous rate CDR to interface directly to an FPGA or digital ASIC, such as a Media Access Controller (MAC), resulting in power and space savings.

The recovered clock is divided by 16 and is used to transfer 8 bits of receive data to the MAC on both the rising and falling edge. Both RXCLKP/N and RXDATAP/N[7:0] use LVDS signaling for noise reasons and have a relative phase which is adjustable via the I2C interface, per table 12 on page 14.

Half rate (1.25Gb/s) transmit data can also be serialised by the ADN2865 at the CML output using the recovered clock from the receive channel. An optional CML clock output is available. The parallel interface consists of 8 LVCMOS / LVTTTL inputs with an optional TXCLK at the divide by 8 rate. Two timing modes are available, sync mode and align mode.

#### Sync Mode

This is the default mode of operation, and does not require a TXCLK signal. Instead, TXDATA[7:0] is timed from RXCLK and the round trip delay between these signals must meet the setup and hold time requirement specified in table 3 to avoid corrupting the serial bit stream. Sync mode is useful in applications which require a stable timing relationship between the input and output serial bit streams.

#### Align Mode

This mode is controlled using the I2C interface and requires the use of TXCLK which is used to latch TXDATA internally. When enabled, align mode centers this latched data with respect to the internal divide by 8 sampling clock, which can render the interface less sensitive to variation in the timing of TXDATA[7:0] relative to RXCLK. In a typical application, the propagation delay between RXCLK and TXDATA[7:0] will vary with process, temperature and supply voltage through the external MAC device. This variation can be calibrated out by enabling and then disabling align mode. The downside to using align mode is that the calibration process leads to additional uncertainty in the serial bit timing relative to the input bit stream by +/- 1 UI. In align mode, it is necessary to meet the setup and hold time for TXDATA[7:0] relative to TXCLK.

Bit order reversal is supported for both the receive and transmit parallel buses using the I2C interface.

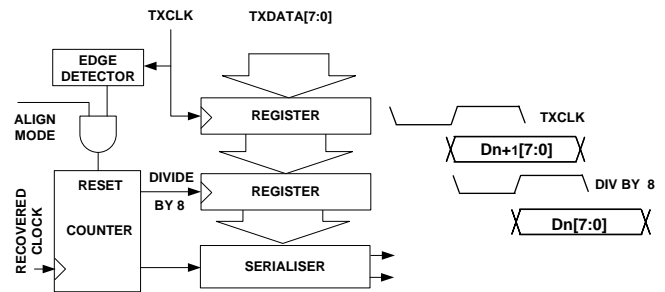


Figure 21. Align Mode Operation

### FREQUENCY ACQUISITION

The ADN2865 acquires frequency from the data over a range of data frequencies from 12.3 Mb/s to 2.7 Gb/s. The lock detector circuit compares the frequency of the VCO and the frequency of the incoming data. When these frequencies differ by more than 1000 ppm, LOL is asserted. This initiates a frequency acquisition cycle. The VCO frequency is reset to the bottom of its range, which is 12.3 MHz. The frequency detector then compares this VCO frequency and the incoming data frequency and increments the VCO frequency, if necessary. Initially, the VCO frequency is incremented in large steps to aid fast acquisition. As the VCO frequency approaches the data frequency, the step size is reduced until the VCO frequency is within 250 ppm of the data frequency, at which point LOL is de-asserted.

Once LOL is de-asserted, the frequency-locked loop is turned off. The PLL/DLL pulls in the VCO frequency the rest of the way until the VCO frequency equals the data frequency.

The frequency loop requires a single external capacitor between CF1 and CF2, Pins 14 and 15. A  $0.47 \mu\text{F} \pm 20\%$ , X7R ceramic chip capacitor with  $< 10 \text{ nA}$  leakage current is recommended. Leakage current of the capacitor can be calculated by dividing the maximum voltage across the  $0.47 \mu\text{F}$  capacitor,  $\sim 3 \text{ V}$ , by the insulation resistance of the capacitor. The insulation resistance of the  $0.47 \mu\text{F}$  capacitor should be greater than  $300 \text{ M}\Omega$ .

### LOCK DETECTOR OPERATION

The lock detector on the ADN2865 has three modes of operation: normal mode, REFCLK mode, and static LOL mode.

#### Normal Mode

In normal mode, the ADN2865 is a continuous rate CDR that locks onto any data rate from 12.3 Mb/s to 2.7 Gb/s without the use of a reference clock as an acquisition aid. In this mode, the lock detector monitors the frequency difference between the VCO and the input data frequency, and de-asserts the loss of lock signal, which appears on LOL Pin 30, when the VCO is

within 250 ppm of the data frequency. This enables the D/PLL, which pulls the VCO frequency in the remaining amount and also acquires phase lock. Once locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss of lock signal is re-asserted and control returns to the frequency loop, which begins a new frequency acquisition starting at the lowest point in the VCO operating range, 12.3 MHz. The LOL pin remains asserted until the VCO locks onto a valid input data stream to within 250 ppm frequency error. This hysteresis is shown in Figure 22.

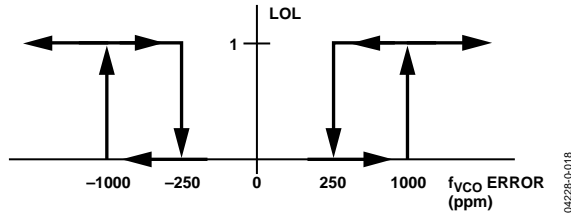


Figure 22. Transfer Function of LOL

**LOL Detector Operation Using a Reference Clock**

In this mode, a reference clock is used as an acquisition aid to lock the ADN2865 VCO. Lock to reference mode is enabled by setting CTRLA[0] to 1. The user also needs to write to the CTRLA[7:6] and CTRLA[5:2] bits in order to set the reference frequency range and the divide ratio of the data rate with respect to the reference frequency. For more details, see the Reference Clock (Optional) section. In this mode, the lock detector monitors the difference in frequency between the divided down VCO and the divided down reference clock. The loss of lock signal, which appears on the LOL Pin 30, is de-asserted when the VCO is within 250 ppm of the desired frequency. This enables the D/PLL, which pulls the VCO frequency in the remaining amount with respect to the input data and also acquires phase lock. Once locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss of lock signal is re-asserted and control returns to the frequency loop, which re-acquires with respect to the reference clock. The LOL pin remains asserted until the VCO frequency is within 250 ppm of the desired frequency. This hysteresis is shown in Figure 22.

**Static LOL Mode**

The ADN2865 implements a static LOL feature, which indicates if a loss of lock condition has ever occurred and remains asserted, even if the ADN2865 regains lock, until the static LOL bit is manually reset. The I<sup>2</sup>C register bit, MISC[4], is the static LOL bit. If there is ever an occurrence of a loss of lock condition, this bit is internally asserted to logic high. The MISC[4] bit remains high even after the ADN2865 has re-acquired lock to a new data rate. This bit can be reset by writing a 1 followed by 0 to I<sup>2</sup>C Register Bit CTRLB[6]. Once reset, the MISC[4] bit remains de-asserted until another loss of lock condition occurs.

Writing a 1 to I<sup>2</sup>C Register Bit CTRLB[7] causes the LOL pin, Pin 16, to become a static LOL indicator. In this mode, the LOL pin mirrors the contents of the MISC[4] bit and has the functionality described in the previous paragraph. The CTRLB[7] bit defaults to 0. In this mode, the LOL pin operates in the normal operating mode, that is, it is asserted only when the ADN2865 is in acquisition mode and de-asserts when the ADN2865 has re-acquired lock.

**HARMONIC DETECTOR**

The ADN2865 provides a harmonic detector, which detects whether or not the input data has changed to a lower harmonic of the data rate that the VCO is currently locked onto. For example, if the input data *instantaneously* changes from OC-48, 2.488 Gb/s, to an OC-12, 622.080 Mb/s bit stream, this could be perceived as a valid OC-48 bit stream, because the OC-12 data pattern is exactly 4x slower than the OC-48 pattern. So, if the change in data rate is instantaneous, a 101 pattern at OC-12 would be perceived by the ADN2865 as a 111100001111 pattern at OC-48. If the change to a lower harmonic is instantaneous, a typical CDR could remain locked at the higher data rate.

The ADN2865 implements a harmonic detector that automatically identifies whether or not the input data has switched to a lower harmonic of the data rate that the VCO is currently locked onto. When a harmonic is identified, the LOL pin is asserted and a new frequency acquisition is initiated. The ADN2865 automatically locks onto the new data rate, and the LOL pin is de-asserted.

However, the harmonic detector does not detect higher harmonics of the data rate. If the input data rate switches to a higher harmonic of the data rate the VCO is currently locked onto, the VCO loses lock, the LOL pin is asserted, and a new frequency acquisition is initiated. The ADN2865 automatically locks onto the new data rate.

The time to detect lock to harmonic is

$$16,384 \times (T_d/\rho)$$

where:

1/T<sub>d</sub> is the new data rate. For example, if the data rate is switched from OC-48 to OC-12, then T<sub>d</sub>= 1/622 MHz.

ρ is the data transition density. Most coding schemes seek to ensure that ρ = 0.5, for example, PRBS, 8B/10B.

When the ADN2865 is placed in lock to reference mode, the harmonic detector is disabled.

**LIMITING AMPLIFIER**

The limiting amplifier on the ADN2865 has differential inputs (PIN/NIN), which are internally terminated with 50 Ω to an on-chip voltage reference (VREF = 2.5 V typically). The inputs are typically ac-coupled externally, although dc coupling is possible as long as the input common mode voltage remains above 2.5 V (see Figure , Figure , and Figure in the Applications

Information section). Input offset is factory trimmed to achieve better than 6 mV typical sensitivity with minimal drift. The limiting amplifier can be driven differentially or single-ended.

### SLICE AND SAMPLE PHASE ADJUST (ADN2817 ONLY)

The quantizer slicing level can be offset by  $\pm 100$  mV to mitigate the effect of amplified spontaneous emission (ASE) noise or duty cycle distortion by applying a differential voltage input of up to  $\pm 0.95$  V to SLICEP/N inputs. If no adjustment of the slice level is needed, SLICEP/N should be tied to VEE. The gain of the slice adjustment is  $\sim 0.1$  V/V.

If the user is not using the BER monitoring function, sample phase adjustment can be utilized to optimize the horizontal sampling point of the incoming data eye. The ADN2865 automatically centers the sampling point to the best of its ability. However, sample phase adjustment could be used to compensate for any static phase offset of the CDR and duty cycle distortion of the incoming eye. Sample phase adjustment is applied to the incoming eye via the PHASE register. It is important to note that sample phase adjustment can not be used if the user is utilizing the BER monitoring capability. This is because the BER monitoring circuit requires control of the sample phase adjustment circuitry. Also, using the sample phase adjustment capability uses an additional 180mW of power.

### LOSS OF SIGNAL (LOS) DETECTOR

The receiver front end LOS detector circuit detects when the input signal level has fallen below a user-adjustable threshold. The threshold is set with a single external resistor from Pin 9, THRAdj, to VEE. The LOS comparator trip point-versus-resistor value is illustrated in Figure 2. If the input level to the ADN2865 drops below the programmed LOS threshold, the output of the LOS detector, LOS Pin 1, is asserted to a Logic 1. The LOS detector's response time is  $\sim 500$  ns by design, but is dominated by the RC time constant in ac-coupled applications. The LOS pin defaults to active high. However, by setting Bit CTRLC[2] to 1, the LOS pin is configured as active low.

There is typically 6 dB of electrical hysteresis designed into the LOS detector to prevent chatter on the LOS pin. This means that, if the input level drops below the programmed LOS threshold causing the LOS pin to assert, the LOS pin is not de-asserted until the input level has increased to 6 dB ( $2\times$ ) above the LOS threshold (see Figure ).

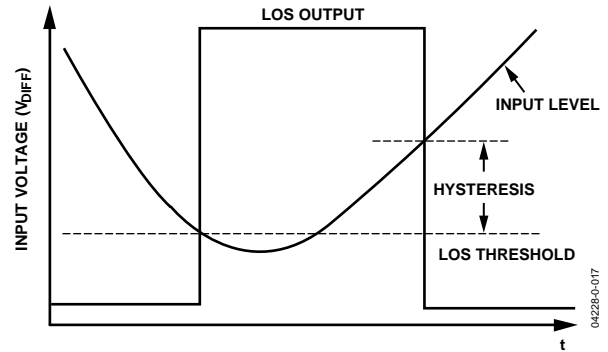


Figure 23. ADN2817 LOS Detector Hysteresis

The LOS detector and the SLICE level adjust can be used simultaneously on the ADN2865. This means that any offset added to the input signal by the SLICE adjust pins does not affect the LOS detector's measurement of the absolute input level.

### I<sup>2</sup>C INTERFACE

The ADN2865 supports a 2-wire, I<sup>2</sup>C compatible, serial bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCK), carry information between any devices connected to the bus. Each slave device is recognized by a unique address. The 7-bit slave address is factory programmed to binary '1100000'. The LSB of the word sets either a read or write operation (see Figure ). Logic 1 corresponds to a read operation, while Logic 0 corresponds to a write operation.

To control the device on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high to low transition on SDA while SCK remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address and the R/W bit). The bits are transferred from MSB to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCK lines waiting for the start condition and correct transmitted address. The R/W bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADN2865 acts as a standard slave device on the bus. The data on the SDA pin is 8 bits long supporting the 7-bit addresses plus the R/W bit. The ADN2865 has 8 subaddresses to enable the user-accessible internal registers (see Table 6 through Table 15). It, therefore, interprets the first byte as the device address and the second byte as the starting subaddress. Autoincrement mode is supported, allowing data to be read from or written to

the starting subaddress and each subsequent address without manually addressing the subsequent subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all registers.

Stop and start conditions can be detected at any stage of the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then they cause an immediate jump to the idle condition. During a given SCK high period, the user should issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADN2865 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while reading back in autoincrement mode, then the highest subaddress register contents continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. In a no-acknowledge condition, the SDATA line is not pulled low on the ninth pulse. See Figure and Figure for sample read and write data transfers and Figure 12 for a more detailed timing diagram.

**REFERENCE CLOCK (OPTIONAL)**

A reference clock is not required to perform clock and data recovery with the ADN2865. However, support for an optional reference clock is provided. The reference clock can be driven differentially or single-ended. If the reference clock is not being used, then REFCLKP should be tied to VCC, and REFCLKN can be left floating or tied to VEE (the inputs are internally terminated to VCC/2). See Figure through Figure for sample configurations.

The REFCLK input buffer accepts any differential signal with a peak-to-peak differential amplitude of greater than 100 mV (for example, LVPECL or LVDS) or a standard single-ended low voltage TTL input, providing maximum system flexibility. Phase noise and duty cycle of the reference clock are not critical and 100 ppm accuracy is sufficient.

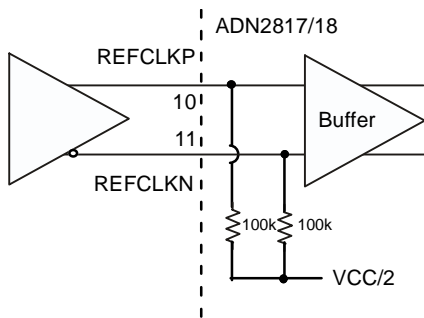


Figure 24. Differential REFCLK Configuration

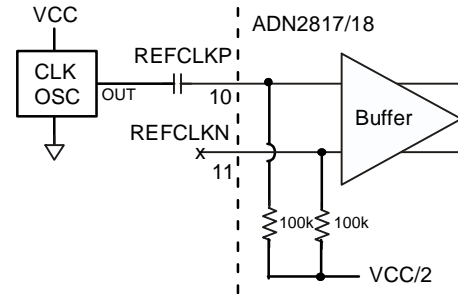


Figure 25. Single-Ended REFCLK Configuration

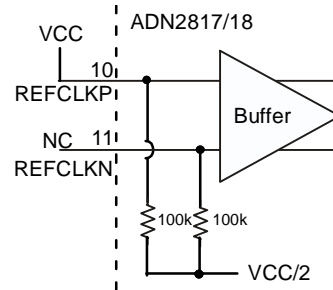


Figure 26. No REFCLK Configuration

The two uses of the reference clock are mutually exclusive. The reference clock can be used either as an acquisition aid for the ADN2865 to lock onto data, or to measure the frequency of the incoming data to within 0.01%. (There is the capability to measure the data rate to approximately ±10% without the use of a reference clock.) The modes are mutually exclusive, because, in the first use, the user knows exactly what the data rate is and wants to force the part to lock onto only that data rate; in the second use, the user does not know what the data rate is and wants to measure it.

Lock to reference mode is enabled by writing a 1 to I<sup>2</sup>C Register Bit CTRLA[0]. Fine data rate readback mode is enabled by writing a 1 to I<sup>2</sup>C Register Bit CTRLA[1]. Writing a 1 to both of these bits at the same time causes an indeterminate state and is not supported.

**Using the Reference Clock to Lock onto Data**

In this mode, the ADN2865 locks onto a frequency derived from the reference clock according to the following equation:

$$Data\ Rate/2^{CTRLA[5:2]} = REFCLK/2^{CTRLA[7:6]}$$

The user must know exactly what the data rate is, and provide a reference clock that is a function of this rate. The ADN2865 can still be used as a continuous rate device in this configuration, provided that the user has the ability to provide a reference clock that has a variable frequency (see Application Note AN-632).

The reference clock can be anywhere between 12.3 MHz and 200 MHz. By default, the ADN2865 expects a reference clock of between 12.3 MHz and 25 MHz. If it is between 25 MHz and

50 MHz, 50 MHz and 100 MHz, or 100 MHz and 200 MHz, the user needs to configure the ADN2865 to use the correct reference frequency range by setting two bits of the CTRLA register, CTRLA[7:6].

**Table 16. CTRLA Settings**

CTRLA[7:6]	Range (MHz)	CTRLA[5:2]	Ratio
00	12.3 to 25	0000	1
01	25 to 50	0001	2
10	50 to 100	n	2 <sup>n</sup>
11	100 to 200	1000	256

The user can specify a fixed integer multiple of the reference clock to lock onto using CTRLA[5:2], where CTRLA should be set to the data rate/DIV\_FREF, where DIV\_FREF represents the divided-down reference referred to the 12.3 MHz to 25 MHz band. For example, if the reference clock frequency was 38.88 MHz and the input data rate was 622.08 Mb/s, then CTRLA[7:6] would be set to [01] to give a divided-down reference clock of 19.44 MHz. CTRLA[5:2] would be set to [0101], that is, 5, because

$$622.08 \text{ Mb/s} / 19.44 \text{ MHz} = 2^5$$

In this mode, if the ADN2865 loses lock for any reason, it relocks onto the reference clock and continues to output a stable clock.

While the ADN2865 is operating in lock to reference mode, if the user ever changes the reference frequency, the FREF range (CTRLA[7:6]), or the FREF ratio (CTRLA[5:2]), this must be followed by writing a 0 to 1 transition into the CTRLA[0] bit to initiate a new lock to reference command.

**Using the Reference Clock to Measure Data Frequency**

The user can also provide a reference clock to measure the recovered data frequency. In this case, the user provides a reference clock, and the ADN2865 compares the frequency of the incoming data to the incoming reference clock and returns a ratio of the two frequencies to 0.01% (100 ppm). The accuracy error of the reference clock is added to the accuracy of the ADN2865 data rate measurement. For example, if a 100-ppm accuracy reference clock is used, the total accuracy of the measurement is within 200 ppm.

The reference clock can range from 12.3 MHz and 200 MHz. The ADN2865 expects a reference clock between 12.3 MHz and 25 MHz by default. If it is between 25 MHz and 50 MHz, 50 MHz and 100 MHz, or 100 MHz and 200 MHz, the user needs to configure the ADN2865 to use the correct reference frequency range by setting two bits of the CTRLA register, CTRLA[7:6]. Using the reference clock to determine the frequency of the incoming data does not affect the manner in which the part locks onto data. In this mode, the reference clock is used only to determine the frequency of the data. For this reason, the user does not need to know the data rate to use the reference clock in this manner.

Prior to reading back the data rate using the reference clock, the CTRLA[7:6] bits must be set to the appropriate frequency range with respect to the reference clock being used. A fine data rate readback is then executed as follows:

Step 1: Write a 1 to CTRLA[1]. This enables the fine data rate measurement capability of the ADN2865. This bit is level sensitive and does not need to be reset to perform subsequent frequency measurements.

Step 2: Reset MISC[2] by writing a 1 followed by a 0 to CTRLB[3]. This initiates a new data rate measurement.

Step 3: Read back MISC[2]. If it is 0, then the measurement is not complete. If it is 1, then the measurement is complete and the data rate can be read back on FREQ[22:0]. The time for a data rate measurement is typically 80 ms.

Step 4: Read back the data rate from registers FREQ2[6:0], FREQ1[7:0], and FREQ0[7:0].

Use the following equation to determine the data rate:

$$f_{\text{DATARATE}} = (FREQ[22..0] \times f_{\text{REFCLK}}) / 2^{(14+SEL\_RATE)}$$

where:

FREQ[22:0] is the reading from FREQ2[6:0] (MSByte), FREQ1[7:0], and FREQ0[7:0] (LSByte).

**Table 17.**

D22	D21...D17	D16	D15	D14...D9	D8	D7	D6...D1	D0
FREQ2[6:0]			FREQ1[7:0]			FREQ0[7:0]		

f<sub>DATARATE</sub> is the data rate (Mb/s).

f<sub>REFCLK</sub> is the REFCLK frequency (MHz).

SEL\_RATE is the setting from CTRLA[7:6].

For example, if the reference clock frequency is 32 MHz, SEL\_RATE = 1, since the CTRLA[7:6] setting would be [01], because the reference frequency would fall into the 25 MHz to 50 MHz range. Assume for this example that the input data rate is 2.488 Gb/s (OC-48). After following Steps 1 through 4, the value that is read back on FREQ[22:0] = 0x26E010, which is equal to 2.5477 × 10<sup>6</sup>. Plugging this value into the equation yields

$$(2.5477 \times 10^6 \times 32 \times 10^6) / (2^{(14+1)}) = 2.488 \text{ Gb/s}$$

If subsequent frequency measurements are required, CTRLA[1] should remain set to 1. It does not need to be reset. The measurement process is reset by writing a 1 followed by a 0 to CTRLB[3]. This initiates a new data rate measurement. Follow Steps 2 through 4 to read back the new data rate.

Note: A data rate readback is valid only if LOL is low. If LOL is high, the data rate readback is invalid.



### **Additional Features Available via the I<sup>2</sup>C Interface Coarse Data Rate Readback**

The data rate can be read back over the I<sup>2</sup>C interface to approximately  $\pm 10\%$  without the need of an external reference clock. A 9-bit register, COARSE\_RD[8:0], can be read back when LOL is de-asserted. The 8 MSBs of this register are the contents of the RATE[7:0] register. The LSB of the COARSE\_RD register is Bit MISC[0].

Table provides coarse data rate readback to within  $\pm 10\%$ .

### **LOS Configuration**

The LOS detector output, LOS Pin 22, can be configured to be either active high or active low. If CTRLC[2] is set to Logic 0 (default), the LOS pin is active high when a loss of signal condition is detected. Writing a 1 to CTRLC[2] configures the LOS pin to be active low when a loss of signal condition is detected.

### **System Reset**

A frequency acquisition can be initiated by writing a 1 followed by a 0 to the I<sup>2</sup>C Register Bit CTRLB[5]. This initiates a new frequency acquisition while keeping the ADN2865 in the operating mode that it was previously programmed to in registers CTRL[A], CTRL[B], and CTRL[C].

### **FDDI Mode**

A scheme has been implemented on the ADN2865 that enables the device to lock to input data streams that appear as subharmonics of the desired datarate, e.g. FDDI during link synchronization. This works for any code where a subharmonic down to the 31st is transmitted. FDDI uses the 5th subharmonic. The implementation requires certain programming by the user and more importantly certain assumptions about the incoming data.

The user is required to program the part into FDDI mode by setting bit FDDI\_MODE[7]=1. The user then needs to program the target datarate, (for FDDI this is 125MHz). This is done by programming an upper and lower 9-bit code into I2C registers HI\_CODE[8..0], LO\_CODE[8..0], and CODE\_LSB[1..0]. See Table XX for a look-up table showing the correct register settings for each datarate. The user must also program the subharmonic ratio into I2C register FDDI\_MODE[6..2] that the ADN2865 needs to lock on to, e.g. FDDI\_MODE[6..2] = 00101 for FDDI (5<sup>th</sup> subharmonic). The user has to de-program FDDI mode before the next datarate is applied.

Here is what is required of the incoming data:

1. The subharmonic must be a clock-type waveform i.e. transition density equal to 1 at the subharmonic frequency.
2. The subharmonic must be continued to be applied until LOL goes LOW, i.e. until acquisition is completed. It doesn't matter how long the subharmonic remains after LOL goes LOW.

In FDDI Mode, the output of the ADN2865 is squelched until the device has acquired lock of the subharmonic input. This causes all zeros to be transmitted out of the 2865 until lock has been achieved. Once locked, the outputs are enabled and begin transmitting data. For FDDI protocol, this would be when the 'H' symbols are being transmitted during link synchronization.

### **CLK HOLDOVER MODE**

#### **CLK Holdover Mode 2A:**

This mode of operation will be available in all LTD modes: The output clock frequency will remain within  $\pm 5\%$  if the input data is removed or changed. To operate in this mode, the user would write to the I2C to put the part into CLK Holdover Mode 2A mode by setting SEL\_MODE[2]=1. The user must then initiate an acquisition via a software reset. The device will then lock onto the input datarate. At this point the output frequency remains within  $\pm 5\%$  of the initial acquired value regardless of whether or not the input data is taken away or the datarate changes. Only a sw reset can initiate a new acquisition in this mode.

#### **CLK Holdover Mode 2B:**

This mode is selected by setting SEL\_MODE[1]=1. In this mode, the output clock stays within  $\pm 5\%$  of the initial acquired frequency, even if the input data is taken away. Unlike CLK Holdover Mode 2A, in this mode the ADN2865 will initiate a new frequency acquisition automatically if the input datarate changes. This mode requires the inputs to be DC coupled because if the inputs are AC coupled and the input is taken away, any noise present on the inputs may be large enough to trigger a new frequency acquisition which would cause the clock output frequency to change.

### **CDR BYPASS MODE**

The CDR on the ADN2865 can be bypassed by setting bit CTRLD[7]=1. In this mode the ADN2865 will feed the input directly through the input amplifiers to the output buffer, completely bypassing the CDR.

### **DISABLE OUTPUT BUFFERS**

The ADN2865 provides the option of disabling the output buffers for power savings. The LVDS output buffers can be disabled by setting CTRLD[6]=1. For additional power savings, e.g. in a low power standby mode, the CML output buffers can also be disabled by setting CTRLD[5]=1.

# APPLICATIONS INFORMATION

## PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used for optimal performance.

### Power Supply Connections and Ground Planes

Use of one low impedance ground plane is recommended. The VEE pins should be soldered directly to the ground plane to reduce series inductance. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias can be used in parallel to reduce the series inductance. The exposed pad should be connected to the GND plane using plugged vias so that solder does not leak through the vias during reflow.

Use of a 10  $\mu\text{F}$  electrolytic capacitor between VCC and VEE is recommended at the location where the 3.3 V supply enters the PCB. When using 0.1  $\mu\text{F}$  and 1 nF ceramic chip capacitors, they should be placed between the IC power supply VCC and VEE, as close as possible to the ADN2865 VCC pins.

If connections to the supply and ground are made through vias, the use of multiple vias in parallel helps to reduce series inductance, especially on Pins 7,45 & 50, which supplies power to the high speed LVDS & CML output buffers. Refer to the schematic in Figure for recommended connections.

By using adjacent power supply and GND planes, excellent high frequency decoupling can be realized by using close spacing between the planes. This capacitance is given by

$$C_{plane} = 0.88\epsilon_r A/d \text{ (pF)}$$

where:

- $\epsilon_r$  is the dielectric constant of the PCB material.
- $A$  is the area of the overlap of power and GND planes ( $\text{cm}^2$ ).
- $d$  is the separation between planes (mm).

For FR-4,  $\epsilon_r = 4.4$  mm and 0.25 mm spacing,  $C \sim 15$  pF/

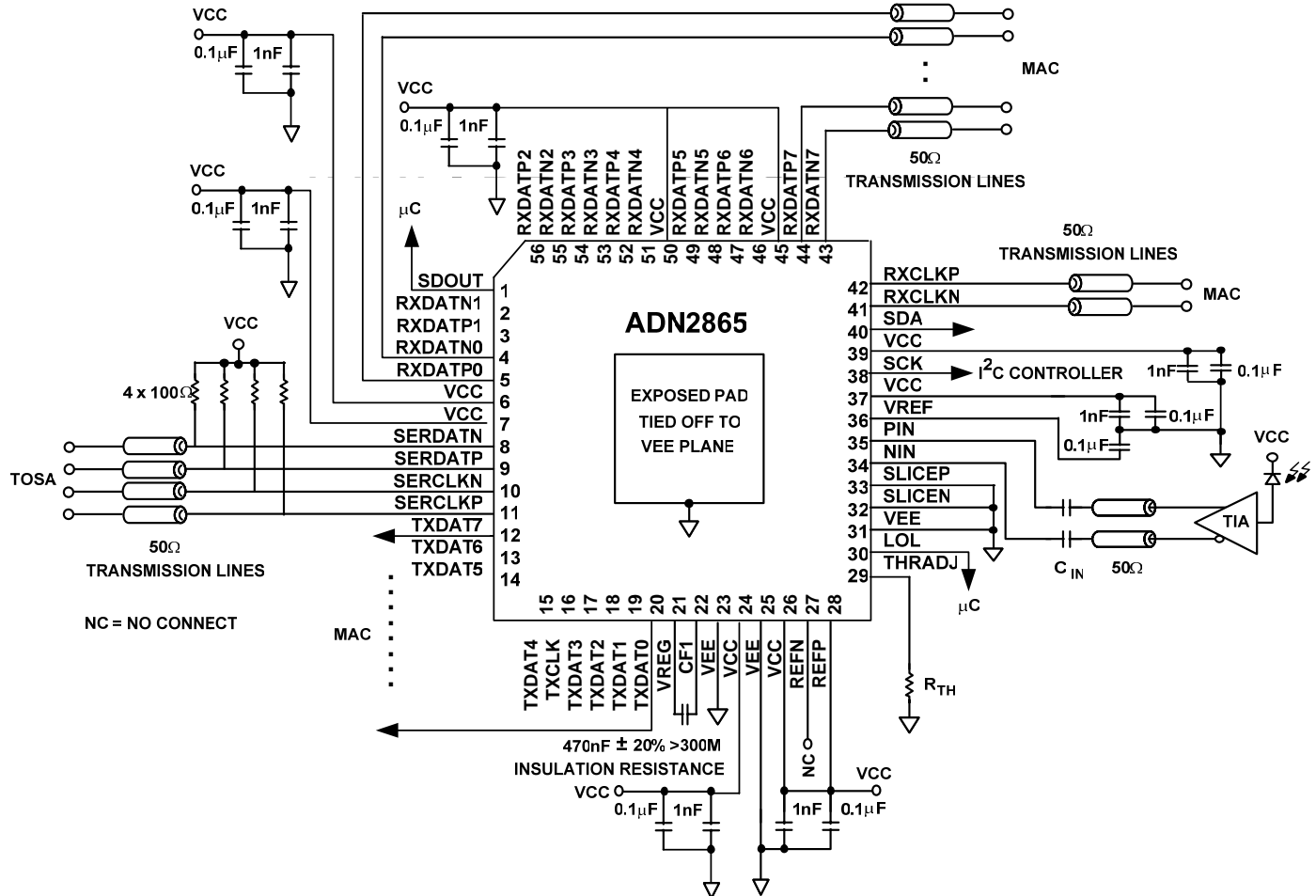


Figure 27. Typical ADN2865 Applications Circuit

**Transmission Lines**

Use of 50 Ω transmission lines is required for all LVDS and CML input and output signals to minimize reflections: PIN, NIN, RXDATAP/N[7:0], RXCLKP/N, SERDATP, SERDATN, SERCLKP, SERCLKN (also REFCLKP, REFCLKN, if a high frequency reference clock is used, such as 155 MHz). It is also necessary for the PIN/NIN input traces to be matched in length, and the parallel bus / CML output traces to be matched in length to avoid skew between the differential traces. All high speed CML outputs, SERDATP, SERDATN, SERCLKP, SERCLKN also require 100 Ω back termination chip resistors connected between the output pin and VCC. These resistors should be placed as close as possible to the output pins. These 100 Ω resistors are in parallel with on-chip 100 Ω termination resistors to create a 50 Ω back termination (see Figure ).

The high speed inputs, PIN and NIN, are internally terminated with 50 Ω to an internal reference voltage (see Figure ). A 0.1 μF is recommended between VREF, Pin 36, and GND to provide an ac ground for the inputs.

As with any high speed mixed-signal design, take care to keep all high speed digital traces away from sensitive analog nodes.

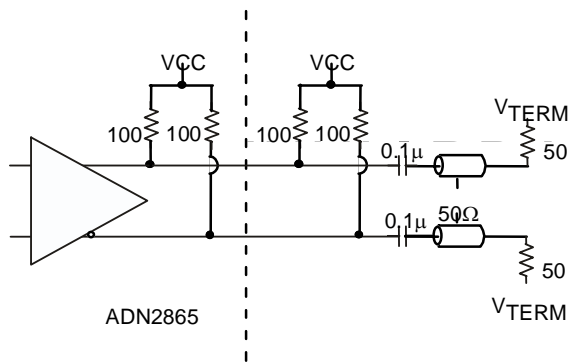


Figure 28. Typical ADN2865 Applications Circuit

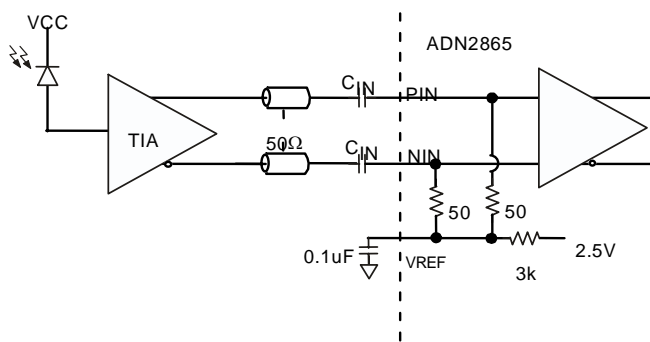


Figure 29. ADN2865 AC-Coupled Input Configuration

**Soldering Guidelines for Chip Scale Package**

The lands on the 56 LFCSP are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale

package has a central exposed pad. The pad on the printed circuit board should be at least as large as this exposed pad. The user must connect the exposed pad to VEE using plugged vias so that solder does not leak through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

**Choosing AC Coupling Capacitors**

AC coupling capacitors at the input (PIN, NIN) and output (SERDATP, SERDATN) of the ADN2865 must be chosen such that the device works properly over the full range of data rates used in the application. When choosing the capacitors, the time constant formed with the two 50 Ω resistors in the signal path must be considered. When a large number of consecutive identical digits (CIDs) are applied, the capacitor voltage can droop due to baseline wander (see Figure ), causing pattern-dependent jitter (PDJ).

The user must determine how much droop is tolerable and choose an ac coupling capacitor based on that amount of droop. The amount of PDJ can then be approximated based on the capacitor selection. The actual capacitor value selection may require some trade-offs between droop and PDJ.

Example: Assuming that 2% droop can be tolerated, then the maximum differential droop is 4%. Normalizing to V<sub>pp</sub>:

$$Droop = \Delta V = 0.04 V = 0.5 V_{pp} (1 - e^{-t/\tau}); \text{ therefore, } \tau = 12t$$

where:

τ is the RC time constant (C is the ac coupling capacitor, R = 100 Ω seen by C).

t is the total discharge time, which is equal to nT.

n is the number of CIDs.

T is the bit period.

The capacitor value can then be calculated by combining the equations for τ and t:

$$C = 12nT/R$$

Once the capacitor value is selected, the PDJ can be approximated as

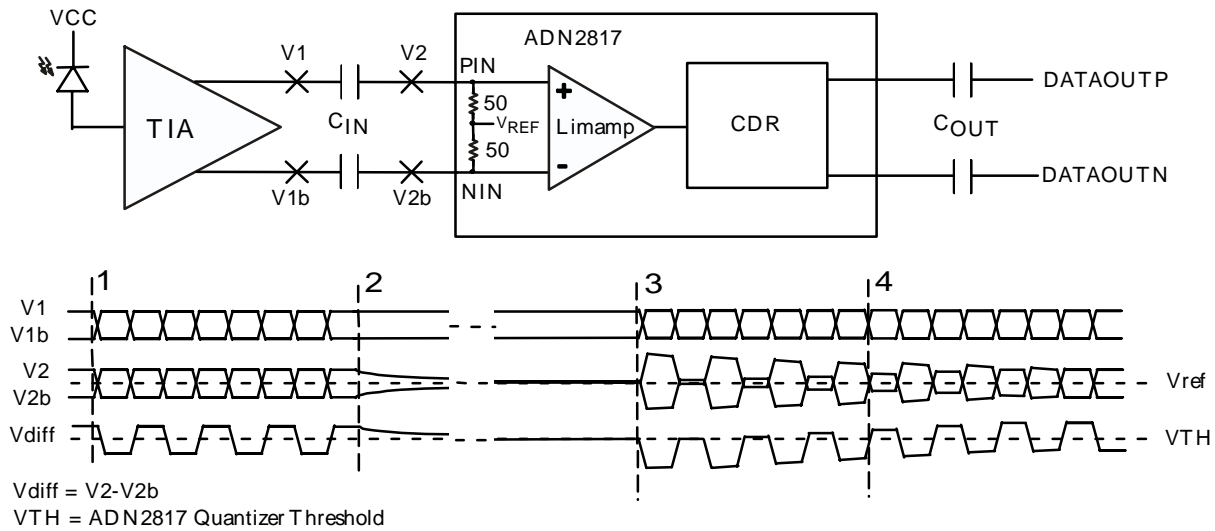
$$PDJ_{pspp} = 0.5t_r (1 - e^{(-nT/RC)}) / 0.6$$

where:

PDJ<sub>pspp</sub> is the amount of pattern-dependent jitter allowed; < 0.01 UI p-p typical.

t<sub>r</sub> is the rise time, which is equal to 0.22/BW, where BW ~ 0.7 (bit rate).

Note that this expression for t<sub>r</sub> is accurate only for the inputs. The output rise time for the ADN2865 is ~100 ps regardless of data rate.



NOTES:

1. During data patterns with high transition density, differential DC voltage at V1 and V2 is zero.
2. When the output of the TIA goes to CID, V1 and V1b are driven to different DC levels. V2 and V2b discharge to the Vref level which effectively introduces a differential DC offset across the AC coupling capacitors.
3. When the burst of data starts again, the differential DC offset across the AC coupling capacitors is applied to the input levels causing a DC shift in the differential input. This shift is large enough such that one of the states, either HI or LO depending on the levels of V1 and V1b when the TIA went to CID, is cancelled out. The quantizer will not recognize this as a valid state.
4. The DC offset slowly discharges until the differential input voltage exceeds the sensitivity of the ADN2817. The quantizer will be able to recognize both HI and LO states at this point.

Figure 30. Example of Baseline Wander

**DC-COUPLED APPLICATION**

The inputs to the ADN2865 can also be dc-coupled. This might be necessary in burst mode applications, where there are long periods of CIDs, and baseline wander cannot be tolerated. If the inputs to the ADN2865 are dc-coupled, care must be taken not to violate the input range and common-mode level requirements of the ADN2865 (see Figure through Figure ). If dc coupling is required, and the output levels of the TIA do not adhere to the levels shown in Figure , then level shifting and/or an attenuator must be between the TIA outputs and the ADN2865 inputs.

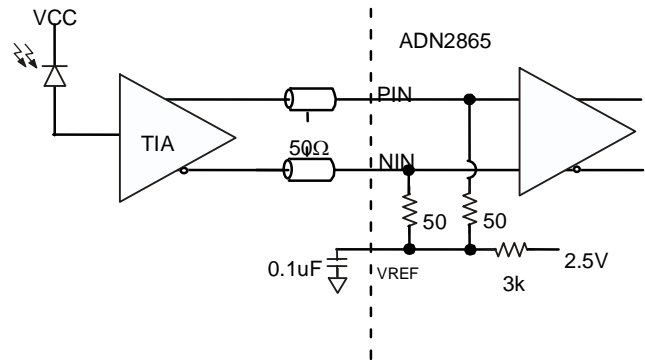


Figure 31. DC-Coupled Application

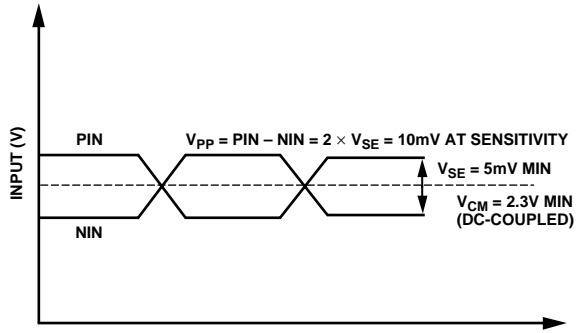


Figure 32. Minimum Allowed DC-Coupled Input Levels

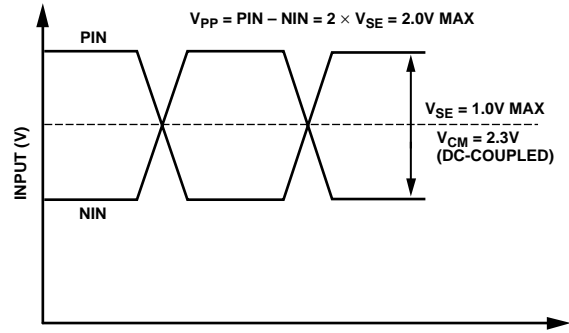


Figure 33. Maximum Allowed DC-Coupled Input Levels

## COARSE DATA RATE READBACK LOOK-UP TABLE

Code is the 9-bit value read back from COARSE\_RD[8:0].

Table 18. Look-Up Table

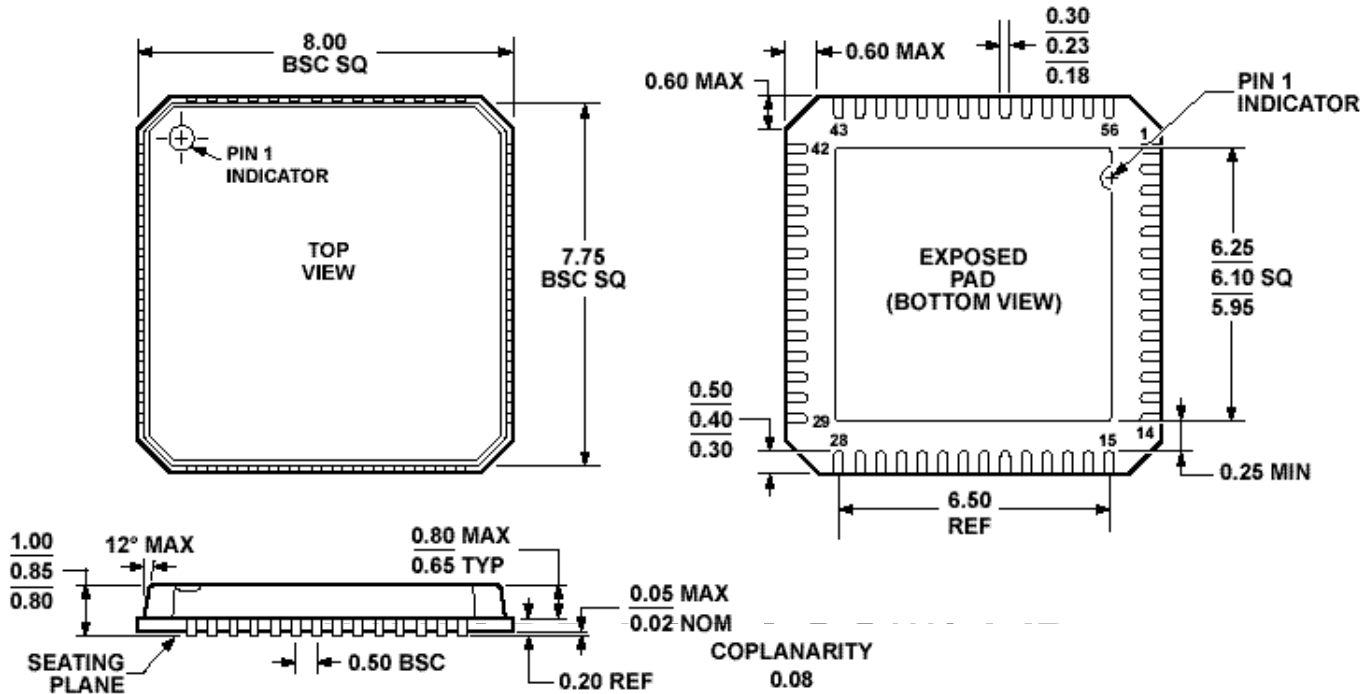
Code	F <sub>MID</sub>	Code	F <sub>MID</sub>	Code	F <sub>MID</sub>	Code	F <sub>MID</sub>
0	5.1934e+06	48	1.4828e+07	96	4.1547e+07	144	1.1862e+08
1	5.1930e+06	49	1.4827e+07	97	4.1544e+07	145	1.1862e+08
2	5.2930e+06	50	1.5121e+07	98	4.2344e+07	146	1.2097e+08
3	5.3989e+06	51	1.5435e+07	99	4.3191e+07	147	1.2348e+08
4	5.5124e+06	52	1.5770e+07	100	4.4099e+07	148	1.2616e+08
5	5.6325e+06	53	1.6127e+07	101	4.5060e+07	149	1.2901e+08
6	5.7612e+06	54	1.6510e+07	102	4.6090e+07	150	1.3208e+08
7	5.8995e+06	55	1.6917e+07	103	4.7196e+07	151	1.3534e+08
8	6.0473e+06	56	1.7357e+07	104	4.8378e+07	152	1.3885e+08
9	6.2097e+06	57	1.7836e+07	105	4.9678e+07	153	1.4269e+08
10	6.3819e+06	58	1.8347e+07	106	5.1055e+07	154	1.4678e+08
11	6.5675e+06	59	1.8896e+07	107	5.2540e+07	155	1.5117e+08
12	6.7688e+06	60	1.9493e+07	108	5.4150e+07	156	1.5594e+08
13	6.9874e+06	61	2.0136e+07	109	5.5899e+07	157	1.6109e+08
14	7.2262e+06	62	2.0833e+07	110	5.7810e+07	158	1.6667e+08
15	7.4863e+06	63	2.1582e+07	111	5.9890e+07	159	1.7266e+08
16	7.4139e+06	64	2.0774e+07	112	5.9311e+07	160	1.6619e+08
17	7.4135e+06	65	2.0772e+07	113	5.9308e+07	161	1.6617e+08
18	7.5606e+06	66	2.1172e+07	114	6.0485e+07	162	1.6938e+08
19	7.7173e+06	67	2.1596e+07	115	6.1739e+07	163	1.7277e+08
20	7.8852e+06	68	2.2049e+07	116	6.3081e+07	164	1.7640e+08
21	8.0633e+06	69	2.2530e+07	117	6.4506e+07	165	1.8024e+08
22	8.2548e+06	70	2.3045e+07	118	6.6038e+07	166	1.8436e+08
23	8.4586e+06	71	2.3598e+07	119	6.7669e+07	167	1.8878e+08
24	8.6784e+06	72	2.4189e+07	120	6.9427e+07	168	1.9351e+08
25	8.9180e+06	73	2.4839e+07	121	7.1344e+07	169	1.9871e+08
26	9.1736e+06	74	2.5527e+07	122	7.3388e+07	170	2.0422e+08
27	9.4481e+06	75	2.6270e+07	123	7.5585e+07	171	2.1016e+08
28	9.7464e+06	76	2.7075e+07	124	7.7971e+07	172	2.1660e+08
29	1.0068e+07	77	2.7950e+07	125	8.0546e+07	173	2.2360e+08
30	1.0417e+07	78	2.8905e+07	126	8.3333e+07	174	2.3124e+08
31	1.0791e+07	79	2.9945e+07	127	8.6328e+07	175	2.3956e+08
32	1.0387e+07	80	2.9655e+07	128	8.3095e+07	176	2.3724e+08
33	1.0386e+07	81	2.9654e+07	129	8.3087e+07	177	2.3723e+08
34	1.0586e+07	82	3.0242e+07	130	8.4689e+07	178	2.4194e+08
35	1.0798e+07	83	3.0869e+07	131	8.6383e+07	179	2.4695e+08
36	1.1025e+07	84	3.1541e+07	132	8.8198e+07	180	2.5233e+08
37	1.1265e+07	85	3.2253e+07	133	9.0120e+07	181	2.5802e+08
38	1.1522e+07	86	3.3019e+07	134	9.2179e+07	182	2.6415e+08
39	1.1799e+07	87	3.3834e+07	135	9.4392e+07	183	2.7067e+08
40	1.2095e+07	88	3.4714e+07	136	9.6757e+07	184	2.7771e+08
41	1.2419e+07	89	3.5672e+07	137	9.9356e+07	185	2.8538e+08
42	1.2764e+07	90	3.6694e+07	138	1.0211e+08	186	2.9355e+08
43	1.3135e+07	91	3.7792e+07	139	1.0508e+08	187	3.0234e+08
44	1.3538e+07	92	3.8985e+07	140	1.0830e+08	188	3.1188e+08
45	1.3975e+07	93	4.0273e+07	141	1.1180e+08	189	3.2218e+08
46	1.4452e+07	94	4.1666e+07	142	1.1562e+08	190	3.3333e+08
47	1.4973e+07	95	4.3164e+07	143	1.1978e+08	191	3.4531e+08

Code	F <sub>MID</sub>	Code	F <sub>MID</sub>	Code	F <sub>MID</sub>	Code	F <sub>MID</sub>
192	3.3238e+08	216	5.5542e+08	240	9.4898e+08	264	1.5481e+09
193	3.3235e+08	217	5.7075e+08	241	9.4893e+08	265	1.5897e+09
194	3.3876e+08	218	5.8711e+08	242	9.6776e+08	266	1.6338e+09
195	3.4553e+08	219	6.0468e+08	243	9.8782e+08	267	1.6813e+09
196	3.5279e+08	220	6.2377e+08	244	1.0093e+09	268	1.7328e+09
197	3.6048e+08	221	6.4437e+08	245	1.0321e+09	269	1.7888e+09
198	3.6872e+08	222	6.6666e+08	246	1.0566e+09	270	1.8499e+09
199	3.7757e+08	223	6.9062e+08	247	1.0827e+09	271	1.9165e+09
200	3.8703e+08	224	6.6476e+08	248	1.1108e+09	272	1.8980e+09
201	3.9742e+08	225	6.6470e+08	249	1.1415e+09	273	1.8979e+09
202	4.0844e+08	226	6.7751e+08	250	1.1742e+09	274	1.9355e+09
203	4.2032e+08	227	6.9106e+08	251	1.2094e+09	275	1.9756e+09
204	4.3320e+08	228	7.0558e+08	252	1.2475e+09	276	2.0186e+09
205	4.4719e+08	229	7.2096e+08	253	1.2887e+09	277	2.0642e+09
206	4.6248e+08	230	7.3743e+08	254	1.3333e+09	278	2.1132e+09
207	4.7912e+08	231	7.5514e+08	255	1.3812e+09	279	2.1654e+09
208	4.7449e+08	232	7.7405e+08	256	1.3295e+09	280	2.2217e+09
209	4.7447e+08	233	7.9485e+08	257	1.3294e+09	281	2.2830e+09
210	4.8388e+08	234	8.1688e+08	258	1.3550e+09	282	2.3484e+09
211	4.9391e+08	235	8.4064e+08	259	1.3821e+09	283	2.4187e+09
212	5.0465e+08	236	8.6640e+08	260	1.4112e+09	284	2.4951e+09
213	5.1605e+08	237	8.9438e+08	261	1.4419e+09	285	2.5775e+09
214	5.2831e+08	238	9.2496e+08	262	1.4749e+09	286	2.6666e+09
215	5.4135e+08	239	9.5825e+08	263	1.5103e+09	287	2.7625e+09

OUTLINE DIMENSIONS



56-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
 8 x 8 mm Body, Very Thin Quad  
 (CP-56)  
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VLLD-2

Figure 34. 56-Lead Frame Chip Scale Package [LFCSP]  
 (CP-56)  
 Dimensions shown in millimeters

112805-0

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADN2865ACP	-40°C to 85°C	56-LFCSP	CP-56
ADN2865ACP-RL	-40°C to 85°C	56-LFCSP, tape-reel, 2500 pcs	CP-56
ADN2865ACP-RL7	-40°C to 85°C	56-LFCSP, tape-reel, 1500 pcs	CP-56



**NOTES**

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