![ANALOG DEVICES]

SHARC Processors

ADSP-21367/ADSP-21368/ADSP-21369

SUMMARY

High performance 32-bit/40-bit floating-point processor optimized for high performance audio processing

Single-instruction, multiple-data (SIMD) computational architecture

On-chip memory—2M bits of on-chip SRAM and 6M bits of on-chip mask programmable ROM

Code compatible with all other members of the SHARC family

The ADSP-21367/ADSP-21368/ADSP-21369 are available with a 400 MHz core instruction rate with unique audiocentric peripherals such as the digital applications interface, S/PDIF transceiver, serial ports, 8-channel asynchronous sample rate converter, precision clock generators, and more. For complete ordering information, see Ordering Guide on Page 55.

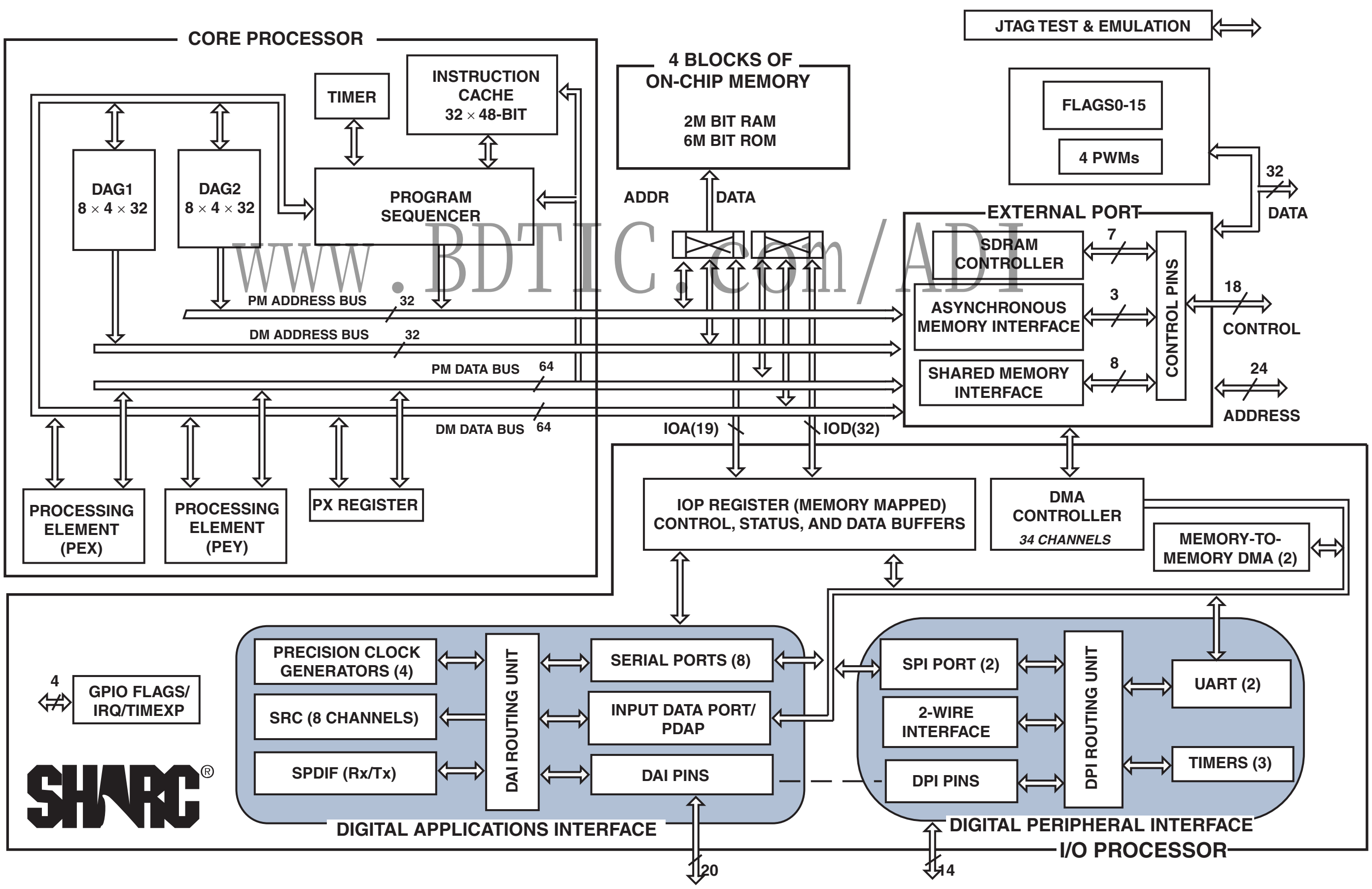

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Figure 1. Functional Block Diagram

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Rev. D

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KEY FEATURES—PROCESSOR CORE

At 400 MHz (2.5 ns) core instruction rate, the processors perform 2.4 GFLOPS/800 MMACS

2M bit on-chip SRAM (0.75M bit in blocks 0 and 1, and 0.25M bit in blocks 2 and 3) for simultaneous access by the core processor and DMA

6M bit on-chip, mask-programmable ROM (3M bit in block 0 and 3M bit in block 1)

Dual data address generators (DAGs) with modulo and bit-reverse addressing

Zero-overhead looping with single-cycle loop setup, providing efficient program sequencing

Single-instruction, multiple-data (SIMD) architecture provides
- Two computational processing elements
- Concurrent execution
- Code compatibility with other SHARC family members at the assembly level
- Parallelism in buses and computational units allows: single-cycle executions (with or without SIMD) of a multiply operation, an ALU operation, a dual memory read or write, and an instruction fetch

Transfers between memory and core at a sustained 6.4 Gbps bandwidth at 400 MHz core instruction rate

INPUT/OUTPUT FEATURES

DMA controller supports
- 34 zero-overhead DMA channels for transfers between internal memory and a variety of peripherals
- 32-bit DMA transfers at peripheral clock speed, in parallel with full-speed processor execution
- 32-bit wide external port provides glueless connection to both synchronous (SDRAM) and asynchronous memory devices
- Programmable wait state options: 2 SCLK to 31 SCLK cycles
- Delay-line DMA engine maintains circular buffers in external memory with tap-/offset-based reads
- SDRAM accesses at 166 MHz and asynchronous accesses at 55 MHz
- Shared-memory support (ADSP-21368 only) allows multiple DSPs to automatically arbitrate for the bus and gluelessly access a common memory device
- Shared memory interface (ADSP-21368 only) support provides Glueless connection for scalable DSP multiprocessing architecture
- Distributed on-chip bus arbitration for parallel bus Connect of up to four ADSP-21368 processors and global memory
- Four memory select lines allow multiple external memory devices

Digital applications interface (DAI) includes eight serial ports, four precision clock generators, an input data port, an S/PDIF transceiver, an 8-channel asynchronous sample rate converter, and a signal routing unit

Digital peripheral interface (DPI) includes three timers, two UARTs, two SPI ports, and a 2-wire interface port

Outputs of PCGs C and D can be driven on to DPI pins

8 dual data line serial ports that operate at up to 50 Mbps on each data line—each has a clock, frame sync, and two data lines that can be configured as either a receiver or transmitter pair

TDM support for telecommunications interfaces including 128 TDM channel support for newer telephony interfaces such as H.100/H.110

Up to 16 TDM stream support, each with 128 channels per frame

Companding selection on a per channel basis in TDM mode

Input data port, configurable as eight channels of serial data or seven channels of serial data and up to a 20-bit wide parallel data channel

Signal routing unit provides configurable and flexible connections between all DAI/DPI components

2 muxed flag/$\overline{\text{IRQ}}$ lines

1 muxed flag/timer expired line /$\overline{\text{MS}}$ pin

1 muxed flag/$\overline{\text{IRQ}}$ /$\overline{\text{MS}}$ pin

DEDICATED AUDIO COMPONENTS

S/PDIF-compatible digital audio receiver/transmitter supports EIAJ CP-340 (CP-1201), IEC-958, AES/EBU standards, left-justified, I²S, or right-justified serial data input with 16-, 18-, 20- or 24-bit word widths (transmitter)

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4 independent asynchronous sample rate converters (SRC). Each converter has separate serial input and output ports, a de-emphasis filter providing up to –140 dB SNR performance, stereo sample rate converter, and supports left-justified, I²S, TDM, and right-justified modes and 24-, 20-, 18-, and 16-audio data word lengths

Pulse-width modulation provides
- 16 PWM outputs configured as four groups of four outputs supports center-aligned or edge-aligned PWM waveforms

ROM-based security features include
- JTAG access to memory permitted with a 64-bit key
- Protected memory regions that can be assigned to limit access under program control to sensitive code

PLL has a wide variety of software and hardware multiplier/divider ratios

Dual voltage: 3.3 V I/O, 1.2 V or 1.3 V core

Available in 256-ball BGA_ED and 208-lead LQFP_EP packages (see Ordering Guide on Page 55)

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REVISION HISTORY

11/08—Rev. C to Rev. D

Corrected all outstanding document errata.

Changed digital audio interface to digital applications interface throughout this document. This change is a naming convention change only and does not effect the operation or specification of this product in any way.

Corrected Functional Block Diagram 1

Revised specification in Clock Input ... 20

Revised t_{DDTE}, t_{SCLK}, t_{SCLKW} specifications in Serial Ports ... 32

Revised t_{IDPCLK}, $t_{IDPCLKW}$ specifications in Input Data Port ... 36

Revised t_{PDCLK}, t_{PDCLKW} specifications in Parallel Data Acquisition Port (PDAP) ... 37

Revised t_{SRCCLK}, $t_{SRCCLKW}$ specifications in Sample Rate Converter—Serial Input Port ... 38
Sample Rate Converter—Serial Input Port ... 38

Added 350 MHz models. See Operating Conditions on Page 16, Clock Input on Page 20, SDRAM Interface Timing (166 MHz SDCLK) on Page 26, and Ordering Guide ... 55

Added Automotive Products ... 55

GENERAL DESCRIPTION

The ADSP-21367/ADSP-21368/ADSP-21369 SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. These processors are source code-compatible with the ADSP-2126x and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The processors are 32-bit/40-bit floating-point processors optimized for high performance automotive audio applications with its large on-chip SRAM, mask programmable ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

As shown in the functional block diagram on Page 1, the processors use two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-21367/ADSP-21368/ADSP-21369 processors achieve an instruction cycle time of up to 2.5 ns at 400 MHz. With its SIMD computational hardware, the processors can perform 2.4 GFLOPS running at 400 MHz.

Table 1 shows performance benchmarks for these devices.

Table 1. Processor Benchmarks (at 400 MHz)

Benchmark Algorithm	Speed (at 400 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	23.2 µs
FIR Filter (per tap)[1]	1.25 ns
IIR Filter (per biquad)[1]	5.0 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	11.25 ns
[4×4] × [4×1]	20.0 ns
Divide (y/x)	8.75 ns
Inverse Square Root	13.5 ns

[1] Assumes two files in multichannel SIMD mode.

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The ADSP-21367/ADSP-21368/ADSP-21369 processors continue SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features.

The block diagram of the ADSP-21368 on Page 1 illustrates the following architectural features:

- Two processing elements, each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Three programmable interval timers with PWM generation, PWM capture/pulse width measurement, and external event counter capabilities
- On-chip SRAM (2M bit)
- On-chip mask-programmable ROM (6M bit)
- JTAG test access port

The block diagram of the ADSP-21368 on Page 1 also illustrates the following architectural features:

- DMA controller
- Eight full-duplex serial ports
- Digital applications interface that includes four precision clock generators (PCG), an input data port (IDP), an S/PDIF receiver/transmitter, eight channels asynchronous sample rate converters, eight serial ports, a 16-bit parallel input port (PDAP), a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes three timers, a 2-wire interface, two UARTs, two serial peripheral interfaces (SPI), and a flexible signal routing unit (DPI SRU).

SHARC FAMILY CORE ARCHITECTURE

The ADSP-21367/ADSP-21368/ADSP-21369 are code compatible at the assembly level with the ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-21367/ADSP-21368/ADSP-21369 processors share architectural features with the ADSP-2126x and ADSP-2116x SIMD SHARC processors, as detailed in the following sections.

SIMD Computational Engine

The processors contain two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel

ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2136x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-21367/ADSP-21368/ADSP-21369 feature an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1 on Page 1). With separate program and data memory buses and on-chip instruction cache, the processors can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The processors include an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The ADSP-21367/ADSP-21368/ADSP-21369 have two data address generators (DAGs). The DAGs are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the ADSP-21367/ADSP-21368/ADSP-21369 can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

MEMORY ARCHITECTURE

The ADSP-21367/ADSP-21368/ADSP-21369 processors add the following architectural features to the SIMD SHARC family core.

On-Chip Memory

The processors contain two megabits of internal RAM and six megabits of internal mask-programmable ROM. Each block can be configured for different combinations of code and data storage (see Table 2 on Page 6). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the I/O processor, in a single cycle.

The SRAM can be configured as a maximum of 64k words of 32-bit data, 128k words of 16-bit data, 42k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to two megabits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

EXTERNAL MEMORY

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The 32-bit wide bus can be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices and DIMMs (dual inline memory module), while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non-SDRAM external memory address space is shown in Table 3.

SDRAM Controller

The SDRAM controller provides an interface of up to four separate banks of industry-standard SDRAM devices or DIMMs, at speeds up to f_{SCLK}. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 16M bytes and 128M bytes of memory. SDRAM external memory address space is shown in Table 4.

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Table 2. Internal Memory Space [1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 BFFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0008 0000–0x0009 7FFF	Block 0 ROM (Reserved) 0x0010 0000–0x0012 FFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 FFFF	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
Block 0 SRAM 0x0004 C000–0x0004 EFFF	Block 0 SRAM 0x0009 0000–0x0009 3FFF	Block 0 SRAM 0x0009 8000–0x0009 DFFF	Block 0 SRAM 0x0013 0000–0x0013 BFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 BFFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x000A 0000–0x000B 7FFF	Block 1 ROM (Reserved) 0x0014 0000–0x0016 FFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
Block 1 SRAM 0x0005 C000–0x0005 EFFF	Block 1 SRAM 0x000B 0000–0x000B 3FFF	Block 1 SRAM 0x000B 8000–0x000B DFFF	Block 1 SRAM 0x0017 0000–0x0017 BFFF
Block 2 SRAM 0x0006 0000–0x0006 0FFF	Block 2 SRAM 0x000C 0000–0x000C 1554	Block 2 SRAM 0x000C 0000–0x000C 1FFF	Block 2 SRAM 0x0018 0000–0x0018 3FFF
Reserved 0x0006 1000– 0x0006 FFFF	Reserved 0x000C 1555–0x000C 3FFF	Reserved 0x000C 2000–0x000D FFFF	Reserved 0x0018 4000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 0FFF	Block 3 SRAM 0x000E 0000–0x000E 1554	Block 3 SRAM 0x000E 0000–0x000E 1FFF	Block 3 SRAM 0x001C 0000–0x001C 3FFF
Reserved 0x0007 1000–0x0007 FFFF	Reserved 0x000E 1555–0x000F FFFF	Reserved 0x000E 2000–0x000F FFFF	Reserved 0x001C 4000–0x001F FFFF

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[1] The ADSP-21368 and ADSP-21369 processors include a customer-definable ROM block. Please contact your Analog Devices sales representative for additional details.

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. The memory banks can be configured as either 32 bits wide for maximum performance and bandwidth or 16 bits wide for minimum device count and lower system cost.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF loads. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Table 3. External Memory for Non-SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	14M	0x0020 0000–0x00FF FFFF
Bank 1	16M	0x0400 0000–0x04FF FFFF
Bank 2	16M	0x0800 0000–0x08FF FFFF
Bank 3	16M	0x0C00 0000–0x0CFF FFFF

Table 4. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

Asynchronous Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, ROM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 14M word window and Banks 1, 2, and 3 occupy a 16M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic. The banks can also be configured as 8-bit, 16-bit, or 32-bit wide buses for ease of interfacing to a range of memories and I/O devices tailored either to high performance or to low cost and power.

The asynchronous memory controller is capable of a maximum throughput of 220 Mbps using a 55 MHz external bus speed. Other features include 8-bit to 32-bit and 16-bit to 32-bit packing and unpacking, booting from Bank Select 1, and support for delay line DMA.

Shared External Memory

The ADSP-21368 processor supports connecting to common shared external memory with other ADSP-21368 processors to create shared external bus processor systems. This support includes:

- Distributed, on-chip arbitration for the shared external bus
- Fixed and rotating priority bus arbitration
- Bus time-out logic
- Bus lock

Multiple processors can share the external bus with no additional arbitration logic. Arbitration logic is included on-chip to allow the connection of up to four processors.

Bus arbitration is accomplished through the $\overline{\text{BR1-4}}$ signals and the priority scheme for bus arbitration is determined by the setting of the RPBA pin. Table 5 on Page 12 provides descriptions of the pins used in multiprocessor systems.

I/O PROCESSOR FEATURES

The I/O processor provides 34 channels of DMA, as well as an extensive set of peripherals. These include a 20-pin digital applications interface which controls:

- Eight serial ports
- S/PDIF receiver/transmitter
- Four precision clock generators
- Four stereo sample rate converters
- Input data port/parallel data acquisition port

The processors also contain a 14-pin digital peripheral interface which controls:

- Three general-purpose timers
- Two serial peripheral interfaces
- Two universal asynchronous receiver/transmitters (UARTs)
- A 2-wire interface (TWI, I^{2}C-compatible)

DMA Controller

The processor's on-chip DMA controller allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP), or the UART. Thirty-four channels of DMA are available on the processors—16 via the serial ports, eight via the input data port, four for the UARTs, two for the SPI interface, two for the external port, and two for memory-to-memory transfers. Programs can be downloaded to the processors using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Delay Line DMA

The ADSP-21367/ADSP-21368/ADSP-21369 processors provide delay line DMA functionality. This allows processor reads and writes to external delay line buffers (in external memory, SRAM, or SDRAM) with limited core interaction.

Digital Applications and Digital Peripheral Interfaces (DAI/DPI)

The digital applications and digital peripheral interfaces (DAI and DPI) provide the ability to connect various peripherals to any of the DSP's DAI or DPI pins (DAI_P20–1 and DPI_P14–1).

Programs make these connections using the signal routing units (SRU1 and SRU2), shown in Figure 1.

The SRUs are matrix routing units (or group of multiplexers) that enable the peripherals provided by the DAI and DPI to be interconnected under software control. This allows easy use of the associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

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The DAI and DPI also include eight serial ports, an S/PDIF receiver/transmitter, four precision clock generators (PCG), eight channels of synchronous sample rate converters, and an input data port (IDP). The IDP provides an additional input path to the processor core, configurable as either eight channels of I^{2}S serial data or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

For complete information on using the DAI and DPI, see the *ADSP-21368 SHARC Processor Hardware Reference*.

Serial Ports

The processors feature eight synchronous serial ports (SPORTs) that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports are enabled via 16 programmable and simultaneous receive or transmit pins that support up to 32 transmit or 32 receive channels of audio data when all eight SPORTs are enabled, or eight full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of 50 Mbps. Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode with support for packed I^{2}S mode
- I^{2}S mode
- Packed I^{2}S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample pair and I^{2}S protocols (I^{2}S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs such as the Analog Devices AD183x family), with two data pins, allowing four left-justified sample pair or I^{2}S channels (using two stereo devices) per serial port, with a maximum of up to 32 I^{2}S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I^{2}S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

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The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example, frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter and Synchronous/Asynchronous Sample Rate Converter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left-justified, I^{2}S, or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), or the sample rate converters (SRC) and are controlled by the SRU control registers.

The sample rate converter (SRC) contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), two universal asynchronous receiver-transmitters (UARTs), a 2-wire interface (TWI), 12 flags, and three general-purpose timers.

Serial Peripheral (Compatible) Interface

The processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI-compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-21367/ADSP-21368/ADSP-21369 SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open-drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for five data bits to eight data bits, one stop bit or two stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from 7 bits to 12 bits per frame.

- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

Where the 16-bit UART_Divisor comes from the DLH register (most significant eight bits) and DLL register (least significant eight bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

Timers

The ADSP-21367/ADSP-21368/ADSP-21369 have a total of four timers: a core timer that can generate periodic software interrupts and three general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general-purpose timers independently.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI master incorporates the following features:

- Simultaneous master and slave operation on multiple device systems with support for multimaster data arbitration
- Digital filtering and timed event processing
- 7-bit and 10-bit addressing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters.

ROM-Based Security

The ADSP-21367/ADSP-21368/ADSP-21369 have a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processor does not boot-load any external code, executing exclusively from internal SRAM/ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or test access port will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the processors can be booted up at system power-up from an 8-bit EPROM via the external port, an SPI master or slave, or an internal boot. Booting is determined by the boot configuration (BOOT_CFG1–0) pins (see Table 7 on Page 15). Selection of the boot source is controlled via the SPI as either a master or slave device, or it can immediately begin executing from ROM.

Power Supplies

The processors have separate power supply connections for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.3 V requirement for the 400 MHz device and 1.2 V for the 333 MHz and 266 MHz devices. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (A_{VDD}) powers the processor's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the A_{VDD} pin. Place the filter components as close as possible to the A_{VDD}/A_{VSS} pins. For an example circuit, see Figure 2. (A recommended ferrite chip is the muRata BLM18AG102SN1D). To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DDINT} and GND. Use wide traces to connect the bypass capacitors to the analog power (A_{VDD}) and ground (A_{VSS}) pins. Note that the A_{VDD} and A_{VSS} pins specified in Figure 2 are inputs to the processor and not the analog ground plane on the board—the A_{VSS} pin should connect directly to digital ground (GND) at the chip.

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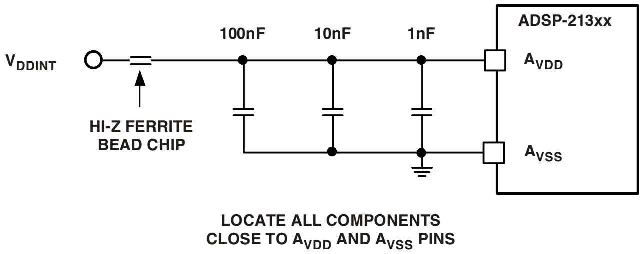

Figure 2. Analog Power (A_{VDD}) Filter Circuit

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21367/ ADSP-21368/ADSP-21369 processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide."

DEVELOPMENT TOOLS

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The processors are supported with a complete set of CROSSCORE® software and hardware development tools, including Analog Devices emulators and VisualDSP++® development environment. The same emulator hardware that supports other SHARC processors also fully emulates the ADSP-21367/ ADSP-21368/ADSP-21369.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to DSP assembly. The SHARC has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the SHARC development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command line switches

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state, when debugging an application that uses the VDK.

VisualDSP++ Component Software Engineering (VCSE) is Analog Devices' technology for creating, using, and reusing software components (independent modules of substantial functionality) to quickly and reliably assemble software applications. The user can download components from the Web, drop them into the application, and publish component archives from within VisualDSP++. VCSE supports component implementation in C/C++ or assembly language.

Use the Expert Linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the processor or external memory with a drag of the mouse and examine runtime stack and heap usage. The expert linker is fully compatible with the existing linker definition file (LDF), allowing the developer to move between the graphical and textual environments.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC processor PC plug-in cards. Third-party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG test access port (TAP) on each JTAG DSP. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

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To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

Evaluation Kit

Analog Devices offers a range of EZ-KIT Lite® evaluation platforms to use as a cost-effective method to learn more about developing or prototyping applications with Analog Devices processors, platforms, and software tools. Each EZ-KIT Lite includes an evaluation board along with an evaluation suite of the VisualDSP++ development and debugging environment with the C/C++ compiler, assembler, and linker. Also included are sample application programs, power supply, and a USB cable. All evaluation versions of the software tools are limited for use only with the EZ-KIT Lite product.

The USB controller on the EZ-KIT Lite board connects the board to the USB port of the user's PC, enabling the VisualDSP++ evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also allows in-circuit programming of the on-board flash device to store user-specific boot code, enabling the board to run as a standalone unit without being connected to the PC.

With a full version of VisualDSP++ installed (sold separately), engineers can develop software for the EZ-KIT Lite or any custom-defined system. Connecting one of Analog Devices JTAG emulators to the EZ-KIT Lite board enables high speed, nonintrusive emulation.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21367/ADSP-21368/ADSP-21369 architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-21368 SHARC Processor Hardware Reference* and the *ADSP-2136x/ADSP-2137x SHARC Processor Programming Reference*.

PIN FUNCTION DESCRIPTIONS

The following symbols appear in the Type column of Table 5: A = asynchronous, G = ground, I = input, O = output, O/T = output three-state, P = power supply, S = synchronous, (A/D) = active drive, (O/D) = open-drain, (pd) = pull-down resistor, (pu) = pull-up resistor.

The ADSP-21367/ADSP-21368/ADSP-21369 SHARC processors use extensive pin multiplexing to achieve a lower pin count. For complete information on the multiplexing scheme, see the *ADSP-21368 SHARC Processor Hardware Reference*, "System Design" chapter.

Table 5. Pin List

Name	Type	State During/ After Reset (ID = 00x)	Description
ADDR$_{23–0}$	O/T (pu)[1]	Pulled high/ driven low	**External Address.** The processors output addresses for external memory and peripherals on these pins.
DATA$_{31–0}$	I/O (pu)[1]	Pulled high/ pulled high	**External Data.** Data pins can be multiplexed to support external memory interface data (I/O), the PDAP (I), FLAGS (I/O), and PWM (O). After reset, all DATA pins are in EMIF mode and FLAG(0-3) pins are in FLAGS mode (default). When configured using the IDP_PDAP_CTL register, IDP Channel 0 scans the DATA$_{31–8}$ pins for parallel input data.
DAI _P$_{20–1}$	I/O with programmable pu[2]	Pulled high/ pulled high	**Digital Applications Interface**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audiocentric peripheral inputs or outputs connected to the pin, and to the pin's output enable. The configuration registers then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins. The DAI SRU provides the connection from the serial ports (8), the SRC module, the S/PDIF module, input data ports (2), and the precision clock generators (4), to the DAI_P20–1 pins. Pull-ups can be disabled via the DAI_PIN_PULLUP register.
DPI _P$_{14–1}$	I/O with programmable pu[2]	Pulled high/ pulled high	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins. The DPI SRU provides the connection from the timers (3), SPIs (2), UARTs (2), flags (12) TWI (1), and general-purpose I/O (9) to the DPI_P14–1 pins. The TWI output is an open-drain output—so the pins used for I^2C data and clock should be connected to logic level 0. Pull-ups can be disabled via the DPI_PIN_PULLUP register.
ACK	I (pu)[1]		**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{\text{RD}}$	O/T (pu)[1]	Pulled high/ driven high	**External Port Read Enable.** $\overline{\text{RD}}$ is asserted whenever the processors read a word from external memory.
$\overline{\text{WR}}$	O/T (pu)[1]	Pulled high/ driven high	**External Port Write Enable.** $\overline{\text{WR}}$ is asserted when the processors write a word to external memory.
$\overline{\text{SDRAS}}$	O/T (pu)[1]	Pulled high/ driven high	**SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDCAS}}$	O/T (pu)[1]	Pulled high/ driven high	**SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.

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Table 5. Pin List

Name	Type	State During/ After Reset (ID = 00x)	Description
$\overline{SDWE}$	O/T (pu)[1]	Pulled high/ driven high	**SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin.
SDCKE	O/T (pu)[1]	Pulled high/ driven high	**SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (pu)[1]	Pulled high/ driven low	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with non-SDRAM accesses. This pin replaces the DSP's A10 pin only during SDRAM accesses.
SDCLK0	O/T	High-Z/driving	**SDRAM Clock Output 0.** Clock driver for this pin differs from all other clock drivers. See Figure 38 on Page 46.
SDCLK1	O/T		**SDRAM Clock Output 1.** Additional clock for SDRAM devices. For systems with multiple SDRAM devices, handles the increased clock load requirements, eliminating need of off-chip clock buffers. Either SDCLK1 or both SDCLKx pins can be three-stated. Clock driver for this pin differs from all other clock drivers. See Figure 38 on Page 46. The SDCLK1 signal is only available on the SBGA package. SDCLK1 is not available on the LQFP_EP package.
$\overline{MS}_{0-1}$	O/T (pu)[1]	Pulled high/ driven high	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{3\text{-}0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring, the $\overline{MS}_{3\text{-}0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. The $\overline{MS}_1$ pin can be used in EPORT/FLASH boot mode. See the hardware reference for more information.
FLAG[0]/$\overline{IRQ0}$	I/O	High-Z/high-Z	**FLAG0/Interrupt Request 0.**
FLAG[1]/$\overline{IRQ1}$	I/O	High-Z/high-Z	**FLAG1/Interrupt Request 1.**
FLAG[2]/$\overline{IRQ2}$/ $\overline{MS}_2$	I/O with programmable pu (for MS mode)	High-Z/high-Z	**FLAG2/Interrupt Request 2/Memory Select 2.**
FLAG[3]/TIMEXP/ $\overline{MS}_3$	I/O with programmable pu (for MS mode)	High-Z/high-Z	**FLAG3/Timer Expired/Memory Select 3.**
TDI	I (pu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic.
TDO	O/T		**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (pu)		**Test Mode Select (JTAG).** Used to control the test state machine.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up, or held low for proper operation of the processor
$\overline{TRST}$	I (pu)		**Test Reset (JTAG).** Resets the test state machine. $\overline{TRST}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
$\overline{EMU}$	O/T (pu)		**Emulation Status.** Must be connected to the ADSP-21367/ADSP-21368/ ADSP-21369 Analog Devices DSP Tools product line of JTAG emulator target board connectors only.

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Table 5. Pin List

Name	Type	State During/ After Reset (ID = 00x)	Description
CLK_CFG_{1-0}	I		**Core/CLKIN Ratio Control.** These pins set the start-up clock frequency. See Table 8 for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
$BOOT\_CFG_{1-0}$	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. See Table 7 for a description of the boot modes.
$\overline{RESET}$	I		**Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{RESET}$ input must be asserted (low) at power-up.
XTAL	O		**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
CLKIN	I		**Local Clock In.** Used with XTAL. CLKIN is the processor's clock input. It configures the processors to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processor to use an external clock such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{RESETOUT}$/ CLKOUT	O/T	Driven low/ driven high	**Reset Out/Local Clock Out.** Reset out provides a 4096 cycle delay that allows the PLL to lock. This pin can also be configured as a CLKOUT signal to clock synchronous peripherals and memory. The functionality can be switched between the PLL output clock and reset out by setting Bit 12 of the PMCTL register. The default is reset out.
$\overline{BR}_{4-1}$	I/O (pu)[1]	Pulled high/ pulled high	**External Bus Request.** Used by the ADSP-21368 processor to arbitrate for bus mastership. A processor only drives its own $\overline{BR}_x$ line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a system with less than four processors, the unused $\overline{BR}_x$ pins should be tied high; the processor's own $\overline{BR}_x$ line must not be tied high or low because it is an output.
ID_{2-0}	I (pd)		**Processor ID.** Determines which bus request ($\overline{BR}_{4-1}$) is used by the ADSP-21368 processor. ID = 001 corresponds to $\overline{BR}_1$, ID = 010 corresponds to $\overline{BR}_2$, and so on. Use ID = 000 or 001 in single-processor systems. These lines are a system configuration selection that should be hardwired or only changed at reset. ID = 101,110, and 111 are reserved.
RPBA	I (pu)[1]		**Rotating Priority Bus Arbitration Select.** When RPBA is high, rotating priority for the ADSP-21368 external bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every processor in the system.

[1] The pull-up is always enabled on the ADSP-21367 and ADSP-21369 processors. The pull-up on the ADSP-21368 processor is only enabled on the processor with ID_{2-0} = 00x

[2] Pull-up can be enabled/disabled, value of pull-up cannot be programmed.

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DATA MODES

The upper 32 data pins of the external memory interface are muxed (using bits in the SYSCTL register) to support the external memory interface data (input/output), the PDAP (input only), the FLAGS (input/output), and the PWM channels (output). Table 6 provides the pin settings.

Table 6. Function of Data Pins

Data Pin Mode	DATA31–16	DATA15–8	DATA7–0
000	EPDATA32–0		
001	FLAGS/PWM15–0[1]	EPDATA15–0	
010	FLAGS/PWM15–0[1]	FLAGS15–8	EPDATA7–0
011	FLAGS/PWM15–0[1]	FLAGS15–0	
100	PDAP (DATA + CTRL)		EPDATA7–0
101	PDAP (DATA + CTRL)		FLAGS7–0
110	Reserved		
111	Three-state all pins		

[1] These signals can be FLAGS or PWM or a mix of both. However, they can be selected only in groups of four. Their function is determined by the control signals FLAGS/PWM_SEL. For more information, see the *ADSP-21368 SHARC Processor Hardware Reference*.

BOOT MODES

Table 7. Boot Mode Selection

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	EPROM/FLASH Boot
11	Reserved

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CORE INSTRUCTION RATE TO CLKIN RATIO MODES

For details on processor timing, see Timing Specifications and Figure 4 on Page 18.

Table 8. Core Instruction Rate/CLKIN Ratio Selection

CLK_CFG1–0	Core to CLKIN Ratio
00	6:1
01	32:1
10	16:1
11	Reserved

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	400 MHz Min	400 MHz Max	350 MHz Min	350 MHz Max	333 MHz Min	333 MHz Max	266 MHz Min	266 MHz Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.25	1.35	1.235	1.365	1.14	1.26	1.14	1.26	V
A_{VDD}	Analog (PLL) Supply Voltage	1.25	1.35	1.235	1.365	1.14	1.26	1.14	1.26	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	3.13	3.47	3.13	3.47	V
V_{IH}[2]	High Level Input Voltage @ V_{DDEXT} = Max	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	V
V_{IL}[2]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	V
V_{IH_CLKIN}[3]	High Level Input Voltage @ V_{DDEXT} = Max	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}[3]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+1.1	–0.5	+1.1	–0.5	+1.1	–0.5	+1.1	V
T_J	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to 70°C	N/A	N/A	0	110	0	110	0	110	°C
T_J	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	N/A	N/A	N/A	N/A	–40	+120	–40	+120	°C
T_J	Junction Temperature 256-Ball BGA_ED @ $T_{AMBIENT}$ 0°C to 70°C	0	95	N/A	N/A	0	105	N/A	N/A	°C
T_J	Junction Temperature 256-Ball BGA_ED @ $T_{AMBIENT}$ –40°C to +85°C	N/A	N/A	N/A	N/A	0	105	N/A	N/A	°C

[1] Specifications subject to change without notice.
[2] Applies to input and bidirectional pins: DATAx, ACK, RPBA, $\overline{BRx}$, IDx, FLAGx, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[3] Applies to input pin CLKIN.

ELECTRICAL CHARACTERISTICS

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Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}[1]	High Level Output Voltage	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[2]	2.4			V
V_{OL}[1]	Low Level Output Voltage	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[2]			0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max			10	μA
I_{IL}[3, 5, 6]	Low Level Input Current	@ V_{DDEXT} = Max, V_{IN} = 0 V			10	μA
I_{IHPD}[5]	High Level Input Current Pull-Down	@ V_{DDEXT} = Max, V_{IN} = 0 V			250	μA
I_{ILPU}[4]	Low Level Input Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V			200	μA
I_{OZH}[7, 8]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max			10	μA
I_{OZL}[7, 9]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = 0 V			10	μA
I_{OZLPU}[8]	Three-State Leakage Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V			200	μA
$I_{DD-INTYP}$[10]	Supply Current (Internal)	t_{CCLK} = 3.75 ns, V_{DDINT} = 1.2 V, 25°C		700		mA
		t_{CCLK} = 3.00 ns, V_{DDINT} = 1.2 V, 25°C		900		mA
		t_{CCLK} = 2.85 ns, V_{DDINT} = 1.3 V, 25°C		1050		mA
		t_{CCLK} = 2.50 ns, V_{DDINT} = 1.3 V, 25°C		1100		mA
AI_{DD}[11]	Supply Current (Analog)	A_{VDD} = Max			11	mA
C_{IN}[12, 13]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.3 V			4.7	pF

[1] Applies to output and bidirectional pins: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, FLAGx, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, SDCLKx, $\overline{EMU}$, TDO, CLKOUT.
[2] See Output Drive Currents on Page 46 for typical drive current capabilities.
[3] Applies to input pins without internal pull-ups: BOOT_CFGx, CLK_CFGx, CLKIN, $\overline{RESET}$, TCK.
[4] Applies to input pins with internal pull-ups: ACK, RPBA, TMS, TDI, $\overline{TRST}$.
[5] Applies to input pins with internal pull-downs: IDx.
[6] Applies to input pins with internal pull-ups disabled: ACK, RPBA.
[7] Applies to three-statable pins without internal pull-ups: FLAGx, SDCLKx, TDO.
[8] Applies to three-statable pins with internal pull-ups: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, $\overline{EMU}$.
[9] Applies to three-statable pins with internal pull-ups disabled: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10
[10] See *Estimating Power Dissipation for ADSP-21368 SHARC Processors (EE-299)* for further information.
[11] Characterized, but not tested.
[12] Applies to all signal pins.
[13] Guaranteed, but not tested.

PACKAGE INFORMATION

The information presented in Figure 3 provides details about the package branding for the ADSP-21367/ADSP-21368/ADSP-21369 processors. For a complete listing of product availability, see Ordering Guide on Page 55.

Figure 3. Typical Package Brand

Table 9. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Option
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

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ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

See *Estimating Power Dissipation for ADSP-21368 SHARC Processors* (EE-299) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 48.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 10 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 10. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.5 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature Under Bias	125°C

TIMING SPECIFICATIONS

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins (see Table 8 on Page 15). To determine switching frequencies for the serial ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports).

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Note the definitions of various clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 11 and Table 12.

In Table 11, CCLK is defined as:

$$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (2 \times PLLN)$$

where:

f_{CCLK} = CCLK frequency

$PLLM$ = Multiplier value programmed

$PLLN$ = Divider value programmed

Table 11. ADSP-21368 Clock Generation Operation

Timing Requirements	Description	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CCLK	Core Clock	$1/t_{CCLK}$

Note the definitions of various clock periods shown in Table 12 which are a function of CLKIN and the appropriate ratio control shown in Table 11.

Table 12. Clock Periods

Timing Requirements	Description[1]
t_{CK}	CLKIN Clock Period
t_{CCLK}	(Processor) Core Clock Period
t_{PCLK}	(Peripheral) Clock Period = 2 × t_{CCLK}
t_{SCLK}	Serial Port Clock Period = (t_{CCLK}) × SR
t_{SDCLK}	SDRAM Clock Period = (t_{CCLK}) × SDR
t_{SPICLK}	SPI Clock Period = (t_{CCLK}) × SPIR

[1] where:
SR = serial port-to-core clock ratio (wide range, determined by SPORT CLKDIV bits in DIVx register)
SPIR = SPI-to-core clock ratio (wide range, determined by SPIBAUD register setting)
SPICLK = SPI clock
SDR = SDRAM-to-core clock ratio (values determined by Bits 20–18 of the PMCTL register)

Figure 4 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the *ADSP-21368 SHARC Processor Hardware Reference* and *Managing the Core PLL on Third-Generation SHARC Processors (EE-290)*.

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 39 on Page 46 under Test Conditions for voltage reference levels.

Note that in the user application, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 14. The VCO frequency is calculated as follows:

$$f_{VCO} = 2 \times PLLM \times f_{INPUT}$$

where:

f_{VCO} is the VCO frequency

PLLM is the multiplier value programmed

f_{INPUT} is the input frequency to the PLL in MHz.

f_{INPUT} = CLKIN when the input divider is disabled

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

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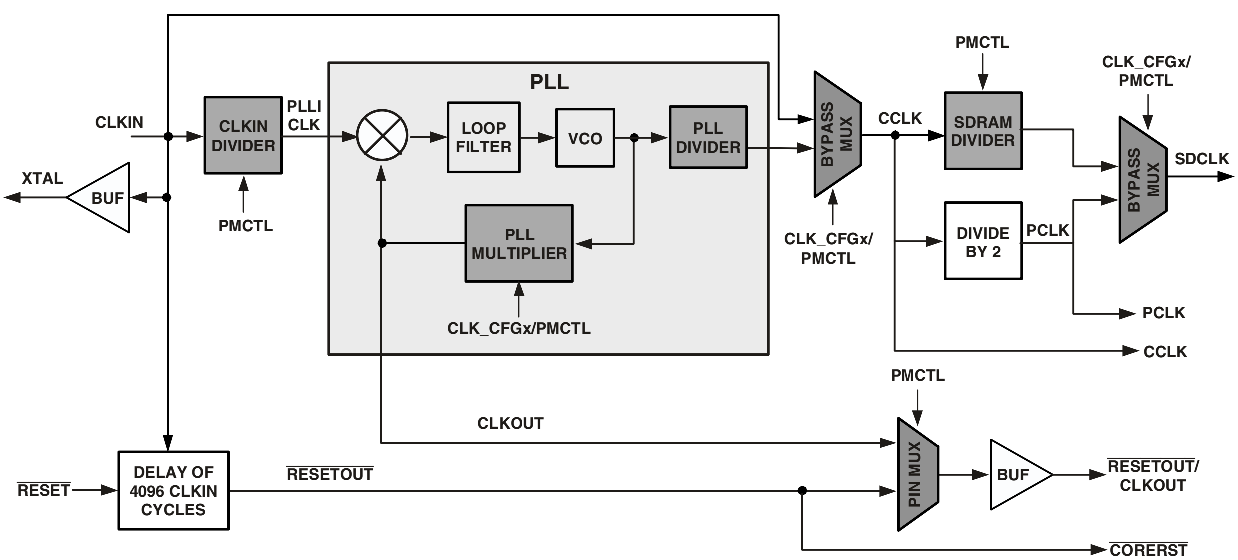

Figure 4. Core Clock and System Clock Relationship to CLKIN

Power-Up Sequencing

The timing requirements for processor start-up are given in Table 13. Note that during power-up, a leakage current of approximately 200µA may be observed on the $\overline{RESET}$ pin if it is driven low before power up is complete. This leakage current results from the weak internal pull-up resistor on this pin being enabled during power-up.

Table 13. Power-Up Sequencing Timing Requirements (Processor Start-up)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{RESET}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} On Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD}[1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{RESET}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{RESET}$ Deasserted	20		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{RESET}$ Deasserted	$4096t_{CK} + 2\ t_{CCLK}$ [3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 V rails and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Applies after the power-up sequence is complete. Subsequent resets require $\overline{RESET}$ to be held low a minimum of four CLKIN cycles in order to properly initialize and propagate default states at all I/O pins.

[4] The 4096 cycle count depends on t_{srst} specification in Table 15. If setup time is not met, 1 additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

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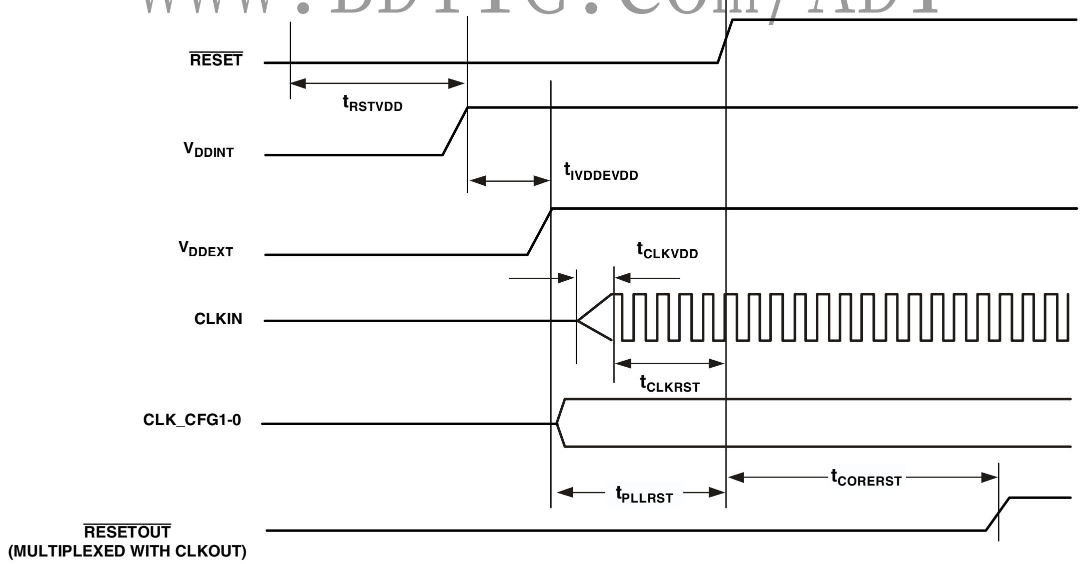

Figure 5. Power-Up Sequencing

Clock Input

Table 14. Clock Input

Parameter		400 MHz[1] Min	400 MHz[1] Max	350 MHz[2] Min	350 MHz[2] Max	333 MHz[3] Min	333 MHz[3] Max	266 MHz[4] Min	266 MHz[4] Max	Unit
Timing Requirements										
t_{CK}	CLKIN Period	15[5]	100	17.14[5]	100	18[5]	100	22.5[5]	100	ns
t_{CKL}	CLKIN Width Low	7.5[1]	45	8.5[1]	45	9[1]	45	11.25[1]	45	ns
t_{CKH}	CLKIN Width High	7.5[1]	45	8.5[1]	45	9[1]	45	11.25[1]	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3	ns
t_{CCLK}[6]	CCLK Period	2.5[5]	10	2.85[5]	10	3.0[5]	10	3.75[5]	10	ns
f_{VCO}[7]	VCO Frequency	100	800	100	800	100	800	100	600	MHz
t_{CKJ}[8, 9]	CLKIN Jitter Tolerance	–250	+250	–250	+250	–250	+250	–250	+250	ps

[1] Applies to all 400 MHz models. See Ordering Guide on Page 55.
[2] Applies to all 350 MHz models. See Ordering Guide on Page 55.
[3] Applies to all 333 MHz models. See Ordering Guide on Page 55.
[4] Applies to all 266 MHz models. See Ordering Guide on Page 55.
[5] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[6] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[7] See Figure 4 on Page 18 for VCO diagram.
[8] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[9] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

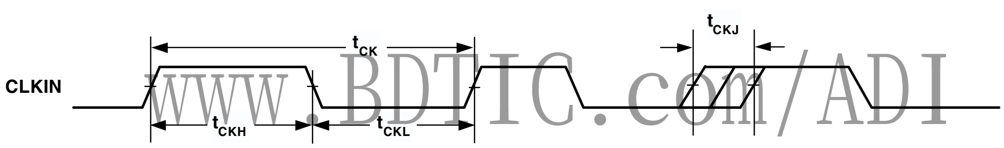

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Figure 6. Clock Input

Clock Signals

The processors can use an external clock or a crystal. See the CLKIN pin description in Table 5 on Page 12. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 7 shows the component connections used for a crystal operating in fundamental mode.

Note that the clock rate is achieved using a 25 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 400 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

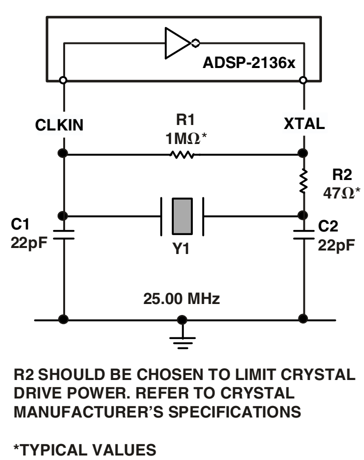

Figure 7. 400 MHz Operation (Fundamental Mode Crystal)

Reset

Table 15. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

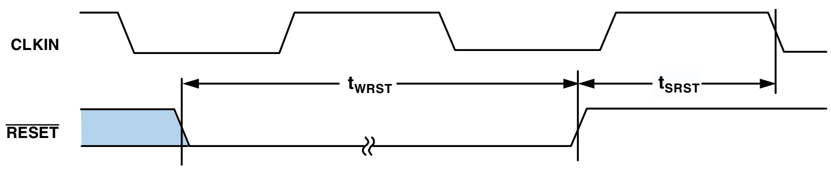

Figure 8. Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts.

Table 16. Interrupts

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Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

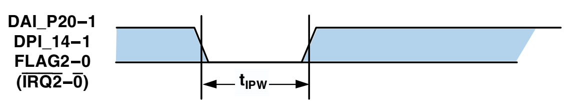

Figure 9. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (CTIMER).

Table 17. Core Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{WCTIM}	CTIMER Pulse Width	$4 \times t_{PCLK} - 1$		ns

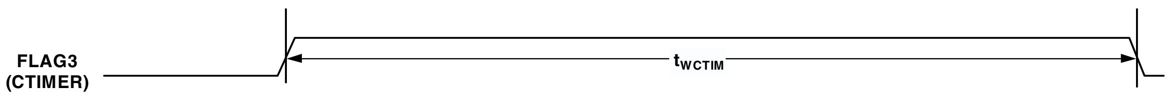

Figure 10. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 18. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

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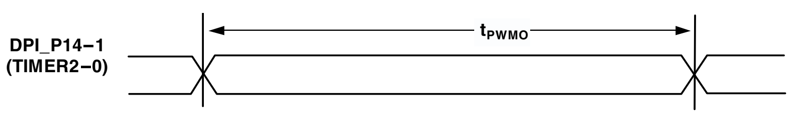

Figure 11. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The following specification applies to Timer0, Timer1, and Timer2 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the specification provided in Table 19 is valid at the DPI_P14–1 pins.

Table 19. Timer Width Capture Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

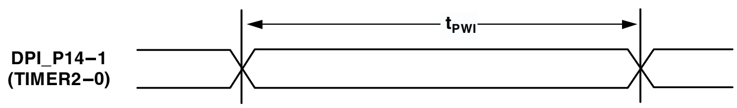

Figure 12. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 20. DAI Pin to Pin Routing

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Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI Pin Input Valid to DAI Output Valid	1.5	12	ns

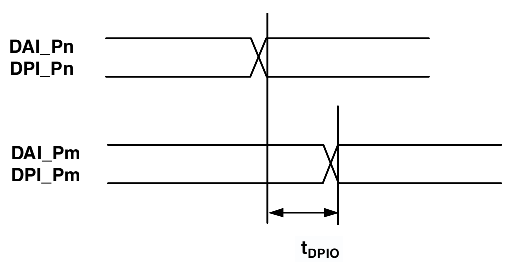

Figure 13. DAI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01–20).

Table 21. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIP}	Input Clock Period	$t_{CCLK} \times 8$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW} [1]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, and PH = FSxPHASE. For more information, see the *ADSP-2136x SHARC Processor Hardware Reference for the ADSP-21368 Processor*, "Precision Clock Generators" chapter.

[1] In normal mode.

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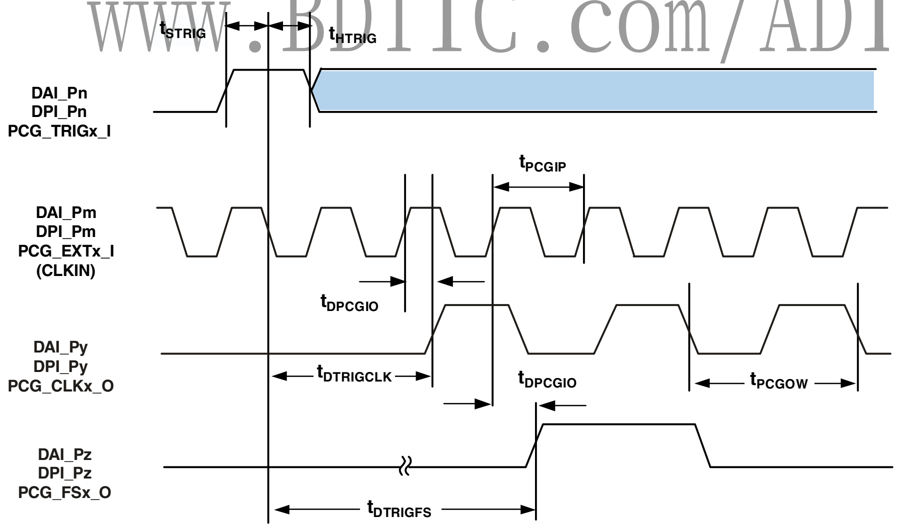

Figure 14. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to the FLAG3–0 and DPI_P14–1 pins, and the serial peripheral interface (SPI). See Table 5 on Page 12 for more information on flag use.

Table 22. Flags

Parameter		Min	Max	Unit
Timing Requirement				
t_{FIPW}	FLAG3–0 IN Pulse Width	$2 \times t_{PCLK} + 3$		ns
Switching Characteristic				
t_{FOPW}	FLAG3–0 OUT Pulse Width	$2 \times t_{PCLK} - 1.5$		ns

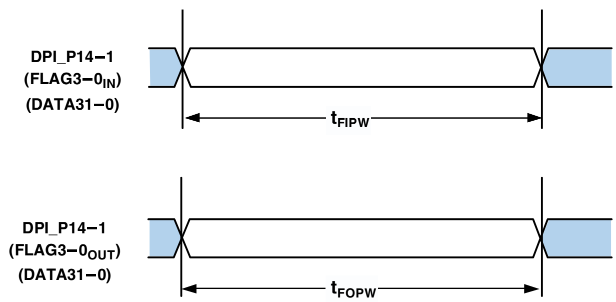

Figure 15. Flags

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SDRAM Interface Timing (166 MHz SDCLK)

The 166 MHz access speed is for a single processor. When multiple ADSP-21368 processors are connected in a shared memory system, the access speed is 100 MHz.

The processor needs to be programmed in $t_{SDCLK} = 2.5 \times t_{CCLK}$ mode when operated at 350 MHz.

Table 23. SDRAM Interface Timing[1]

Parameter		350 MHz Min	350 MHz Max	All Other Speed Grades Min	All Other Speed Grades Max	Unit
Timing Requirements						
t_{SSDAT}	DATA Setup Before SDCLK	500		500		ps
t_{HSDAT}	DATA Hold After SDCLK	1.23		1.23		ns
Switching Characteristics						
t_{SDCLK}	SDCLK Period	7.14		6.0		ns
t_{SDCLKH}	SDCLK Width High	3		2.6		ns
t_{SDCLKL}	SDCLK Width Low	3		2.6		ns
t_{DCAD}	Command, ADDR, Data Delay After SDCLK[2]		4.8		4.8	ns
t_{HCAD}	Command, ADDR, Data Hold After SDCLK[2]	1.2		1.2		ns
t_{DSDAT}	Data Disable After SDCLK		5.3		5.3	ns
t_{ENSDAT}	Data Enable After SDCLK	1.3		1.3		ns

[1] For f_{CCLK} = 400 MHz (SDCLK ratio = 1:2.5).
[2] Command pins include: $\overline{SDCAS}$, $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{MSx}$, SDA10, SDCKE.

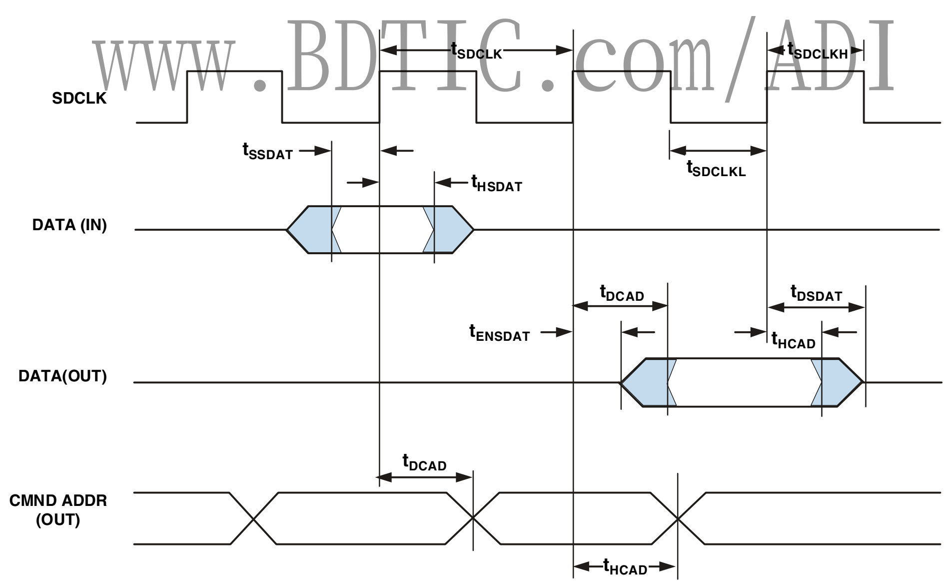

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Figure 16. SDRAM Interface Timing

SDRAM Interface Enable/Disable Timing (166 MHz SDCLK)

Table 24. SDRAM Interface Enable/Disable Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DSDC}	Command Disable After CLKIN Rise		$2 \times t_{PCLK} + 3$	ns
t_{ENSDC}	Command Enable After CLKIN Rise	4.0		ns
t_{DSDCC}	SDCLK Disable After CLKIN Rise		8.5	ns
t_{ENSDCC}	SDCLK Enable After CLKIN Rise	3.8		ns
t_{DSDCA}	Address Disable After CLKIN Rise		9.2	ns
t_{ENSDCA}	Address Enable After CLKIN Rise	$2 \times t_{PCLK} - 4$	$4 \times t_{PCLK}$	ns

[1] For f_{CCLK} = 400 MHz (SDCLK ratio = 1:2.5).

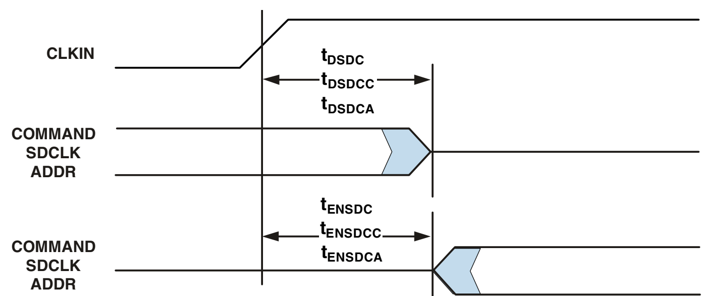

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Figure 17. SDRAM Interface Enable/Disable Timing

Memory Read

Use these specifications for asynchronous interfacing to memories. These specifications apply when the processors are the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 25. Memory Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1]		W + t_{SDCLK} –5.12	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid		W – 3.2	ns
t_{SDS}	Data Setup to $\overline{RD}$ High	2.5		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[2, 3]	0		ns
t_{DAAK}	ACK Delay from Address, Selects[1, 4]		t_{SDCLK} –9.5 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	RH + 0.20		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[1]	t_{SDCLK} – 3.3		ns
t_{RW}	$\overline{RD}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$ Low	HI + t_{SDCLK} – 0.8		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
HI =RHC + IC (RHC = number of read hold cycles specified in AMICTLx register) × t_{SDCLK}
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}.
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

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[1] The falling edge of $\overline{MSx}$ is referenced.
[2] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.
[3] Data hold: User must meet t_{HDA} or t_{HDRH} in asynchronous access mode. See Test Conditions on Page 46 for the calculation of hold times given capacitive and dc loads.
[4] ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high), user must meet t_{DAAK} or t_{DSAK}.

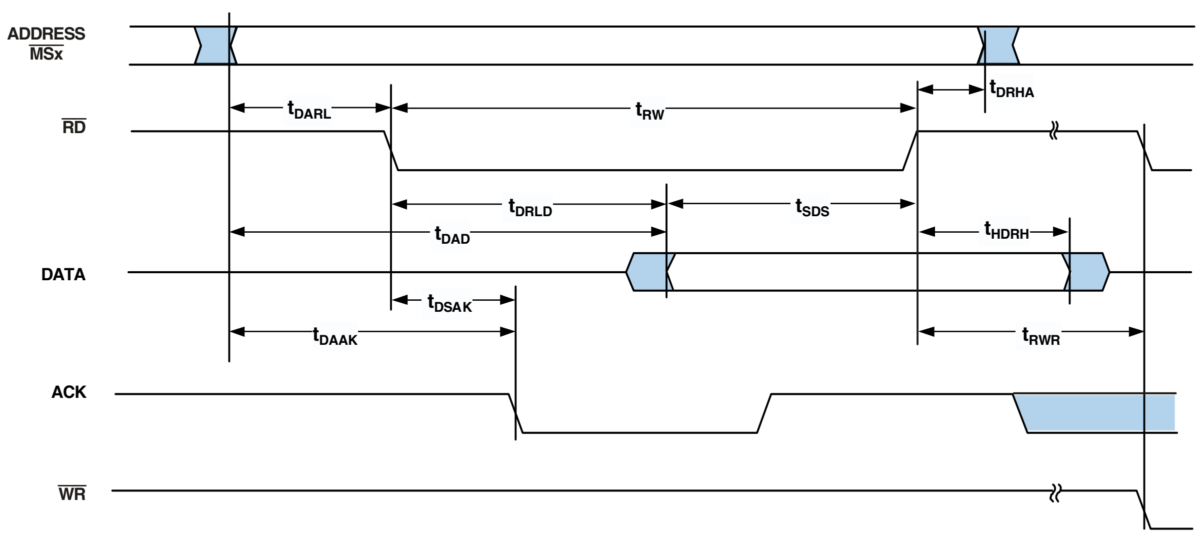

Figure 18. Memory Read

Memory Write

Use these specifications for asynchronous interfacing to memories. These specifications apply when the processors are the bus masters, accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.

Table 26. Memory Write

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		$t_{SDCLK} – 9.7 + W$	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low [1, 3]		$W – 4.9$	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	$t_{SDCLK} – 3.1 + W$		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	$t_{SDCLK} – 2.7$		ns
t_{WW}	$\overline{WR}$ Pulse Width	$W – 1.3$		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	$t_{SDCLK} – 3.0 + W$		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	$H + 0.15$		ns
t_{DWHD}	Data Hold After $\overline{WR}$ Deasserted	$H + 0.02$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	$t_{SDCLK} – 1.5 + H$		ns
t_{DDWR}	Data Disable Before $\overline{RD}$ Low	$2t_{SDCLK} – 4.11$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	$t_{SDCLK} – 3.5$		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.

H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high), user must meet t_{DAAK} or t_{DSAK}.

[2] The falling edge of $\overline{MSx}$ is referenced.

[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.

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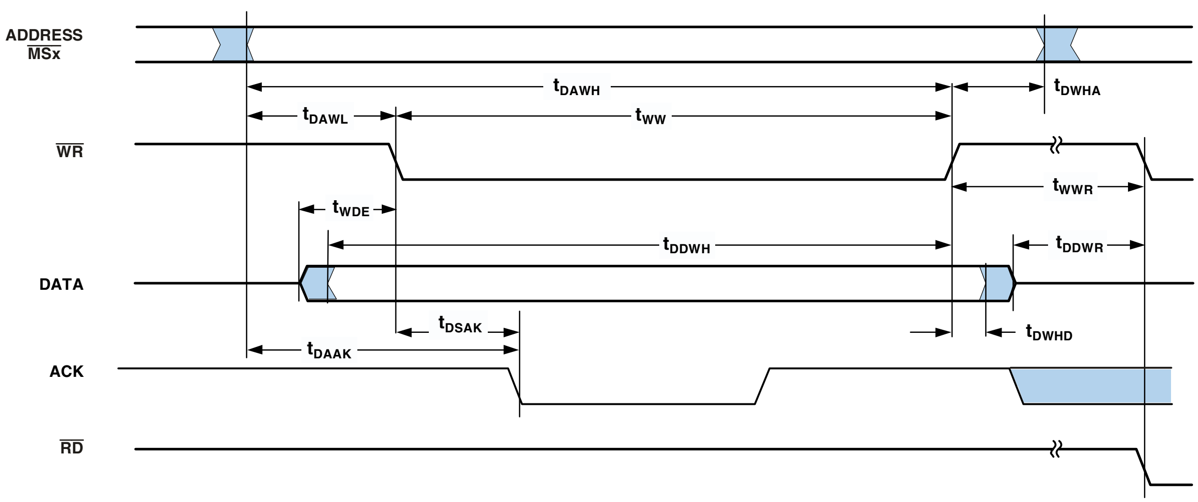

Figure 19. Memory Write

Asynchronous Memory Interface (AMI) Enable/Disable

Use these specifications for passing bus mastership between ADSP-21368 processors ($\overline{BRx}$).

Table 27. AMI Enable/Disable

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{ENAMIAC}$	Address/Control Enable After Clock Rise	4		ns
t_{ENAMID}	Data Enable After Clock Rise	$t_{SDCLK} + 4$		ns
$t_{DISAMIAC}$	Address/Control Disable After Clock Rise		8.7	ns
$t_{DISAMID}$	Data Disable After Clock Rise		0	ns

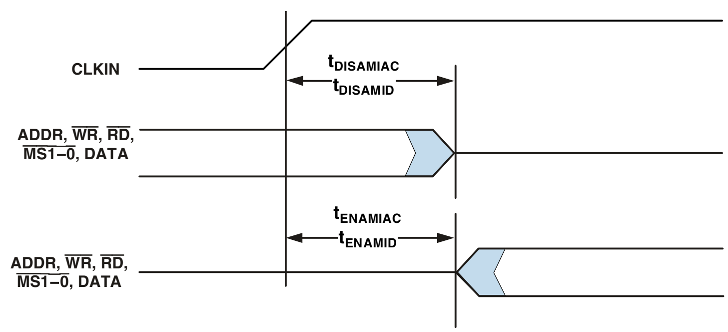

Figure 20. AMI Enable/Disable

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Shared Memory Bus Request

Use these specifications for passing bus mastership between ADSP-21368 processors ($\overline{BRx}$).

Table 28. Multiprocessor Bus Request

Parameter		Min	Max	Unit
Timing Requirements				
t_{SBRI}	$\overline{BRx}$, Setup Before CLKIN High	9		ns
t_{HBRI}	$\overline{BRx}$, Hold After CLKIN High	0.5		ns
Switching Characteristics				
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN High		9	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN High	1.0		ns

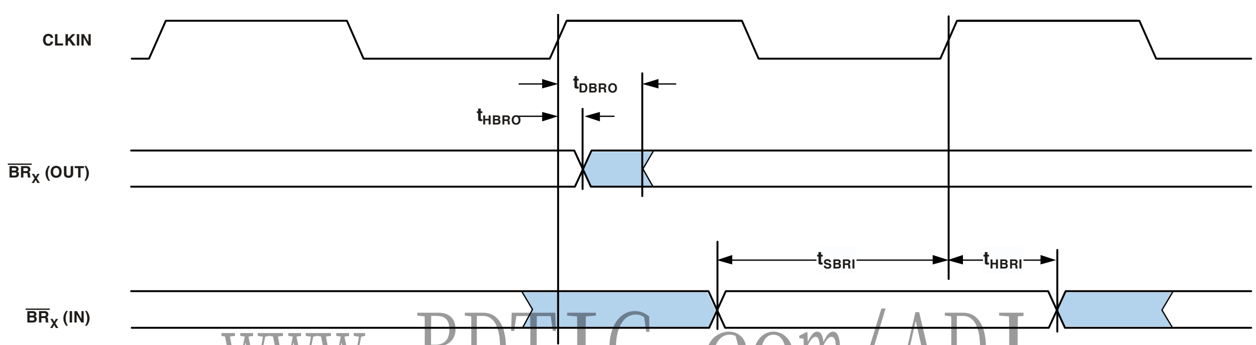

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Figure 21. Shared Memory Bus Request

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals SCLK, frame sync (FS), data channel A, data channel B are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 29. Serial Ports—External Clock

Parameter		400 MHz Min	400 MHz Max	333 MHz Min	333 MHz Max	266 MHz Min	266 MHz Max	Unit
Timing Requirements								
t_{SFSE}[1]	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		2.5		2.5		ns
t_{HFSE}[1]	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		2.5		2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	1.9		2.0		2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		2.5		2.5		ns
t_{SCLKW}	SCLK Width	$(t_{CCLK} \times 8) \div 2 - 0.5$		$(t_{CCLK} \times 8) \div 2 - 0.5$		$(t_{CCLK} \times 8) \div 2 - 0.5$		ns
t_{SCLK}	SCLK Period	$t_{CCLK} \times 8$		$t_{CCLK} \times 8$		$t_{CCLK} \times 8$		ns
Switching Characteristics								
t_{DFSE}[2]	FS Delay After SCLK (Internally Generated FS in Either Transmit or Receive Mode)		10.25		10.25		10.25	ns
t_{HOFSE}[2]	FS Hold After SCLK (Internally Generated FS in Either Transmit or Receive Mode)	2		2		2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		7.8		9.6		9.8	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		2		2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

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Table 30. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	FS Delay After SCLK (Internally Generated FS in Transmit Mode)		4	ns
t_{HOFSI}[2]	FS Hold After SCLK (Internally Generated FS in Transmit Mode)	–1.0		ns
t_{DFSIR}[2]	FS Delay After SCLK (Internally Generated FS in Receive Mode)		9.75	ns
t_{HOFSIR}[2]	FS Hold After SCLK (Internally Generated FS in Receive Mode)	–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.25	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		ns
t_{SCLKIW}[3]	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.
[3] Minimum SPORT divisor register value.

Table 31. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		10	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1		ns

[1] Referenced to drive edge.

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Table 32. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0		7.75	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair as well as DSP serial mode, and MCE = 1, MFD = 0.

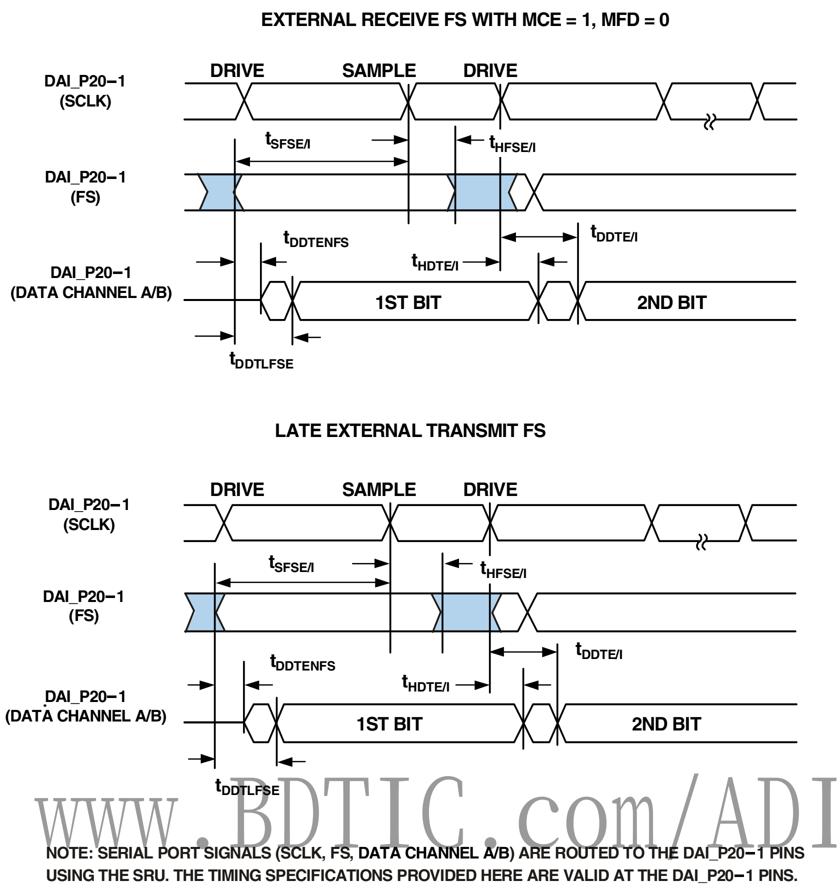

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Figure 22. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified sample pair mode.

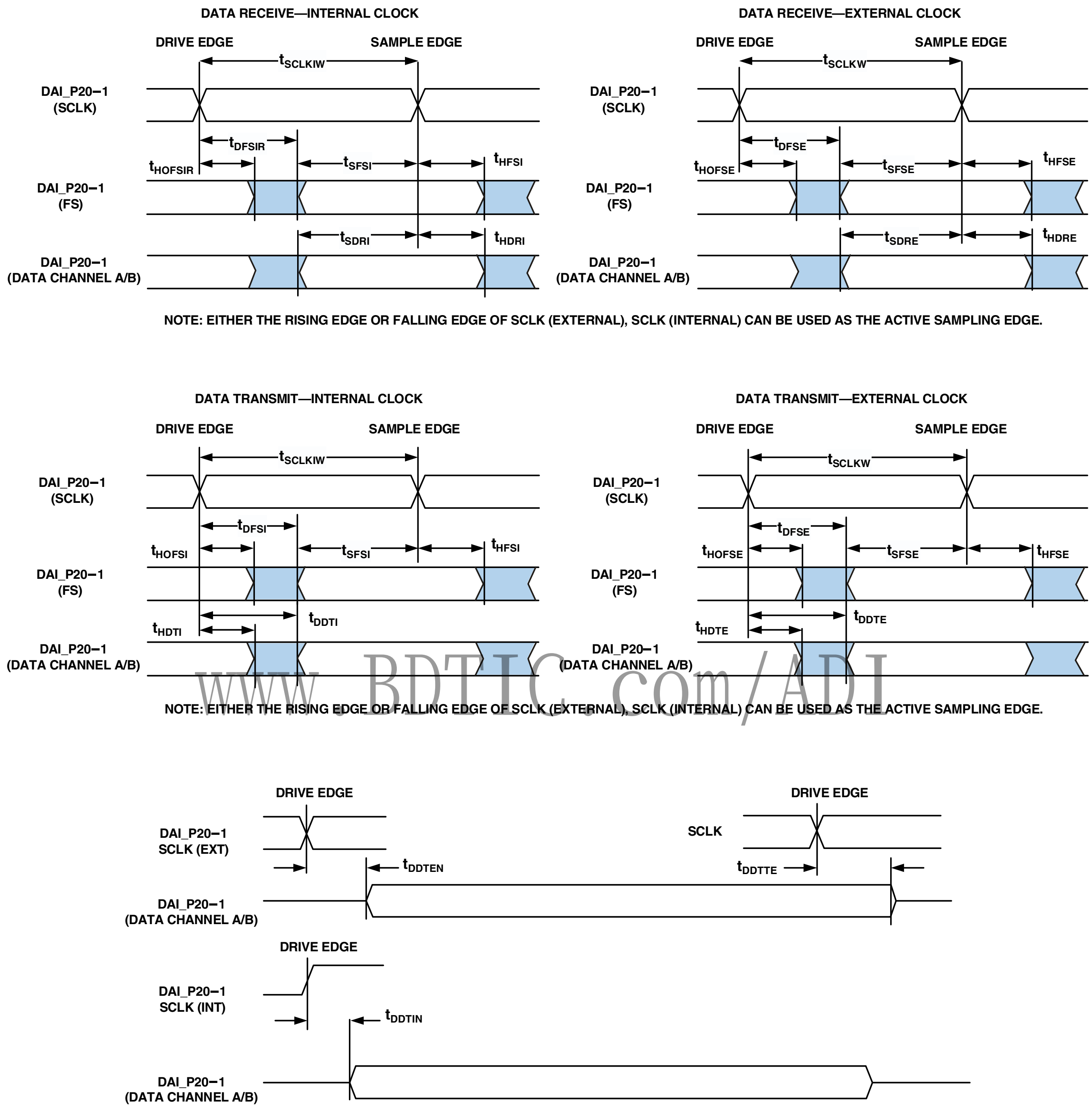

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Figure 23. Serial Ports

Input Data Port

The timing requirements for the IDP are given in Table 33. IDP signals SCLK, frame sync (FS), and SDATA are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 33. IDP

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	2.5		ns
t_{SISD}[1]	SDATA Setup Before SCLK Rising Edge	2.5		ns
t_{SIHD}[1]	SDATA Hold After SCLK Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{CCLK} \times 8) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{CCLK} \times 8$		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

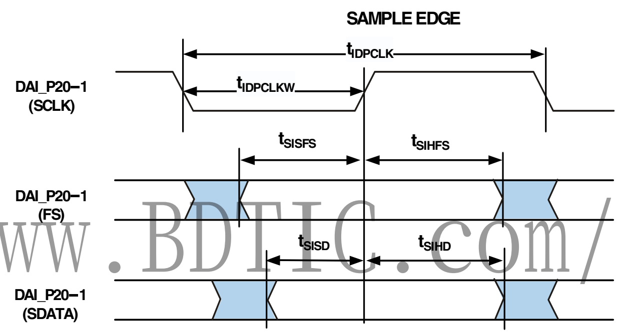

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Figure 24. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 34. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the IDP, see the IDP chapter of the *ADSP-21368 SHARC Processor Hardware Reference*. Note that the most significant 16 bits of external PDAP data can be provided through the DATA31–16 pins. The remaining four bits can only be sourced through DAI_P4–1. The timing below is valid at the DATA31–16 pins.

Table 34. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPCLKEN}$[1]	PDAP_CLKEN Setup Before PDAP_CLK Sample Edge	2.5		ns
$t_{HPCLKEN}$[1]	PDAP_CLKEN Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	$(t_{CCLK} \times 8) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{CCLK} \times 8$		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1$		ns

[1] Source pins of DATA are ADDR7–0, DATA7–0, or DAI pins. Source pins for SCLK and FS are: 1) DAI pins, 2) CLKIN through PCG, or 3) DAI pins through PCG.

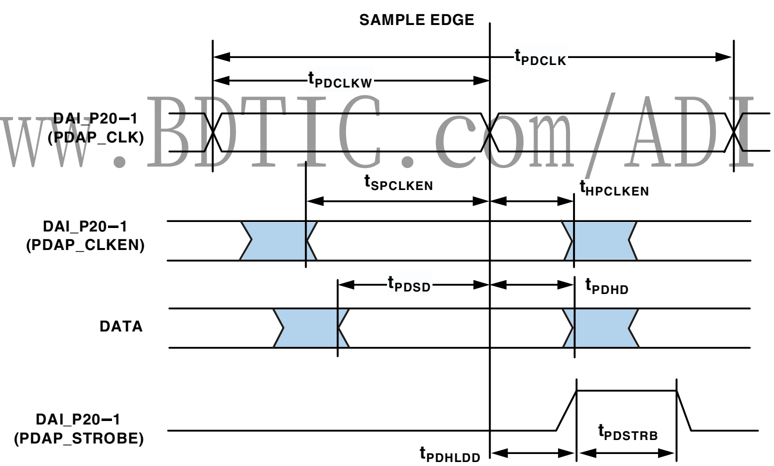

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Figure 25. PDAP Timing

Pulse-Width Modulation Generators

Table 35. PWM Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK} - 2$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK} - 1.5$	ns

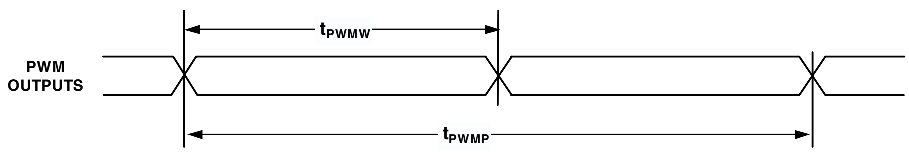

Figure 26. PWM Timing

Sample Rate Converter—Serial Input Port

The SRC input signals SCLK, frame sync (FS), and SDATA are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 36 are valid at the DAI_P20–1 pins.

Table 36. SRC, Serial Input Port

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Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	5.5		ns
t_{SRCSD}[1]	SDATA Setup Before SCLK Rising Edge	4		ns
t_{SRCHD}[1]	SDATA Hold After SCLK Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{CCLK} \times 8) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{CCLK} \times 8$		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

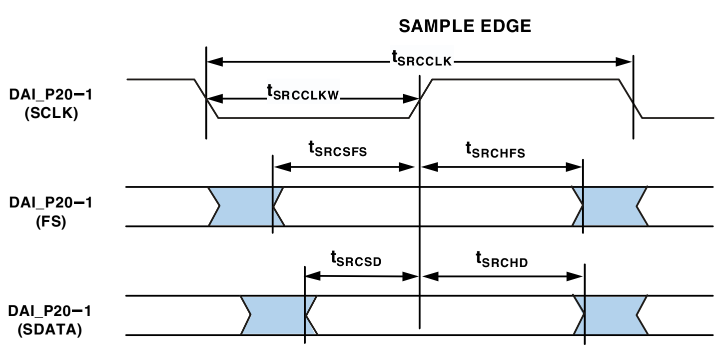

Figure 27. SRC Serial Input Port Timing

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and it should meet setup and hold times with regard to SCLK on the output port. The serial data output, SDATA, has a hold time and delay specification with regard to SCLK. Note that SCLK rising edge is the sampling edge and the falling edge is the drive edge.

Table 37. SRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{CCLK} \times 8) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{CCLK} \times 8$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After SCLK Falling Edge		9.9	ns
t_{SRCTDH}[1]	Transmit Data Hold After SCLK Falling Edge	1		ns

[1] DATA, SCLK, and FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

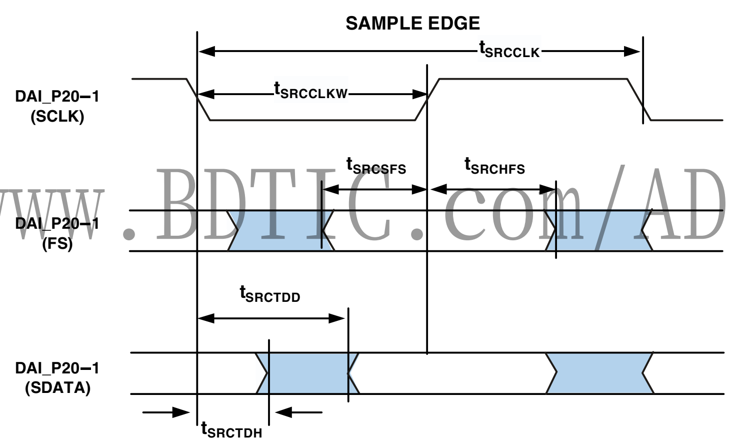

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Figure 28. SRC Serial Output Port Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I²S, or right justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter—Serial Input Waveforms

Figure 29 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of SCLK. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 SCLK periods per LRCLK period, the LSB of the data is right-justified to the next LRCLK transition.

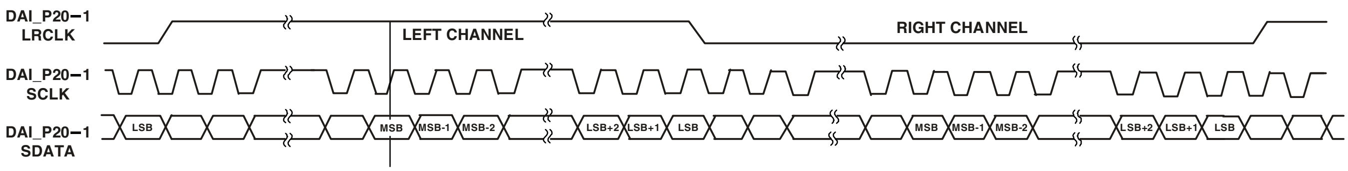

Figure 29. Right-Justified Mode

Figure 30 shows the default I²S-justified mode. LRCLK is low for the left channel and high for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition but with a single SCLK period delay.

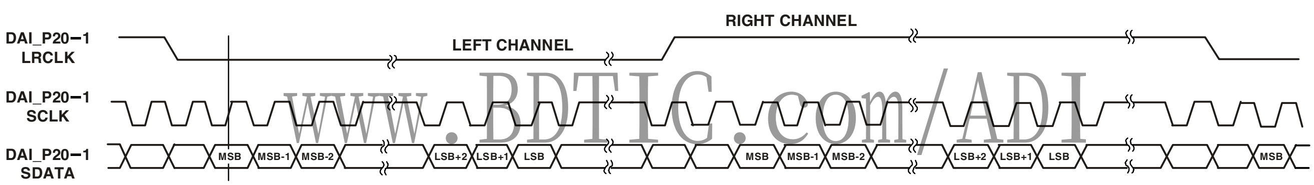

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Figure 30. I²S-Justified Mode

Figure 31 shows the left-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition with no MSB delay.

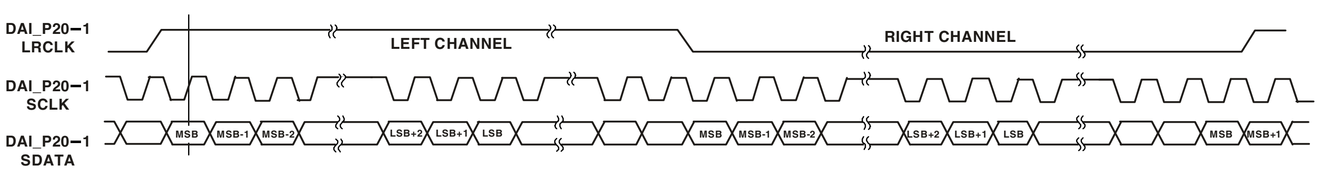

Figure 31. Left-Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the input port are given in Table 38. Input signals SCLK, frame sync (FS), and SDATA are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 38. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	3		ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	3		ns
t_{SISD}[1]	SData Setup Before SCLK Rising Edge	3		ns
t_{SIHD}[1]	SData Hold After SCLK Rising Edge	3		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns

[1] DATA, SCLK, and FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

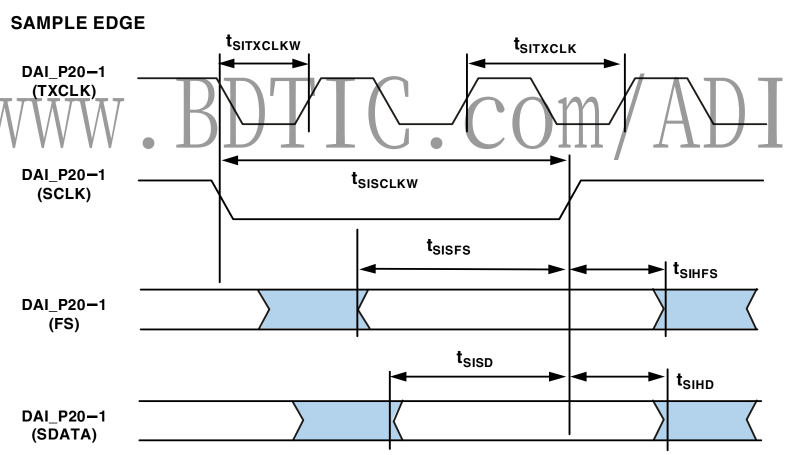

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Figure 32. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter has an oversampling clock. This TxCLK input is divided down to generate the biphase clock.

Table 39. Oversampling Clock (TxCLK) Switching Characteristics

Parameter	Min	Max	Unit
TxCLK Frequency for TxCLK = 384 × FS		73.8	MHz
TxCLK Frequency for TxCLK = 256 × FS		49.2	MHz
Frame Rate		192.0	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

Table 40. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	LRCLK Delay After SCLK		5	ns
t_{HOFSI}	LRCLK Hold After SCLK	–2		ns
t_{DDTI}	Transmit Data Delay After SCLK		5	ns
t_{HDTI}	Transmit Data Hold After SCLK	–2		ns
t_{SCLKIW} [1]	Transmit SCLK Width	40		ns

[1] SCLK frequency is 64 × FS where FS = the frequency of LRCLK.

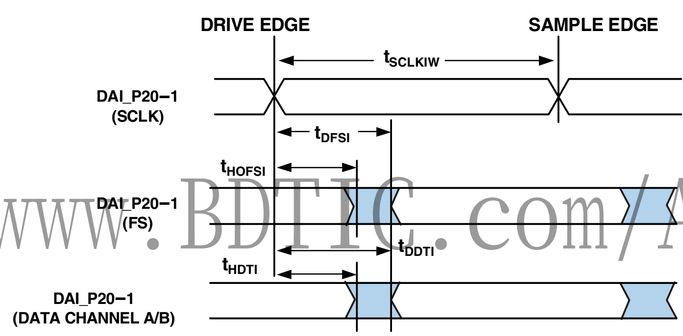

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Figure 33. S/PDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Master

The processors contain two SPI ports. The primary has dedicated pins and the secondary is available through the DPI. The timing provided in Table 41 and Table 42 on Page 44 applies to both.

Table 41. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	FLAG3–0IN (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to FLAG3–0IN High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		ns

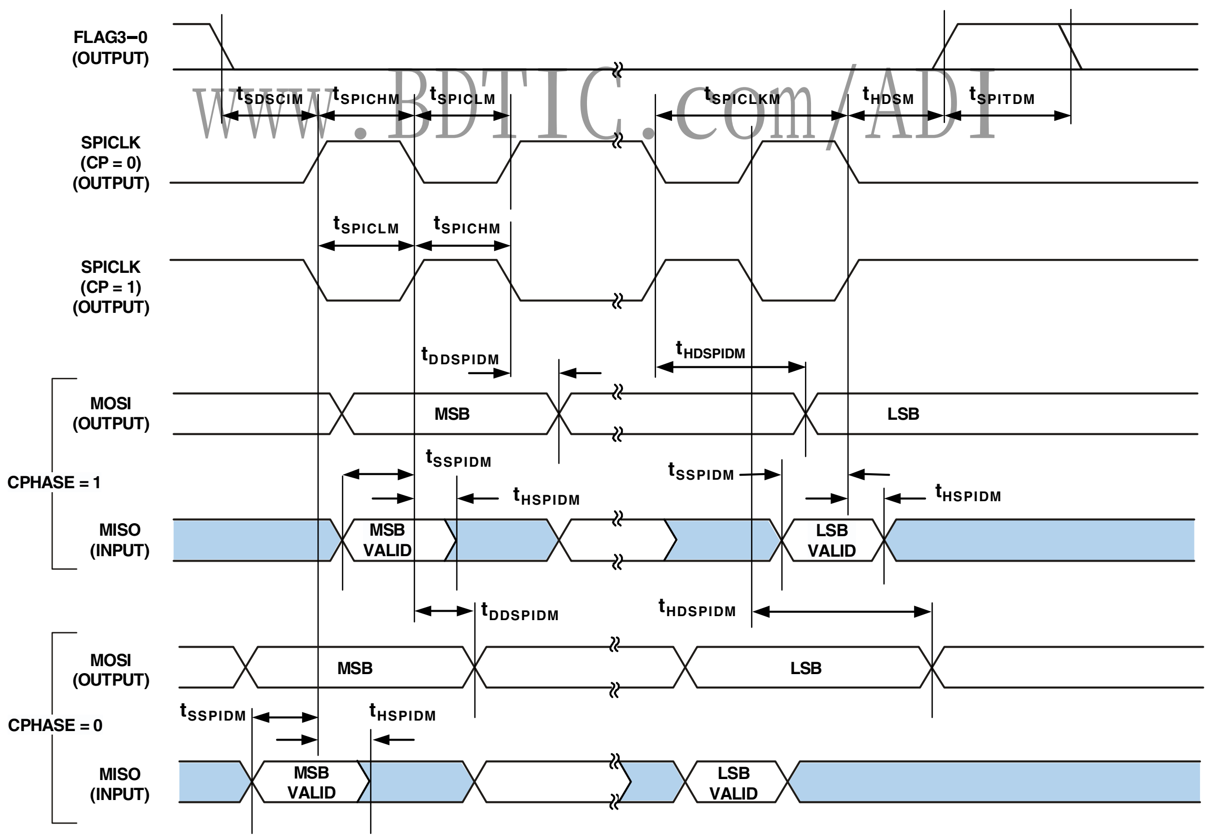

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Figure 34. SPI Master Timing

SPI Interface—Slave

Table 42. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$		ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge, CPHASE = 0 or CPHASE = 1	$2 \times t_{PCLK}$		ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$		ns
t_{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	2		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE = 0)	$2 \times t_{PCLK}$		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	6.8	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	8	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	6.8	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	8.6	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$		ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, see the *ADSP-21368 SHARC Processor Hardware Reference*, "Serial Peripheral Interface Port" chapter.

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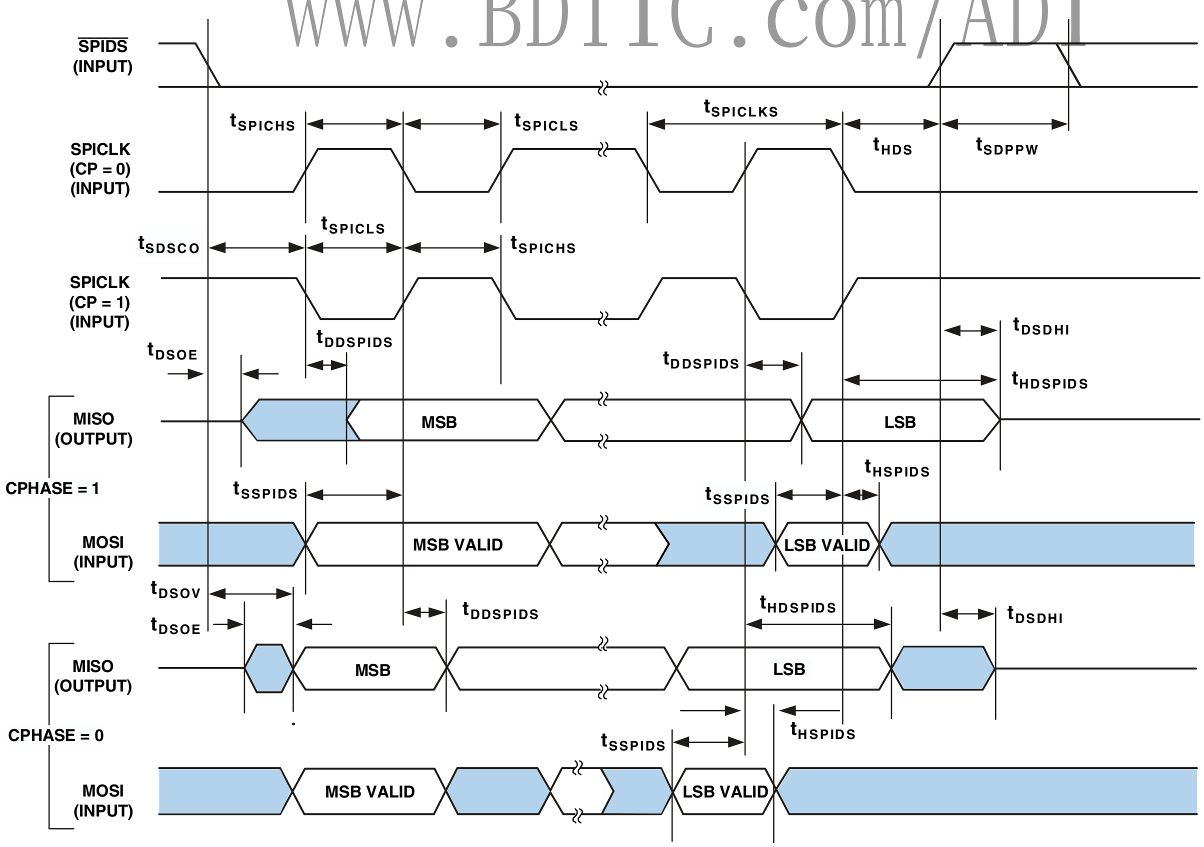

Figure 35. SPI Slave Timing

JTAG Test Access Port and Emulation

Table 43. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = AD15–0, $\overline{SPIDS}$, CLK_CFG1–0, $\overline{RESET}$, BOOT_CFG1–0, MISO, MOSI, SPICLK, DAI_Px, FLAG3–0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, AD15–0, $\overline{RD}$, $\overline{WR}$, FLAG3–0, CLKOUT, $\overline{EMU}$.

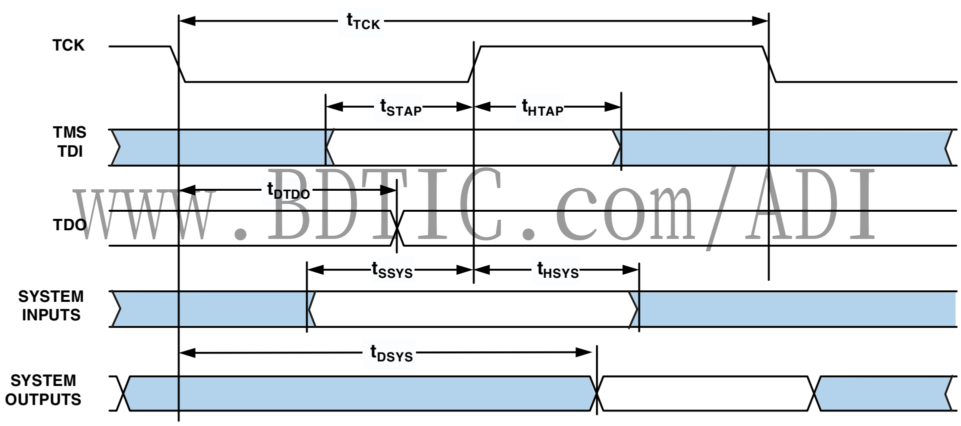

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Figure 36. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 37 shows typical I-V characteristics for the output drivers and Figure 38 shows typical I-V characteristics for the SDCLK output drivers. The curves represent the current drive capability of the output drivers as a function of output voltage.

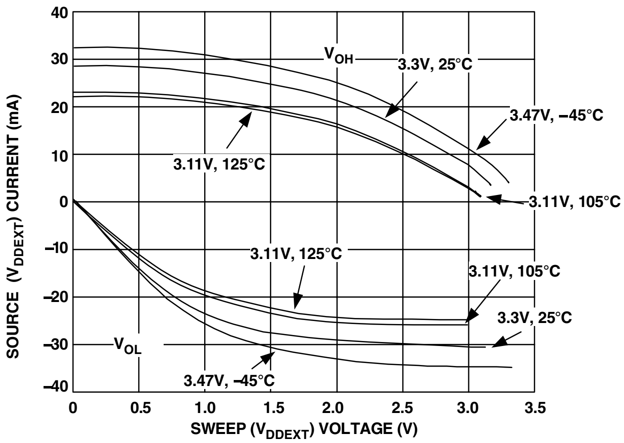

Figure 37. Typical Drive at Junction Temperature

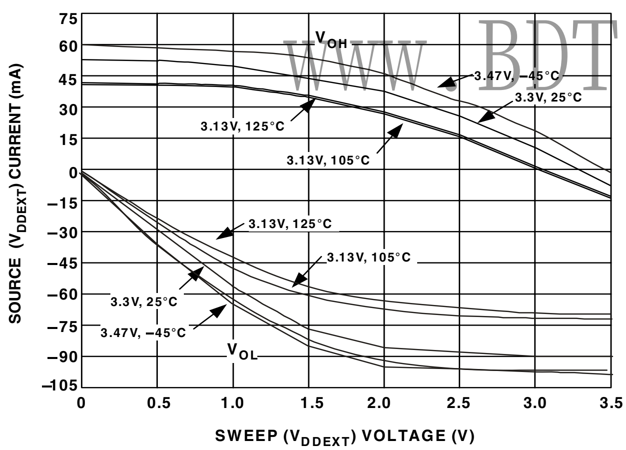

Figure 38. SDCLK1–0 Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 15 on Page 21 through Table 43 on Page 45. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 39.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 39. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

Figure 39. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 40). Figure 45 and Figure 46 show graphically how output delays and holds vary with load capacitance. The graphs of Figure 41 through Figure 46 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

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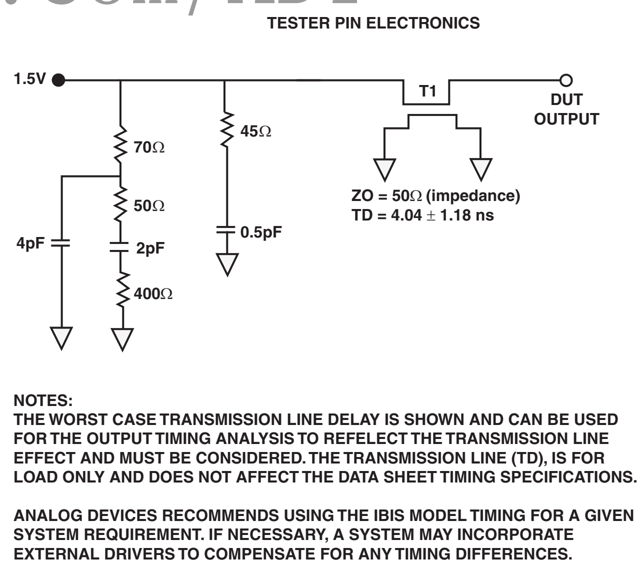

Figure 40. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

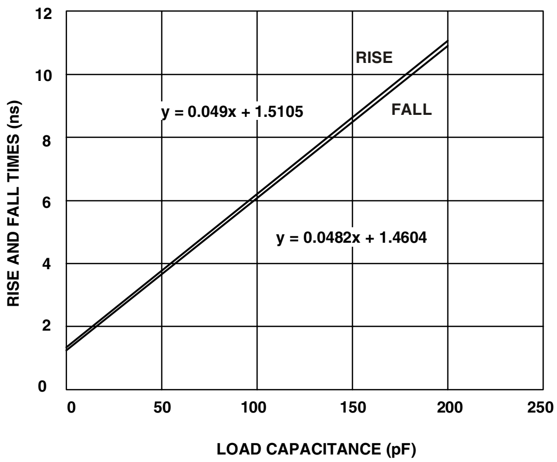

Figure 41. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

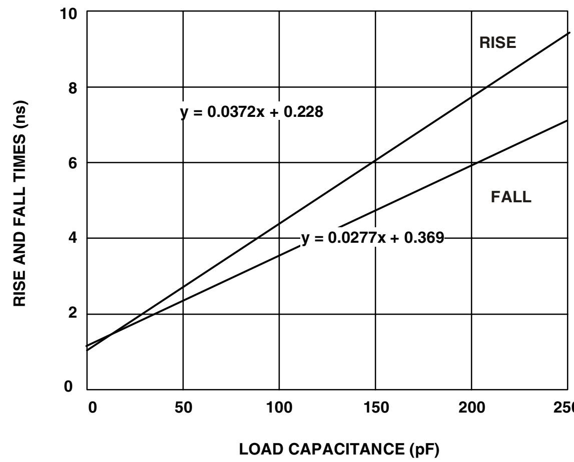

Figure 43. SDCLK Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

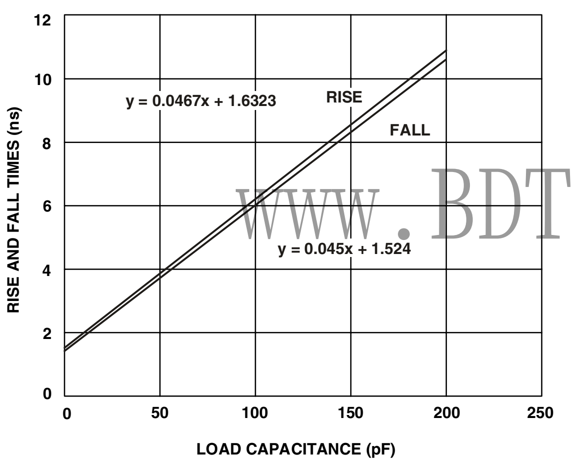

Figure 42. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

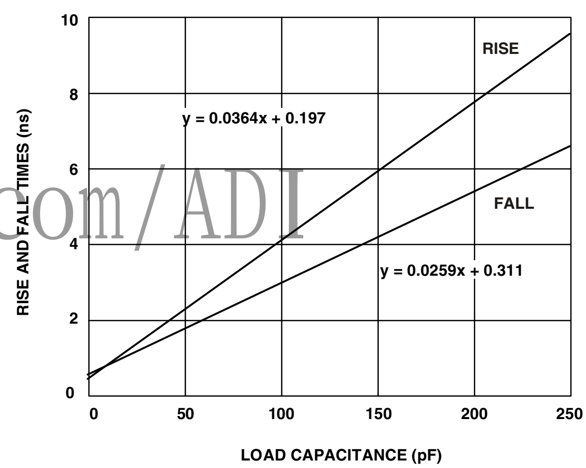

Figure 44. SDCLK Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

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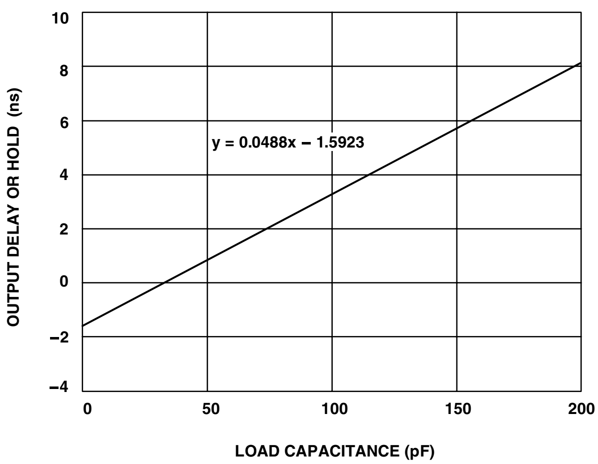

Figure 45. Typical Output Delay or Hold vs. Load Capacitance (at Junction Temperature)

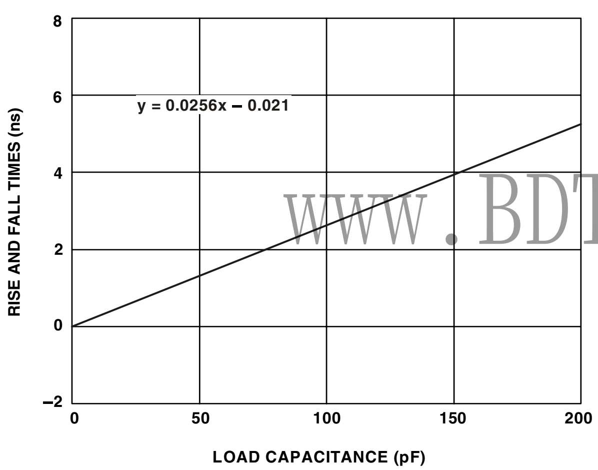

Figure 46. SDCLK Typical Output Delay or Hold vs. Load Capacitance (at Junction Temperature)

THERMAL CHARACTERISTICS

The ADSP-21367/ADSP-21368/ADSP-21369 processors are rated for performance over the temperature range specified in Operating Conditions on Page 16.

Table 44 and Table 45 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-9 (BGA_ED) and JESD51-8 (LQFP_EP). The junction-to-case measurement complies with MIL-STD-883. All measurements use a 2S2P JEDEC test board.

The LQFP-EP package requires thermal trace squares and thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-5 for more information.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{TOP} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_{TOP} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 44 and Table 45.

P_D = power dissipation (see EE Note EE-299)

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required. This is only applicable when a heat sink is used.

Values of θ_{JB} are provided for package comparison and PCB design considerations. The thermal characteristics values provided in Table 44 and Table 45 are modeled values @ 2 W.

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Table 44. Thermal Characteristics for 256-Ball BGA_ED

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	12.5	°C/W
θ_{JMA}	Airflow = 1 m/s	10.6	°C/W
θ_{JMA}	Airflow = 2 m/s	9.9	°C/W
θ_{JC}		0.7	°C/W
θ_{JB}		5.3	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.3	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.3	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.3	°C/W

Table 45. Thermal Characteristics for 208-Lead LQFP EPAD (With Exposed Pad Soldered to PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	17.1	°C/W
θ_{JMA}	Airflow = 1 m/s	14.7	°C/W
θ_{JMA}	Airflow = 2 m/s	14.0	°C/W
θ_{JC}		9.6	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.23	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.39	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.45	°C/W
Ψ_{JB}	Airflow = 0 m/s	11.5	°C/W
Ψ_{JMB}	Airflow = 1 m/s	11.2	°C/W
Ψ_{JMB}	Airflow = 2 m/s	11.0	°C/W

256-BALL BGA_ED PINOUT

Table 46. 256-Ball BGA_ED Pin Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A01	NC	B01	DAI5	C01	DAI9	D01	DAI10
A02	TDI	B02	SDCLK1[1]	C02	DAI7	D02	DAI6
A03	TMS	B03	$\overline{\text{TRST}}$	C03	GND	D03	GND
A04	CLK_CFG0	B04	TCK	C04	V_{DDEXT}	D04	V_{DDEXT}
A05	CLK_CFG1	B05	BOOT_CFG0	C05	GND	D05	GND
A06	$\overline{\text{EMU}}$	B06	BOOT_CFG1	C06	GND	D06	V_{DDEXT}
A07	DAI4	B07	TDO	C07	V_{DDINT}	D07	V_{DDINT}
A08	DAI1	B08	DAI3	C08	GND	D08	GND
A09	DPI14	B09	DAI2	C09	GND	D09	V_{DDEXT}
A10	DPI12	B10	DPI13	C10	V_{DDINT}	D10	V_{DDINT}
A11	DPI10	B11	DPI11	C11	GND	D11	GND
A12	DPI9	B12	DPI8	C12	GND	D12	V_{DDEXT}
A13	DPI7	B13	DPI5	C13	V_{DDINT}	D13	V_{DDINT}
A14	DPI6	B14	DPI4	C14	GND	D14	GND
A15	DPI3	B15	DPI1	C15	GND	D15	V_{DDEXT}
A16	DPI2	B16	$\overline{\text{RESET}}$	C16	V_{DDINT}	D16	GND
A17	$\overline{\text{RESETOUT}}$/CLKOUT	B17	DATA30	C17	V_{DDINT}	D17	V_{DDEXT}
A18	DATA31	B18	DATA29	C18	V_{DDINT}	D18	GND
A19	NC	B19	DATA28	C19	DATA27	D19	DATA26
A20	NC	B20	NC	C20	NC/RPBA[2]	D20	DATA24
E01	DAI11	F01	DAI14	G01	DAI15	H01	DAI17
E02	DAI8	F02	DAI12	G02	DAI13	H02	DAI16
E03	V_{DDINT}	F03	GND	G03	GND	H03	V_{DDINT}
E04	V_{DDINT}	F04	GND	G04	V_{DDEXT}	H04	V_{DDINT}
E17	GND	F17	V_{DDEXT}	G17	V_{DDINT}	H17	V_{DDEXT}
E18	GND	F18	GND	G18	V_{DDINT}	H18	GND
E19	DATA25	F19	GND/ID2[2]	G19	DATA22	H19	DATA19
E20	DATA23	F20	DATA21	G20	DATA20	H20	DATA18
J01	DAI19	K01	FLAG0	L01	FLAG2	M01	ACK
J02	DAI18	K02	DAI20	L02	FLAG1	M02	FLAG3
J03	GND	K03	GND	L03	V_{DDINT}	M03	GND
J04	GND	K04	V_{DDEXT}	L04	V_{DDINT}	M04	GND

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Table 46. 256-Ball BGA_ED Pin Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
J17	GND	K17	V_{DDINT}	L17	V_{DDINT}	M17	V_{DDEXT}
J18	GND	K18	V_{DDINT}	L18	V_{DDINT}	M18	GND
J19	GND/ID1[2]	K19	GND/ID0[2]	L19	DATA15	M19	DATA12
J20	DATA17	K20	DATA16	L20	DATA14	M20	DATA13
N01	$\overline{\text{RD}}$	P01	SDA10	R01	$\overline{\text{SDWE}}$	T01	SDCKE
N02	SDCLK0	P02	$\overline{\text{WR}}$	R02	$\overline{\text{SDRAS}}$	T02	$\overline{\text{SDCAS}}$
N03	GND	P03	V_{DDINT}	R03	GND	T03	GND
N04	V_{DDEXT}	P04	V_{DDINT}	R04	GND	T04	V_{DDEXT}
N17	GND	P17	V_{DDINT}	R17	V_{DDEXT}	T17	GND
N18	GND	P18	V_{DDINT}	R18	GND	T18	GND
N19	DATA11	P19	DATA8	R19	DATA6	T19	DATA5
N20	DATA10	P20	DATA9	R20	DATA7	T20	DATA4
U01	$\overline{\text{MS0}}$	V01	ADDR22	W01	GND	Y01	GND
U02	$\overline{\text{MS1}}$	V02	ADDR23	W02	ADDR21	Y02	NC
U03	V_{DDINT}	V03	V_{DDINT}	W03	ADDR19	Y03	NC
U04	GND	V04	GND	W04	ADDR20	Y04	ADDR18
U05	V_{DDEXT}	V05	GND	W05	ADDR17	Y05	NC/$\overline{\text{BR1}}$[2]
U06	GND	V06	GND	W06	ADDR16	Y06	NC/$\overline{\text{BR2}}$[2]
U07	V_{DDEXT}	V07	GND	W07	ADDR15	Y07	XTAL
U08	V_{DDINT}	V08	V_{DDINT}	W08	ADDR14	Y08	CLKIN
U09	V_{DDEXT}	V09	GND	W09	A_{VDD}	Y09	NC
U10	GND	V10	GND	W10	A_{VSS}	Y10	NC
U11	V_{DDEXT}	V11	GND	W11	ADDR13	Y11	NC/$\overline{\text{BR3}}$[2]
U12	V_{DDINT}	V12	V_{DDINT}	W12	ADDR12	Y12	NC/$\overline{\text{BR4}}$[2]
U13	V_{DDEXT}	V13	V_{DDEXT}	W13	ADDR10	Y13	ADDR11
U14	V_{DDEXT}	V14	GND	W14	ADDR8	Y14	ADDR9
U15	V_{DDINT}	V15	V_{DDINT}	W15	ADDR5	Y15	ADDR7
U16	V_{DDEXT}	V16	GND	W16	ADDR4	Y16	ADDR6
U17	V_{DDINT}	V17	GND	W17	ADDR1	Y17	ADDR3
U18	V_{DDINT}	V18	GND	W18	ADDR2	Y18	GND
U19	DATA0	V19	DATA1	W19	ADDR0	Y19	GND
U20	DATA2	V20	DATA3	W20	NC	Y20	NC

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[1] The SDCLK1 signal is only available on the SBGA package. SDCLK1 is not available on the LQFP_EP package.
[2] Applies to ADSP-21368 models only.

Figure 47 shows the bottom view of the BGA_ED ball configuration. Figure 48 shows the top view of the BGA_ED ball configuration.

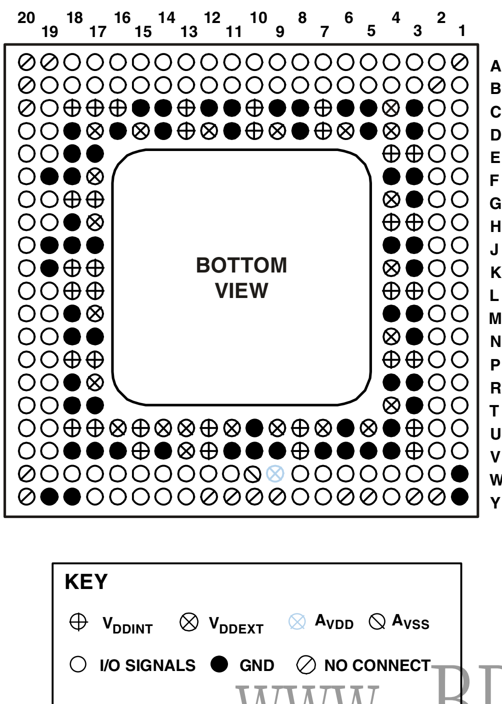

Figure 47. 256-Ball BGA_ED Ball Configuration (Bottom View)

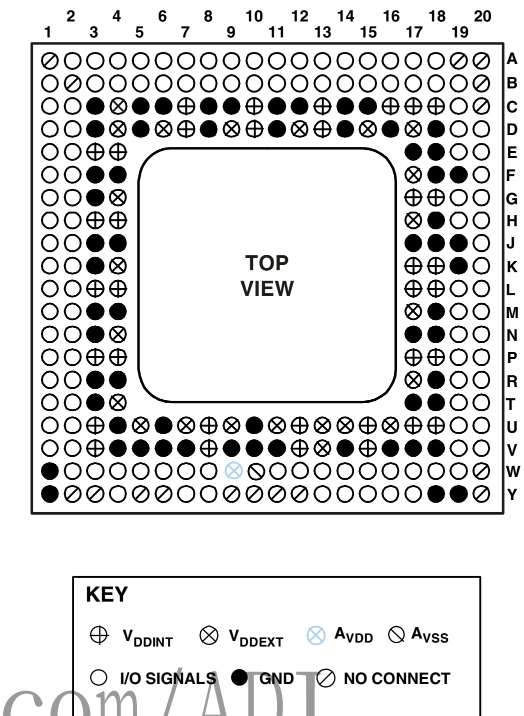

Figure 48. 256-Ball BGA_ED Ball Configuration (Top View)

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208-LEAD LQFP_EP PINOUT

Table 47. 208-Lead LQFP_EP Pin Assignment (Numerically by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	V_{DDINT}	43	V_{DDINT}	85	V_{DDEXT}	127	V_{DDINT}	169	CLK_CFG0
2	DATA28	44	DATA4	86	GND	128	GND	170	BOOT_CFG0
3	DATA27	45	DATA5	87	V_{DDINT}	129	V_{DDEXT}	171	CLK_CFG1
4	GND	46	DATA2	88	ADDR14	130	DAI19	172	$\overline{\text{EMU}}$
5	V_{DDEXT}	47	DATA3	89	GND	131	DAI18	173	BOOT_CFG1
6	DATA26	48	DATA0	90	V_{DDEXT}	132	DAI17	174	TDO
7	DATA25	49	DATA1	91	ADDR15	133	DAI16	175	DAI4
8	DATA24	50	V_{DDEXT}	92	ADDR16	134	DAI15	176	DAI2
9	DATA23	51	GND	93	ADDR17	135	DAI14	177	DAI3
10	GND	52	V_{DDINT}	94	ADDR18	136	DAI13	178	DAI1
11	V_{DDINT}	53	V_{DDINT}	95	GND	137	DAI12	179	V_{DDEXT}
12	DATA22	54	GND	96	V_{DDEXT}	138	V_{DDINT}	180	GND
13	DATA21	55	V_{DDEXT}	97	ADDR19	139	V_{DDEXT}	181	V_{DDINT}
14	DATA20	56	ADDR0	98	ADDR20	140	GND	182	GND
15	V_{DDEXT}	57	ADDR2	99	ADDR21	141	V_{DDINT}	183	DPI14
16	GND	58	ADDR1	100	ADDR23	142	GND	184	DPI13
17	DATA19	59	ADDR4	101	ADDR22	143	DAI11	185	DPI12
18	DATA18	60	ADDR3	102	$\overline{\text{MS1}}$	144	DAI10	186	DPI11
19	V_{DDINT}	61	ADDR5	103	$\overline{\text{MS0}}$	145	DAI8	187	DPI10
20	GND	62	GND	104	V_{DDINT}	146	DAI9	188	DPI9
21	DATA17	63	V_{DDINT}	105	V_{DDINT}	147	DAI6	189	DPI8
22	V_{DDINT}	64	GND	106	GND	148	DAI7	190	DPI7
23	GND	65	V_{DDEXT}	107	V_{DDEXT}	149	DAI5	191	V_{DDEXT}
24	V_{DDINT}	66	ADDR6	108	$\overline{\text{SDCAS}}$	150	V_{DDEXT}	192	GND
25	GND	67	ADDR7	109	$\overline{\text{SDRAS}}$	151	GND	193	V_{DDINT}
26	DATA16	68	ADDR8	110	SDCKE	152	V_{DDINT}	194	GND
27	DATA15	69	ADDR9	111	$\overline{\text{SDWE}}$	153	GND	195	DPI6
28	DATA14	70	ADDR10	112	$\overline{\text{WR}}$	154	V_{DDINT}	196	DPI5
29	DATA13	71	GND	113	SDA10	155	GND	197	DPI4
30	DATA12	72	V_{DDINT}	114	GND	156	V_{DDINT}	198	DPI3
31	V_{DDEXT}	73	GND	115	V_{DDEXT}	157	V_{DDINT}	199	DPI1
32	GND	74	V_{DDEXT}	116	SDCLK0	158	V_{DDINT}	200	DPI2
33	V_{DDINT}	75	ADDR11	117	GND	159	GND	201	$\overline{\text{RESETOUT}}$/CLKOUT
34	GND	76	ADDR12	118	V_{DDINT}	160	V_{DDINT}	202	$\overline{\text{RESET}}$
35	DATA11	77	ADDR13	119	$\overline{\text{RD}}$	161	V_{DDINT}	203	V_{DDEXT}
36	DATA10	78	GND	120	ACK	162	V_{DDINT}	204	GND
37	DATA9	79	V_{DDINT}	121	FLAG3	163	TDI	205	DATA30
38	DATA8	80	AVSS	122	FLAG2	164	$\overline{\text{TRST}}$	206	DATA31
39	DATA7	81	AVDD	123	FLAG1	165	TCK	207	DATA29
40	DATA6	82	GND	124	FLAG0	166	GND	208	V_{DDINT}
41	V_{DDEXT}	83	CLKIN	125	DAI20	167	V_{DDINT}		
42	GND	84	XTAL	126	GND	168	TMS		

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PACKAGE DIMENSIONS

The ADSP-21367/ADSP-21368/ADSP-21369 processors are available in 256-ball RoHS compliant and leaded BGA_ED, and 208-lead RoHS compliant LQFP_EP packages.

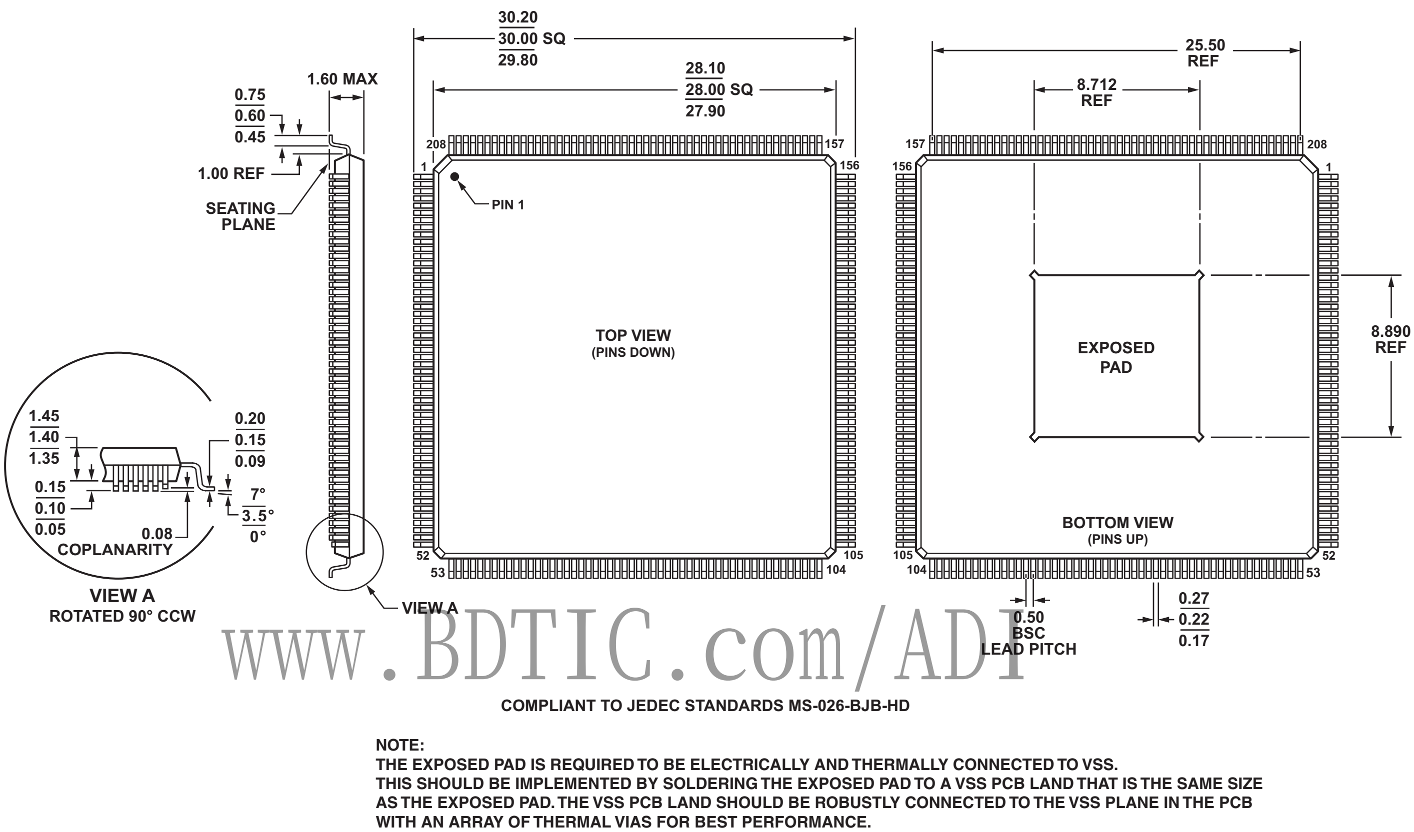

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Figure 49. 208-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]
(SW-208-1)
Dimensions shown in millimeters

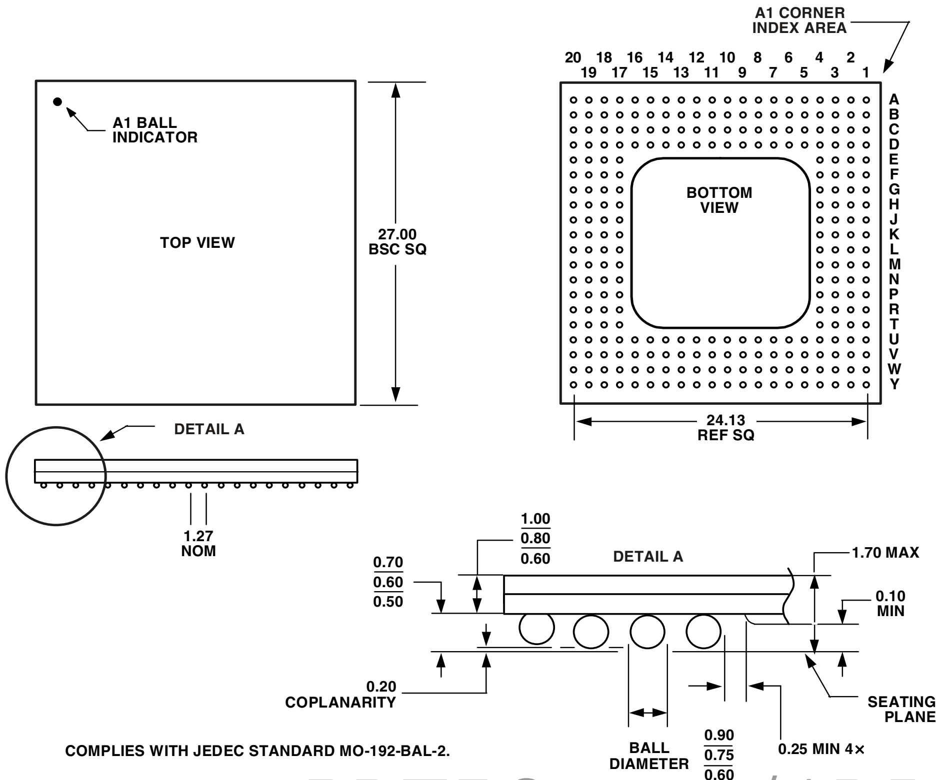

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Figure 50. 256-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-256)
Dimension shown in millimeters

SURFACE-MOUNT DESIGN

Table 48 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 48. BGA_ED Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
256-Lead Ball Grid Array BGA_ED (BP-256)	Solder Mask Defined (SMD)	0.63 mm	0.73 mm

AUTOMOTIVE PRODUCTS

An ADSP-21369 model is available for automotive applications with controlled manufacturing. Note that this special model may have specifications that differ from the general release models.

The automotive grade product shown in Table 49 is available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 49. Automotive Products

Model	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
AD21369WBSWZ1xx	–40°C to +85°C	266 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1

[1] Referenced temperature is ambient temperature.

ORDERING GUIDE

Model	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
ADSP-21367KBP-2A[2]	0°C to +70°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21367KBPZ-2A[2, 3]	0°C to +70°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21367BBP-2A[2]	–40°C to +85°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21367BBPZ-2A[2, 3]	–40°C to +85°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21367KBPZ-3A[2, 3]	0°C to +70°C	400 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21367KSWZ-1A[2, 3]	0°C to +70°C	266 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21367KSWZ-2A[2, 3]	0°C to +70°C	333 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21367KSWZ-4A[2, 3]	0°C to +70°C	350 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21367BSWZ-1A[2, 3]	–40°C to +85°C	266 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21368KBP-2A	0°C to +70°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21368KBPZ-2A[3]	0°C to +70°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21368BBP-2A	–40°C to +85°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21368BBPZ-2A[3]	–40°C to +85°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21368KBPZ-3A[3]	0°C to +70°C	400 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21369KBP-2A	0°C to +70°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21369KBPZ-2A[3]	0°C to +70°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21369BBP-2A	–40°C to +85°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21369BBPZ-2A[2]	–40°C to +85°C	333 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21369KBPZ-3A[3]	0°C to +70°C	400 MHz	2M bit	6M bit	256-Ball BGA_ED	BP-256
ADSP-21369KSWZ-1A[3]	0°C to +70°C	266 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21369KSWZ-2A[3]	0°C to +70°C	333 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21369KSWZ-4A[3]	0°C to +70°C	350 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21369BSWZ-1A[3]	–40°C to +85°C	266 MHz	2M bit	6M bit	208-Lead LQFP_EP	SW-208-1

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[1] Referenced temperature is ambient temperature.
[2] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/SHARC.
[3] Z = RoHS Compliant Part.

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