ANALOG DEVICES

SPI-/I^{2}C-Compatible, Temperature Sensor, 4-Channel ADC and Quad Voltage Output

ADT7516/ADT7517/ADT7519

FEATURES

ADT7516: four 12-bit DACs
ADT7517: four 10-bit DACs
ADT7519: four 8-bit DACs
Buffered voltage output
Guaranteed monotonic by design over all codes
10-bit temperature-to-digital converter
10-bit 4-channel ADC
DC input bandwidth
Input range: 0 V to 2.28 V
Temperature range: −40°C to +120°C
Temperature sensor accuracy: ±0.5°C typ
Supply range: 2.7 V to 5.5 V
DAC output range: 0 V to 2 V$_{REF}$
Power-down current: <10 µA
Internal 2.28 V$_{REF}$ option
Double-buffered input logic
Buffered reference input
Power-on reset to 0 V DAC output
Simultaneous update of outputs (LDAC function)
On-chip, rail-to-rail output buffer amplifier
SPI˚, I^{2}C˚, QSPI™, MICROWIRE™, and DSP compatible
4-wire serial interface
SMBus packet error checking (PEC) compatible
16-lead QSOP package

APPLICATIONS

Portable battery-powered instruments
Personal computers
Smart battery chargers
Telecommunications systems
Electronic text equipment
Domestic appliances
Process control

PIN CONFIGURATION

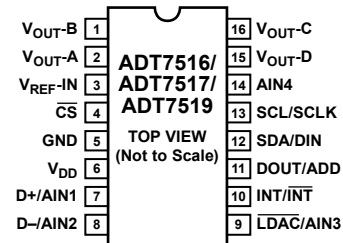|					
V$_{OUT}$-B	1		ADT7516/	16	V$_{OUT}$-C
V$_{OUT}$-A	2		ADT7517/	15	V$_{OUT}$-D
V$_{REF}$-IN	3		ADT7519	14	AIN4
$\overline{CS}$	4			13	SCL/SCLK
GND	5		TOP VIEW (Not to Scale)	12	SDA/DIN
V$_{DD}$	6			11	DOUT/ADD
D+/AIN1	7			10	INT/$\overline{INT}$
D−/AIN2	8			9	$\overline{LDAC}$/AIN3

Figure 1.

GENERAL DESCRIPTION

The ADT7516/ADT7517/ADT7519[1] combine a 10-bit temperature-to-digital converter, a 10-bit 4-channel ADC, and a quad 12-/10-/8-bit DAC, respectively, in a 16-lead QSOP package. The parts also include a band gap temperature sensor and a 10-bit ADC to monitor and digitize the temperature reading to a resolution of 0.25°C.

The ADT7516/ADT7517/ADT7519 operate from a single 2.7 V to 5.5 V supply. The input voltage range on the ADC channels is 0 V to 2.28 V, and the input bandwidth is dc. The reference for the ADC channels is derived internally. The output voltage of the DAC ranges from 0 V to V$_{DD}$, with an output voltage settling time of 7 µs typical.

The ADT7516/ADT7517/ADT7519 provide two serial interface options: a 4-wire serial interface that is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards, and a 2-wire SMBus/I^{2}C interface. They feature a standby mode that is controlled through the serial interface.

The reference for the four DACs is derived either internally or from a reference pin. The outputs of all DACs can be updated simultaneously using the software LDAC function or the external $\overline{LDAC}$ pin. The ADT7516/ADT7517/ADT7519 incorporate a power-on reset circuit, ensuring that the DAC output powers up to 0 V and remains there until a valid write takes place.

The wide supply voltage range, low supply current, and SPI-/I^{2}C-compatible interface of the ADT7516/ADT7517/ADT7519 make them ideal for a variety of applications, including personal computers, office equipment, and domestic appliances.

[1] Protected by U.S. Patent Numbers: 6,169,442; 5,867,012; and 5,764,174. Other patents pending.

ADT7516/ADT7517/ADT7519

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REVISION HISTORY

SPECIFICATIONS

Temperature range is as follows: A version: −40°C to +120°C, V_{DD} = 2.7 V to 5.5 V, GND = 0 V, REF_{IN} = 2.25 V, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
DAC DC PERFORMANCE[2, 3]					
ADT7519					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed monotonic over all codes
ADT7517					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed monotonic over all codes
ADT7516					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSB	
Differential Nonlinearity		±0.02	±0.9	LSB	Guaranteed monotonic over all codes
Offset Error		±0.4	±2	% of FSR	
Gain Error		±0.3	±2	% of FSR	
Lower Deadband		20	65	mV	Lower deadband exists only if offset error is negative, see Figure 40
Upper Deadband		60	100	mV	Upper deadband exists if V_{REF} = V_{DD} and off-set plus gain error is positive, see Figure 41
Offset Error Drift[4]		−12		ppm of FSR/°C	
Gain Error Drift[4]		−5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[4]		−60		dB	$\Delta V_{DD} = \pm10\%$
DC Crosstalk[4]		200		µV	See Figure 5
ADC DC ACCURACY					Maximum V_{DD} = 5 V
Resolution			10	Bits	
Total Unadjusted Error (TUE)		2	3	% of FSR	V_{DD} = 2.7 V to 5.5 V
Total Unadjusted Error (TUE)			2	% of FSR	V_{DD} = 3.3 V ±10%
Offset Error			±0.5	% of FSR	
Gain Error			±2	% of FSR	
ADC BANDWIDTH			DC	Hz	
ANALOG INPUTS					
Input Voltage Range	0		2.28	V	AIN1 to AIN4, C4 = 0 in Control Configuration 3
	0		V_{DD}	V	AIN1 to AIN4, C4 = 0 in Control Configuration 3
DC Leakage Current			±1	µA	
Input Capacitance		5	20	pF	
Input Resistance		10		MΩ	
THERMAL CHARACTERISTICS					
Internal Temperature Sensor					Internal reference used, averaging on
Accuracy @ V_{DD} = 3.3 V ±10%			±1.5	°C	T_A = 85°C
		±0.5	±3	°C	T_A = 0°C to +85°C
		±2	±5	°C	T_A = −40°C to +120°C
Accuracy @ V_{DD} = 5 V ±5%		±2	±3	°C	T_A = 0°C to +85°C
		±3	±5	°C	T_A = −40°C to +120°C
Resolution			10	Bits	Equivalent to 0.25°C
Long-Term Drift		0.25		°C	Drift over 10 years if part is operated at 55°C

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
External Temperature Sensor					External transistor = 2N3906
Accuracy @ V_{DD} = 3.3 V ±10%			±1.5	°C	T_A = 85°C
			±3	°C	T_A = 0°C to +85°C
			±5	°C	T_A = −40°C to +120°C
Accuracy @ V_{DD} = 5 V ±5%		±2	±3	°C	T_A = 0°C to +85°C
		±3	±5	°C	T_A = −40°C to +120°C
Resolution			10	Bits	Equivalent to 0.25°C
Output Source Current		180		µA	High level
		11		µA	Low level
Thermal Voltage Output					
8-Bit DAC Output					
Resolution	1			°C	
Scale Factor		8.97		mV/°C	0 V to V_{REF} output, T_A = −40°C to +120°C
		17.58		mV/°C	0 V to 2 V_{REF} output, T_A = −40°C to +120°C
10-Bit DAC Output					
Resolution	0.25			°C	
Scale Factor		2.2		mV/°C	0 V to V_{REF} output, T_A = −40°C to +120°C
		4.39		mV/°C	0 V to 2 V_{REF} output, T_A = −40°C to +120°C
CONVERSION TIMES					Single channel mode
Slow ADC					
V_{DD}/AIN		11.4		ms	Averaging (16 samples) on
		712		µs	Averaging off
Internal Temperature		11.4		ms	Averaging (16 samples) on
		712		µs	Averaging off
External Temperature		24.22		ms	Averaging (16 samples) on
		1.51		ms	Averaging off
Fast ADC					
V_{DD}/AIN		712		µs	Averaging (16 samples) on
		44.5		µs	Averaging off
Internal Temperature		2.14		ms	Averaging (16 samples) on
		134		µs	Averaging off
External Temperature		14.25		ms	Averaging (16 samples) on
		890		µs	Averaging off
ROUND ROBIN UPDATE RATE[5]					Time to complete one measurement cycle through all channels
Slow ADC @ 25°C					
Averaging On		79.8		ms	AIN1 and AIN2 are selected on Pin 7 and Pin 8
Averaging Off		4.99		ms	AIN1 and AIN2 are selected on Pin 7 and Pin 8
Averaging On		94.76		ms	D+ and D− are selected on Pin 7 and Pin 8
Averaging Off		9.26		ms	D+ and D− are selected on Pin 7 and Pin 8
Fast ADC @ 25°C					
Averaging On		6.41		ms	AIN1 and AIN2 are selected on Pin 7 and Pin 8
Averaging Off		400.84		µs	AIN1 and AIN2 are selected on Pin 7 and Pin 8
Averaging On		21.77		ms	D+ and D− are selected on Pin 7 and Pin 8
Averaging Off		3.07		ms	D+ and D− are selected on Pin 7 and Pin 8
DAC EXTERNAL REFERENCE INPUT[4]					
V_{REF} Input Range	1		V_{DD}	V	Buffered reference
V_{REF} Input Impedance		>10		MΩ	Buffered reference and power-down mode
Reference Feedthrough		−90		dB	Frequency = 10 kHz
Channel-to-Channel Isolation		−75		dB	Frequency = 10 kHz

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
ON-CHIP REFERENCE					
Reference Voltage[4]	2.2662	2.28	2.2938	V	
Temperature Coefficient[4]		80		ppm/°C	
OUTPUT CHARACTERISTICS[4]					
Output Voltage[6]	0.001		$V_{DD} - 0.1$	V	This is a measure of the minimum and maximum drive capability of the output amplifier
DC Output Impedance		0.5		Ω	
Short Circuit Current		25		mA	V_{DD} = 5 V
		16		mA	V_{DD} = 3 V
Power-Up Time		2.5		µs	Coming out of power-down mode, V_{DD} = 5 V
		5		µs	Coming out of power-down mode, V_{DD} = 3.3 V
DIGITAL INPUTS[4]					
Input Current			±1	µA	V_{IN} = 0 V to V_{DD}
V_{IL}, Input Low Voltage			0.8	V	
V_{IH}, Input High Voltage	1.89			V	
Pin Capacitance		3	10	pF	All digital inputs
SCL, SDA Glitch Rejection			50	ns	Input filtering suppresses noise spikes of less than 50 ns
$\overline{LDAC}$ Pulse Width	20			ns	Edge triggered input
DIGITAL OUTPUT					
Digital High Voltage, V_{OH}	2.4			V	I_{SOURCE} = I_{SINK} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 3 mA
Output High Current, I_{OH}			1	mA	V_{OH} = 5 V
Output Capacitance, C_{OUT}			50	pF	
INT/$\overline{INT}$ Output Saturation Voltage			0.8	V	I_{OUT} = 4 mA
I²C TIMING CHARACTERISTICS[7, 8]					
Serial Clock Period, t_1	2.5			µs	Fast mode I²C, see Figure 2
Data In Setup Time to SCL High, t_2	50			ns	
Data Out Stable after SCL Low, t_3	0			ns	See Figure 2
SDA Low Setup Time to SCL Low (Start Condition), t_4	50			ns	See Figure 2
SDA High Hold Time after SCL High (Stop Condition), t_5	50			ns	See Figure 2
SDA and SCL Fall Time, t_6			300	ns	See Figure 2
SDA and SCL Rise Time, t_7			300[9]	ns	See Figure 2
SPI TIMING CHARACTERISTICS[4, 10]					
$\overline{CS}$ to SCLK Setup Time, t_1	0			ns	See Figure 3
SCLK High Pulse Width, t_2	50			ns	See Figure 3
SCLK Low Pulse Width, t_3	50			ns	See Figure 3
Data Access Time after SCLK Falling Edge, t_4[11]			35	ns	
Data Setup Time Prior to SCLK Rising Edge, t_5	20			ns	See Figure 3
Data Hold Time after SCLK Rising Edge, t_6	0			ns	See Figure 3
$\overline{CS}$ to SCLK Hold Time, t_7	0			µs	See Figure 3
$\overline{CS}$ to DOUT High Impedance, t_8			40	ns	See Figure 3
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
V_{DD} Settling Time			50	ms	V_{DD} settles to within 10% of its final voltage level
I_{DD} (Normal Mode)[12]			3	mA	V_{DD} = 3.3 V, V_{IH} = V_{DD}, and V_{IL} = GND
		2.2	3	mA	V_{DD} = 5 V, V_{IH} = V_{DD}, and V_{IL} = GND

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
I$_{DD}$ (Power-Down Mode)			10	µA	V$_{DD}$ = 3.3 V, V$_{IH}$ = V$_{DD}$, and V$_{IL}$ = GND
			10	µA	V$_{DD}$ = 5 V, V$_{IH}$ = V$_{DD}$, and V$_{IL}$ = GND
Power Dissipation			10	mW	V$_{DD}$ = 3.3 V, normal mode
			33	µW	V$_{DD}$ = 3.3 V, shutdown mode

[1] See the Terminology section.
[2] DC specifications are tested with the outputs unloaded.
[3] Linearity is tested using a reduced code range: ADT7516 (Code 115 to 4095); ADT7517 (Code 28 to 1023); ADT7519 (Code 8 to 255).
[4] Guaranteed by design and characterization, not production tested.
[5] Round robin is the continuous sequential measurement of the following channels: V$_{DD}$, internal temperature, external temperature (AIN1, AIN2), AIN3, and AIN4.
[6] For the amplifier output to reach its minimum voltage, the offset error must be negative. For the amplifier output to reach its maximum voltage (V$_{REF}$ = V$_{DD}$), the offset plus gain error must be positive.
[7] The SDA and SCL timing is measured with the input filters turned on to meet the fast mode I²C specification. Switching off the input filters improves the transfer rate but has a negative effect on the EMC behavior of the part.
[8] Guaranteed by design, not production tested. All I²C timing specifications are for fast mode operation but the interface is still capable of handling the slower standard rate specifications.
[9] The interface is also capable of handling the I²C standard mode rise time specification of 1000 ns.
[10] All input signals are specified with tr = tf = 5 ns (10% to 90% of V$_{DD}$), and timed from a voltage level of 1.6 V.
[11] Measured with the load circuit shown in Figure 4.
[12] The I$_{DD}$ specification is valid for all DAC codes and full-scale analog input voltages. Interface inactive. All DACs and ADCs active. Load currents excluded.

DAC AC CHARACTERISTICS

V$_{DD}$ = 2.7 V to 5.5 V, R$_L$ = 4.7 kΩ to GND, C$_L$ = 200 pF to GND, 4.7 kΩ to V$_{DD}$, all specifications T$_{MIN}$ to T$_{MAX}$, unless otherwise noted.

Table 2.

Parameter[1, 2]	Min	Typ[3]	Max	Unit	Conditions/Comments
Output Voltage Settling Time					V$_{REF}$ = V$_{DD}$ = 5 V
ADT7519		6	8	µs	1/4 scale to 3/4 scale change (0x40 to 0xC0)
ADT7517		7	9	µs	1/4 scale to 3/4 scale change (0x100 to 0x300)
ADT7516		8	10	µs	1/4 scale to 3/4 scale change (0x400 to 0xC00)
Slew Rate		0.7		V/µs	
Major-Code Change Glitch Energy		12		nV-s	1 LSB change around major carry
Digital Feedthrough		0.5		nV-s	
Digital Crosstalk		1		nV-s	
Analog Crosstalk		0.5		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		200		kHz	V$_{REF}$ = 2 V ±0.1 V p-p
Total Harmonic Distortion		−70		dB	V$_{REF}$ = 2.5 V ±0.1 V p-p; frequency = 10 kHz

[1] See the Terminology section.
[2] Guaranteed by design and characterization, not production tested.
[3] At 25°C.

TIMING DIAGRAMS

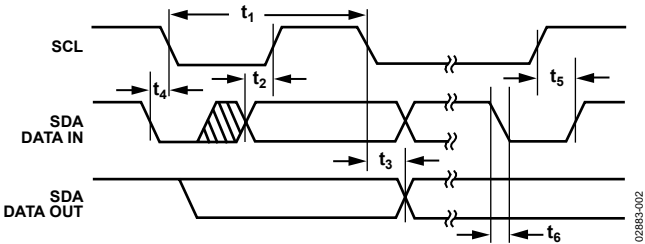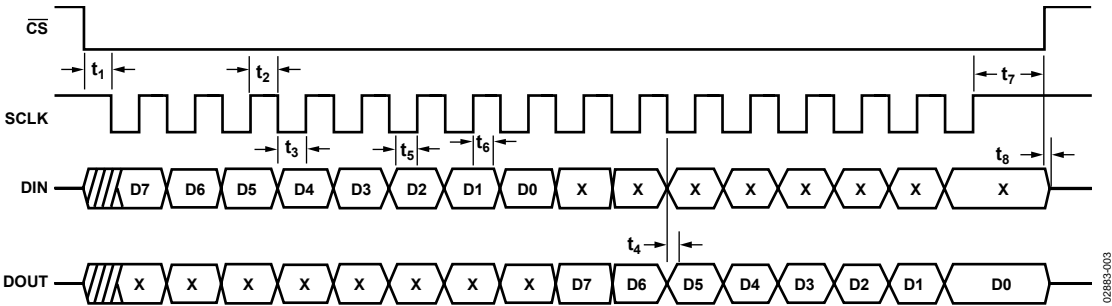

Figure 2. I²C Bus Timing Diagram
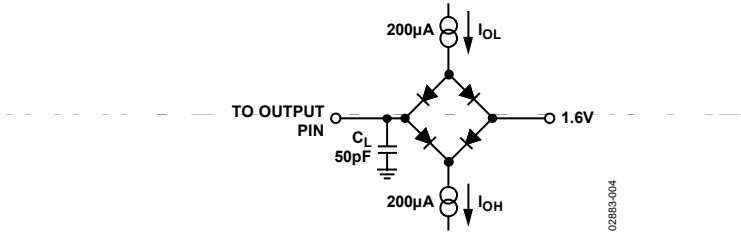

Figure 3. SPI Bus Timing Diagram

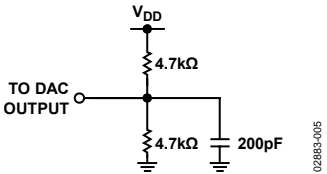Figure 4. Load Circuit for Access Time and Bus Relinquish Time

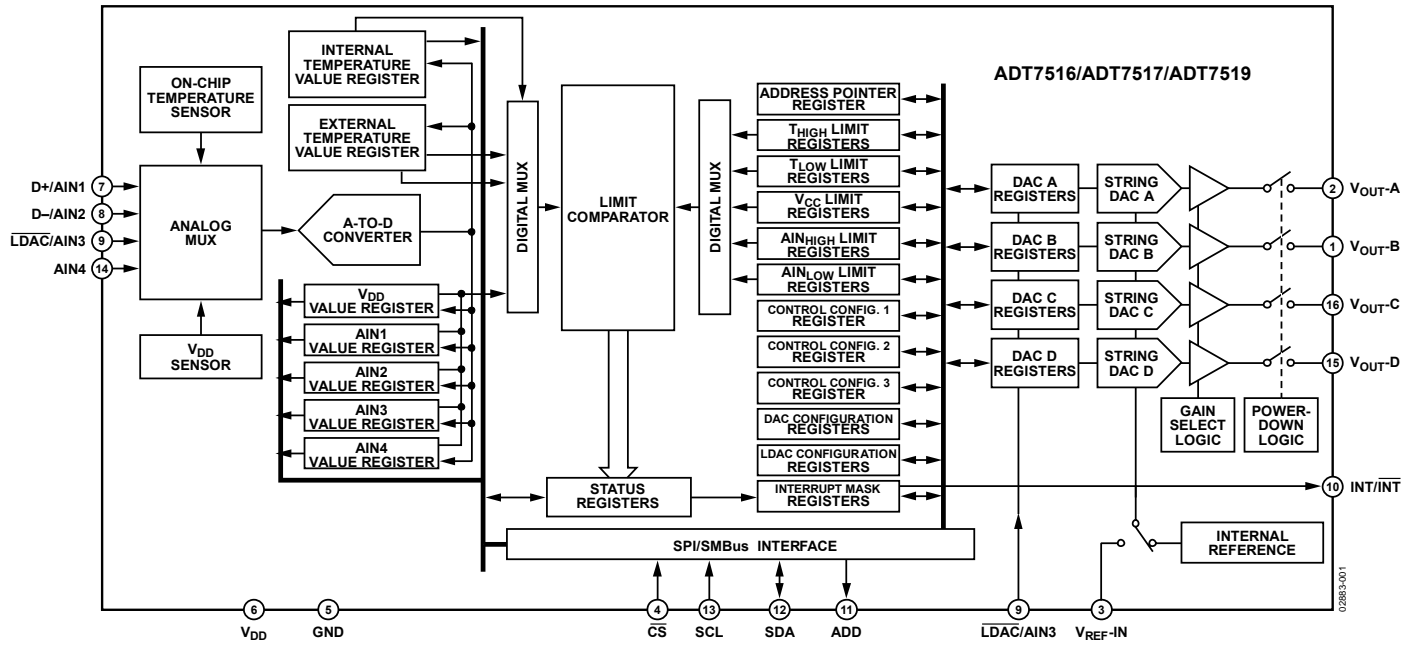Figure 5. Load Circuit for DAC Outputs

FUNCTIONAL BLOCK DIAGRAM

Figure 6. Functional Block Diagram for the ADT7516/ADT7517/ADT7519

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +120°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation[1]	$(T_J$ max − $T_A)/\theta_{JA}$
Thermal Impedance[2]	
θ_{JA} Junction-to-Ambient	105.44°C/W
θ_{JC} Junction-to-Case	38.8°C/W
IR Reflow Soldering	
Peak Temperature	220°C (0°C/5°C)
Time at Peak Temperature	10 sec to 20 sec
Ramp-Up Rate	3°C/sec maximum
Ramp-Down Rate	−6°C/sec maximum
Time 25°C to Peak Temperature	6 min maximum
IR Reflow Soldering (Pb-Free Package)	
Peak Temperature	260°C (+0°C)
Time at Peak Temperature	20 sec to 40 sec
Ramp-Up Rate	3°C/sec maximum
Ramp-Down Rate	−6°C/sec maximum
Time 25°C to Peak Temperature	8 min maximum

[1] Values relate to the package being used on a 4-layer board.
[2] Junction-to-case resistance is applicable to components featuring a preferential flow direction, for example, components mounted on a heat sink. Junction-to-ambient resistance is more useful for air cooled PCB-mounted components.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. I²C Address Selection

ADD Pin	I²C Address
Low	1001 000
Float	1001 010
High	1001 011

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
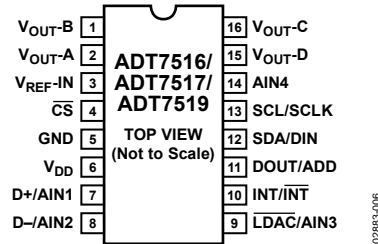
PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

Figure 7. Pin Configuration (QSOP Package)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}-B	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
2	V_{OUT}-A	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
3	V_{REF}-IN	Reference Input Pin for All Four DACs. This input is buffered and has an input range from 1 V to V_{DD}.
4	$\overline{CS}$	SPI Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{CS}$ goes low, it enables the input register, and data is transferred in on the rising edges and out on the falling edges of the subsequent serial clocks. It is recommended that this pin be tied high to V_{DD} when operating the serial interface in I²C mode.
5	GND	Ground Reference Point. Ground reference point for all circuitry on the part. Analog and digital ground.
6	V_{DD}	Positive Supply Voltage, 2.7 V to 5.5 V. The supply should be decoupled to ground.
7	D+/AIN1	D+: Positive Connection to External Temperature Sensor. AIN1: Analog Input. Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
8	D−/AIN2	D−: Negative Connection to External Temperature Sensor. AIN2: Analog Input. Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
9	$\overline{LDAC}$/AIN3	$\overline{LDAC}$: Active Low Control Input. Transfers the contents of the input registers to their respective DAC registers. A falling edge on this pin forces any or all DAC registers to be updated if the input registers have new data. A minimum pulse width of 20 ns must be applied to the $\overline{LDAC}$ pin to ensure proper loading of a DAC register. This allows simultaneous update of all DAC outputs. Bit C3 of the Control Configuration 3 register enables the $\overline{LDAC}$ pin. Default is with the $\overline{LDAC}$ pin controlling the loading of the DAC registers. AIN3: Analog Input. Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
10	INT/$\overline{INT}$	Over Limit Interrupt. The output polarity of this pin can be set to give an active low or active high interrupt when temperature, V_{DD}, or AIN limits are exceeded. The default is active low. Open-drain output, needs a pull-up resistor.
11	DOUT/ADD	DOUT: SPI Serial Data Output. Logic output. Data is clocked out of any register at this pin. Data is clocked out on the falling edge of SCLK. Open-drain output, needs a pull-up resistor. ADD: I²C Serial Bus Address Selection Pin. Logic input. A low on this pin gives the Address 1001 000; leaving it floating gives the Address 1001 010; and setting it high gives the address 1001 011. The I²C address set up by the ADD pin is not latched by the device until after this address has been sent twice. On the eighth SCL cycle of the second valid communication, the serial bus address is latched in. Any subsequent change on this pin has no effect on the I²C serial bus address.
12	SDA/DIN	SDA: I²C Serial Data Input/Output. I²C serial data to be loaded into the registers of the part and read from these registers is provided on this pin. Open-drain configuration, needs a pull-up resistor. DIN: SPI Serial Data Input. Serial data to be loaded into the part's registers is provided on this pin. Data is clocked into a register on the rising edge of SCLK. Open-drain configuration, needs a pull-up resistor.
13	SCL/SCLK	Serial Clock Input. This is the clock input for the serial port. The serial clock is used to clock data out of any register of the ADT7516/ADT7517/ADT7519, and also to clock data into any register that can be written to. Open-drain configuration, needs a pull-up resistor.
14	AIN4	Analog Input. Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
15	V_{OUT}-D	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
16	V_{OUT}-C	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.

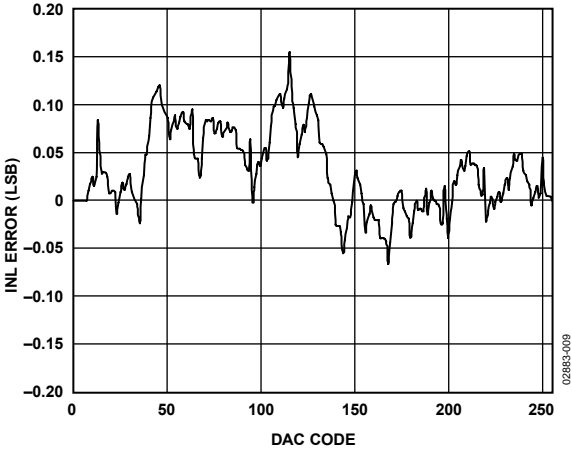# TYPICAL PERFORMANCE CHARACTERISTICS

Figure 8. ADT7519 Typical DAC INL Plot
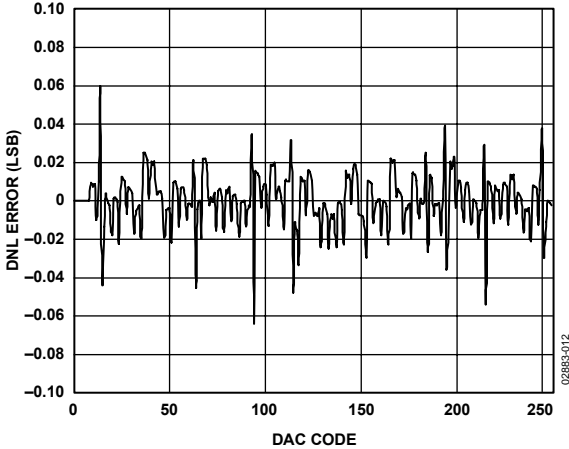
Figure 11. ADT7519 Typical DAC DNL Plot
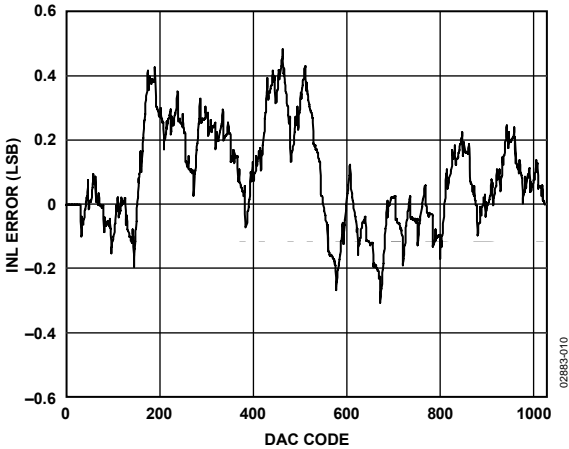
Figure 9. ADT7517 Typical DAC INL Plot
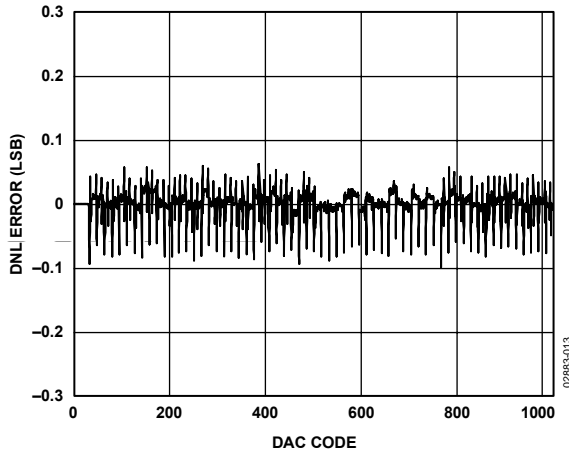
Figure 12. ADT7517 Typical DAC DNL Plot
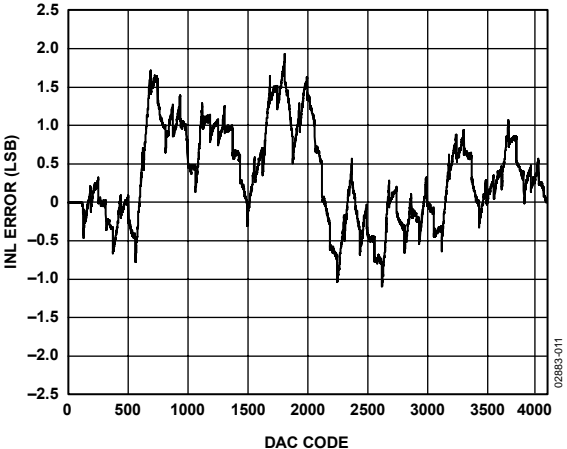
Figure 10. ADT7516 Typical DAC INL Plot
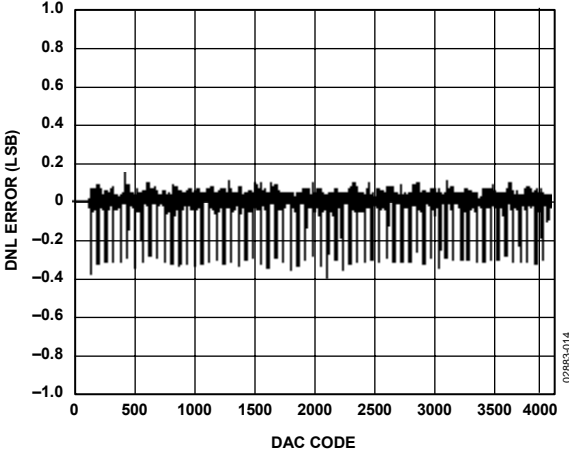
Figure 13. ADT7516 Typical DAC DNL Plot
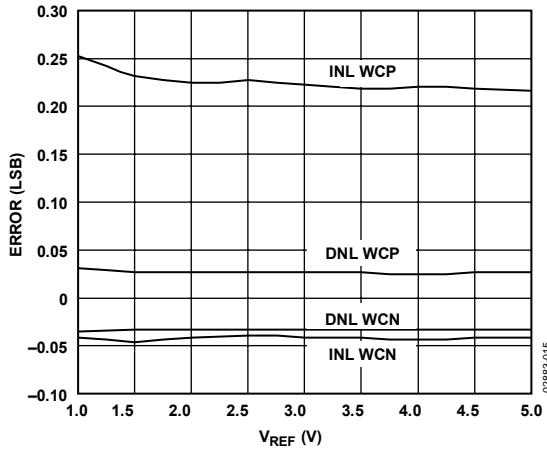
Figure 14. ADT7519 DAC INL and DNL Error vs. V_{REF}
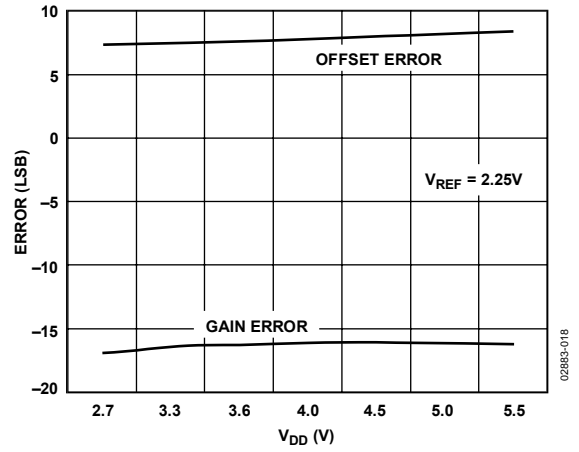
Figure 17. DAC Offset Error and Gain Error vs. V_{DD}
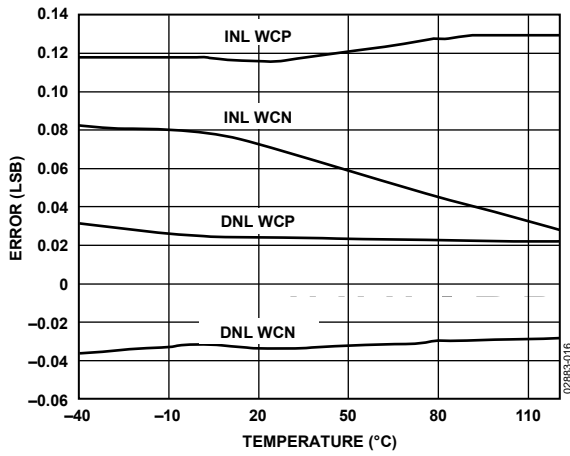
Figure 15. ADT7519 DAC INL Error and DNL Error vs. Temperature
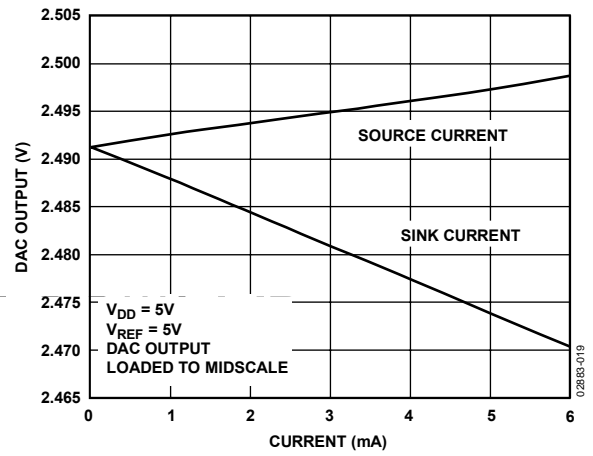
Figure 18. DAC V_{OUT} Source and Sink Current Capability
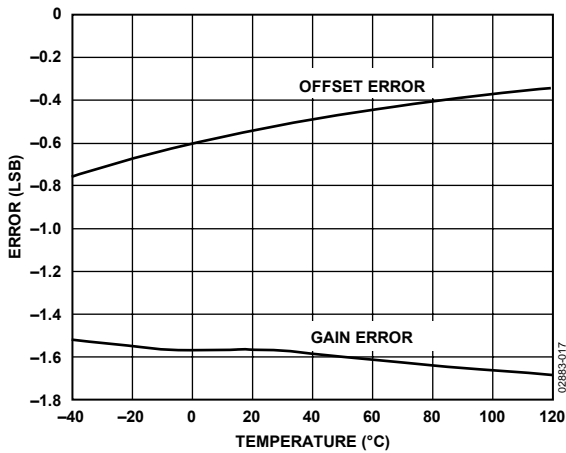
Figure 16. DAC Offset Error and Gain Error vs. Temperature
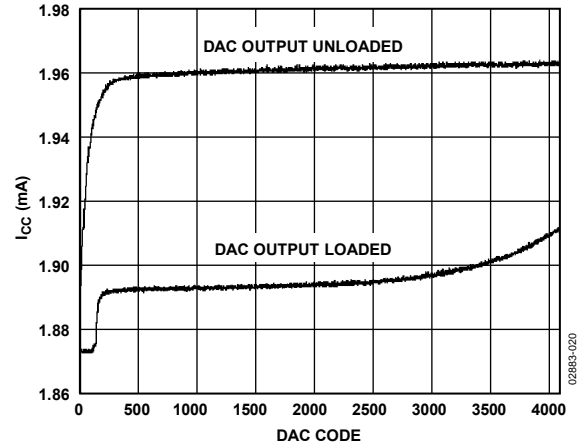
Figure 19. Supply Current vs. DAC Code
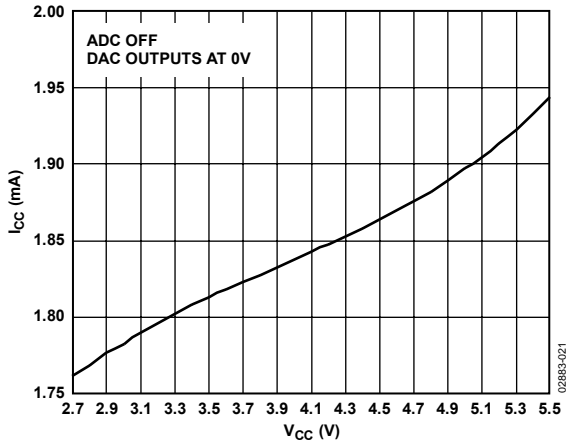
Figure 20. Supply Current vs. Supply Voltage @ 25℃

Figure 21. Power-Down Current vs. Supply Voltage @ 25℃

Figure 22. DAC Half-Scale Settling (1/4 to 3/4 Scale Code Change)

Figure 23. Exiting Power-Down to Midscale

Figure 24. ADT7516 DAC Major Code Transition Glitch Energy;
011…11 to 100…00
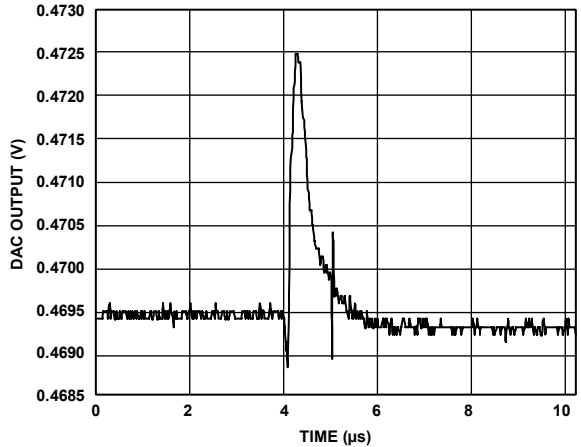
Figure 25. ADT7516 DAC Major Code Transition Glitch Energy;
100…00 to 011…11
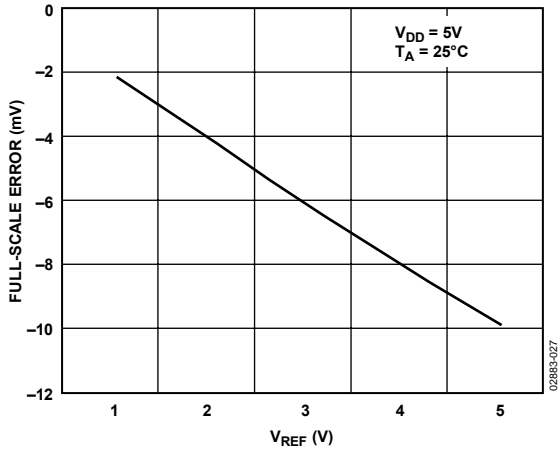
Figure 26. DAC Full-Scale Error vs. V_REF

Figure 27. DAC-to-DAC Crosstalk

Figure 28. ADC INL with V_REF = V_DD (3.3 V)

Figure 29. PSRR vs. Supply Ripple Frequency

Figure 30. Internal Temperature Error @ 3.3 V and 5 V
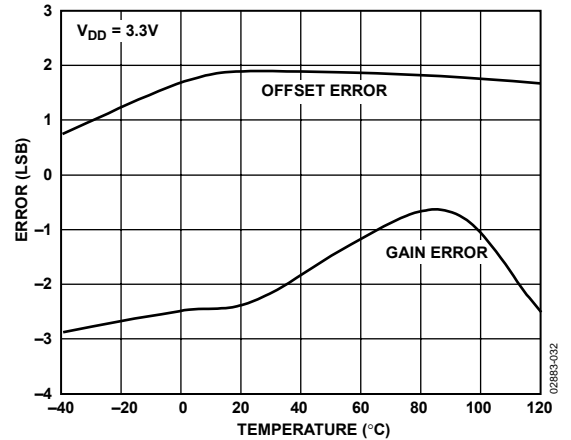
Figure 31. ADC Offset Error and Gain Error vs. Temperature
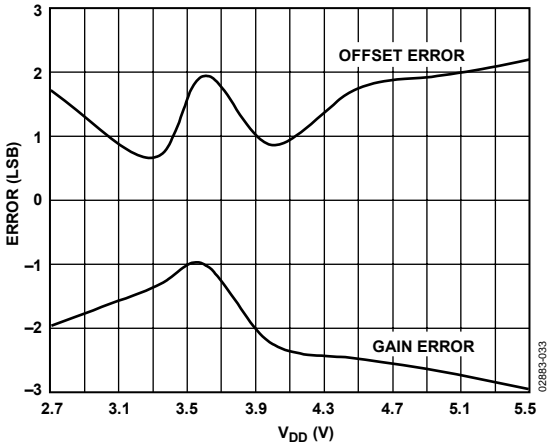
Figure 32. ADC Offset Error and Gain Error vs. V_DD
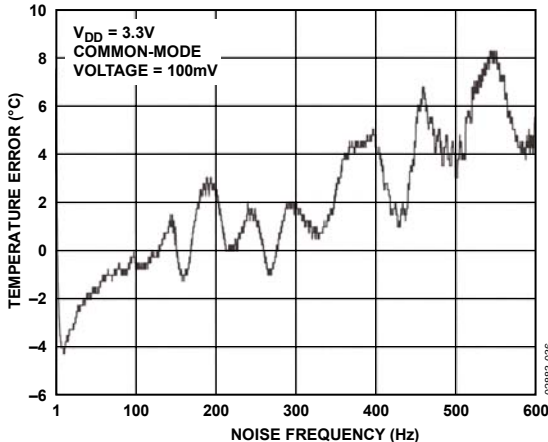
Figure 35. External Temperature Error vs. Common-Mode Noise Frequency
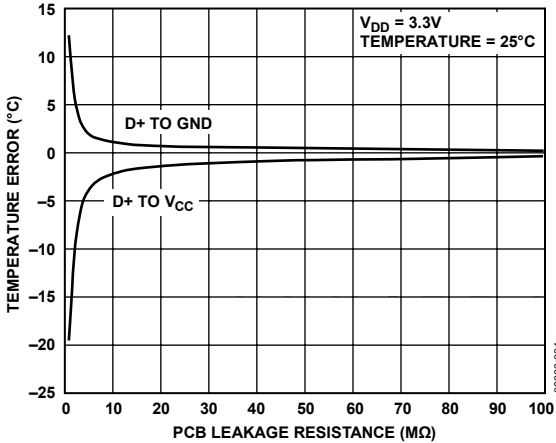
Figure 33. External Temperature Error vs. PCB Leakage Resistance
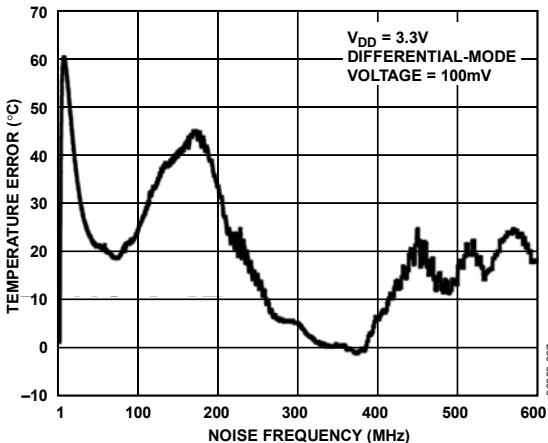
Figure 36. External Temperature Error vs. Differential-Mode Noise Frequency
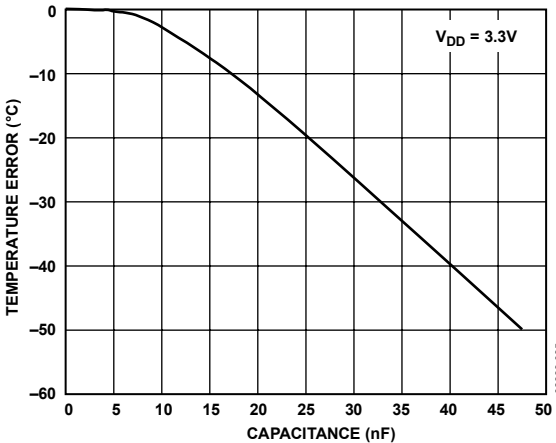
Figure 34. External Temperature Error vs. Capacitance Between D+ and D–
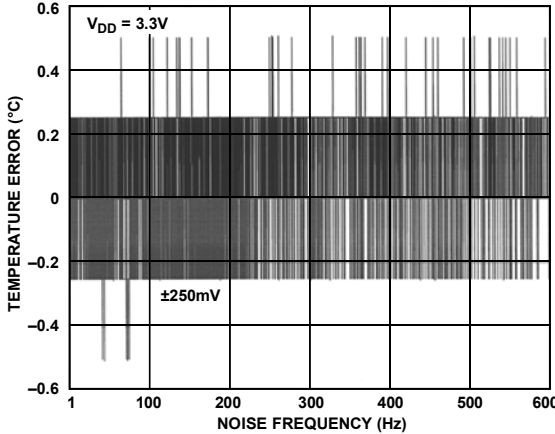
Figure 37. Internal Temperature Error vs. Power Supply Noise Frequency
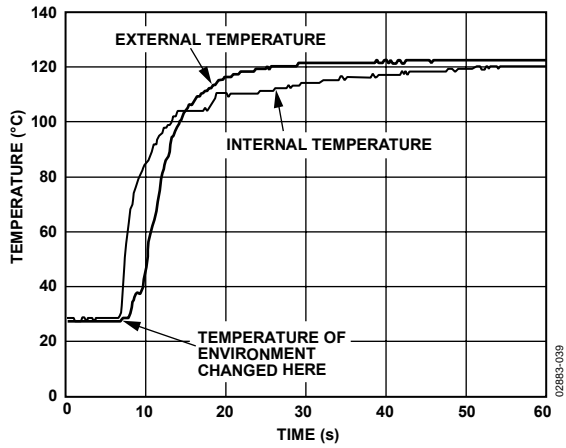
Figure 38. Temperature Sensor Response to Thermal Shock
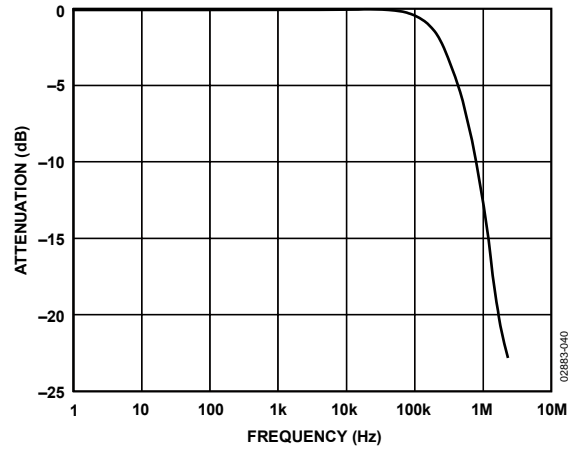
Figure 39. DAC Multiplying Bandwidth (Small Signal Frequency Response)

TERMINOLOGY

Relative Accuracy

Relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the transfer function. Typical INL vs. code plots are shown in Figure 8, Figure 9, and Figure 10.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±0.9 LSB maximum ensures monotonicity. Typical DAC DNL vs. code plots can be seen in Figure 11, Figure 12, and Figure 13.

Total Unadjusted Error (TUE)

Total unadjusted error is a comprehensive specification that includes the sum of the relative accuracy error, gain error, and offset error under a specified set of conditions.

Offset Error

Offset error is a measure of the offset error of the DAC and the output amplifier (see Figure 40 and Figure 41). It can be negative or positive, and it is expressed in mV.

Offset Error Match

Offset error match is the difference in offset error between any two channels.

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

Gain Error Match

Gain error match is the difference in gain error between any two channels.

Offset Error Drift

Offset error drift is a measure of the change in offset error with changes in temperature. It is expressed in ppm of full-scale range/°C.

Gain Error Drift

Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in ppm of full-scale range/°C.

Long-Term Temperature Drift

Long-term temperature drift is a measure of the change in temperature error with the passage of time. It is expressed in °C. The concept of long-term stability has been used for many years to describe the amount an IC parameter shifts during its lifetime. This is a concept that has typically been applied to both voltage references and monolithic temperature sensors.

Unfortunately, integrated circuits cannot be evaluated at room temperature (25°C) for 10 years or so to determine this shift. Manufacturers perform accelerated lifetime testing of integrated circuits by operating ICs at elevated temperatures (between 125°C and 150°C) over a shorter period (typically between 500 hours and 1000 hours). As a result, the lifetime of an integrated circuit is significantly accelerated due to the increase in rates of reaction within the semiconductor material.

DC Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in μV.

Reference Feedthrough

Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, LDAC is high). It is expressed in dB.

Channel-to-Channel Isolation

Channel-to-channel isolation is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in dB.

Major Code Transition Glitch Energy

Major code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device. However, it is measured when the DAC is not being written to. It is specified in nV-s and is measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s or vice versa.

Digital Crosstalk

Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk

Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{LDAC}$ high. Then pulse $\overline{LDAC}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{LDAC}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth

The multiplying bandwidth is a measure of the finite bandwidth of the amplifiers within the DAC. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output, expressed in dB.

Round Robin

The term round robin is used to describe the ADT7516/ADT7517/ ADT7519 cycling through the available measurement channels in sequence, taking a measurement on each channel.

DAC Output Settling Time

DAC output settling time is the time required, following a prescribed data change, for the output of a DAC to reach and remain within ±0.5 LSB of the final value. A typical prescribed change is from 1/4 scale to 3/4 scale.

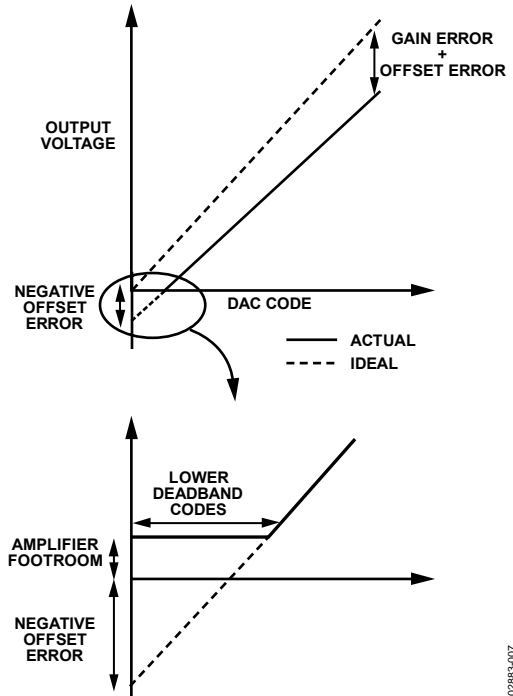Figure 40. DAC Transfer Function with Negative Offset

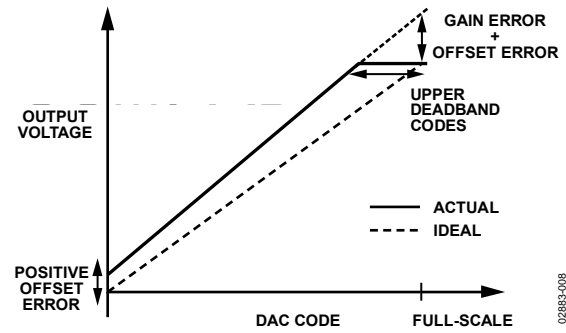Figure 41. DAC Transfer Function with Positive Offset ($V_{REF} = V_{DD}$)

THEORY OF OPERATION

Directly after the power-up calibration routine, the ADT7516/ADT7517/ADT7519 go into idle mode. In this mode, the devices are not performing any measurements and are fully powered up. All four DAC outputs are at 0 V.

To begin monitoring, write to the Control Configuration 1 register (Address 0x18) and set Bit C0 = 1. The ADT7516/ADT7517/ADT7519 go into the power-up default measurement mode (round robin). The devices proceed to take measurements on the V_{DD} channel, internal temperature sensor channel, external temperature sensor channel (AIN1 and AIN2), AIN3, and finally AIN4. After they finish taking measurements on the AIN4 channel, the devices immediately loop back to start taking measurements on the V_{DD} channel and repeat the same cycle as before. This loop continues until the monitoring is stopped by resetting Bit C0 of the Control Configuration 1 register to 0.

It is also possible to continue monitoring as well as switching to single-channel mode by writing to the Control Configuration 2 register (Address 0x19) and setting Bit C4 = 1. Further explanation of the single-channel and round robin measurement modes is given in later sections. All measurement channels have averaging enabled on them at power-up. Averaging forces the devices to take an average of 16 readings before giving a final measured result. To disable averaging and consequently decrease the conversion time by a factor of 16, set Bit C5 = 1 in the Control Configuration 2 register.

There are four single-ended analog input channels on the ADT7516/ADT7517/ADT7519, AIN1 to AIN4. AIN1 and AIN2 are multiplexed with the external temperature sensor terminals (D+ and D−). Bit C1 and Bit C2 of the Control Configuration 1 register (Address 0x18) are used to select between AIN1/AIN2 and the external temperature sensor. The input range on the analog input channels is dependent on whether the ADC reference used is the internal V_{REF} or V_{DD}. To meet linearity specifications, it is recommended that the maximum V_{DD} value is 5 V. Bit C4 of the Control Configuration 3 register be used to select between the internal reference and V_{DD} as the ADC reference of the analog inputs.

Controlling the DAC outputs can be done by writing to the MSB and LSB registers of the DAC (Address 0x10 to Address 0x17). The power-up default setting is to have a low going pulse on the LDAC pin (Pin 9) controlling the updating of the DAC outputs from the DAC registers. Alternatively, one can configure the updating of the DAC outputs to be controlled by means other than the LDAC pin by setting Bit C3 = 1 of the Control Configuration 3 register (Address 0x1A). The DAC configuration register (Address 0x1B) and the LDAC configuration register (Address 0x1C) can now be used to control the DAC updating. These two registers also control the output range of the DACs and select between the internal or external reference.

DAC A and DAC B outputs can be configured to give a voltage output proportional to the temperature of the internal and external temperature sensors, respectively.

The dual serial interface defaults to the I²C protocol on power-up. To select and lock in the SPI protocol, follow the selection process as described in the Serial Interface Selection section. The I²C protocol cannot be locked in, though the SPI protocol is automatically locked in on selection. The interface can be switched back to be I²C on selection when the device is powered off and on. When using I²C, the CS pin should be tied to either V_{DD} or GND.

There are a number of different operating modes on the ADT7516/ADT7517/ADT7519 devices and all of them can be controlled by the configuration registers. These features consist of enabling and disabling interrupts, polarity of the INT/INT pin, enabling and disabling the averaging on the measurement channels SMBus timeout, and software reset.

POWER-UP CALIBRATION

It is recommended that no communication to the part be initiated until approximately 5 ms after V_{DD} has settled to within 10% of its final value. It is generally accepted that most systems take a maximum of 50 ms to power up. Power-up time is directly related to the amount of decoupling on the voltage supply line.

During the 5 ms after V_{DD} has settled, the part is performing a calibration routine. Any communication to the device during calibration interrupts this routine, and can cause erroneous temperature measurements. If it is not possible to have V_{DD} at its nominal value by the time 50 ms has elapsed or if communication to the device has started prior to V_{DD} settling, it is recommended that a measurement be taken on the V_{DD} channel before a temperature measurement is taken. The V_{DD} measurement is used to calibrate out any temperature measurement error due to different supply voltage values.

CONVERSION SPEED

The internal oscillator circuit used by the ADC has the capability to output two different clock frequencies. This means that the ADC is capable of running at two different speeds when doing a conversion on a measurement channel. Thus, the time taken to perform a conversion on a channel can be reduced by setting Bit C0 of the Control Configuration 3 register (Address 0x1A). This increases the ADC clock speed from 1.4 kHz to 22 kHz. At the higher clock speed, the analog filters on the D+ and D− input pins (external temperature sensors) are switched off. This is why the power-up default setting is to have the ADC working at the slow speed. The typical times for fast and slow ADC speeds are given in the Specifications section.

The ADT7516/ADT7517/ADT7519 power up with averaging on. This means every channel is measured 16 times and internally averaged to reduce noise. The conversion time can also be sped up by turning off the averaging. This is done by setting Bit C5 of the Control Configuration 2 register (Address 0x19) to 1.

FUNCTION DESCRIPTION—VOLTAGE OUTPUT

Digital-to-Analog Converters

The ADT7516/ADT7517/ADT7519 have four resistor string DACs fabricated on a CMOS process with resolutions of 12, 10, and 8 bits, respectively. They contain four output buffer amplifiers and are written to via I²C serial interface or SPI serial interface. See the Serial Interface section for more information.

The ADT7516/ADT7517/ADT7519 operate from a single supply of 2.7 V to 5.5 V, and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/μs. All four DACs share a common reference input, V_{REF}-IN. The reference input is buffered to draw virtually no current from the reference source because it offers the source a high impedance input. The devices have a power-down mode to completely turn off all DACs with a high impedance output.

Each DAC output is not updated until it receives the LDAC command. Therefore, though the DAC registers would have been written to with a new value, this value is not represented by a voltage output until the DACs receive the LDAC command. Reading back from any DAC register prior to issuing an LDAC command results in the digital value that corresponds to the DAC output voltage. Thus, the digital value written to the DAC register cannot be read back until after the LDAC command has been initiated. This LDAC command can be given by either pulling the $\overline{LDAC}$ pin low (falling edge loads DACs), setting up Bit D4 and Bit D5 of the DAC configuration register (Address 0x1B), or using the LDAC register (Address 0x1C).

When using the $\overline{LDAC}$ pin to control the DAC register loading, the low going pulse width should be 20 ns minimum. The $\overline{LDAC}$ pin has to go high and low again before the DAC registers can be reloaded.

Digital-to-Analog Section

The architecture of one DAC channel consists of a resistor string DAC followed by an output buffer amplifier. The voltage at the V_{REF}-IN pin or the on-chip reference of 2.28 V provides the reference voltage for the corresponding DAC. Figure 42 shows a block diagram of the DAC architecture. Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:
D = decimal equivalent of the binary code that is loaded to the DAC register

0 to 255 for ADT7519 (8 bits)
0 to 1023 for ADT7517 (10 bits)
0 to 4095 for ADT7516 (12 bits)

N = DAC resolution.

Resistor String

The resistor string section is shown in Figure 43. It is simply a string of resistors, each of approximately 603 Ω. The digital code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.
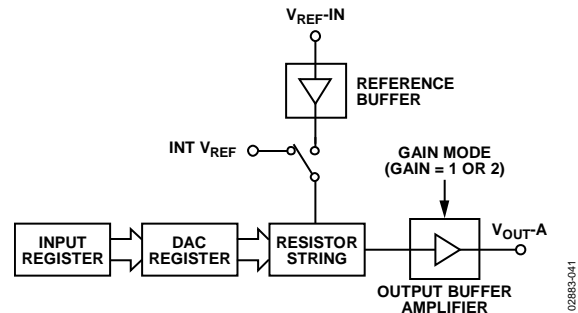
Figure 42. Single DAC Channel Architecture
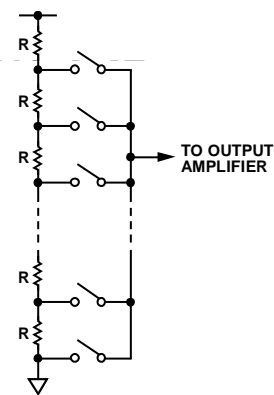
Figure 43. Resistor String
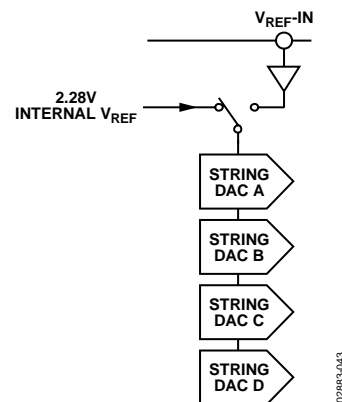
Figure 44. DAC Reference Buffer Circuit

DAC Reference Inputs

There is an input reference pin for the DACs. This reference input is buffered (see Figure 44).

The advantage of the buffered input is the high impedance it presents to the voltage source driving it. The user can have an external reference voltage as low as 1 V and as high as V_{DD}. The restriction of 1 V is due to the footroom of the reference buffer.

The $\overline{LDAC}$ configuration register controls the option to select between internal and external voltage references. The default selection is external reference.

Output Amplifier

The output buffer amplifier can generate output voltages to within 1 mV of either rail. Its actual range depends on the value of V_{REF}, gain, and offset error.

If a gain of 1 is selected (Bit 0 to Bit 3 of the DAC configuration register = 0), the output range is 0.001 V to V_{REF}.

If a gain of 2 is selected (Bit 0 to Bit 3 of the DAC configuration register = 1), the output range is 0.001 V to 2 V_{REF}. Because of clamping, however, the maximum output is limited to $V_{DD} - 0.001$ V.

The output amplifier can drive a load of 4.7 kΩ to GND or V_{DD}, in parallel with 200 pF to GND or V_{DD} (see Figure 5). The source and sink capabilities of the output amplifier can be seen in the plot of Figure 18.

The slew rate is 0.7 V/μs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6 μs.

Thermal Voltage Output

The ADT7516/ADT7517/ADT7519 can output voltages that are proportional to temperature. DAC A output can be configured to represent the temperature of the internal sensor and the DAC B output can be configured to represent the external temperature sensor. Bit C5 and Bit C6 of the Control Configuration 3 register select the temperature proportional output voltage. Each time a temperature measurement is taken, the DAC output is updated. The output resolution for the ADT7519 is 8 bits with 1°C change corresponding to 1 LSB change. The output resolution for the ADT7516 and ADT7517 is capable of 10 bits with 0.25°C change

corresponding to 1 LSB change. The default output resolution for the ADT7516 and ADT7517 is 8 bits. To increase this to 10 bits, set C1 = 1 in the Control Configuration 3 register. The default output range is 0 V to V_{REF} and this can be increased to 0 V to 2 V_{REF}. Increasing the output voltage span to 2 V_{REF} can be done by setting D0 = 1 for DAC A (internal temperature sensor) and D1 = 1 for DAC B (external temperature sensor) in the DAC configuration register (Address 0x1B).

The output voltage is capable of tracking a maximum temperature range of −128°C to +127°C, but the default setting is −40°C to +127°C. If the output voltage range is 0 V to V_{REF}-IN (V_{REF}-IN = 2.25 V), then this corresponds to 0 V representing −40°C, and 1.48 V representing +127°C. This, of course, gives an upper deadband between 1.48 V and V_{REF}.

The internal and external analog temperature offset registers can be used to vary this upper deadband and, consequently, the temperature that 0 V corresponds to. Table 6 and Table 7 give examples of how this is done using a DAC output voltage span of V_{REF} and 2 V_{REF}, respectively. Simply write in the temperature value, in twos complement format, at which 0 V is to start. For example, if using the DAC A output and 0 V to start at −40°C, program 0xD8 into the internal analog temperature offset register (Address 0x21). This is an 8-bit register and has a temperature offset resolution of only 1°C for all device models. Use Equation 1 to Equation 4 to determine the value to program into the offset registers.

Table 6. Thermal Voltage Output (0 V to V_{REF})

O/P Voltage (V)	Default °C	Max °C	Sample °C
0	−40	−128	0
0.5	+17	−71	+56
1	+73	−15	+113
1.12	+87	−1	+127
1.47	+127	+39	UDB[1]
1.5	UDB[1]	+42	UDB[1]
2	UDB[1]	+99	UDB[1]
2.25	UDB[1]	+127	UDB[1]

[1] Upper deadband has been reached. DAC output is not capable of increasing. See Figure 41.
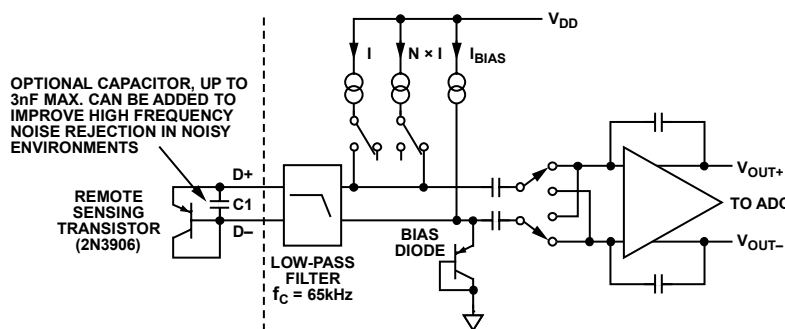
Figure 45. Signal Conditioning for External Diode Temperature Sensor
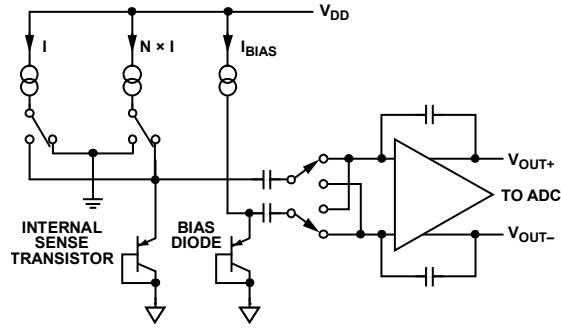
Figure 46. Top Level Structure of Internal Temperature Sensor

Table 7. Thermal Voltage Output (0 V to 2 V_{REF})

O/P Voltage (V)	Default °C	Max °C	Sample °C
0	−40	−128	0
0.25	−26	−114	+14
0.5	+12	−100	+28
0.75	+3	−85	+43
1	+17	−71	+57
1.12	+23	−65	+63
1.47	+43	−45	+83
1.5	+45	−43	+85
2	+73	−15	+113
2.25	+88	0	+127
2.5	+102	+14	UDB[1]
2.75	+116	+28	UDB[1]
3	UDB[1]	+42	UDB[1]
3.25	UDB[1]	+56	UDB[1]
3.5	UDB[1]	+70	UDB[1]
3.75	UDB[1]	+85	UDB[1]
4	UDB[1]	+99	UDB[1]
4.25	UDB[1]	+113	UDB[1]
4.5	UDB[1]	+127	UDB[1]

[1] Upper deadband has been reached. DAC output is not capable of increasing. See Figure 41.

For negative temperatures,

$$Offset\ Register\ Code\ (d) = (0\ V\ Temp) + 128 \quad (1)$$

where D7 of *Offset Register Code* is set to 1 for negative temperatures.

For example,

$$Offset\ Register\ Code\ (d) = −40 + 128 = 88d = 0x58$$

Since a negative temperature has been inserted into the equation, DB7 (MSB) of the offset register code is set to 1. Therefore, 0x58 becomes 0xD8.

$$0x58 + DB7(1) = 0xD8$$

For positive temperatures,

$$Offset\ Register\ Code\ (d) = 0\ V\ Temp \quad (2)$$

For example,

$$Offset\ Register\ Code\ (d) = 10d = 0x0A$$

The following equation is used to work out the various temperatures for the corresponding 8-bit DAC output:

$$8\text{-}Bit\ Temp = (DAC\ O/P)/1\ LSB + (0\ V\ Temp) \quad (3)$$

For example, if the output is 1.5 V, V_{REF}-IN = 2.25 V, 8-bit DAC has an LSB size = 2.25 V/256 = 8.79×10^{-3}, and 0 V temp is at −128°C, then the resultant temperature is

$$1.5/(8.79 \times 10^{-3}) + (−128) = +43°C$$

The following equation is used to work out the various temperatures for the corresponding 10-bit DAC output:

$$10\text{-}Bit\ Temp = [(DAC\ O/P)/1\ LSB] \times 0.25 + (0\ V\ Temp) \quad (4)$$

For example, if the output is 0.4991 V, V_{REF}-IN = 2.25 V, 10-bit DAC has an LSB size = 2.25 V/1024 = 2.197×10^{-3}, and 0 V temperature is at −40°C, then the resulting temperature is

$$[0.4991/(2.197 \times 10^{-3})] \times 0.25 + (−40) = +16.75°C$$

Figure 47 shows a graph of the DAC output vs. temperature for a V_{REF}-IN = 2.25 V.
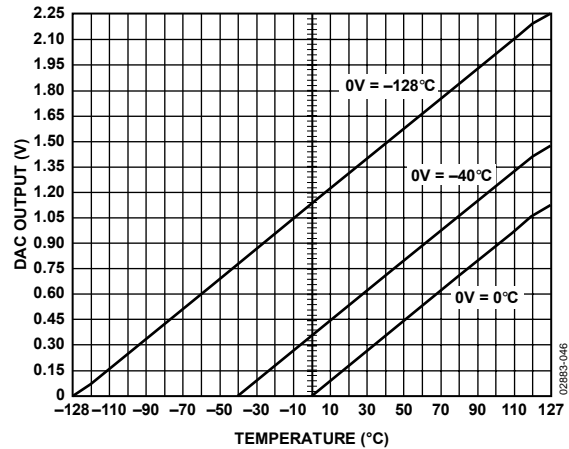
Figure 47. DAC Output vs. Temperature V_{REF}-IN = 2.25 V

FUNCTIONAL DESCRIPTION—ANALOG INPUTS

Single-Ended Inputs

The ADT7516/ADT7517/ADT7519 offer four single-ended analog input channels. The analog input range is from 0 V to 2.28 V, or 0 V to V_{DD}. To maintain the linearity specification, it is recommended that the maximum V_{DD} value be set at 5 V. Selection between the two input ranges is done by Bit C4 of the Control Configuration 3 register (Address 0x1A). Setting this bit to 0 sets up the analog input ADC reference to be sourced from the internal voltage reference of 2.28 V. Setting the bit to 1 sets up the ADC reference to be sourced from V_{DD}.

The ADC resolution is 10 bits and is mostly suitable for dc input signals. Bits[C1:C2] of the Control Configuration 1 register (Address 0x18) are used to set up Pin 7 and Pin 8 as AIN1 and AIN2. Figure 48 shows the overall view of the 4-channel analog input path.
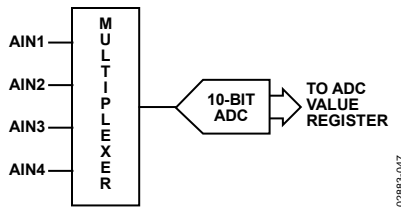
Figure 48. Quad Analog Input Path

Converter Operation

The analog input channels use a successive approximation ADC based on a capacitor DAC. Figure 49 and Figure 50 show simplified schematics of the ADC. Figure 49 shows the ADC during acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on AIN.
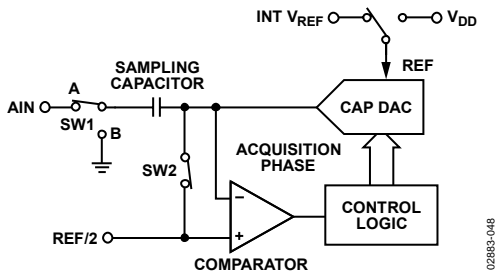
Figure 49. ADC Acquisition Phase
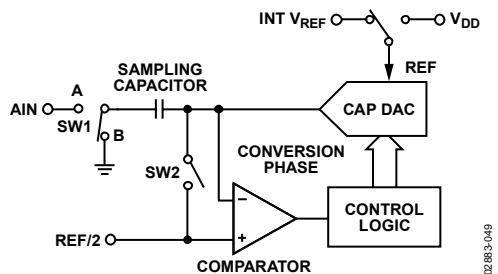
Figure 50. ADC Conversion Phase

When the ADC eventually goes into conversion phase (see Figure 50), SW2 opens and SW1 moves to Position B, causing

the comparator to become unbalanced. The control logic and the DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 51 shows the ADC transfer function for the analog inputs.

ADC TRANSFER FUNCTION

The output coding of the ADT7516/ADT7517/ADT7519 analog inputs is straight binary. The designed code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSB). The LSB is $V_{DD}/1024$ or internal $V_{REF}/1024$, internal V_{REF} = 2.28 V. The ideal transfer characteristic is shown in Figure 51.
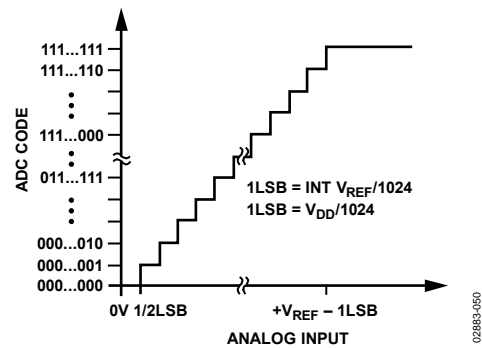
Figure 51. Single-Ended Transfer Function

To work out the voltage on any analog input channel, the following method can be used:

1 LSB = reference (V)/1024

Convert value read back from AIN value register into decimal.

AIN voltage = AIN value (d) × LSB size

where d = decimal.

For example, if internal reference is used, V_{REF} = 2.28 V. AIN value = 512d

1 LSB size = 2.28 V/1024 = 2.226×10^{-3}

AIN voltage = $512 \times 2.226 \times 10^{-3}$ = 1.14 V

Analog Input ESD Protection

Figure 52 shows the input structure on any of the analog input pins that provide ESD protection. The diode provides the main ESD protection for the analog inputs. Care must be taken that the analog input signal never drops below the GND rail by more than 200 mV. If this happens, the diode becomes forward-biased and starts conducting current into the substrate. The 4 pF capacitor is the typical pin capacitance and the resistor is a lumped component made up of the on resistance of the multiplexer switch.
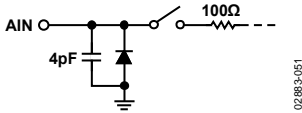
Figure 52. Equivalent Analog Input ESD Circuit

AIN Interrupts

The measured results from the AIN inputs are compared with the AIN V_{HIGH} (greater than comparison) and V_{LOW} (less than or equal to comparison) limits. An interrupt occurs if the AIN inputs exceed or equal the limit registers. These voltage limits are stored in on-chip registers. Note that the limit registers are 8 bits long and the AIN conversion result is 10 bits long. If the voltage limits are not masked out, then any out-of-limit comparisons generate flags that are stored in the Interrupt Status 1 register (Address = 0x00) and one or more out-of-limit results cause the INT/$\overline{INT}$ output to pull either high or low depending on the output polarity setting. It is good design practice to mask out interrupts for channels that are of no concern to the application. Figure 53 shows the interrupt structure for the ADT7516/ ADT7517/ADT7519. It gives a block diagram representation of how the various measurement channels affect the INT/$\overline{INT}$ pin.
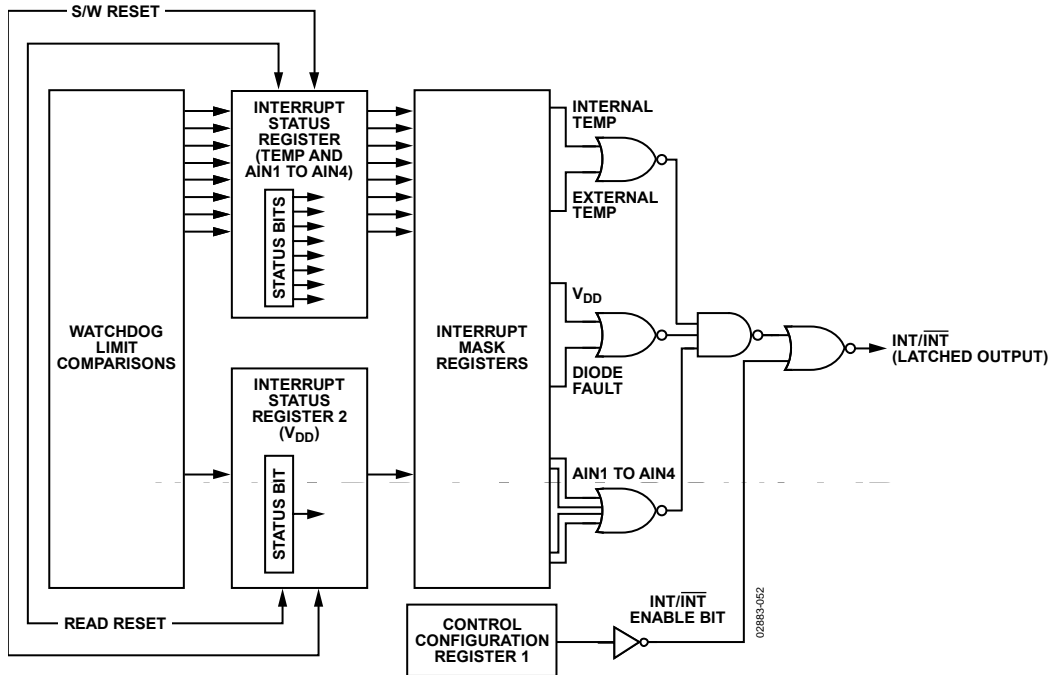
Figure 53. ADT7516/ADT7517/ADT7519 Interrupt Structure

FUNCTIONAL DESCRIPTION—MEASUREMENT

Temperature Sensor

The ADT7516/ADT7517/ADT7519 contain an ADC with special input signal conditioning to enable operation with external and on-chip diode temperature sensors. When the ADT7516/ADT7517/ADT7519 operate in single-channel mode, the ADC continually processes the measurement taken on one channel only. This channel is preselected by Bits[C0:C2] in the Control Configuration 2 register (Address 0x19). When in round robin mode, the analog input multiplexer sequentially selects the V_{DD} input channel, the on-chip temperature sensor to measure its internal temperature, either the external tempera-ture sensor or AIN1 and AIN2, AIN3, and then AIN4. These signals are digitized by the ADC and the results are stored in the various value registers.

The measured results from the temperature sensors are com-pared with the internal and external T_{HIGH} and T_{LOW} limits. These temperature limits are stored in on-chip registers. If the temperature limits are not masked, any out-of-limit comparisons generate flags that are stored in the Interrupt Status 1 register. One or more out-of-limit results cause the INT/$\overline{INT}$ output to pull either high or low depending on the output polarity setting.

Theoretically, the temperature measuring circuit can measure temperatures from −128°C to +127°C with a resolution of 0.25°C. However, temperatures outside T_A are outside the guaranteed operating temperature range of the device. Temperature measurement from −128°C to +127°C is possible using an external sensor.

Temperature measurement is initiated by three methods. The first method is applicable when the part is in single-channel measurement mode. The temperature is measured 16 times and internally averaged to reduce noise. In single-channel mode, the part is continuously monitoring the selected channel, that is, as soon as one measurement is taken another one is started on the same channel. The total time to measure a temperature channel with the ADC operating at slow speed is typically 11.4 ms (712 μs × 16) for the internal temperature sensor and 24.22 ms (1.51 ms × 16) for the external temperature sensor. The new temperature value is stored in two 8-bit registers and is ready for reading by the I²C or SPI interface. The user has the option of disabling the averaging by setting Bit 5 in the Control Configuration 2 register (Address 0x19). The ADT7516/ADT7517/ADT7519 default on power-up is with averaging enabled.

The second method is applicable when the part is in round robin measurement mode. The part measures both the internal and external temperature sensors as it cycles through all possible measurement channels. The two temperature channels are measured each time the part runs a round robin sequence. In round robin mode, the part is continuously measuring all channels.

Temperature measurement is also initiated after every read or write to the part when the part is in either single-channel measurement mode or round robin measurement mode.

Once serial communication has started, any conversion in progress stops and the ADC resets. Conversion restarts immediately after the serial communication has finished. The temperature measurement proceeds normally as described above.

V_{DD} Monitoring

The ADT7516/ADT7517/ADT7519 also have the ability to monitor their own power supply. The part measures the voltage on its V_{DD} pin to a resolution of 10 bits. The resulting value is stored in two 8-bit registers; the two LSBs are stored in register Address 0x03 and the eight MSBs are stored in register Address 0x06. This allows the option of doing just a 1-byte read if 10-bit resolution is not important. The measured result is compared with the V_{HIGH} and V_{LOW} limits. If the V_{DD} interrupt is not masked, any out-of-limit comparison generates a flag in the Interrupt Status 2 register and one or more out-of-limit results cause the INT/$\overline{INT}$ output to pull either high or low, depending on the output polarity setting.

Measuring the voltage on the V_{DD} pin is regarded as monitoring a channel along with the internal, external, and AIN channels. The user can select the V_{DD} channel for single-channel measurement by setting Bit C4 = 1 and setting Bits[C0:C2] to all 0s in the Control Configuration 2 register.

When measuring the V_{DD} value, the reference for the ADC is sourced from the internal reference. Table 8 shows the data format. As the maximum measurable V_{DD} voltage is 7 V, internal scaling is performed on the V_{DD} voltage to match the 2.28 V internal reference value. Following is an example of how the transfer function works:

V_{DD} = 5 V

ADC Reference = 2.28 V

1 LSB = ADC Reference/2^{10}
= 2.28/1024
= 2.226 mV

Scale Factor = Full-Scale V_{CC}/ADC Reference
= 7/2.28
= 3.07

Conversion Result = V_{DD}/(Scale Factor × LSB size)
= 5/(3.07 × 2.226 mV)
= 0x2DC

Table 8. V_{DD} Data Format (V_{REF} = 2.28 V)

V_{DD} Value (V)	Digital Output	
	Binary	Hex
2.7	01 1000 1011	18B
3	01 1011 0111	1B7
3.5	10 0000 0000	200
4	10 0100 1001	249
4.5	10 1001 0010	292
5	10 1101 1100	2DC
5.5	11 0010 0101	325
6	11 0110 1110	36E
6.5	11 1011 0111	3B7
7	11 1111 1111	3FF

On-Chip Reference

The ADT7516/ADT7517/ADT7519 have an on-chip 1.2 V band gap reference that is gained up by a switched capacitor amplifier to give an output of 2.28 V. The amplifier is powered up for the duration of the device monitoring phase and is powered down once monitoring is disabled. This saves on current consumption. The internal reference is used as the reference for the ADC. The ADC is used for measuring V_{DD}, internal temperature sensor, external temperature sensor, and AIN inputs. The internal reference is always used when measuring V_{DD}, and the internal and external temperature sensors. The external reference is the default power-up reference for the DACs.

Round Robin Measurement

On power-up, the ADT7516/ADT7517/ADT7519 go into round robin mode, but monitoring is disabled. Setting Bit C0 of the Control Configuration 1 register to 1 enables conversions. It sequences through all the available channels, taking a measurement from each in the following order: V_{DD}, internal temperature sensor, external temperature sensor (AIN1 and AIN2), AIN3, and AIN4. Pin 7 and Pin 8 can be configured to be either external temperature sensor pins or standalone analog input pins. Once conversion is completed on the AIN4 channel, the device loops around for another measurement cycle. This method of taking a measurement on all the channels in one cycle is called round robin. Setting Bit C4 of Control Configuration 2 (Address 0x19) disables the round robin mode and in turn sets up the single-channel mode. In single-channel mode, only one channel (for example, the internal temperature sensor) is measured in each conversion cycle.

The time taken to monitor all channels is normally not of interest, because the most recently measured value can be read at any time. For applications where the round robin time is important, typical times at 25°C are given in the Specifications section.

Single Channel Measurement

Setting C4 of the Control Configuration 2 register enables the single channel mode and allows the ADT7516/ADT7517/ADT7519 to focus on one channel only. A channel is selected by writing to Bits[C0:C2] in the Control Configuration 2 register. For example, to select the V_{DD} channel for monitoring, write to the Control Configuration 2 register and set C4 to 1 (if not done so already), then write all 0s to Bits[C0:C2]. All subsequent conversions are done on the V_{DD} channel only. To change the channel selection to the internal temperature channel, write to the Control Configuration 2 register and set C0 = 1. When measuring in single channel mode, conversions on the channel selected occur directly after each other. Any communication to the ADT7516/ADT7517/ADT7519 stops the conversions, but they are restarted once the read or write operation is completed.

Temperature Measurement Method

Internal Temperature Measurement

The ADT7516/ADT7517/ADT7519 contain an on-chip band gap temperature sensor whose output is digitized by the on-chip ADC. The temperature data is stored in the internal temperature value register. Because both positive and negative temperatures can be measured, the temperature data is stored in twos complement format, as shown in Table 9. The thermal characteristics of the measurement sensor can change and, therefore, an offset is added to the measured value to enable the transfer function to match the thermal characteristics. This offset is added before the temperature data is stored. The offset value used is stored in the internal temperature offset register.

External Temperature Measurement

The ADT7516/ADT7517/ADT7519 can measure the temperature of one external diode sensor or diode-connected transistor.

The forward voltage of a diode or diode connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about −2 mV/°C. Unfortunately, because the absolute value of V_{BE} varies from device to device, and individual calibration is required to null this out, the technique is unsuitable for mass production.

The technique used in the ADT7516/ADT7517/ADT7519 is to measure the change in V_{BE} when the device is operated at two different currents. This is given by

$$\Delta V_{BE} = kT/q \times \ln(N)$$

where:

k is Boltzmann's constant.
q is the charge on the carrier.
T is the absolute temperature in kelvins.
N is the ratio of the two currents.

Figure 45 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors, but it can equally well be a discrete transistor.

If a discrete transistor is used, the collector is not grounded, and should be linked to the base. If a PNP transistor is used, the base is connected to the D− input and the emitter to the D+

input. If an NPN transistor is used, the emitter is connected to the D− input and the base to the D+ input.

A 2N3906 is recommended as the external transistor.

To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D− input. As the sensor is operating in a noisy environment, C1 is provided as a noise filter. See the Layout Considerations section for more information on C1.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a low-pass filter to remove noise, then to a chopper stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10-bit twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

Layout Considerations

Digital boards can be electrically noisy environments and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

- Place the ADT7516/ADT7517/ADT7519 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses, and CRTs are avoided, this distance can be 4 inches to 8 inches.

- Route the D+ and D− tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks, if possible.

- Use wide tracks to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended.
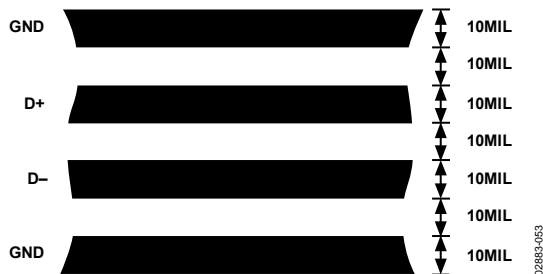
Figure 54. Arrangement of Signal Tracks

- Try to minimize the number of copper/solder joints because they can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D− path and are at the same temperature.

  Thermocouple effects should not be a major problem because 1°C corresponds to about 240 μV, and thermocouple voltages are about 3 μV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 mV.

- Place 0.1 μF bypass and 2200 pF input filter capacitors close to the ADT7516/ADT7517/ADT7519.

- If the distance to the remote sensor is more than 8 inches, the use of twisted-pair cable is recommended. This works up to about 6 feet to 12 feet.

- For long distances (up to 100 feet), use shielded twisted-pair cable, such as Belden® #8451 microphone cable. Connect the twisted pair to D+ and D− and the shield to GND, close to the ADT7516/ADT7517/ADT7519. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor can be reduced or removed.

Cable resistance can also introduce errors. Series resistance of 1 Ω introduces about 0.5°C error.

Temperature Value Format

One LSB of the ADC corresponds to 0.25°C. The ADC can theoretically measure a temperature span of 255°C. The internal temperature sensor is guaranteed to a low value limit of −40°C. It is possible to measure the full temperature span using the external temperature sensor. The temperature data format is shown in Table 9.

The result of the internal or external temperature measurements is stored in the temperature value registers, and is compared with limits programmed into the internal or external high and low registers.

**Table 9. Temperature Data Format
(Internal and External Temperature)**

Temperature	Digital Output
−40°C	11 0110 0000
−25°C	11 1001 1100
−10°C	11 1101 1000
−0.25°C	11 1111 1111
0°C	00 0000 0000
+0.25°C	00 0000 0001
+10°C	00 0010 1000
+25°C	00 0110 0100
+50°C	00 1100 1000
+75°C	01 0010 1100
+100°C	01 1001 0000
+105°C	01 1010 0100
+125°C	01 1111 0100

Temperature conversion formula:

$Positive\ Temperature = ADC\ Code/4$

$Negative\ Temperature = (ADC\ Code - 512)/4$

where DB9 is removed from the *ADC Code* in the *Negative Temperature* equation.

Interrupts

The measured results from the internal temperature sensor, external temperature sensor, V_{DD} pin, and AIN inputs are compared with the T_{HIGH}/V_{HIGH} (greater than comparison) and T_{LOW}/V_{LOW} (less than or equal to comparison) limits. An interrupt occurs if the measurement exceeds or equals the limit registers. These limits are stored in on-chip registers. Note that the limit registers are 8 bits long and the conversion results are 10 bits long. If the limits are not masked, any out-of-limit comparisons generate flags that are stored in the Interrupt Status 1 register (Address 0x00) and Interrupt Status 2 register (Address 0x01). One or more out-of-limit results cause the INT/$\overline{INT}$ output to pull either high or low depending on the output polarity setting. It is good design practice to mask out interrupts for channels that are of no concern to the application.

Figure 53 shows the interrupt structure for the ADT7516/ADT7517/ADT7519. It gives a block diagram representation of how the various measurement channels affect the INT/$\overline{INT}$ pin.

ADT7516/ADT7517/ADT7519 REGISTERS

The ADT7516/ADT7517/ADT7519 contain registers that are used to store the results of external and internal temperature measurements, V_{DD} value measurements, analog input measurements, high and low temperature limits, supply voltage and analog input limits, set output DAC voltage levels, configure multipurpose pins, and generally to control the device. A description of these registers follows.

The register map is divided into registers of 8 bits. Each register has its own individual address, but some consist of data that is linked with other registers. These registers hold the 10-bit

conversion results of measurements taken on the temperature, V_{DD}, and AIN channels. For example, the eight MSBs of the V_{DD} measurement are stored in Register Address 0x06 and the two LSBs are stored in Register Address 0x03. These types of registers are linked so that when the LSB register is read first, the MSB registers associated with that LSB register are locked to prevent any updates. To unlock these MSB registers, the user only has to read any one of them; this has the effect of unlocking all previously locked MSB registers. Therefore, for the preceding example, if Register 0x03 is read first, MSB Register 0x06 and Register 0x07 would be locked to prevent any updates to them. If Register 0x06 is read, this register and Register 0x07 would be subsequently unlocked.
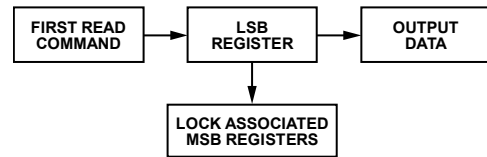
Figure 55. Phase 1 of 10-Bit Read
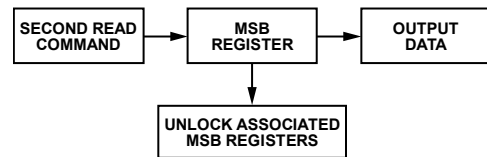
Figure 56. Phase 2 of 10-Bit Read

If an MSB register is read first, its corresponding LSB register is not locked, leaving the user with the option of just reading back 8 bits (MSB) of a 10-bit conversion result. Reading an MSB register first does not lock other MSB registers, and likewise, reading an LSB register first does not lock other LSB registers.

Table 10. ADT7516/ADT7517/ADT7519 Registers

R/W Address	Name	Power-On Default
0x00	Interrupt Status 1	0x00
0x01	Interrupt Status 2	0x00
0x02	Reserved	
0x03	Internal Temp and V_{DD} LSBs	0x00
0x04	External Temp and AIN1 to AIN4 LSBs	0x00
0x05	Reserved	0x00
0x06	V_{DD} MSBs	No default value
0x07	Internal Temp MSBs	0x00
0x08	External Temp MSBs/AIN1 MSBs	0x00
0x09	AIN2 MSBs	0x00
0x0A	AIN3 MSBs	0x00
0x0B	AIN4 MSBs	0x00
0x0C to 0x0F	Reserved	0x00
0x10	DAC A LSBs (ADT7516/ADT7517 Only)	0x00
0x11	DAC A MSBs	0x00
0x12	DAC B LSBs (ADT7516/ADT7517 Only)	0x00
0x13	DAC B MSBs	0x00

R/W Address	Name	Power-On Default
0x14	DAC C LSBs (ADT7516/ADT7517 only)	0x00
0x15	DAC C MSBs	0x00
0x16	DAC D LSBs (ADT7516/ADT7517 only)	0x00
0x17	DAC D MSBs	0x00
0x18	Control Configuration 1	0x00
0x19	Control Configuration 2	0x00
0x1A	Control Configuration 3	0x00
0x1B	DAC Configuration	0x00
0x1C	LDAC Configuration	0x00
0x1D	Interrupt Mask 1	0x00
0x1E	Interrupt Mask 2	0x00
0x1F	Internal Temp Offset	0x00
0x20	External Temp Offset	0x00
0x21	Internal Analog Temp Offset	0xD8
0x22	External Analog Temp Offset	0xD8
0x23	V_{DD} V_{HIGH} Limit	0xC7
0x24	V_{DD} V_{LOW} Limit	0x62
0x25	Internal T_{HIGH} Limit	0x64
0x26	Internal T_{LOW} Limit	0xC9
0x27	External T_{HIGH}/AIN1 V_{HIGH} Limits	0xFF
0x28	External T_{LOW}/AIN1 V_{LOW} Limits	0x00
0x29 to 0x2A	Reserved	
0x2B	AIN2 V_{HIGH} Limit	0xFF
0x2C	AIN2 V_{LOW} Limit	0x00
0x2D	AIN3 V_{HIGH} Limit	0xFF
0x2E	AIN3 V_{LOW} Limit	0x00
0x2F	AIN4 V_{HIGH} Limit	0xFF
0x30	AIN4 V_{LOW} Limit	0x00
0x31 to 0x4C	Reserved	
0x4D	Device ID	0x03/0x0B/0x07
0x4E	Manufacturer's ID	0x41
0x4F	Silicon Revision	Check register for current silicon revision
0x50 to 0x7E	Reserved	0x00
0x7F	SPI Lock Status	0x00
0x80 to 0xFF	Reserved	0x00

Interrupt Status 1 Register (Read-Only) [Address 0x00]

This 8-bit read-only register reflects the status of some of the interrupts that can cause the INT/$\overline{INT}$ pin to go active. This register is reset by a read operation, provided that any out-of-limit event has been corrected. It is also reset by a software reset.

D7	D6	D5	D4	D3	D2	D1	D0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Table 11.

Bit	Function
D0	1 when the internal temperature value exceeds T_{HIGH} limit. Any internal temperature reading greater than the set limit causes an out-of-limit event.
D1	1 when internal temperature value exceeds T_{LOW} limit. Any internal temperature reading less than or equal to the set limit causes an out-of-limit event.
D2	This status bit is linked to the configuration of Pin 7 and Pin 8. If configured for external temperature sensor, this bit is 1 when the external temperature value exceeds T_{HIGH} limit. The default value for this limit register is −1°C, so any external temperature reading greater than the set limit causes an out-of-limit event. If configured for AIN1 and AIN2, this bit is 1 when AIN1 input voltage exceeds V_{HIGH} or V_{LOW} limits.
D3	1 when external temperature value exceeds T_{LOW} limit. The default value for this limit register is 0°C, so any external temperature reading less than or equal to the set limit causes an out-of-limit event.
D4	1 indicates a fault (open or short) for the external temperature sensor.
D5	1 when AIN2 voltage is greater than its corresponding V_{HIGH} limit. 1 when AIN2 voltage is less than or equal to its corresponding V_{LOW} limit.
D6	1 when AIN3 voltage is greater than its corresponding V_{HIGH} limit. 1 when AIN3 voltage is less than or equal to its corresponding V_{LOW} limit.
D7	1 when AIN4 voltage is greater than its corresponding V_{HIGH} limit. 1 when AIN4 voltage is less than or equal to its corresponding V_{LOW} limit.

Interrupt Status 2 Register (Read-Only) [Address = 0x01]

This 8-bit read-only register reflects the status of the V_{DD} interrupt that can cause the INT/$\overline{INT}$ pin to go active. This register is reset by a read operation, provided that any out-of-limit event has been corrected. It is also reset by a software reset.

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	0[1]	N/A	N/A	N/A	N/A

[1] Default settings at power-up.

Table 12.

Bit	Function
D4	1 when V_{DD} value is greater than its corresponding V_{HIGH} limit. 1 when V_{DD} is less than or equal to its corresponding V_{LOW} limit.

Internal Temperature Value/V_{DD} Value Register LSBs (Read-Only) [Address = 0x03]

This 8-bit read-only register stores the two LSBs of the 10-bit temperature reading from the internal temperature sensor and the two LSBs of the 10-bit supply voltage reading.

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	N/A	V1	LSB	T1	LSB
N/A	N/A	N/A	N/A	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Table 13.

Bit	Function
D0	LSB of internal temperature value.
D1	Bit 1 of internal temperature value.
D2	LSB of V_{DD} value.
D3	Bit 1 of V_{DD} value.

External Temperature Value and Analog Input 1 to Analog Input 4 Register LSBs (Read-Only) [Address = 0x04]

This is an 8-bit, read-only register. Bits[D2:D7] store the two LSBs of the analog inputs AIN2 to AIN4. Bits[D0:D1] store the two LSBs of either the external temperature value or AIN1 input value. The type of input for D0 and D1 is selected by Bits[C1:C2] of the Control Configuration Register 1.

D7	D6	D5	D4	D3	D2	D1	D0
A4	A4$_{LSB}$	A3	A3$_{LSB}$	A2	A2$_{LSB}$	T/A	T/A$_{LSB}$
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Table 14.

Bit	Function
D0	LSB of external temperature value or AIN1 value.
D1	Bit 1 of external temperature value or AIN1 value.
D2	LSB of AIN2 value.
D3	Bit 1 of AIN2 value.
D4	LSB of AIN3 value.
D5	Bit 1 of AIN3 value.
D6	LSB of AIN4 value.
D7	Bit 1 of AIN4 value.

V_{DD} Value Register MSBs (Read-Only) [Address = 0x06]

This 8-bit read-only register stores the supply voltage value. The eight MSBs of the 10-bit value are stored in this register.

D7	D6	D5	D4	D3	D2	D1	D0
V9	V8	V7	V6	V5	V4	V3	V2
x[1]	x[1]	x[1]	x[1]	x[1]	x[1]	x[1]	x[1]

[1] Loaded with V_{DD} value after power-up.

Internal Temperature Value Register MSBs (Read-Only) [Address = 0x07]

This 8-bit read-only register stores the internal temperature value from the internal temperature sensor in twos complement format. The eight MSBs of the 10-bit value are stored in this register.

D7	D6	D5	D4	D3	D2	D1	D0
T9	T8	T7	T6	T5	T4	T3	T2
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

External Temperature Value or Analog Input AIN1 Register MSBs (Read-Only) [Address = 0x08]

This 8-bit read-only register stores, if selected, the external temperature value or the analog input AIN1 value. Selection is done in the Control Configuration 1 register. The external temperature value is stored in twos complement format. The eight MSBs of the 10-bit value are stored in this register.

D7	D6	D5	D4	D3	D2	D1	D0
T/A9	T/A8	T/A7	T/A6	T/A5	T/A4	T/A3	T/A2
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

AIN2 Register MSBs (Read) [Address = 0x09]

This 8-bit read register contains the eight MSBs of the AIN2 analog input voltage word. The value in this register is combined with Bits[D2:D3] of the external temperature value and Analog Input 1 to Analog Input 4 register LSBs, Address 0x04, to give the full 10-bit conversion result of the analog value on the AIN2 pin.

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

AIN3 Register MSBs (Read) [Address = 0x0A]

This 8-bit read register contains the eight MSBs of the AIN3 analog input voltage word. The value in this register is combined with Bits[D4:D5] of the external temperature value and Analog Input 1 to Analog Input 4 register LSBs, Address 0x04, to give the full 10-bit conversion result of the analog value on the AIN3 pin.

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

AIN4 Register MSBs (Read) [Address = 0x0B]

This 8-bit read register contains the eight MSBs of the AIN4 analog input voltage word. The value in this register is combined with Bits[D6:D7] of the external temperature value and Analog Input 1 to Analog Input 4 register LSBs, Address 0x04, to give the full 10-bit conversion result of the analog value on the AIN4 pin.

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

DAC A Register LSBs (Read/Write) [Address = 0x10]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7516/ADT7517 DAC A word, respectively. The value in this register is combined with the value in the DAC A register MSBs and converted to an analog voltage on the V_{OUT}-A pin. On power-up, the voltage output on the V_{OUT}-A pin is 0 V.

ADT7516

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0[1]	0[1]	0[1]	0[1]	N/A	N/A	N/A	N/A

[1] Default settings at power-up.

ADT7517

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0[1]	0[1]	N/A	N/A	N/A	N/A	N/A	N/A

[1] Default settings at power-up.

DAC A Register MSBs (Read/Write) [Address = 0x11]

This 8-bit read/write register contains the eight MSBs of the DAC A word. The value in this register is combined with the value in the DAC A register LSBs and converted to an analog voltage on the V_{OUT}-A pin. On power-up, the voltage output on the V_{OUT}-A pin is 0 V.

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

DAC B Register LSBs (Read/Write) [Address = 0x12]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7516/ADT7517 DAC B word, respectively. The value in this register is combined with the value in the DAC B register MSBs and converted to an analog voltage on the V_{OUT}-B pin. On power-up, the voltage output on the V_{OUT}-B pin is 0 V.

ADT7516

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0[1]	0[1]	0[1]	0[1]	N/A	N/A	N/A	N/A

[1] Default settings at power-up.

ADT7517

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0[1]	0[1]	N/A	N/A	N/A	N/A	N/A	N/A

[1] Default settings at power-up.

DAC B Register MSBs (Read/Write) [Address = 0x13]

This 8-bit read/write register contains the eight MSBs of the DAC B word. The value in this register is combine with the value in the DAC B register LSBs and converts to an analog voltage on the V_{OUT}-B pin. On power-up, the voltage output on the V_{OUT}-B pin is 0 V.

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

DAC C Register LSBs (Read/Write) [Address = 0x14]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7516/ADT7517 DAC C word, respectively. The value in this register is combined with the value in the DAC C register MSBs and converted to an analog voltage on the V_{OUT}-C pin. On power-up, the voltage output on the V_{OUT}-C pin is 0 V.

ADT7516

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0[1]	0[1]	0[1]	0[1]	N/A	N/A	N/A	N/A

[1] Default settings at power-up.

ADT7517

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0[1]	0[1]	N/A	N/A	N/A	N/A	N/A	N/A

[1] Default settings at power-up.

DAC C Register MSBs (Read/Write) [Address = 0x15]

This 8-bit read/write register contains the eight MSBs of the DAC C word. The value in this register is combined with the value in the DAC C register LSBs and converted to an analog voltage on the V_{OUT}-C pin. On power-up, the voltage output on the V_{OUT}-C pin is 0 V.

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

DAC D Register LSBs (Read/Write) [Address = 0x16]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7516/ADT7517 DAC D word, respectively. The value in this register is combined with the value in the DAC D register MSBs and converted to an analog voltage on the V_{OUT}-D pin. On power-up, the voltage output on the V_{OUT}-D pin is 0 V.

ADT7516

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0[1]	0[1]	0[1]	0[1]	N/A	N/A	N/A	N/A

[1] Default settings at power-up.

ADT7517

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0[1]	0[1]	N/A	N/A	N/A	N/A	N/A	N/A

[1] Default settings at power-up.

DAC D Register MSBs (Read/Write) [Address = 0x17]

This 8-bit read/write register contains the eight MSBs of the DAC D word. The value in this register combines with the value in the DAC D register LSBs and converts to an analog voltage on the V_{OUT}-D pin. On power-up, the voltage output on the V_{OUT}-D pin is 0 V.

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Control Configuration 1 Register (Read/Write) [Address = 0x18]

This configuration register is an 8-bit read/write register that is used to set up some of the operating modes of the ADT7516/ADT7517/ADT7519.

Table 15. Control Configuration 1

D7	D6	D5	D4	D3	D2	D1	D0
PD	C6	C5	C4	C3	C2	C1	C0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Table 16.

Bit	Function
C0	This bit enables/disables conversions in round robin and single-channel mode. ADT7516/ADT7517/ADT7519 powers up in round robin mode but monitoring is not initiated until this bit is set. The default = 0. 0 = stop monitoring. 1 = start monitoring.
[C1:C2]	Selects between the two different analog inputs on Pin 7 and Pin 8. ADT7516/ADT7517/ADT7519 powers up with AIN1 and AIN2 selected. 00 = AIN1 and AIN2 selected. 01 = undefined. 10 = external TDM selected. 11 = undefined.
C3	Selects between digital (LDAC) and analog inputs (AIN3) on Pin 9. When AIN3 is selected, Bit C3 of the Control Configuration 3 register is masked and has no effect until LDAC is selected as the input on Pin 9. 0 = LDAC selected. 1 = AIN3 selected.
C4	Reserved. Write 0 only.
C5	0 = enable INT/INT output. 1 = disable INT/INT output.
C6	Configures INT/INT output polarity. 0 = active low. 1 = active high.
PD	Power-Down Bit. Setting this bit to 1 puts the ADT7516/ADT7517/ADT7519 into standby mode. In this mode, both ADC and DACs are fully powered down, but the serial interface is still operational. To power up the part again, just write 0 to this bit.

Control Configuration 2 Register (Read/Write) [Address = 0x19]

This configuration register is an 8-bit read/write register that is used to set up some of the operating modes of the ADT7516/ADT7517/ADT7519.

D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5	C4	C3	C2	C1	C0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Table 17.

Bit	Function
[C0:C2]	In single-channel mode, these bits select between V_{DD}, the internal temperature sensor, external temperature sensor/AIN1, AIN2, AIN3, and AIN4 for conversion. The default is V_{DD}. 000 = V_{DD}. 001 = internal temperature sensor. 010 = external temperature sensor/AIN1. (Bits[C1:C2] of the Control Configuration 1 register affect this selection). 011 = AIN2. 100 = AIN3. 101 = AIN4. 110 to 111 = reserved.
C3	Reserved.
C4	Selects between single-channel and round robin conversion cycle. The default is round robin. 0 = round robin. 1 = single channel.
C5	Default condition is to average every measurement on all channels 16 times. This bit disables this averaging. Channels affected are temperature, analog inputs, and V_{DD}. 0 = enable averaging. 1 = disable averaging.
C6	SMBus timeout on the serial clock puts a 25 ms limit on the pulse width of the clock, ensuring that a fault on the master SCL does not lock up the SDA line. 0 = disable SMBus timeout. 1 = enable SMBus timeout.
C7	Software Reset. Setting this bit to 1 causes a software reset. All registers and DAC outputs reset to their default settings.

Control Configuration 3 Register (Read/Write) [Address = 0x1A]

This configuration register is an 8-bit read/write register that is used to set up some of the operating modes of the ADT7516/ADT7517/ADT7519.

D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5	C4	C3	C2	C1	C0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Table 18.

Bit	Function
C0	Selects between fast and slow ADC conversion speeds.
	0 = ADC clock at 1.4 kHz.
	1 = ADC clock at 22.5 kHz. D+ and D− analog filters are disabled.
C1	On the ADT7516 and ADT7517, this bit selects between 8-bit and 10-bit DAC output resolution on the thermal voltage output feature. The default is 8 bits. This bit has no effect on the ADT7519 output because this part has only an 8-bit DAC. For the ADT7519, write 0 to this bit.
	0 = 8-bit resolution.
	1 = 10-bit resolution.
C2	Reserved. Write 0 only.
C3	0 = $\overline{LDAC}$ pin controls updating of DAC outputs.
	1 = DAC configuration register and LDAC configuration register control updating of DAC outputs.
C4	Selects the ADC reference to be either internal V_{REF} or V_{DD} for analog inputs.
	0 = internal V_{REF}.
	1 = V_{DD}.
C5	Setting this bit selects DAC A voltage output to be proportional to the internal temperature measurement.
C6	Setting this bit selects DAC B voltage output to be proportional to the external temperature measurement.
C7	Reserved. Write 0 only.

DAC Configuration Register (Read/Write) [Address = 0x1B]

This configuration register is an 8-bit read/write register that is used to control the output ranges of all four DACs and also to control the loading of the DAC registers if the $\overline{LDAC}$ pin is disabled (Bit C3 = 1, Control Configuration 3 register).

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Table 19.

Bit	Function
D0	Selects the output range of DAC A.
	0 = 0 V to V_{REF}.
	1 = 0 V to 2 V_{REF}.
D1	Selects the output range of DAC B.
	0 = 0 V to V_{REF}.
	1 = 0 V to 2 V_{REF}.
D2	Selects the output range of DAC C.
	0 = 0 V to V_{REF}.
	1 = 0 V to 2 V_{REF}.
D3	Selects the output range of DAC D.
	0 = 0 V to V_{REF}.
	1 = 0 V to 2 V_{REF}.

Bit	Function
[D4:D5]	00 = MSB write to any DAC register generates LDAC command that updates that DAC only.
	01 = MSB write to DAC B or DAC D register generates LDAC command that updates DAC A and DAC B or DAC C and DAC D, respectively.
	10 = MSB write to DAC D register generates LDAC command that updates all four DACs.
	11 = LDAC command generated from LDAC register.
[D6:D7]	Reserved. Write 0s only.

LDAC Configuration Register (Write-Only)[Address = 0x1C]

This configuration register is an 8-bit write register that is used to control the updating of the quad DAC outputs if the $\overline{LDAC}$ pin is disabled and Bits[D4:D5] of the DAC configuration register are both set to 1. Also selects either the internal or the external V_{REF} for all four DACs. Bits[D0:D3] in this register are self-clearing, that is, reading back from this register always gives 0s for these bits.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Table 20.

Bit	Function
D0	Writing a 1 to this bit generates the LDAC command to update DAC A output only.
D1	Writing a 1 to this bit generates the LDAC command to update DAC B output only.
D2	Writing a 1 to this bit generates the LDAC command to update DAC C output only.
D3	Writing a 1 to this bit generates the LDAC command to update DAC D output only.
D4	Selects either internal V_{REF} or external V_{REF} for DAC A and DAC B.
	0 = external V_{REF}.
	1 = internal V_{REF}.
D5	Selects either internal V_{REF} or external V_{REF} for DAC C and DAC D.
	0 = external V_{REF}.
	1 = internal V_{REF}.
[D6:D7]	Reserved. Write 0s only.

Interrupt Mask 1 Register (Read/Write) [Address = 0x1D]

This mask register is an 8-bit read/write register that can be used to mask any interrupts that can cause the INT/$\overline{INT}$ pin to go active.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Table 21.

Bit	Function
D0	0 = enable internal T_{HIGH} interrupt. 1 = disable internal T_{HIGH} interrupt.
D1	0 = enable internal T_{LOW} interrupt. 1 = disable internal T_{LOW} interrupt.
D2	0 = enable external T_{HIGH} interrupt or AIN1 interrupt. 1 = disable external T_{HIGH} interrupt or AIN1 interrupt.
D3	0 = enable external T_{LOW} interrupt. 1 = disable external T_{LOW} interrupt.
D4	0 = enable external temperature fault interrupt. 1 = disable external temperature fault interrupt.
D5	0 = enable AIN2 interrupt. 1 = disable AIN2 interrupt.
D6	0 = enable AIN3 interrupt. 1 = disable AIN3 interrupt.
D7	0 = enable AIN4 interrupt. 1 = disable AIN4 interrupt.

Interrupt Mask 2 Register (Read/Write) [Address = 0x1E]

This mask register is an 8-bit read/write register that can be used to mask any interrupts that can cause the INT/$\overline{INT}$ pin to go active.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Table 22.

Bit	Function
[D0:D3]	Reserved. Write 0s only.
D4	0 = enable V_{DD} interrupts. 1 = disable V_{DD} interrupts.
[D5:D7]	Reserved. Write 0s only.

Internal Temperature Offset Register (Read/Write) [Address = 0x1F]

This register contains the offset value for the internal temperature channel. A twos complement number can be written to this register and then added to the measured result before it is stored or compared to limits. In this way, a one-point calibration can be done, whereby the whole transfer function of the channel can be moved up or down. From a software point of view, this can be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change. Because it is an 8-bit register, the temperature resolution is 1°C.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

External Temperature Offset Register (Read/Write) [Address = 0x20]

This register contains the offset value for the external temperature channel. A twos complement number can be written to this register and is then added to the measured result before it is stored or compared to limits. In this way, a one-point calibration can be done, whereby the whole transfer function of the channel can be moved up or down. From a software point of view, this can be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change. Because it is an 8-bit register, the temperature resolution is 1°C.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Internal Analog Temperature Offset Register (Read/Write) [Address = 0x21]

This register contains the offset value for the internal thermal voltage output. A twos complement number can be written to this register and then added to the measured result before it is converted by DAC A. Varying the value in this register has the effect of varying the temperature span. For example, the output voltage can represent a temperature span of −128°C to +127°C or even 0°C to +127°C. In essence, this register changes the position of 0 V on the temperature scale. Temperatures other than −128°C to +127°C produce an upper deadband on the DAC A output. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is −40°C.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1[1]	1[1]	0[1]	1[1]	1[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

External Analog Temperature Offset Register (Read/Write) [Address = 0x22]

This register contains the offset value for the external thermal voltage output. A twos complement number can be written to this register and then added to the measured result before it is converted by DAC B. Varying the value in this register has the effect of varying the temperature span. For example, the output voltage can represent a temperature span of −128°C to +127°C or even 0°C to +127°C. In essence, this register changes the position of 0 V on the temperature scale. Temperatures other than −128°C to +127°C produce an upper deadband on the DAC B output. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is −40°C.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1[1]	1[1]	0[1]	1[1]	1[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

V_{DD} V_{HIGH} Limit Register (Read/Write) [Address = 0x23]

This limit register is an 8-bit read/write register that stores the V_{DD} upper limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured V_{DD} value has to be greater than the value in this register. The default value is 5.46 V.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1[1]	1[1]	0[1]	0[1]	0[1]	1[1]	1[1]	1[1]

[1] Default settings at power-up.

V_{DD} V_{LOW} Limit Register (Read/Write) [Address = 0x24]

This limit register is an 8-bit read/write register that stores the V_{DD} lower limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured V_{DD} value has to be less than or equal to the value in this register. The default value is 2.7 V.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	1[1]	1[1]	0[1]	0[1]	0[1]	1[1]	0[1]

[1] Default settings at power-up.

Internal T_{HIGH} Limit Register (Read/Write) [Address = 0x25]

This limit register is an 8-bit read/write register that stores the twos complement of the internal temperature upper limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured internal temperature value has to be greater than the value in this register. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is +100°C.

Positive Temperature = Limit Register Code (d)

Negative Temperature = Limit Register Code (d) − 256

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	1[1]	1[1]	0[1]	0[1]	1[1]	0[1]	0[1]

[1] Default settings at power-up.

Internal T_{LOW} Limit Register (Read/Write) [Address = 0x26]

This limit register is an 8-bit read/write register that stores the twos complement of the internal temperature lower limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured internal temperature value has to be more negative than or equal to the value in this register. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is −55°C.

Positive Temperature = Limit Register Code (d)

Negative Temperature = Limit Register Code (d) − 256

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1[1]	1[1]	0[1]	0[1]	1[1]	0[1]	0[1]	1[1]

[1] Default settings at power-up.

External T_{HIGH}/AIN1 V_{HIGH} Limit Register (Read/Write) [Address = 0x27]

If Pin 7 and Pin 8 are configured for the external temperature sensor, this limit register is an 8-bit read/write register that stores the twos complement of the external temperature upper limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured external temperature value has to be greater than the value in this register. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is −1°C.

Positive Temperature = Limit Register Code (d)

Negative Temperature = Limit Register Code (d) − 256

If Pin 7 and Pin 8 are configured for AIN1 and AIN2 inputs, this limit register is an 8-bit read/write register that stores the AIN1 input upper limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN1 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. Because the power-up default settings for Pin 7 and Pin 8 are AIN1 and AIN2 inputs, the default value for this limit register is full-scale voltage.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]

[1] Default settings at power-up.

External T_{LOW}/AIN1 V_{LOW} Limit Register (Read/Write) [Address = 0x28]

If Pin 7 and Pin 8 are configured for the external temperature sensor, this limit register is an 8-bit read/write register that stores the twos complement of the external temperature lower limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured external temperature value has to be more negative than or equal to the value in this register. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is 0°C.

Positive Temperature = Limit Register Code (d)

Negative Temperature = Limit Register Code (d) − 256

If Pin 7 and Pin 8 are configured for AIN1 and AIN2 inputs, this limit register is an 8-bit read/write register that stores the AIN1 input lower limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN1 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. Because the power-up default settings for Pin 7 and Pin 8 are AIN1 and AIN2 inputs, the default value for this limit register is 0 V.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

AIN2 V$_{HIGH}$ Limit Register (Read/Write) [Address = 0x2B]

This limit register is an 8-bit read/write register that stores the AIN2 input upper limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN2 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]

[1] Default settings at power-up.

AIN2 V$_{LOW}$ Limit Register (Read/Write) [Address = 0x2C]

This limit register is an 8-bit read/write register that stores the AIN2 input lower limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN2 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.[1] Default settings at power-up.

AIN3 V$_{HIGH}$ Limit Register (Read/Write) [Address = 0x2D]

This limit register is an 8-bit read/write register that stores the AIN3 input upper limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN3 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]

[1] Default settings at power-up.

AIN3 V$_{LOW}$ Limit Register (Read/Write) [Address = 0x2E]

This limit register is an 8-bit read/write register that stores the AIN3 input lower limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN3 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

AIN4 V$_{HIGH}$ Limit Register (Read/Write) [Address = 0x2F]

This limit register is an 8-bit read/write register that stores the AIN4 input upper limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN4 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]

[1] Default settings at power-up.

AIN4 V$_{LOW}$ Limit Register (Read/Write) [Address = 0x30]

This limit register is an 8-bit read/write register that stores the AIN4 input lower limit, and causes an interrupt and activates the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN4 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]

[1] Default settings at power-up.

Device ID Register (Read-Only) [Address = 0x4D]

This 8-bit read-only register indicates the part model of the device: ADT7516 = 0x03, ADT7517 = 0x07, and ADT7519 = 0x0B.

Manufacturer's ID Register (Read-Only) [Address = 0x4E]

This register contains the manufacturer's identification number. ID number of Analog Devices, Inc. is 0x41.

Silicon Revision Register (Read-Only) [Address = 0x4F]

This register is divided into the four LSBs representing the stepping and the four MSBs representing the version. The stepping contains the manufacturer's code for minor revisions or steppings to the silicon. The version is the ADT7516/ADT7517/ADT7519 version number.

SPI Lock Status Register (Read-Only) [Address = 0x7F]

Bit D0 (LSB) of this read-only register indicates whether or not the SPI interface is locked. Writing to this register causes the device to malfunction. The default value is 0x00.

   0 = I²C interface.

   1 = SPI interface selected and locked.

SERIAL INTERFACE

There are two serial interfaces that can be used on this part, I²C and SPI. The device powers up with the serial interface in I²C mode, but it is not locked into this mode. To stay in I²C mode, it is recommended that the user tie the $\overline{CS}$ line to either V_{CC} or GND. It is not possible to lock the I²C mode, but it is possible to select and lock the SPI mode.

To select and lock the interface into the SPI mode, a number of pulses must be sent down the $\overline{CS}$ line (Pin 4). The following section describes how this is done.

Once the SPI communication protocol has been locked in, it cannot be unlocked while the device is still powered up. Bit D0 of the SPI lock status register (Address 0x7F) is set to 1 when a successful SPI interface lock has been accomplished. To reset the serial interface, the user must power down the part and power it up again. A software reset does not reset the serial interface.

Serial Interface Selection

The $\overline{CS}$ line controls the selection between I²C and SPI. Figure 59 shows the selection process necessary to lock the SPI interface mode.

To communicate to the ADT7516/ADT7517/ADT7519 using the SPI protocol, send three pulses down the $\overline{CS}$ line as shown in Figure 59. On the third rising edge (marked as C in Figure 59), the part selects and locks the SPI interface. The user is now limited to communicating to the device using the SPI protocol.

As per most SPI standards, the $\overline{CS}$ line must be low during every SPI communication to the ADT7516/ADT7517/ADT7519 and high all other times. Typical examples of how to connect the dual interface as I²C or SPI are shown in Figure 57 and Figure 58. The following sections describe in detail how to use the I²C and SPI protocols associated with the ADT7516/ADT7517/ADT7519.
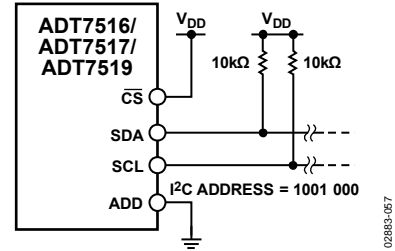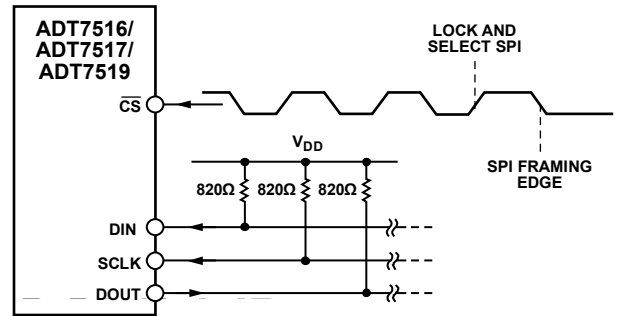

Figure 57. Typical I²C Interface Connection
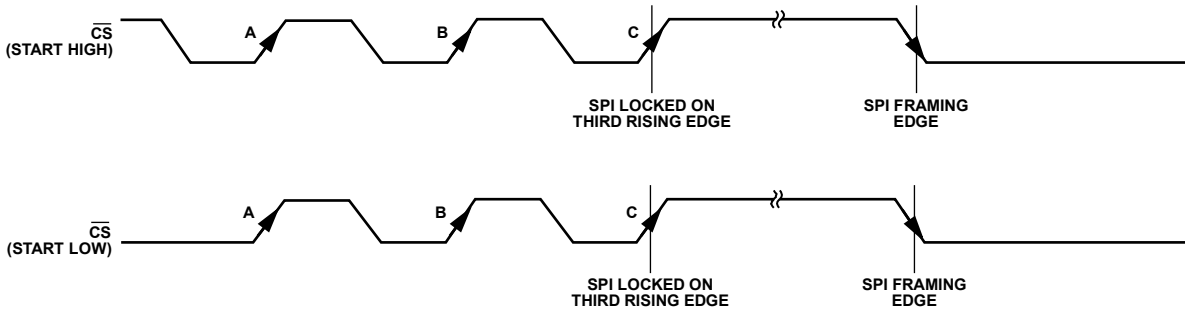

Figure 58. Typical SPI Interface Connection.

Figure 59. Serial Interface—Selecting and Locking SPI Protocol

I²C Serial Interface

Like all I²C-compatible devices, the ADT7516/ADT7517/ADT7519 have a 7-bit serial address. The four MSBs of this address for the ADT7516/ADT7517/ADT7519 are set to 1001. The three LSBs are set by Pin 11, ADD. The ADD pin can be configured three ways to give three different address options: low, floating, and high. Setting the ADD pin low gives a serial bus address of 1001 000, leaving it floating gives the Address 1001 010, and setting it high gives the Address 1001 011. The recommended pull-up resistor value is 10 kΩ.

There is an enable/disable bit for the SMBus timeout. When this is enabled, the SMBus times out after 25 ms of no activity. To enable it, set Bit 6 of the Control Configuration 2 register. The power-on default is with the SMBus timeout disabled.

The ADT7516/ADT7517/ADT7519 support SMBus packet error checking (PEC), but its use is optional. It is triggered by supplying the extra clocks for the PEC byte. The PEC is calculated using CRC-8. The frame clock sequence (FCS) conforms to CRC-8 by the polynomial

$$C(x) = x^8 + x^2 + x^1 + 1$$

Consult the SMBus specification for more information.

The serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, defined as a high to low transition on the serial data line (SDA) while the serial clock line (SCL) remains high. This indicates that an address/data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus a R/$\overline{W}$ bit; this determines the direction of the data transfer, that is, whether data is written to or read from the slave device.

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is 0, the master writes to the slave device. If the R/$\overline{W}$ bit is 1, the master reads from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low to high transition when the clock is high can be interpreted as a stop signal.

3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device pulls the data line high during the low period before the ninth clock pulse. This is known as no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

The I²C address set up by the ADD pin is not latched by the device until after this address has been sent twice. On the eighth SCL cycle of the second valid communication, the serial bus address is latched in. This is the SCL cycle directly after the device has seen its own I²C serial bus address. Any subsequent changes on this pin have no effect on the I²C serial bus address.

Writing to the ADT7516/ADT7517/ADT7519

Depending on the register being written to, there are two different writes for the ADT7516/ADT7517/ADT7519. It is not possible to do a block write to this part, that is, no I²C auto-increment.

Writing to the Address Pointer Register for a Subsequent Read

To read data from a particular register, the address pointer register must contain the address of that register. If it does not, the correct address must be written to the address pointer register by performing a single-byte write operation, as shown in Figure 60. The write operation consists of the serial bus address followed by the address pointer byte. No data is written to any of the data registers. A read operation is then performed to read the register.
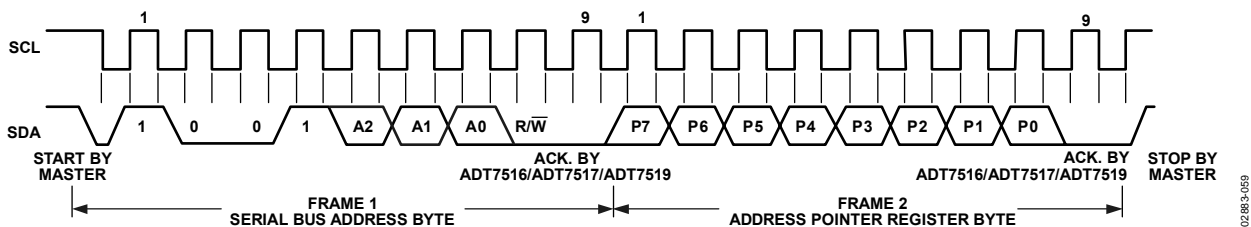

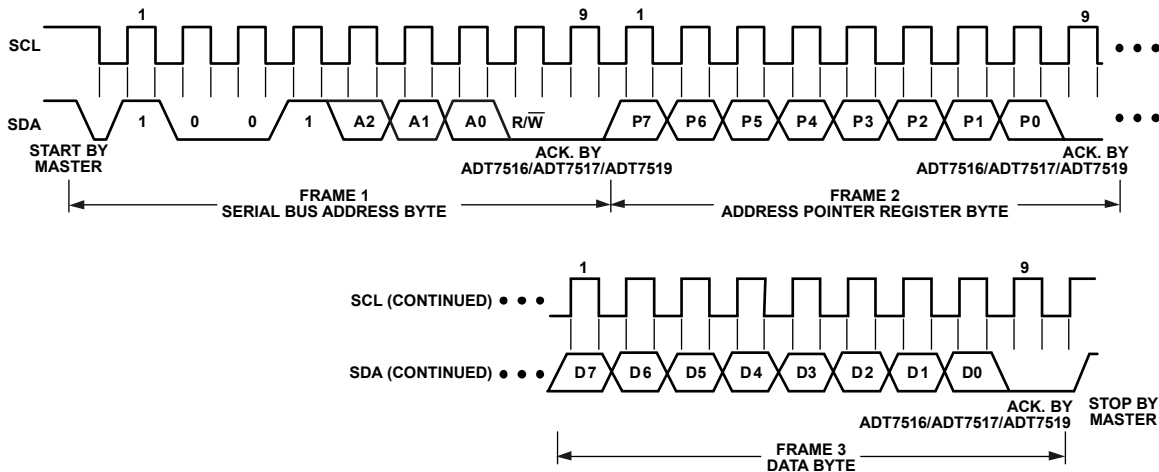Figure 60. I²C—Writing to the Address Pointer Register to Select a Register for a Subsequent Read Operation

Figure 61. I²C—Writing to the Address Pointer Register Followed by a Single Byte of Data to the Selected Register
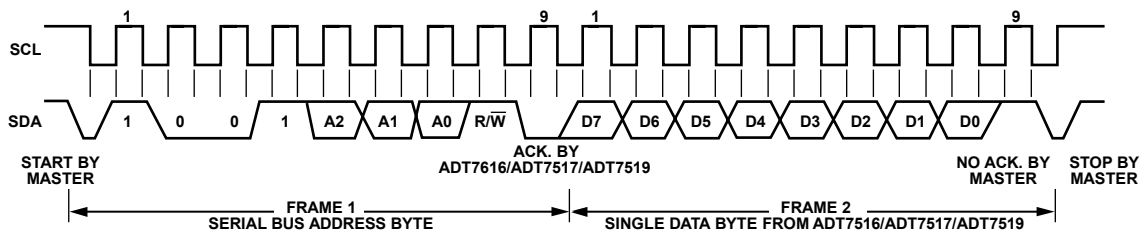

Figure 62. I²C—Reading a Single Byte of Data from a Selected Register

Writing Data to a Register

All registers are 8-bit registers, therefore only one byte of data can be written to each register. Writing a single byte of data to one of these read/write registers consists of the serial bus address, the data register address written to the address pointer register, followed by the data byte written to the selected data register. This is illustrated in Figure 61. To write to a different register, another start or repeated start is required. If more than one byte of data is sent in one communication operation, the addressed register is repeatedly loaded until the last data byte has been sent.

Reading Data from the ADT7516/ADT7517/ADT7519

Reading data from the ADT7516/ADT7517/ADT7519 is done in a one-byte operation. Reading back the contents of a register is shown in Figure 62. The register address had previously been set up by a single-byte write operation to the address pointer register. To read from another register, write to the address pointer register again to set up the relevant register address. Thus, block reads are not possible, that is, no I²C auto-increment.

SPI Serial Interface

The SPI serial interface of the ADT7516/ADT7517/ADT7519 consists of four wires: $\overline{CS}$, SCLK, DIN, and DOUT. The $\overline{CS}$ is used to select the device when more than one device is connected to the serial clock and data lines. The $\overline{CS}$ is also used to distinguish between any two separate serial communications (see Figure 67 for a graphical explanation). The SCLK is used to clock data in and out of the part. The DIN line is used to write to the registers, and the DOUT line is used to read data back from the registers. The recommended pull-up resistor value is between 500 Ω and 820 Ω. Strong pull-ups are needed when serial clock speeds that are close to the maximum limit are used or when the SPI interface lines are experiencing large capacitive loading. Larger resistor values can be used for pull-up resistors when the serial clock speed is reduced.

The part operates in slave mode and requires an externally applied serial clock to the SCLK input. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

There are two types of serial operations, read and write. Command words are used to distinguish read operations from write operations. These command words are given in Table 23. Address auto-increment is possible in SPI mode.

Table 23. SPI Command Words

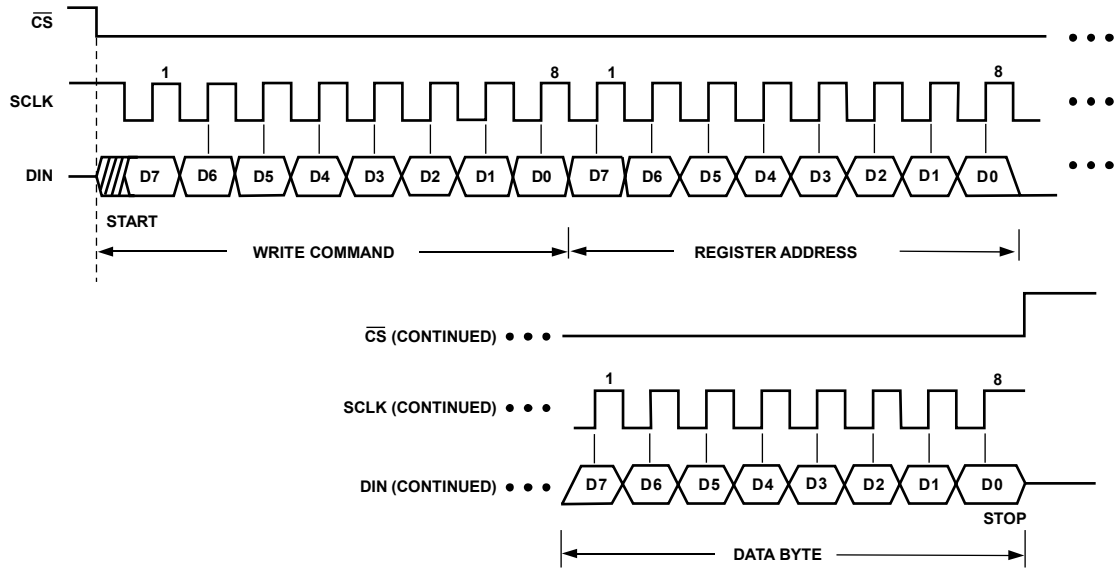| Write	Read
0x90 (1001 0000)	0x91 (1001 0001)

Figure 63. SPI—Writing to the Address Pointer Register Followed by a Single Byte of Data to the Selected Register

Write Operation

Figure 63 shows the timing diagram for a write operation to the ADT7516/ADT7517/ADT7519. Data is clocked into the registers on the rising edge of SCLK. When the $\overline{CS}$ line is high, the DIN and DOUT lines are in three-state mode. Only when the $\overline{CS}$ goes from a high to a low does the part accept any data on the DIN line. In SPI mode, the address pointer register is capable of auto-incrementing to the next register in the register map without having to load the address pointer register each time. In Figure 63, the register address portion gives the first register that is written to. Subsequent data bytes are written into sequential writable registers. Thus, after each data byte has been written into a register, the address pointer register auto-increments its value to the next available register. The address pointer register auto-increments from 0x00 to 0x3F and loops back to start again at 0x00 when it reaches 0x3F.

Read Operation

Figure 64 to Figure 66 show the timing diagrams necessary to accomplish correct read operations. To read back from a register, first write to the address pointer register with the address of the register to be read from. This operation is shown in Figure 64. Figure 65 shows the procedure for reading back a single byte of data. The read command is first sent to the part during the first eight clock cycles. As the read command is being sent, irrelevant data is output onto the DOUT line. During the following eight clock cycles, the data contained in the register selected by the address pointer register is output onto the DOUT line. Data is output onto the DOUT line on the falling edge of SCLK. Figure 66 shows the procedure when reading data from two sequential registers. Multiple data reads are possible in the SPI interface mode as the address pointer register is auto-incremental. The address pointer register auto-increments from 0x00 to 0x3F and loops back to start again at 0x00 when it reaches 0x3F.
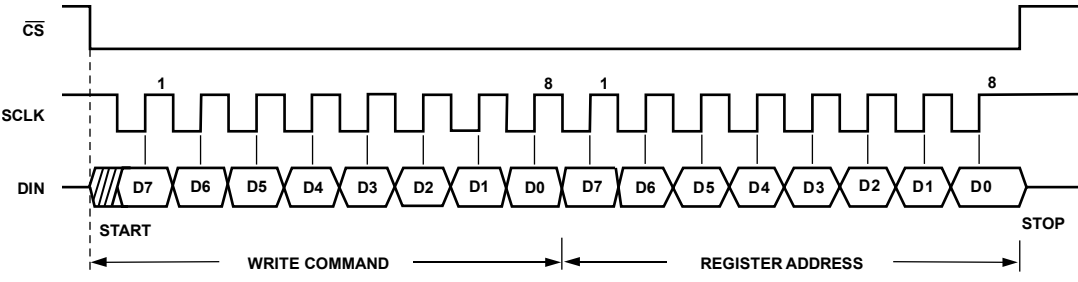
Figure 64. SPI—Writing to the Address Pointer Register to Select a Register for a Subsequent Read Operation
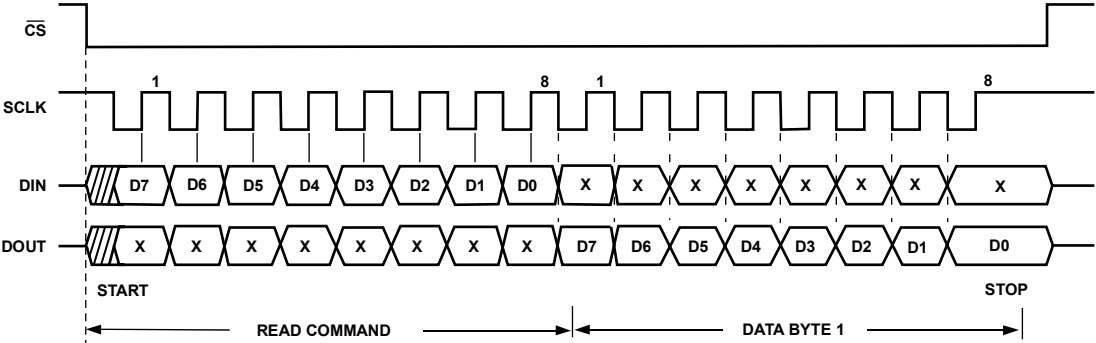

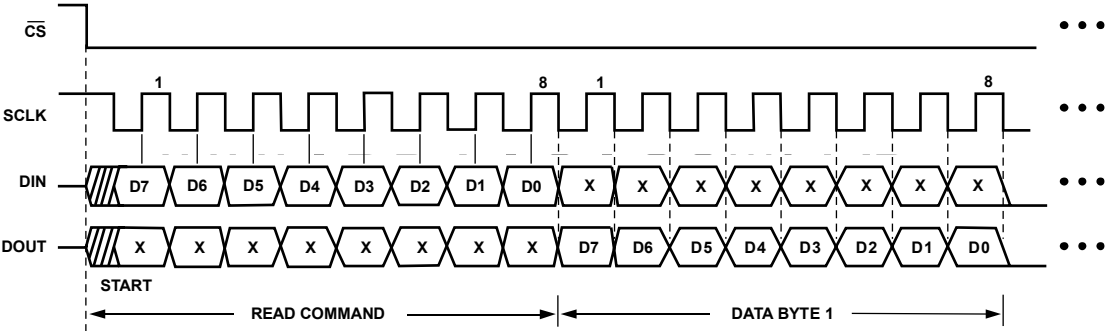Figure 65. SPI—Reading a Single Byte of Data From a Selected Register

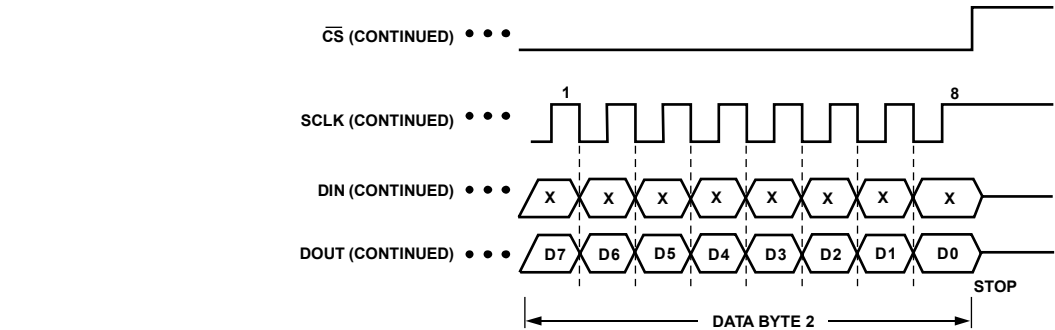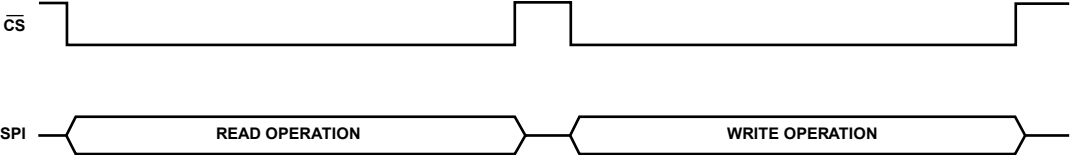Figure 66. SPI—Reading Two Bytes of Data from Two Sequential Registers

Figure 67. SPI—Correct Use of CS during SPI Communication

SMBus/SPI INT/$\overline{INT}$

The ADT7516/ADT7517/ADT7519 INT/$\overline{INT}$ outputs are an interrupt line for devices that want to trade their ability to master for an extra pin. The ADT7516/ADT7517/ADT7519 are slave devices and use the SMBus/SPI INT/$\overline{INT}$ to signal the host device that it wants to talk to. The SMBus/SPI INT/$\overline{INT}$ on the ADT7516/ADT7517/ADT7519 is used as an over/under limit indicator.

The INT/$\overline{INT}$ pin has an open-drain configuration that allows the outputs of several devices to be wire-AND'ed together when the INT/$\overline{INT}$ pin is active low. Use C6 of the Control Configuration 1 register to set the active polarity of the INT/$\overline{INT}$ output. The power-up default is active low. The INT/$\overline{INT}$ output can be disabled or enabled by setting C5 of the Control Configuration 1 register to 1 or 0, respectively.

The INT/$\overline{INT}$ output becomes active when either the internal temperature value, the external temperature value, V_{DD} value, or any of the AIN input values exceed the values in their corresponding T_{HIGH}/V_{HIGH} or T_{LOW}/V_{LOW} registers. The INT/$\overline{INT}$ output goes inactive again when a conversion result has the measured value back within the trip limits and when the status register associated with the out-of-limit event is read. The two interrupt status registers show the event that caused the INT/$\overline{INT}$ pin to go active.

The INT/$\overline{INT}$ output requires an external pull-up resistor. This can be connected to a voltage different from V_{DD}, provided the maximum voltage rating of the INT/$\overline{INT}$ output pin is not exceeded. The value of the pull-up resistor depends on the application but should be large enough to avoid excessive sink currents at the INT/$\overline{INT}$ output because they can heat the chip and affect the temperature reading.

SMBUS ALERT RESPONSE

The INT/$\overline{INT}$ pin behaves the same way as an SMBus alert pin when the SMBus/I²C interface is selected. It is an open-drain output and requires a pull-up to V_{DD}. Several INT/$\overline{INT}$ outputs can be wire-AND'ed together, so that the common line goes low if one or more of the INT/$\overline{INT}$ outputs goes low. The polarity of the INT/$\overline{INT}$ pin must be set active low for a number of outputs to be wire-AND'ed together.

The INT/$\overline{INT}$ output can operate as an $\overline{SMBALERT}$ function. Slave devices on the SMBus cannot normally signal to the master that they want to talk, but the $\overline{SMBALERT}$ function

allows them to do so. $\overline{SMBALERT}$ is used in conjunction with the SMBus general call address.

One or more INT/$\overline{INT}$ outputs can be connected to a common $\overline{SMBALERT}$ line connected to the master. When the $\overline{SMBALERT}$ line is pulled low by one of the devices, the following procedure occurs as shown in Figure 68:

1. $\overline{SMBALERT}$ is pulled low.

2. Master initiates a read operation and sends the alert response address (ARA = 0001 100). This general call address must not be used as a specific device address.

3. A device whose INT/$\overline{INT}$ output is low responds to the alert response address and the master reads its device address. As the device address is seven bits long, an LSB of 1 is added. The address of the device is now known and it can be interrogated in the usual way.

4. If INT/$\overline{INT}$ output of more than one device is low, the one with the lowest device address has priority in accordance with normal SMBus specifications.

5. When the ADT7516/ADT7517/ADT7519 have responded to the alert response address, they reset their INT/$\overline{INT}$ output, provided that the condition that caused the out-of-limit event no longer exists and that the status register associated with the out-of-limit event is read. If the $\overline{SMBALERT}$ line remains low, the master sends the ARA again. It continues to do this until all devices whose $\overline{SMBALERT}$ outputs were low have responded.
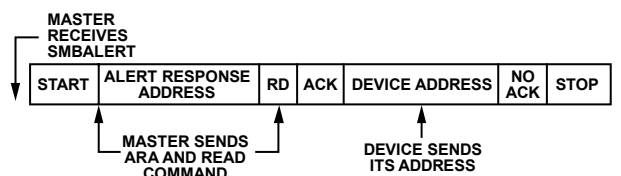

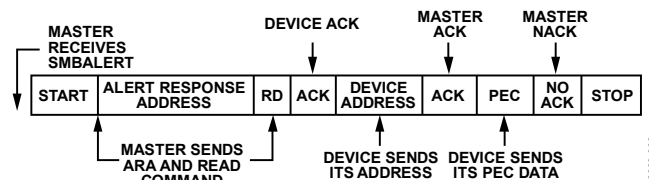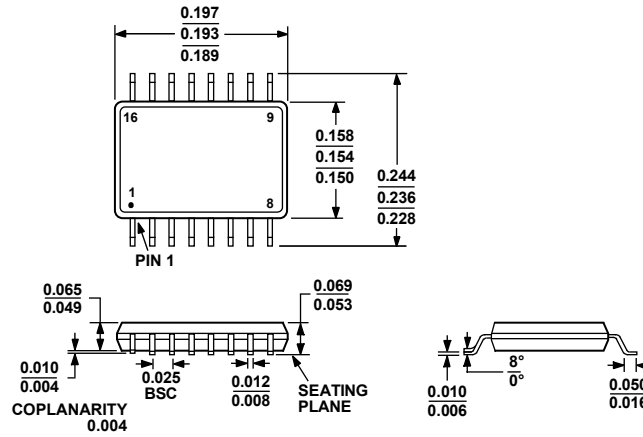Figure 68. INT/$\overline{INT}$ Responds to $\overline{SMBALERT}$ ARA

Figure 69. INT/$\overline{INT}$ Responds to $\overline{SMBALERT}$ ARA
with Packet Error Checking (PEC)

OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MO-137-AB

Figure 70. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	DAC Resolution	Package Description	Package Option	Ordering Quantity
ADT7519ARQ	−40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	98
ADT7519ARQ-REEL	−40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	2,500
ADT7519ARQ-REEL7	−40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	1,000
ADT7519ARQZ[1]	−40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	98
ADT7519ARQZ-REEL[1]	−40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	2,500
ADT7519ARQZ-REEL7[1]	−40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	1,000
ADT7517ARQ	−40°C to +120°C	10 Bits	16-Lead QSOP	RQ-16	98
ADT7517ARQ-REEL	−40°C to +120°C	10 Bits	16-Lead QSOP	RQ-16	2,500
ADT7517ARQ-REEL7	−40°C to +120°C	10 Bits	16-Lead QSOP	RQ-16	1,000
ADT7517ARQZ[1]	−40°C to +120°C	10 Bits	16-Lead QSOP	RQ-16	98
ADT7517ARQZ-REEL[1]	−40°C to +120°C	10 Bits	16-Lead QSOP	RQ-16	2,500
ADT7517ARQZ-REEL7[1]	−40°C to +120°C	10 Bits	16-Lead QSOP	RQ-16	1,000
ADT7516ARQ	−40°C to +120°C	12 Bits	16-Lead QSOP	RQ-16	98
ADT7516ARQ-REEL	−40°C to +120°C	12 Bits	16-Lead QSOP	RQ-16	2,500
ADT7516ARQ-REEL7	−40°C to +120°C	12 Bits	16-Lead QSOP	RQ-16	1,000
ADT7516ARQZ[1]	−40°C to +120°C	12 Bits	16-Lead QSOP	RQ-16	98
ADT7516ARQZ-REEL[1]	−40°C to +120°C	12 Bits	16-Lead QSOP	RQ-16	2,500
ADT7516ARQZ-REEL7[1]	−40°C to +120°C	12 Bits	16-Lead QSOP	RQ-16	1,000
EVAL-ADT7516EB			Evaluation Board		

[1] Z = Pb-free part.

NOTES

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