

Quad-Channel Digital Isolators ADuM1400/ADuM1401/ADuM1402

FEATURES

Automotive versions gualified per AEC-Q100 Low power operation **5 V operation** 1.0 mA per channel maximum @ 0 Mbps to 2 Mbps 3.5 mA per channel maximum @ 10 Mbps 31 mA per channel maximum @ 90 Mbps **3 V operation** 0.7 mA per channel maximum @ 0 Mbps to 2 Mbps 2.1 mA per channel maximum @ 10 Mbps 20 mA per channel maximum @ 90 Mbps **Bidirectional communication** 3 V/5 V level translation High temperature operation: 125°C High data rate: dc to 90 Mbps (NRZ) **Precise timing characteristics** 2 ns maximum pulse width distortion 2 ns maximum channel-to-channel matching High common-mode transient immunity: >25 kV/µs **Output enable function** 16-lead SOIC wide body package **RoHS-compliant models available** Safety and regulatory approvals UL recognition: 2500 V rms for 1 minute per UL 1577 CSA Component Acceptance Notice #5A **VDE Certificate of Conformity** DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 VIORM = 560 V peak TÜV approval: IEC/EN/UL/CSA 61010-1

APPLICATIONS

General-purpose multichannel isolation SPI interface/data converter isolation RS-232/RS-422/RS-485 transceivers Industrial field bus isolation **Automotive systems**

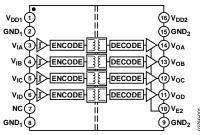


Figure 1. ADuM1400

FUNCTIONAL BLOCK DIAGRAMS

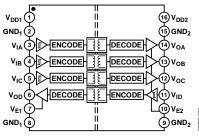
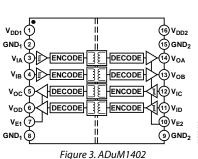


Figure 2. ADuM1401



Rev. G

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GENERAL DESCRIPTION

The ADuM140x1 are quad-channel digital isolators based on Analog Devices, Inc., iCoupler[®] technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple iCoupler digital interfaces and stable performance characteristics.

The need for external drivers and other discrete components is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices consume one-tenth to one-sixth of the power of optocouplers at comparable signal data rates.

The ADuM140x isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the ADuM140x provides low pulse width distortion (<2 ns for CRW grade) and tight channel-to-channel matching (<2 ns for CRW grade). Unlike other optocoupler alternatives, the ADuM140x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and when power is not applied to one of the supplies.

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

TABLE OF CONTENTS

Features 1
Applications1
General Description 1
Functional Block Diagrams 1
Revision History 3
Specifications
Electrical Characteristics—5 V, 105°C Operation 4
Electrical Characteristics—3 V, 105°C Operation
Electrical Characteristics—Mixed 5 V/3 V or 3 V/5 V, 105°C Operation
Electrical Characteristics—5 V, 125°C Operation11
Electrical Characteristics—3 V, 125°C Operation13
Electrical Characteristics—Mixed 5 V/3 V, 125°C Operation
Electrical Characteristics—Mixed 3 V/5 V, 125°C Operation
Package Characteristics19
Regulatory Information19
0 /

Insulation and Safety-Related Specifications	19
DIN V VDE V 0884-10 (VDE V 0884-10) Insulation	
Characteristics	20
Recommended Operating Conditions	20
Absolute Maximum Ratings	21
ESD Caution	21
Pin Configurations and Function Descriptions	22
Typical Performance Characteristics	25
Applications Information	27
PC Board Layout	27
Propagation Delay-Related Parameters	27
DC Correctness and Magnetic Field Immunity	27
Power Consumption	28
Insulation Lifetime	29
Automotive Products	29
Outline Dimensions	30
Ordering Guide	30

REVISION HISTORY

5/08—Rev. F to Rev. G Added ADuM1400W, ADuM1401W, and ADuM	/1402W
Parts	Universal
Added Table 4	11
Added Table 5	
Added Table 6	15
Added Table 7	17
Changes to Table 12	20
Changes to Table 13	21
Added Automotive Products Section	29
Changes to Ordering Guide	

11/07—Rev. E to Rev. F

Changes to Note 11
Added ADuM140xARW Change vs. Temperature Parameter4
Added ADuM140xARW Change vs. Temperature Parameter5
Added ADuM140xARW Change vs. Temperature Parameter8
Changes to Figure 17
6 6

6/07—Rev. D to Rev. E

Updated VDE Certification Throughout	1
Changes to Features and Note 1	1
Changes to Figure 1, Figure 2, and Figure 3	1
Changes to Regulatory Information Section	10
Changes to Table 7	11
Added Table 10	12
Added Insulation Lifetime Section	20
Updated Outline Dimensions	21
Changes to Ordering Guide	21

2

2/06—Rev. C to Rev. D
Updated Format
Added TÜV Approval Universal
5/05—Rev. B to Rev. C
Changes to Format Universal
Changes to Figure 2
Changes to Table 3
Changes to Table 6
Changes to Ordering Guide21
6/04—Rev. A to Rev. B
Changes to FormatUniversal
Changes to Features
Changes to Electrical Characteristics—5 V Operation
Changes to Electrical Characteristics—3 V Operation
Changes to Electrical Characteristics—Mixed 5 V/3 V or 3 V/5
Changes to Electrical Characteristics—Mixed 5 V/3 V or 3 V/5 V Operation

14
15
nunity
21
22

Changes to the Ordering Guide19

Updated Format Universal

9/03—Revision 0: Initial Version

5/04—Rev. 0 to Rev. A

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V, 105°C OPERATION¹

 $4.5 \text{ V} \le V_{DD1} \le 5.5 \text{ V}$, $4.5 \text{ V} \le V_{DD2} \le 5.5 \text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^{\circ}$ C, $V_{DD1} = V_{DD2} = 5 \text{ V}$. These specifications do not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Table 1.

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	I _{DDI (Q)}		0.50	0.53	mA	
Output Supply Current per Channel, Quiescent	I _{DDO (Q)}		0.19	0.21	mA	
ADuM1400 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
VDD1 Supply Current	I _{DD1 (Q)}		2.2	2.8	mA	DC to 1 MHz logic signal freq.
VDD2 Supply Current	I _{DD2 (Q)}		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
VDD1 Supply Current	I _{DD1 (10)}		8.6	10.6	mA	5 MHz logic signal freq.
VDD2 Supply Current	I _{DD2 (10)}		2.6	3.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
VDD1 Supply Current	IDD1 (90)		70	100	mA	45 MHz logic signal freq.
VDD2 Supply Current	IDD2 (90)		18	25	mA	45 MHz logic signal freq.
ADuM1401 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	IDD1 (Q)		1.8	2.4	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	DD2 (Q)		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V _{DD1} Supply Current	IDD1 (10)		7.1	9.0	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (10)}		4.1	5.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V _{DD1} Supply Current	I _{DD1 (90)}		57	82	mA	45 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (90)}		31	43	mA	45 MHz logic signal freq.
ADuM1402 Total Supply Current, Four Channels ²						5 5 1
DC to 2 Mbps						
V _{DD1} or V _{DD2} Supply Current	IDD1 (Q), IDD2 (Q)		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)	(2)					
V _{DD1} or V _{DD2} Supply Current	IDD1 (10), IDD2 (10)		5.6	7.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)	1001(10), 1002(10)					
V _{DD1} or V _{DD2} Supply Current	DD1 (90), DD2 (90)		44	62	mA	45 MHz logic signal freq.
For All Models	1001 (30), 1002 (30)					
Input Currents	IIA, IIB, IIC, IID, IE1, IE2	-10	+0.01	+10	μA	$ \begin{array}{ c c c c c } 0 & V \leq V_{\text{IA}}, V_{\text{IB}}, V_{\text{IC}}, V_{\text{ID}} \leq V_{\text{DD1}} \text{ or } V_{\text{DD2}}, \\ 0 & V \leq V_{\text{E1}}, V_{\text{E2}} \leq V_{\text{DD1}} \text{ or } V_{\text{DD2}} \end{array} $
Logic High Input Threshold	VIH, VEH	2.0			v	
Logic Low Input Threshold	VIL, VEL			0.8	v	
Logic High Output Voltages	VOAH, VOBH,	(V _{DD1} or V _{DD2}) – 0.1	5.0	0.0	v	$I_{Ox} = -20 \ \mu A$, $V_{Ix} = V_{IxH}$
	Voch, Vodh	$(V_{DD1} \text{ or } V_{DD2}) - 0.4$			v	$I_{\text{Ox}} = -4 \text{ mA}, V_{\text{Ix}} = V_{\text{IxH}}$
Logic Low Output Voltages	Voal, Vobl,	(1001 01 1002) 011	0.0	0.1	v	$I_{\text{Ox}} = 20 \mu\text{A}, V_{\text{Ix}} = V_{\text{IxL}}$
	Vocl, Vodl		0.04	0.1	v	$I_{0x} = 400 \ \mu\text{A}, V_{1x} = V_{1xL}$
			0.2	0.4	v	$I_{\text{Ox}} = 4 \text{ mA}, V_{\text{Ix}} = V_{\text{IxL}}$
SWITCHING SPECIFICATIONS						
ADuM140xARW						
Minimum Pulse Width ³	PW			1000	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ⁴		1			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
		1.				$C_L = 15 \text{ pF}$, CMOS signal levels

ParameterSymbolMinTypMaxUnitTest ConditionsPulse Width Distortion, $ t_{Ru} - t_{Ru} ^3$ PWD40nsC, = 15 pF, CMOS signal levelsChange vs. Temperaturetrac50nsC, = 15 pF, CMOS signal levelsPropagation Delay Skew*trac50nsC, = 15 pF, CMOS signal levelsADUM140xBRWtrace/traceo50nsC, = 15 pF, CMOS signal levelsMaximum Data Rate*10msC, = 15 pF, CMOS signal levelsPropagation Delay*trnt, trnt203250nsC, = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{ru} - t_{ru} ^5$ trnt, trnt203250nsC, = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{ru} - t_{ru} ^5$ trnt, trnt203250nsC, = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{ru} - t_{ru} ^5$ trnt, trnt203nsC, = 15 pF, CMOS signal levelsPropagation Delay Skew*trac15nsC, = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels'trac, tran8.311.1nsC, = 15 pF, CMOS signal levelsADUM140xCRWtrac, tran, tran, tran, tran, tran, trac, tran, tran, tran, tran, tran, tran, tran, trac, tran, tran, trac, tran, t			1				r
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Parameter	Symbol	Min	Тур	Мах	Unit	Test Conditions
Propagation Delay Skew ⁶ tsx50nsC _i = 15 pF, CMOS signal levelsChannel-to-Channel Matching? t_{xxxv}/t_{bxxxv} 50nsC _i = 15 pF, CMOS signal levelsMinimum Pulse Width ³ PW10nsC _i = 15 pF, CMOS signal levelsMaximum Data Rate ⁴ 103250nsC _i = 15 pF, CMOS signal levelsPropagation Delay ⁵ tmit. twit203250nsC _i = 15 pF, CMOS signal levelsPulse Width Distortion, [tx+ - twt] ³ PWD3nsC _i = 15 pF, CMOS signal levelsPropagation Delay Skew ⁶ trax5pp?'CC _i = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channels'trax6nsC _i = 15 pF, CMOS signal levelsDirectional Channels'traxco6nsC _i = 15 pF, CMOS signal levelsMultimum Pulse Width ³ PW8.311.1nsC _i = 15 pF, CMOS signal levelsDirectional Channels'traxco6nsC _i = 15 pF, CMOS signal levelsPulse Width Distortion, [tx ₁₁ - twt] ³ PWD0.52nsC _i = 15 pF, CMOS signal levelsPulse Width Distortion, [tx ₁₁ - twt] ³ PWD0.52nsC _i = 15 pF, CMOS signal levelsPropagation Delay ⁵ trax10nsC _i = 15 pF, CMOS signal levels10Channel-to-Channel Matching, Codirectional Channel-to-Channel Matching, Codirectional Channel-to-Channel Matching, Codirectional Channel-to-Channel Matching, Codirectional Channel-to-Channel Matching, C	Pulse Width Distortion, t _{PLH} – t _{PHL} ⁵	PWD			40	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Change vs. Temperature			11		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
ADuM140x8RW Minimum Pulse Width³ Maximum Data Rate³PW10nsC = 15 pF, CMOS signal levels C = 15 pF, CMOS signal levels C = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{1,1} = t_{pre} ^{5}$ PWD3250nsC = 15 pF, CMOS signal levels C = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{1,1} = t_{pre} ^{5}$ PWD3nsC = 15 pF, CMOS signal levels D = 15 pF, CMOS signal levelsPropagation Delay Skew6tsx15nsC = 15 pF, CMOS signal levels T = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels7tsxco6nsC = 15 pF, CMOS signal levelsADuM140xCRWtsxco6nsC = 15 pF, CMOS signal levelsMaximum Data Rate³PWD8.311.1nsC = 15 pF, CMOS signal levelsPropagation Delay Stsxco6nsC = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{1,1} = t_{pre} ^{5}$ twit, $t_{1,11}$ 182732nsC = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{1,1} = t_{pre} ^{5}$ twit, $t_{1,11}$ 182732nsC = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{1,1} = t_{pre} ^{5}$ twit, $t_{1,11}$ 182732nsC = 15 pF, CMOS signal levelsPropagation Delay Skew6tsxco52nsC = 15 pF, CMOS signal levelstsxcoChannel-to-Channel Matching, Codirectional Channels7tsxco5nsC = 15 pF, CMOS signal levelsOutput Rise/Fa	Propagation Delay Skew ⁶	t _{PSK}			50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Minimum Pulse Width3 Maximum Data Rate4PW100ns $C_{i} = 15 pF, CMOS signal levelsMppsPropagation Delay5Pulse Width Distortion, [truit - truit]5T_{mit}, truitPWD203250nsC_{i} = 15 pF, CMOS signal levelsPulse Width Distortion, [truit - truit]5PWD31nsC_{i} = 15 pF, CMOS signal levelsPropagation Delay Skew5Channel-to-Channel Matching, CodirectionalChannels7tractor15nsC_{i} = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing-Directional Channels7tractor6nsC_{i} = 15 pF, CMOS signal levelsMinimum Pulse Width3Minimum Dulse Width3PW8.311.1nsC_{i} = 15 pF, CMOS signal levelsPropagation Delay6tractor100120MbpsC_{i} = 15 pF, CMOS signal levelsPropagation Delay6tractor182732nsC_{i} = 15 pF, CMOS signal levelsPropagation Delay6tractor100nsC_{i} = 15 pF, CMOS signal levels100Propagation Delay6tractor100nsC_{i} = 15 pF, CMOS signal levelsPropagation Delay6tractor100nsC_{i} = 15 pF, CMOS signal levelsPropagation Delay76tractor182732nsC_{i} = 15 pF, CMOS signal levelsPropagation Delay76tractor100nsC_{i} = 15 pF, CMOS signal levels100Propagation Delay76tractor2nsC_{i} = 15 pF, CMOS signal levelsPropagation Delay76$	Channel-to-Channel Matching ⁷	t _{PSKCD} /t _{PSKOD}			50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ⁴ 10 $C_{c} = 15 pF, CMOS signal levelsPropagation Delay5twit, twit203250nsC_{c} = 15 pF, CMOS signal levelsPulse Width Distortion, t_{DLI} - t_{rel} ^{5}PWD3nsC_{c} = 15 pF, CMOS signal levelsPropagation Delay Skew6tryx15nsC_{c} = 15 pF, CMOS signal levelsPropagation Delay Skew6tryx15nsC_{c} = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channels7tryx3nsC_{c} = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing-Directional Channels7tryx6nsC_{c} = 15 pF, CMOS signal levelsADUM 140xCRWminimum Pulse Width3PW8.311.1nsC_{c} = 15 pF, CMOS signal levelsPropagation Delay6trw, trut182732nsC_{c} = 15 pF, CMOS signal levelsPropagation Delay6trw, trut182732nsC_{c} = 15 pF, CMOS signal levelsPropagation Delay6trw, trut182732nsC_{c} = 15 pF, CMOS signal levelsPropagation Delay Skew6trex10nsC_{c} = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channels7trex10nsC_{c} = 15 pF, CMOS signal levelsPropagation Delay Skew6trex10nsC_{c} = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional channels7trex2nsC_{c} = 15 pF, CMOS signal l$	ADuM140xBRW						
Propagation Delays t_{eval}, t_{truel} 203250ns $C_{c} = 15 pF, CMOS signal levels$ Pulse Width Distortion, $ t_{W,H} - t_{eval} ^{5}$ PWD5ns $C_{c} = 15 pF, CMOS signal levels$ Propagation Delay Skew ⁶ t_exc1ns $C_{c} = 15 pF, CMOS signal levels$ Channel-to-Channel Matching, Codirectional Channels't_exc3ns $C_{c} = 15 pF, CMOS signal levels$ Channel-to-Channel Matching, Opposing- Directional Channels't_exco3ns $C_{c} = 15 pF, CMOS signal levels$ ADUM140xCRWt_exco8.311.1ns $C_{c} = 15 pF, CMOS signal levels$ Minimum Pulse Width ³ PW8.311.1ns $C_{c} = 15 pF, CMOS signal levels$ Propagation Delay Kew ⁶ t_exco32ns $C_{c} = 15 pF, CMOS signal levels$ Propagation Delay Kew ⁶ text, truu182732ns $C_{c} = 15 pF, CMOS signal levels$ Propagation Delay Skew ⁶ text, truu182732ns $C_{c} = 15 pF, CMOS signal levels$ Propagation Delay Skew ⁶ text, truu182732ns $C_{c} = 15 pF, CMOS signal levels$ Channel-to-Channel Matching, Codirectional Channel-to-Channel Matching, Opposing- Directional Channels'text, truu1ns $C_{c} = 15 pF, CMOS signal levels$ Output Disable Propagation Delay (High/Low to High Impedance)text, truu1ns $C_{c} = 15 pF, CMOS signal levels$ Output Enable Propagation Delay (High/Low to High Impedance)text, truu <td>Minimum Pulse Width³</td> <td>PW</td> <td></td> <td></td> <td>100</td> <td>ns</td> <td>$C_L = 15 \text{ pF}$, CMOS signal levels</td>	Minimum Pulse Width ³	PW			100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, $ t_{VH} - t_{PHL} ^S$ PWD3nsC _i = 15 pF, CMOS signal levelsPropagation Delay Skew ⁶ t_{Pask15nsC _i = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channels't_Pasko3nsC _i = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels't_Pasko6nsC _i = 15 pF, CMOS signal levelsADuM140xCRWt_Pasko6nsC _i = 15 pF, CMOS signal levelsC _i = 15 pF, CMOS signal levelsMaximum Pulse Width ³ PW8.311.1nsC _i = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{VH} - t_{PRL} ^S$ PW8.311.1nsC _i = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{VH} - t_{PRL} ^S$ PWD0.52nsC _i = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{VH} - t_{PRL} ^S$ PWD0.52nsC _i = 15 pF, CMOS signal levelsPropagation Delay'st_Paskot_Pasko10nsC _i = 15 pF, CMOS signal levelsPropagation Delay Skew ⁶ t_Pasko10nsC _i = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channel't_Pasko5nsC _i = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channel't_Pasko5nsC _i = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channel't_Pasko5nsC _i = 15 pF, CMOS signal levelsOutput Enable Propagat	Maximum Data Rate ⁴		10			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperatureps//CC = 15 pF, CMOS signal levelsPropagation Delay Skew ⁴ tesc15nsC = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels'tesco6nsC = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels'tesco6nsC = 15 pF, CMOS signal levelsADuM140xCRWtesco6nsC = 15 pF, CMOS signal levelsMaximum Data Rate ⁴ PW8.311.1nsC = 15 pF, CMOS signal levelsPropagation Delaytesco6nsC = 15 pF, CMOS signal levelsPulse Width Distortion, [tsun - tone]tesco8.311.1nsC = 15 pF, CMOS signal levelsPropagation Delaytesco6nsC = 15 pF, CMOS signal levelsc = 15 pF, CMOS signal levelsPropagation Delaytesco0.52nsC = 15 pF, CMOS signal levelsPropagation Delay Skew ⁴ tesc10nsC = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channels'tesco2nsC = 15 pF, CMOS signal levelsDirectional Channels'tesco5nsC = 15 pF, CMOS signal levelsOutput Disable Propagation Delay (High Impedance)tesco5nsC = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%)tescotesco5nsC = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%)tescotesco5nsC = 15 pF, CMOS sig	Propagation Delay ⁵	t _{PHL} , t _{PLH}	20	32	50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶ t_{55K} t_{55K} 15ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Channel-to-Channel Matching, Opposing- Directional Channels7 t_{55K00} s_{5K00} ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ ADuM140xCRWPW8.311.1ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Minimum Pulse Width3PW8.311.1ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Maximum Data Rate490120Mbps $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Propagation Delay5tr=t_H_L tr_LH182732ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$ PWD 0.5 2ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Propagation Delay5tr=t_H_L tr_LH182732ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Propagation Delay Skew ⁶ tr=t_R_L tr_LH182732ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Channel to-Channel Matching, Codirectional Channels7tr=sxc10ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Channel-to-Channel Matching, Opposing- Directional Channels7tr=sxc5ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Output Disable Propagation Delay (High/Low to High Impedance)tr=sxc68ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Output Rise/Fall Time (10% to 90%) High Output8tr=st_L tr=st_L tr=	Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Change vs. Temperature			5		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Propagation Delay Skew ⁶	t _{PSK}			15	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Directional Channels?PW8.31.1nsCL = 15 pF, CMOS signal levelsMunimum Pulse Width3PW8.311.1nsCL = 15 pF, CMOS signal levelsMaximum Data Rate490120MbpsCL = 15 pF, CMOS signal levelsPropagation Delay5treat, true182732nsCL = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$ PWD0.52nsCL = 15 pF, CMOS signal levelsChange vs. Temperature3ps/°CCL = 15 pF, CMOS signal levelssignal levelsPropagation Delay Skew6trsx10nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channels7trsx10nsCL = 15 pF, CMOS signal levelsFor All Modelstrsx, true5nsCL = 15 pF, CMOS signal levelsOutput Disable Propagation Delay (High/Low to High Impedance)trax, true68nsCL = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%)tr/tr2.5nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic High Output8[CMi,]2535kV/µsV _N = Voi, or Voice, Voin = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current per Channel9fr.1.2MbpskV/µsV _N = 000 V, transient magnitude = 800 V		t _{PSKCD}			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Minimum Pulse Width3PW8.311.1nsCL = 15 pF, CMOS signal levelsMaximum Data Rate490120MbpsCL = 15 pF, CMOS signal levelsPropagation Delay5tPHL, tPLH182732nsCL = 15 pF, CMOS signal levelsPulse Width Distortion, [tpLH - tPHL]5PWD0.52nsCL = 15 pF, CMOS signal levelsPropagation Delay Skew6tesk3ps/°CCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channels7tesk10nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels7tesk5nsCL = 15 pF, CMOS signal levelsFor All Modelsteskcteskc5nsCL = 15 pF, CMOS signal levelsOutput Disable Propagation Delay (High/Low to High Impedance)teskcteskc5nsCL = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%)ta/trteskc68nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output8[CMH]2535kV/µsV _k = Voit or Voicy, Vcin = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current per Channel9fr1.2MbpskV/µsV _k = 0.0 V, transient magnitude = 800 V		t _{PSKOD}			6	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate490120Mbps $C_L = 15 \text{ pF}$, CMOS signal levelsPropagation Delay5 t_{PHL}, t_{PLH} 182732ns $C_L = 15 \text{ pF}$, CMOS signal levelsPulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$ PWD0.52ns $C_L = 15 \text{ pF}$, CMOS signal levelsChange vs. Temperature3 $ps/^{9}C$ $C_L = 15 \text{ pF}$, CMOS signal levels rs_{K} 10ns $C_L = 15 \text{ pF}$, CMOS signal levelsPropagation Delay Skew6 t_{rs_K} 10ns $C_L = 15 \text{ pF}$, CMOS signal levels rs_{K} $L = 15 \text{ pF}$, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channels7 t_{PSKOD} s_{SKOD} s_{SKO	ADuM140xCRW						
Propagation Delays t_{PHL}, t_{PLH} 182732ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^S$ PWD0.52ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Change vs. Temperature30ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Propagation Delay Skew ⁶ tesk10ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Channel-to-Channel Matching, Codirectional Channels7tesk2ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Channel-to-Channel Matching, Opposing- Directional Channels7teskoo5ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ For All Modelsthigh Impedance)teskooteskoo68ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Output Enable Propagation Delay (High/Low to High Impedance to High/Lowtes/te2sns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Output Rise/Fall Time (10% to 90%)tes/tetes/te2.5ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}$ Common-Mode Transient Immunity at Logic Low Output ⁸ [CML]2535kV/µs $V_{ix} = V_{DD1} \text{ or V}_{DD2}, V_{CM} = 1000 V,transient magnitude = 800 VRefresh RateInput Dynamic Supply Current per Channel9fr1.2MbpsM/Mbps$	Minimum Pulse Width ³	PW		8.3	11.1	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t_{PLH} - t_PHL 5PWD0.52nsCL = 15 pF, CMOS signal levelsChange vs. Temperature3ps/°CCL = 15 pF, CMOS signal levelsCL = 15 pF, CMOS signal levelsPropagation Delay Skew ⁶ t_PSK10nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channels7t_PSKD2nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels7t_PSKD5nsCL = 15 pF, CMOS signal levelsFor All ModelstpskDt_PHZ, tPLH68nsCL = 15 pF, CMOS signal levelsOutput Disable Propagation Delay (High/Low to High Impedance)t_PHZ, tPLH68nsCL = 15 pF, CMOS signal levelsOutput Enable Propagation Delay (High Impedance to High/Low High Output ⁸ t_PZH, tPZL68nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output ⁸ [CML]2535kV/µsV _{Ik} = Voi or Vooz, VCM = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current per Channel ⁹ fr1.2MbpsWbps	Maximum Data Rate ⁴		90	120		Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperature3ps/°CCL = 15 pF, CMOS signal levelsPropagation Delay Skew6tresk10nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channels7tresk02nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels7tresk0D5nsCL = 15 pF, CMOS signal levelsFor All ModelsOutput Disable Propagation Delay (High/Low to High Impedance)tresk0D5nsCL = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%)trest, trezh, trezh68nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output*Common-Mode Transient Immunity at Logic Low Output*[CML]2535kV/µsV _{ix} = Void or Void V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current per Channel*fr1.2MbpsMps	Propagation Delay ⁵	t _{PHL} , t _{PLH}	18	27	32	ns	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew6trsk10nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Codirectional Channels7trskcD2nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels7trskoD5nsCL = 15 pF, CMOS signal levelsFor All ModelsOutput Disable Propagation Delay (High/Low to High Impedance)trext, trezt,68nsCL = 15 pF, CMOS signal levelsOutput Enable Propagation Delay (High Impedance of High/Low Output Rise/Fall Time (10% to 90%)trezt, trezt,68nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output8tre/tre2.5nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output8[CML]2535kV/µsV _{Ik} = 0 v, V _{CM} = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current per Channel9fr1.2MbpsMpsInput Dynamic Supply Current per Channel9fr1.2Mbps	Pulse Width Distortion, t _{PLH} – t _{PHL} ⁵	PWD		0.5	2	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels7t PSKCD2nsC L = 15 pF, CMOS signal levelsChannels7Channels75nsC L = 15 pF, CMOS signal levelsFor All Models5nsC L = 15 pF, CMOS signal levelsOutput Disable Propagation Delay (High/Low to High Impedance)t PHZ, t PZH, t MZH, t MERt PHZ, t PZH,	Change vs. Temperature			3		ps/°C	C _L = 15 pF, CMOS signal levels
Channels7tPSKOD5nsCL = 15 pF, CMOS signal levelsDirectional Channels7TorHZ, tPLH68nsCL = 15 pF, CMOS signal levelsFor All ModelstorHz, tPLH68nsCL = 15 pF, CMOS signal levelsOutput Disable Propagation Delay (High/Low to High Impedance)torHz, tPLH68nsCL = 15 pF, CMOS signal levelsOutput Enable Propagation Delay (High Impedance to High/LowtpzH, tPZL68nsCL = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%)ta/tF2.5nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic High Output8[CMH]2535kV/µsVix = VDD1 or VDD2, VCM = 1000 V, transient magnitude = 800 VCommon-Mode Transient Immunity at Logic Low Output8fr1.2MbpsNsVix = 0 V, VCM = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current per Channel9fr1.2MbpsMaps	Propagation Delay Skew ⁶	t _{PSK}			10	ns	C _L = 15 pF, CMOS signal levels
Directional Channels?The second s	5.	t _{PSKCD}			2	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Disable Propagation Delay (High/Low to High Impedance) tPHZ, tPLH - - 6 8 ns CL = 15 pF, CMOS signal levels Output Enable Propagation Delay (High Impedance) tp2H, tp2L 6 8 ns CL = 15 pF, CMOS signal levels Output Enable Propagation Delay (High Impedance to High/Low tp2H, tp2L 6 8 ns CL = 15 pF, CMOS signal levels Output Rise/Fall Time (10% to 90%) ts/ts 2.5 ns CL = 15 pF, CMOS signal levels Common-Mode Transient Immunity at Logic Low Output ⁸ [CMH] 25 35 kV/µs Vix = VpD1 or VpD2, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V Vix = 0 V, VcM = 1000 V, transient magnitude = 800 V <td></td> <td>tрsкоd</td> <td></td> <td></td> <td>5</td> <td>ns</td> <td>$C_L = 15 \text{ pF}$, CMOS signal levels</td>		t рsкоd			5	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
to High Impedance)tOutput Enable Propagation Delay (High Impedance to High/LowtOutput Rise/Fall Time (10% to 90%)tCommon-Mode Transient Immunity at Logic High Output8tCommon-Mode Transient Immunity at Logic Low Output 8ICMH2535KV/µsVIx = VDD1 or VDD2, VCM = 1000 V, transient magnitude = 800 VCommon-Mode Transient Immunity at Logic Low Output8ICML2535KV/µsRefresh Rate Input Dynamic Supply Current per Channel9fr1.2Mbps 0.19MbpsMapping	For All Models						
Impedance to High/Lowta/tr2.5nsCL = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%)ta/tr2535kV/µsVL = V_{DD1} or V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 VCommon-Mode Transient Immunity at Logic High Output8ICML2535kV/µsVL = 0 V, V_{CM} = 1000 V, transient magnitude = 800 VCommon-Mode Transient Immunity at Logic Low Output8ICML2535kV/µsVL = 0 V, V_{CM} = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current per Channel9fr1.2MbpsMbps		TPHZ, TPLH		6	- 8 -	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output8ICMH2535kV/µsVIx = V_{DD1} or V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 VCommon-Mode Transient Immunity at Logic Low Output8ICML2535kV/µsVIx = 0 V, V_{CM} = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current per Channel9fr1.2MbpsMbps		t _{PZH} , t _{PZL}		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
High Output ⁸ Image: Common-Mode Transient Immunity at Logic Low Output ⁸ ICML 25 35 KV/µs transient magnitude = 800 V Refresh Rate fr 1.2 Mbps Input Dynamic Supply Current per Channel ⁹ Input Dynamic Supply Current per Channel ⁹ 0.19 mA/Mbps	Output Rise/Fall Time (10% to 90%)	t _R /t _F		2.5		ns	C _L = 15 pF, CMOS signal levels
Low Output ⁸ Image: Constraint of the second se		CM _H	25	35		kV/μs	
Input Dynamic Supply Current per Channel ⁹ IDDI (D) 0.19 MA/Mbps		CML	25	35		kV/μs	
	Refresh Rate	fr		1.2		Mbps	
Output Dynamic Supply Current per Channel ⁹ IDDO (D) 0.05 mA/Mbps	Input Dynamic Supply Current per Channel ⁹	I _{DDI (D)}		0.19		mA/Mbps	
	Output Dynamic Supply Current per Channel ⁹	IDDO (D)		0.05		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V, 105°C OPERATION¹

 $2.7 \text{ V} \le V_{DD1} \le 3.6 \text{ V}$, $2.7 \text{ V} \le V_{DD2} \le 3.6 \text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^{\circ}$ C, $V_{DD1} = V_{DD2} = 3.0 \text{ V}$. These specifications do not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
DC SPECIFICATIONS			.,,			
Input Supply Current per Channel, Quiescent	IDDI (Q)		0.26	0.31	mA	
Output Supply Current per Channel, Quiescent			0.11	0.14	mA	
ADuM1400 Total Supply Current, Four Channels ²	1000 (Q)		0.11	0.11		
DC to 2 Mbps						
V _{DD1} Supply Current	IDD1 (Q)		1.2	1.9	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (Q)}		0.5	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)	1002(0)		0.0	012		2 c to 1
V _{DD1} Supply Current	I _{DD1 (10)}		4.5	6.5	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	IDD2 (10)		1.4	2.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)	1002 (10)			2.0		5 ···· · <u>-</u> · · · g· · · · · · · · · · · · · · · ·
V _{DD1} Supply Current	I _{DD1 (90)}		37	65	mA	45 MHz logic signal freq.
V _{DD2} Supply Current	IDD1 (90)		11	15	mA	45 MHz logic signal freq.
ADuM1401 Total Supply Current, Four Channels ²	1002 (90)		••	15		is mile logic signal freq.
DC to 2 Mbps						
V _{DD1} Supply Current	IDD1 (Q)		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current			0.7	1.2	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)	1002 (Q)		0.7	1.2		De to Think logic signarrieq.
V _{DD1} Supply Current	I _{DD1 (10)}		3.7	5.4	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	IDD1 (10)		2.2	3.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)	1002(10)		2.2	5.0		5 Minz logic signar req.
V _{DD1} Supply Current	I _{DD1 (90)}		30	52	mA	45 MHz logic signal freq.
V _{DD2} Supply Current	IDD1 (90)		18	27	mA	45 MHz logic signal freq.
ADuM1402 Total Supply Current, Four Channels ²	IDD2 (90)		10	27		+5 Miliz logic signarrieq.
DC to 2 Mbps						
V _{DD1} or V _{DD2} Supply Current	I _{DD1 (Q)} , I _{DD2 (Q)}		0.9	1.5	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)	DD1 (Q), DD2 (Q)		0.9	1.5		De to T Minz logic signal freq.
V _{DD1} or V _{DD2} Supply Current	I _{DD1 (10)} , I _{DD2 (10)}		3.0	4.2	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)	DD1 (10), DD2 (10)		5.0	7.2		5 miliziogie signal freq.
V _{DD1} or V _{DD2} Supply Current	IDD1 (90), IDD2 (90)		24	39	mA	45 MHz logic signal freq.
For All Models	IDD1 (90), IDD2 (90)		24	29	IIIA	
Input Currents	IIA, IIB, IIC,	-10	+0.01	+10	μA	$0 \text{ V} \leq V_{IA}, V_{IB}, V_{IC}, V_{ID} \leq V_{DD1} \text{ or } V_{DD2}$
input currents	IIA, IIB, IIC, IID, IE1, IE2	-10	+0.01	+10	μΑ	$0 V \leq V_{IA}$, VIB, VIC, VID $\leq V_{DD1}$ OI VDD2 $0 V \leq V_{E1}$, $V_{E2} \leq V_{DD1}$ or V_{DD2}
Logic High Input Threshold	VIH, VEH	1.6			v	
Logic Low Input Threshold	VIL, VEL			0.4	v	
Logic High Output Voltages	Vоан, Vовн,	(V _{DD1} or V _{DD2}) – 0.1	3.0	•••	v	$I_{0x} = -20 \ \mu A, V_{1x} = V_{1xH}$
	V _{OCH} , V _{ODH}	$(V_{DD1} \text{ or } V_{DD2}) - 0.4$	2.8		v	$I_{0x} = -4 \text{ mA}, V_{1x} = V_{1xH}$
Logic Low Output Voltages	VOAL, VOBL,	(1001 01 1002) 011	0.0	0.1	v	$I_{\text{Ox}} = 20 \ \mu\text{A}, V_{\text{Ix}} = V_{\text{IxL}}$
	Vocl, Vodl		0.04	0.1	v	$I_{0x} = 400 \ \mu A, V_{1x} = V_{1xL}$
			0.2	0.4	v	$I_{\text{Ox}} = 4 \text{ mA}, V_{\text{Ix}} = V_{\text{IxL}}$
WITCHING SPECIFICATIONS			0.2	0.1	ŀ	
ADuM140xARW						
Minimum Pulse Width ³	PW			1000	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴	· · ·	1			Mbps	
Propagation Delay ⁵	tphl, tplh	50	75	100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD		, ,	40	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperature			11	10	ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			50	ns	$C_L = 15 \text{ pF}, \text{CMOS signal levels}$ $C_L = 15 \text{ pF}, \text{CMOS signal levels}$
riopugation Delay sitew	•PSK			50	113	$c_{L} = 15 \text{ pr}$, civitos signal levels

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Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
ADuM140xBRW						
Minimum Pulse Width ³	PW			100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁵	tphl, tplh	20	38	50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			22	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t _{PSKCD}			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels ⁷	t pskod			6	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
ADuM140xCRW						
Minimum Pulse Width ³	PW		8.3	11.1	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ⁴		90	120		Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	tphl, tplh	20	34	45	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, t _{PLH} – t _{PHL} ⁵	PWD		0.5	2	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			16	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t pskcd			2	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels ⁷	t pskod			5	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	tphz, tplh		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	tpzh, tpzl		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		3		ns	C _L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output [®]	CM _H	25	35		kV/µs	$V_{Ix} = V_{DD1}$ or V_{DD2} , $V_{CM} = 1000$ V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	CM⊾	25	35		kV/µs	$V_{lx} = 0 V, V_{CM} = 1000 V,$ transient magnitude = 800 V
Refresh Rate	fr		1.1		Mbps	
Input Dynamic Supply Current per Channel ⁹	I _{DDI (D)}		0.10		mA/ Mbps	
Output Dynamic Supply Current per Channel ⁹	I _{DDO (D)}		0.03		mA/ Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.</p>

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

ELECTRICAL CHARACTERISTICS-MIXED 5 V/3 V OR 3 V/5 V, 105°C OPERATION¹

5 V/3 V operation: $4.5 \text{ V} \le \text{V}_{\text{DD1}} \le 5.5 \text{ V}$, $2.7 \text{ V} \le \text{V}_{\text{DD2}} \le 3.6 \text{ V}$; 3 V/5 V operation: $2.7 \text{ V} \le \text{V}_{\text{DD1}} \le 3.6 \text{ V}$, $4.5 \text{ V} \le \text{V}_{\text{DD2}} \le 5.5 \text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^{\circ}\text{C}$; $V_{\text{DD1}} = 3.0 \text{ V}$, $V_{\text{DD2}} = 5 \text{ V}$ or $V_{\text{DD1}} = 5 \text{ V}$, $V_{\text{DD2}} = 3.0 \text{ V}$. These specifications do not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Table	3.
I ubic	••

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	I _{DDI (Q)}					
5 V/3 V Operation			0.50	0.53	mA	
3 V/5 V Operation			0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	IDDO (Q)					
5 V/3 V Operation			0.11	0.14	mA	
3 V/5 V Operation			0.19	0.21	mA	
ADuM1400 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	IDD1 (Q)					
5 V/3 V Operation			2.2	2.8	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.9	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (Q)}					
5 V/3 V Operation			0.5	0.9	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V _{DD1} Supply Current	I _{DD1 (10)}					
5 V/3 V Operation			8.6	10.6	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.5	6.5	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (10)}					
5 V/3 V Operation			1.4	2.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.6	3.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V _{DD1} Supply Current	I _{DD1 (90)}					
5 V/3 V Operation			70	100	mA	45 MHz logic signal freq.
3 V/5 V Operation			37	65	mA	45 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (90)}					
5 V/3 V Operation			11	15	mA	45 MHz logic signal freq.
3 V/5 V Operation			18	25	mA	45 MHz logic signal freq.
ADuM1401 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	IDD1 (Q)					
5 V/3 V Operation			1.8	2.4	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.0	1.6	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	IDD2 (Q)					
5 V/3 V Operation			0.7	1.2	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V _{DD1} Supply Current	I _{DD1 (10)}					
5 V/3 V Operation			7.1	9.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.7	5.4	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (10)}					
5 V/3 V Operation			2.2	3.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.1	5.0	mA	5 MHz logic signal freq.

Parameter	Symbol	Min	Тур	Мах	Unit	Test Conditions
90 Mbps (CRW Grade Only)	59/11501		• 7 P	Max	0	
V _{DD1} Supply Current	I _{DD1 (90)}					
5 V/3 V Operation	IDD1 (90)		57	82	mA	45 MHz logic signal freq.
3 V/5 V Operation			30	52	mA	45 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (90)}		50	52	110.	45 Milž logic signal freq.
5 V/3 V Operation	1002 (90)		18	27	mA	45 MHz logic signal freq.
3 V/5 V Operation			31	43	mA	45 MHz logic signal freq.
ADuM1402 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	IDD1 (Q)					
5 V/3 V Operation	IDDT (Q)		1.5	2.1	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.5	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	IDD2 (Q)		0.9	1.5	110.	De to i milžiogle signa neq.
5 V/3 V Operation	1002 (Q)		0.9	1.5	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)			1.5	2.1		be to think logic signal freq.
V _{DD1} Supply Current	I _{DD1 (10)}					
5 V/3 V Operation	1001 (10)		5.6	7.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.0	4.2	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	IDD2 (10)		5.0			s milž logic signar req.
5 V/3 V Operation	1002 (10)		3.0	4.2	mA	5 MHz logic signal freq.
3 V/5 V Operation			5.6	7.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)			510			5 <u>2</u> .eg.e signal neq.
V _{DD1} Supply Current	IDD1 (90)					
5 V/3 V Operation	1001 (50)		44	62	mA	45 MHz logic signal freq.
3 V/5 V Operation			24	39	mA	45 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (90)}		- ·			
5 V/3 V Operation	1002 (50)		24	39	mA	45 MHz logic signal freq.
3 V/5 V Operation			44	62	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I _{IA} , I _{IB} , I _{IC} ,	-10	+0.01	+10	μA	$0 \text{ V} \leq V_{IA}, V_{IB}, V_{IC}, V_{ID} \leq V_{DD1} \text{ or}$
	I _{ID} , I _{E1} , I _{E2}				T.	V_{DD2} , $0 V \le V_{E1}$, $V_{E2} \le V_{DD1}$ or V_{DD2}
Logic High Input Threshold	VIH, VEH					
5 V/3 V Operation		2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	VIL, VEL					
5 V/3 V Operation				0.8	V	
3 V/5 V Operation				0.4	V	
Logic High Output Voltages	Vоан, Vовн,	(V _{DD1} or V _{DD2}) - 0.1	(V _{DD1} or V _{DD2})		V	$I_{\text{Ox}} = -20 \; \mu\text{A} \text{, } V_{\text{Ix}} = V_{\text{IxH}}$
	Voch, Vodh	$(V_{DD1} \text{ or } V_{DD2}) - 0.4$	$(V_{DD1} \text{ or } V_{DD2}) - 0.2$		V	$I_{Ox} = -4 \text{ mA}, V_{Ix} = V_{IxH}$
Logic Low Output Voltages	VOAL, VOBL,		0.0	0.1	V	$I_{Ox}=20~\mu A,V_{Ix}=V_{IxL}$
	Vocl, Vodl		0.04	0.1	V	$I_{\text{Ox}} = 400 \; \mu\text{A}, V_{\text{Ix}} = V_{\text{IxL}}$
			0.2	0.4	V	$I_{Ox} = 4 \text{ mA}, V_{Ix} = V_{IxL}$
SWITCHING SPECIFICATIONS						
ADuM140xARW						
Minimum Pulse Width ³	PW			1000	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ⁴		1			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁵	tphl, tplh	50	70	100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, tplh – tphl ⁵	PWD			40	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			11		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching ⁷	t _{PSKCD} /t _{PSKOD}			50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
ADuM140xBRW						
Minimum Pulse Width ³	PW			100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁵	tphl, tplh	15	35	50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
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Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			3	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			22	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t pskcd			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels ⁷	t pskod			6	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
ADuM140xCRW						
Minimum Pulse Width ³	PW		8.3	11.1	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ⁴		90	120		Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁵	tphl, tplh	20	30	40	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD		0.5	2	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperature			3		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			14	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t _{PSKCD}			2	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels ⁷	t pskod			5	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	tphz, tplh		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	tpzh, tpzl		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F					$C_L = 15 \text{ pF}$, CMOS signal levels
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output ⁸	CM _H	25	35		kV/μs	$V_{Ix} = V_{DD1}$ or V_{DD2} , $V_{CM} = 1000$ V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	CML	25	35		kV/μs	$V_{Ix} = 0 V$, $V_{CM} = 1000 V$, transient magnitude = 800 V
Refresh Rate	fr					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current per Channel ⁹	I _{DDI (D)}					
5 V/3 V Operation			0.19		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current per Channel ⁹	IDDO (D)					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

 8 CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—5 V, 125°C OPERATION¹

 $4.5 \text{ V} \le V_{DD1} \le 5.5 \text{ V}$, $4.5 \text{ V} \le V_{DD2} \le 5.5 \text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^{\circ}$ C, $V_{DD1} = V_{DD2} = 5 \text{ V}$. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Table 4.	1	1				
Parameter	Symbol	Min	Тур	Мах	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	I _{DDI (Q)}		0.50	0.53	mA	
Output Supply Current per Channel, Quiescent	IDDO (Q)		0.19	0.21	mA	
ADuM1400W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
VDD1 Supply Current	I _{DD1 (Q)}		2.2	2.8	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (Q)}		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
VDD1 Supply Current	I _{DD1 (10)}		8.6	10.6	mA	5 MHz logic signal freq.
VDD2 Supply Current	I _{DD2 (10)}		2.6	3.5	mA	5 MHz logic signal freq.
ADuM1401W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
VDD1 Supply Current	IDD1 (Q)		1.8	2.4	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (Q)}		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} Supply Current	I _{DD1 (10)}		7.1	9.0	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	IDD2 (10)		4.1	5.0	mA	5 MHz logic signal freq.
ADuM1402W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} or V _{DD2} Supply Current	IDD1 (Q), IDD2 (Q)		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} or V _{DD2} Supply Current	I _{DD1 (10)} , I _{DD2 (10)}		5.6	7.0	mA	5 MHz logic signal freq.
For All Models						
Input Currents	IIA, IIB, IIC,	-10	+0.01	+10	μA	$0 \leq V_{IA}, V_{IB}, V_{IC}, V_{ID} \leq V_{DD1} \text{ or } V_{DD2},$
	IID, IE1, IE2				L	$0 \le V_{E1}, V_{E2} \le V_{DD1} \text{ or } V_{DD2}$
Logic High Input Threshold	VIH, VEH	2.0			V	
Logic Low Input Threshold	VIL, VEL			0.8	v	
Logic High Output Voltages	Voah, Vobh,	(V _{DD1} or V _{DD2}) - 0.1	5.0		v	$I_{Ox} = -20 \ \mu A$, $V_{Ix} = V_{IxH}$
	Voch, Vodh	(V _{DD1} or V _{DD2}) - 0.4	4.8		v	$I_{\text{Ox}} = -4 \text{ mA}, V_{\text{Ix}} = V_{\text{IxH}}$
Logic Low Output Voltages	VOAL, VOBL,		0.0	0.1	v	$I_{Ox} = 20 \ \mu A$, $V_{Ix} = V_{IxL}$
	Vocl, Vodl		0.04	0.1	v	$I_{0x} = 400 \ \mu A, V_{1x} = V_{1xL}$
			0.2	0.4	v	$I_{\text{Ox}} = 4 \text{ mA}, V_{\text{Ix}} = V_{\text{IxL}}$
SWITCHING SPECIFICATIONS						
ADuM140xWSRWZ						
Minimum Pulse Width ³	PW			1000	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate⁴		1			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁵	tphl, tplh	50	65	100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			40	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching ⁷	t _{PSKCD} /t _{PSKOD}			50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels

Parameter	Symbol	Min	Тур	Мах	Unit	Test Conditions
ADuM140xWTRWZ	-					
Minimum Pulse Width ³	PW			100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁵	tphl, tplh	18	27	32	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			15	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t _{PSKCD}			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels ⁷	t pskod			6	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	tphz, tplh		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low	tpzh, tpzl		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		2.5		ns	$C_{L} = 15 \text{ pF}$, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁸	CM _H	25	35		kV/μs	$V_{lx} = V_{DD1}/V_{DD2}$, $V_{CM} = 1000 V$, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	CM∟	25	35		kV/μs	$V_{lx} = 0 V, V_{CM} = 1000 V,$ transient magnitude = 800 V
Refresh Rate	fr		1.2		Mbps	
Input Dynamic Supply Current per Channel ⁹	I _{DDI (D)}		0.19		mA/Mbps	
Output Dynamic Supply Current per Channel ⁹	IDDO (D)		0.05		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V, 125°C OPERATION¹

 $3.0 \text{ V} \le \text{V}_{\text{DD1}} \le 3.6 \text{ V}$, $3.0 \text{ V} \le \text{V}_{\text{DD2}} \le 3.6 \text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{\text{DD1}} = V_{\text{DD2}} = 3.0 \text{ V}$. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Table 5. Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
DC SPECIFICATIONS	Symbol		тур	Max	Unit	
Input Supply Current per Channel, Quiescent	IDDI (O)		0.26	0.31	mA	
Output Supply Current per Channel, Quescent			0.20	0.14	mA	
ADuM1400W, Total Supply Current, Four Channels ²	IDDO (Q)		0.11	0.14	mA	
DC to 2 Mbps						
•			1.2	1.9	mA	DC to 1 MHz logic signal freq.
V _{DD1} Supply Current V _{DD2} Supply Current	DD1 (Q)		0.5	0.9	mA	DC to 1 MHz logic signal freq.
	DD2 (Q)		0.5	0.9	mA	DC to T MHZ logic signal freq.
10 Mbps (TRWZ Grade Only)			4 5	65		
V _{DD1} Supply Current	DD1 (10)		4.5	6.5	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	DD2 (10)		1.4	2.0	mA	5 MHz logic signal freq.
ADuM1401W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	DD1 (Q)		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (Q)}		0.7	1.2	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
	IDD1 (10)		3.7	5.4	mA	5 MHz logic signal freq.
VDD2 Supply Current	I _{DD2 (10)}		2.2	3.0	mA	5 MHz logic signal freq.
ADuM1402W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
VDD1 or VDD2 Supply Current	$I_{\text{DD1 (Q)}}, I_{\text{DD2 (Q)}}$		0.9	1.5	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
VDD1 or VDD2 Supply Current	I _{DD1 (10)} , I _{DD2 (10)}		3.0	4.2	mA	5 MHz logic signal freq.
For All Models						
Input Currents	I _{IA} , I _{IB} , I _{IC,} IID, IE1, IE2	-10	+0.01	+10	μA	$\begin{array}{l} 0 \leq V_{\text{IA}}, V_{\text{IB}}, V_{\text{IC}}, V_{\text{ID}} \leq V_{\text{DD1}} \text{ or } V_{\text{DD2}}, \\ 0 \leq V_{\text{E1}}, V_{\text{E2}} \leq V_{\text{DD1}} \text{ or } V_{\text{DD2}} \end{array}$
Logic High Input Threshold	VIH, VEH	1.6			v	
Logic Low Input Threshold	VIL, VEL			0.4	v	
Logic High Output Voltages	VOAH, VOBH,	(V _{DD1} or V _{DD2}) – 0.1	3.0		v	$I_{0x} = -20 \ \mu A$, $V_{1x} = V_{1xH}$
	Voch, Vodh	$(V_{DD1} \text{ or } V_{DD2}) - 0.4$	2.8		v	$I_{\text{Ox}} = -4 \text{ mA}, V_{\text{Ix}} = V_{\text{IxH}}$
Logic Low Output Voltages	VOAL, VOBL,	(1001 01 1002) 011	0.0	0.1	V	$I_{0x} = 20 \ \mu A, V_{1x} = V_{1xL}$
	Vocl, Vodl		0.04	0.1	V	$I_{0x} = 400 \ \mu A, \ V_{1x} = V_{1xL}$
			0.2	0.4	v	$I_{\text{Ox}} = 4 \text{ mA}, V_{\text{Ix}} = V_{\text{IxL}}$
SWITCHING SPECIFICATIONS			0.2		-	
ADuM140xWSRWZ						
Minimum Pulse Width ³	PW			1000	ns	$C_{L} = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ⁴		1		1000	Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
	t _{PHL} , t _{PLH}	50	75	100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels $C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, tplh – tphl ⁵	PWD	50		40	ns	$C_L = 15 \text{ pF}$, CMOS signal levels $C_L = 15 \text{ pF}$, CMOS signal levels
	_					$C_L = 15 \text{ pF}$, CMOS signal levels $C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			50 50	ns	
Channel-to-Channel Matching ⁷	t _{PSKCD} /t _{PSKOD}			50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
ADuM140xWTRWZ						
Minimum Pulse Width ³	PW			100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁵	tphl, tplh	20	34	45	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			22	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t _{PSKCD}			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels ⁷	t _{PSKOD}			6	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	tphz, tplh		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t _{PZH} , t _{PZL}		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		3		ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁸	CM _H	25	35		kV/μs	$V_{Ix} = V_{DD1}/V_{DD2}, V_{CM} = 1000 V,$ transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	CM⊾	25	35		kV/μs	$V_{Ix} = 0 V, V_{CM} = 1000 V,$ transient magnitude = 800 V
Refresh Rate	fr		1.1		Mbps	
Input Dynamic Supply Current per Channel ⁹	I _{DDI (D)}		0.10		mA/Mbps	
Output Dynamic Supply Current per Channel ⁹	IDDO (D)		0.03		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS-MIXED 5 V/3 V, 125°C OPERATION¹

 $4.5 \text{ V} \le \text{V}_{\text{DD1}} \le 5.5 \text{ V}$, $3.0 \text{ V} \le \text{V}_{\text{DD2}} \le 3.6 \text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^{\circ}\text{C}$; $V_{\text{DD1}} = 5 \text{ V}$, $V_{\text{DD2}} = 3.0 \text{ V}$. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Symbol	Min	Тур	Max	Unit	Test Conditions
IDDI (Q)		0.50	0.53	mA	
IDDO (Q)		0.11	0.14	mA	
IDD1 (Q)		2.2	2.8	mA	DC to 1 MHz logic signal freq
IDD2 (Q)		0.5	0.9	mA	DC to 1 MHz logic signal freq
IDD1 (10)		8.6	10.6	mA	5 MHz logic signal freq.
IDD2 (10)		1.4	2.0	mA	5 MHz logic signal freq.
					5 5 1
		1.8	2.4	mA	DC to 1 MHz logic signal freq
		0.7			DC to 1 MHz logic signal freq
1002 (Q)					
DD1 (10)		7.1	9.0	mA	5 MHz logic signal freq.
					5 MHz logic signal freq.
1002 (10)					······································
		15	21	mΑ	DC to 1 MHz logic signal freq
					DC to 1 MHz logic signal freq
1002 (Q)					
DD1 (10)		56	70	mA	5 MHz logic signal freq.
					5 MHz logic signal freq.
JDD2 (10)		5.0	1.2	110.	s will logic signarried.
ا بي ا	_10	+0.01	+10	ΠΑ	$0 \le V_{IA}$, V_{IB} , V_{IC} , $V_{ID} \le V_{DD1}$ or
	10	10.01	110	μ	V_{DD2} , $0 \le V_{E1}$, $V_{E2} \le V_{DD1}$ or V_{DD2}
,	2.0			v	
				v	
- 12/ - 22			0.8	v	
			0.4		
VOAH, VOBH,	(Vpp1 or Vpp2) - 0.1				$I_{0x} = -20 \ \mu A$, $V_{1x} = V_{1xH}$
V _{OCH} , V _{ODH}	,				$I_{Ox} = -4 \text{ mA}, V_{Ix} = V_{IxH}$
VOAL, VOBL	(1001111002) 111		0.1		$I_{0x} = 20 \ \mu A, V_{1x} = V_{1xL}$
V _{OCL} , V _{ODL}					$I_{0x} = 400 \ \mu A, V_{1x} = V_{1xL}$
					$I_{Ox} = 4 \text{ mA}, V_{Ix} = V_{IxL}$
				-	
PW			1000	ns	C _L = 15 pF, CMOS signal level
	1				$C_L = 15 \text{ pF}$, CMOS signal level
тень, теги		70	100	-	$C_L = 15 \text{ pF}$, CMOS signal level
PWD			40	ns	$C_L = 15 \text{ pF}$, CMOS signal level
	1				
t _{PSK}			50	ns	$C_{L} = 15 \text{ pF}$, CMOS signal level
	IDDI (Q) <	IDD1 (Q) IDD1 (Q) IDD1 (Q) IDD2 (Q) IDD1 (Q) IDD1 (Q) IDD1 (Q) IDD1 (Q) IDD1 (Q) IDD1 (Q) IDD1 (Q) IDD1 (Q) IDD2 (Q) ID1 (Q) VIL, VEL VOD1 OT VDD2) - 0.1 VOLI, VOD1	IDDI (Q) 0.50 IDDI (Q) 0.50 IDDI (Q) 0.11 IDDI (Q) 2.2 IDDI (Q) 0.5 IDDI (10) 8.6 IDDI (Q) 1.4 IDDI (Q) 1.8 IDDI (Q) 1.8 IDDI (Q) 7.1 IDDI (Q) 7.1 IDDI (Q) 7.1 IDDI (Q) 0.7 IDDI (Q) 7.1 IDDI (Q) 0.9 IDDI (Q) 5.6 IDDI (Q) 5.6 IDD2 (Q) 0.9 IDDI (10) 5.6 IDD2 (10) 3.0 IA, Hg, HG, -10 HODI (10) 5.6 IDD2 (10) 1.6 VIL, VEH 2.0 VOAH, VOBH, (VDD1 OT VDD2) - 0.1 VDD1 OT VDD2 VOAL, VOBL, 0.0 0.04 VOAL, VOBL, 0.04 0.2 PW 1 50 70	IDDI (Q) 0.50 0.53 IDDI (Q) 0.11 0.14 IDDI (Q) 2.2 2.8 IDD2 (Q) 0.5 0.9 IDDI (10) 8.6 10.6 IDD2 (Q) 1.4 2.0 IDDI (10) 1.4 2.0 IDDI (Q) 1.8 2.4 IDD2 (Q) 0.7 1.2 IDD1 (10) 7.1 9.0 IDD2 (10) 7.1 9.0 IDD1 (10) 7.1 9.0 IDD2 (10) 5.6 7.0 IDD1 (10) 5.6 7.0 IDD2 (10) 3.0 4.2 IA, IB, IC, -10 +0.01 +10 IDD2 (10) 3.0 4.2 IA, IB, IC, -10 +0.01 +10 IDD2 (10) 3.0 4.2 VIL, VEL 0.0 0.4 VOAH, VOBH, VDD1 OF VDD2) - 0.1 VDD1 OF VDD2 VOAL, VOBL, VDD1 OF VDD2) - 0.4 VDD1 VDD2	IDDI (0) 0.50 0.53 mA IDDI (0) 2.2 2.8 mA IDDI (0) 0.5 0.9 mA IDDI (10) 8.6 10.6 mA IDDI (10) 8.6 10.6 mA IDDI (10) 1.4 2.0 mA IDDI (10) 1.8 2.4 mA IDDI (10) 1.8 2.4 mA IDDI (10) 1.5 2.1 mA IDDI (10) 7.1 9.0 mA IDDI (10) 7.1 9.0 mA IDDI (10) 5.6 7.0 mA IDDI (10) 1.6 V V VIL, VEH 0.0 V V VIL, VEH 0.0 0.1 V VOAH, VOBH, VODI OF VDD2) - 0.1 VDDI OF VDD2

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
ADuM140xWTRWZ						
Minimum Pulse Width ³	PW			100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁵	tphl, tplh	20	30	40	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			22	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t _{PSKCD}			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels ⁷	t pskod			6	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	tphz, tplh		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	tpzh, tpzl		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		3.0		ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁸	CM _H	25	35		kV∕µs	$V_{1x} = V_{DD1}/V_{DD2}, V_{CM} = 1000 V,$ transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	CM∟	25	35		kV/μs	$V_{lx} = 0 V, V_{CM} = 1000 V,$ transient magnitude = 800 V
Refresh Rate	f _r		1.2		Mbps	
Input Dynamic Supply Current per Channel ⁹	I _{DDI (D)}		0.19		mA/Mbps	
Output Dynamic Supply Current per Channel ⁹	IDDO (D)		0.03		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

 8 CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS-MIXED 3 V/5 V, 125°C OPERATION¹

 $3.0 \text{ V} \le V_{DD1} \le 3.6 \text{ V}, 4.5 \text{ V} \le V_{DD2} \le 5.5 \text{ V};$ all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^{\circ}\text{C}$; $V_{DD1} = 3.0 \text{ V}, V_{DD2} = 5 \text{ V}$. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	I _{DDI (Q)}		0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	I _{DDO (Q)}		0.19	0.21	mA	
ADuM1400W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	IDD1 (Q)		1.2	1.9	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (Q)}		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
VDD1 Supply Current	IDD1 (10)		4.5	6.5	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (10)}		2.6	3.5	mA	5 MHz logic signal freq.
ADuM1401W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
VDD1 Supply Current	IDD1 (Q)		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2 (Q)}		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						5 5 1
V _{DD1} Supply Current	I _{DD1 (10)}		3.7	5.4	mA	5 MHz logic signal freg.
V _{DD2} Supply Current	IDD2 (10)		4.1	5.0	mA	5 MHz logic signal freq.
ADuM1402W, Total Supply Current, Four Channels ²						5 5 1
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1 (Q)}		0.9	1.5	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	IDD2 (Q)		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)	· 552 (Q)					
V _{DD1} Supply Current	IDD1 (10)	·	3.0	4.2	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	IDD2 (10)		5.6	7.0	mA	5 MHz logic signal freq.
For All Models						
Input Currents	IIA, IIB, IIC,	-10	+0.01	+10	μA	$0 \leq V_{IA}$, V_{IB} , V_{IC} , $V_{ID} \leq V_{DD1}$ or V_{DD2}
	lid, le1, le2				P	$0 \le V_{E1}, V_{E2} \le V_{DD1} \text{ or } V_{DD2}$
Logic High Input Threshold	VIH, VEH	1.6			v	
Logic Low Input Threshold	VIL, VEL			0.4	V	
Logic High Output Voltages	Voah, Vobh,	(V _{DD1} or V _{DD2}) - 0.1	V _{DD1} , V _{DD2}		V	$I_{Ox} = -20 \ \mu A$, $V_{Ix} = V_{IxH}$
	Voch, Vodh	(V _{DD1} or V _{DD2}) - 0.4	V _{DD1} , V _{DD2} - 0.2		V	$I_{Ox} = -4 \text{ mA}, V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V _{OAL} , V _{OBL} ,		0.0	0.1	V	$I_{Ox} = 20 \ \mu A$, $V_{Ix} = V_{IxL}$
	Vocl, Vodl		0.04	0.1	v	$I_{0x} = 400 \ \mu A, V_{1x} = V_{1xL}$
			0.2	0.4	v	$I_{Ox} = 4 \text{ mA}, V_{Ix} = V_{IxL}$
SWITCHING SPECIFICATIONS						
ADuM140xWSRWZ						
Minimum Pulse Width ³	PW			1000	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		1			Mbps	$C_{L} = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁵	tphl, tplh	50	70	100	ns .	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			40	ns	$C_{L} = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁶	tрsк			50	ns	$C_{L} = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching ⁷	t _{PSKCD} /t _{PSKOD}			50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
ADuM140xWTRWZ						
Minimum Pulse Width ³	PW			100	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁵	tphl, tplh	20	30	40	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperature			5		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			22	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t PSKCD			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels ⁷	t _{PSKOD}			6	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t _{PHZ} , t _{PLH}		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	tpzh, tpzl		6	8	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		2.5		ns	C _L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁸	CM _H	25	35		kV/μs	$V_{lx} = V_{DD1}/V_{DD2}$, $V_{CM} = 1000 V$, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	CM∟	25	35		kV/μs	$\label{eq:Vix} \begin{split} V_{ix} &= 0 \ V, \ V_{CM} = 1000 \ V, \ transient \\ magnitude &= 800 \ V \end{split}$
Refresh Rate	fr		1.1		Mbps	
Input Dynamic Supply Current per Channel ⁹	IDDI (D)		0.10		mA/Mbps	
Output Dynamic Supply Current per Channel ⁹	IDDO (D)		0.05		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V₀ < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 8.

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
Resistance (Input-to-Output) ¹	R _{I-O}		10 ¹²		Ω	
Capacitance (Input-to-Output) ¹	CI-O		2.2		pF	f = 1 MHz
Input Capacitance ²	Cı		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ」		33		°C/W	Thermocouple located at
IC Junction-to-Case Thermal Resistance, Side 2	θιςο		28		°C/W	center of package underside

¹ Device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, Pin 4, Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together and Pin 9, Pin 10, Pin 11, Pin 12, Pin 13, Pin 14, Pin 15, and Pin 16 are shorted together.

² Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM140x are approved by the organizations listed in Table 9. Refer to Table 14 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 9.

UL	CSA	VDE	ΤÜV
Recognized under 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ²	Approved according to: IEC 61010-1:2001 (2 nd Edition), EN 61010-1:2001 (2 nd Edition) UL 61010-1:2004 CSA C22.2.61010.1:2005
Double/reinforced insulation, 2500 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage	Reinforced insulation, 560 V peak	Reinforced insulation, 400 V rms maximum working voltage
File E214100	File 205078	File 2471900-4880-0001	Certificate U8V 05 06 56232 002

¹ In accordance with UL 1577, each ADuM140x is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 μA).
² In accordance with DIN V VDE V 0884-10, each ADuM140x is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 10.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		Illa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 11.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			l to IV	
For Rated Mains Voltage ≤ 300 V rms			l to III	
For Rated Mains Voltage ≤ 400 V rms			l to ll	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		VIORM	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC	Vpr	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC	VPR		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{\text{IORM}} \times 1.2 = V_{\text{PR}}, t_{\text{m}} = 60$ sec, partial discharge $< 5 \text{ pC}$		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ seconds	VTR	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure			
	(see Figure 4)			
Case Temperature		Ts	150	°C
Side 1 Current		I _{S1}	265	mA
Side 2 Current		Is ₂	335	mA
Insulation Resistance at Ts	$V_{10} = 500 V$	Rs	>109	Ω

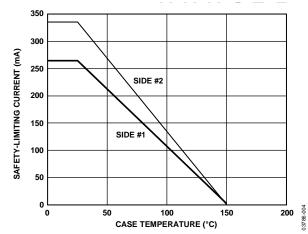


Figure 4. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 12.	
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Parameter	Rating
Operating Temperature (T _A) ¹	-40°C to +105°C
Operating Temperature $(T_A)^2$	-40°C to +125°C
Supply Voltages (V _{DD1} , V _{DD2}) ^{1, 3}	2.7 V to 5.5 V
Supply Voltages (V _{DD1} , V _{DD2}) ^{2, 3}	3.0 V to 5.5 V
Input Signal Rise and Fall Times	1.0 ms

¹ Does not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

² Applies to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

³ All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 13.

Parameter	Rating
Storage Temperature (T _{ST})	–65°C to +150°C
Ambient Operating Temperature (T _A) ¹	–40°C to +105°C
Ambient Operating Temperature (T _A) ²	–40°C to +125°C
Supply Voltages (V _{DD1} , V _{DD2}) ³	–0.5 V to +7.0 V
Input Voltage (V_{IA} , V_{IB} , V_{IC} , V_{ID} , V_{E1} , V_{E2}) ^{3, 4}	-0.5 V to V _{DDI} + 0.5 V
Output Voltage (V _{OA} , V _{OB} , V _{OC} , V _{OD}) ^{3, 4}	-0.5 V to V _{DDO} + 0.5 V
Average Output Current per Pin⁵	
Side 1 (I ₀₁)	-18 mA to +18 mA
Side 2 (I ₀₂)	-22 mA to +22 mA
Common-Mode Transients ⁶	–100 kV/µs to +100 kV/µs

¹ Does not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

² Applies to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

³ All voltages are relative to their respective ground.

⁴ V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.

⁵ See Figure 4 for maximum rated current values for various temperatures.

⁶ This refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings may cause latch-up or permanent damage.

Table 14. Maximum Continuous Working Voltage¹

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Tuble The Huminian Continuous (Continue Contage						
Parameter	Max	Unit	Constraint			
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime			
AC Voltage, Unipolar Waveform						
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1			
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10			
DC Voltage						
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1			
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10			

¹ Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

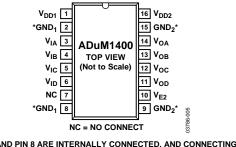
Table 15. Truth Table (Positive Logic)

	V _{Ex} Input ^{1, 2}	V _{DDI} State ¹	V _{DDO} State ¹		Notes
Н	H or NC	Powered	Powered	Н	
L	H or NC	Powered	Powered	L	
Х	L	Powered	Powered	Z	
Х	H or NC	Unpowered	Powered	н	Outputs return to the input state within 1 μ s of V _{DDI} power restoration.
Х	L	Unpowered	Powered	Z	
Х	х	Powered	Unpowered	Indeterminate	Outputs return to the input state within 1 μ s of V _{DDO} power restoration if the V _{Ex} state is H or NC. Outputs return to a high impedance state within 8 ns of V _{DDO} power restoration if the V _{Ex} state is L.

¹ V_{lx} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D). V_{Ex} refers to the output enable signal on the same side as the V_{Ox} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

² In noisy environments, connecting V_{Ex} to an external logic high or low is recommended.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



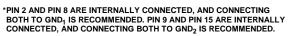


Figure 5. ADuM1400 Pin Configuration

Table 16. ADuM1400 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	GND1	Ground 1. Ground reference for Isolator Side 1.
3	VIA	Logic Input A.
4	VIB	Logic Input B.
5	VIC	Logic Input C.
6	VID	Logic Input D.
7	NC	No Connect.
8	GND1	Ground 1. Ground reference for Isolator Side 1.
9	GND ₂	Ground 2. Ground reference for Isolator Side 2.
10	V _{E2}	Output Enable 2. Active high logic input. V_{OA} , V_{OB} , V_{OC} , and V_{OD} outputs are enabled when V_{E2} is high or disconnected. V_{OA} , V_{OB} , V_{OC} , and V_{OD} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	Vod	Logic Output D.
12	Voc	Logic Output C.
13	Vob	Logic Output B.
14	Voa	Logic Output A.
15	GND ₂	Ground 2. Ground reference for Isolator Side 2.
16	V _{DD2}	Supply Voltage for Isolator Side 2.

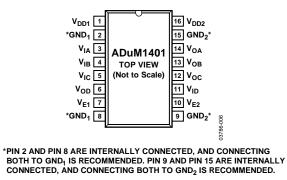


Figure 6. ADuM1401 Pin Configuration

Table 17. ADuM1401 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	GND1	Ground 1. Ground reference for Isolator Side 1.
3	VIA	Logic Input A.
4	VIB	Logic Input B.
5	V _{IC}	Logic Input C.
6	Vod	Logic Output D.
7	V _{E1}	Output Enable 1. Active high logic input. V_{OD} output is enabled when V_{E1} is high or disconnected. V_{OD} is disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.
8	GND1	Ground 1. Ground reference for Isolator Side 1.
9	GND ₂	Ground 2. Ground reference for Isolator Side 2.
10	V _{E2}	Output Enable 2. Active high logic input. V_{OA} , V_{OB} , and V_{OC} outputs are enabled when V_{E2} is high or disconnected. V_{OA} , V_{OB} , and V_{OC} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	VID	Logic Input D.
12	Voc	Logic Output C.
13	V _{OB}	Logic Output B.
14	Voa	Logic Output A.
15	GND ₂	Ground 2. Ground reference for Isolator Side 2.
16	V _{DD2}	Supply Voltage for Isolator Side 2.

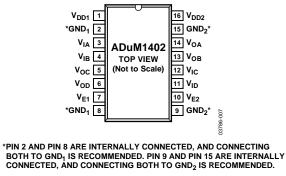


Figure 7. ADuM1402 Pin Configuration

Table 18. ADuM1402 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	GND1	Ground 1. Ground reference for Isolator Side 1.
3	VIA	Logic Input A.
4	VIB	Logic Input B.
5	Voc	Logic Output C.
6	Vod	Logic Output D.
7	V _{E1}	Output Enable 1. Active high logic input. V_{OC} and V_{OD} outputs are enabled when V_{E1} is high or disconnected. V_{OC} and V_{OD} outputs are disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.
8	GND1	Ground 1. Ground reference for Isolator Side 1.
9	GND ₂	Ground 2. Ground reference for Isolator Side 2.
10	V _{E2}	Output Enable 2. Active high logic input. V_{OA} and V_{OB} outputs are enabled when V_{E2} is high or disconnected. V_{OA} and V_{OB} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	VID	Logic Input D.
12	V _{IC}	Logic Input C.
13	V _{OB}	Logic Output B.
14	VOA	Logic Output A.
15	GND ₂	Ground 2. Ground reference for Isolator Side 2.
16	V _{DD2}	Supply Voltage for Isolator Side 2.

TYPICAL PERFORMANCE CHARACTERISTICS

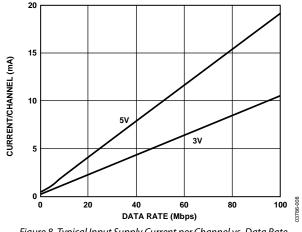


Figure 8. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

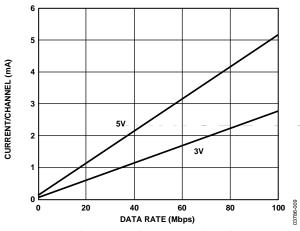


Figure 9. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

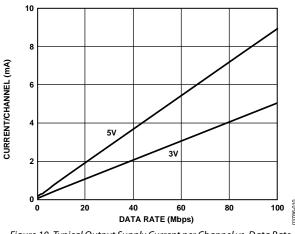


Figure 10. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

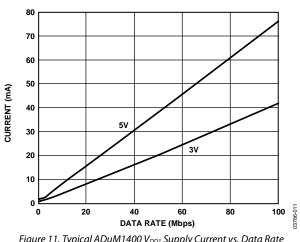


Figure 11. Typical ADuM1400 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

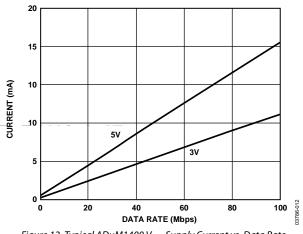
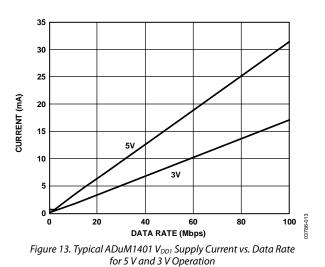
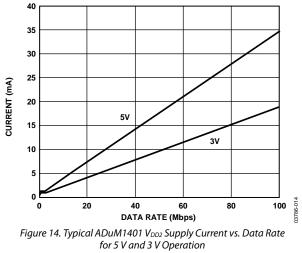


Figure 12. Typical ADuM1400 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation





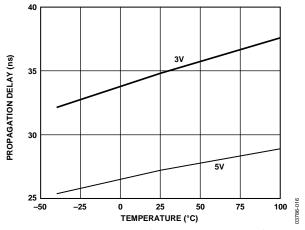
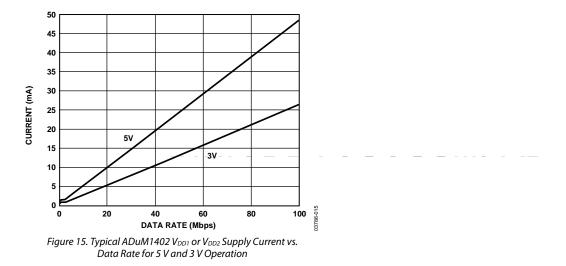


Figure 16. Propagation Delay vs. Temperature, C Grade



APPLICATIONS INFORMATION PC BOARD LAYOUT

The ADuM140x digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 17). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2} . The capacitor value should be between 0.01 μ F and 0.1 μ F. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered, unless the ground pair on each package side is connected close to the package.

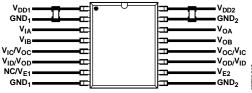
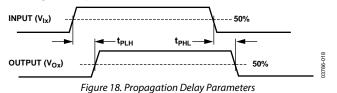


Figure 17. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.



Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM140x component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM140x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 μ s, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5 μ s, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 15) by the watchdog timer circuit.

The limitation on the magnetic field immunity of the ADuM140x is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM140x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \Sigma \prod r_n^2; \ n = 1, 2, \dots, N$$

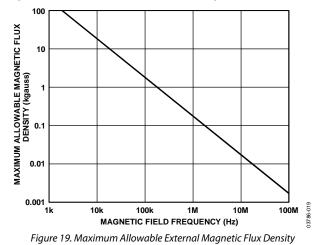
where:

 β is magnetic flux density (gauss).

N is the number of turns in the receiving coil.

 r_n is the radius of the nth turn in the receiving coil (cm).

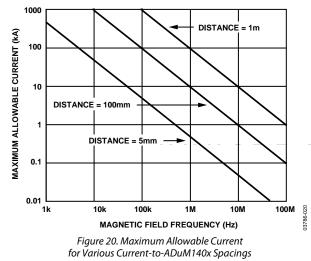
Given the geometry of the receiving coil in the ADuM140x and an imposed requirement that the induced voltage be 50% at most of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 19.



Rev. G | Page 27 of 32

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and has the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM140x transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM140x is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM140x to affect the operation of the component.



Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM140x isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \qquad \qquad f \le 0.5 f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)}$$
 $f > 0.5 f_r$

For each output channel, the supply current is given by

$I_{DDO} = I_{DDO(Q)}$	$f \le 0.5 f_r$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)}$$

$$f > 0.5 f_r$$

where:

*I*_{DDI (D)}, *I*_{DDO (D)} are the input and output dynamic supply currents per channel (mA/Mbps).

 C_L is the output load capacitance (pF).

 V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.

 f_r is the input stage refresh rate (Mbps).

 $I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 8 and Figure 9 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 10 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 11 through Figure 15 provide total V_{DD1} and V_{DD2} supply current as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM140x.

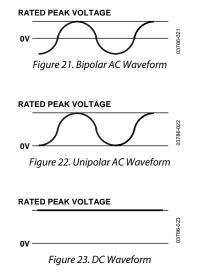
Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 14 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than a 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM140x depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 21, Figure 22, and Figure 23 illustrate these different isolation voltage waveforms, respectively.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition_ determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower, which allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 14 can be applied while maintaining the 50-year minimum lifetime, provided the voltage conforms to either the unipolar ac or dc voltage cases. Any crossinsulation voltage waveform that does not conform to Figure 22 or Figure 23 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 14.

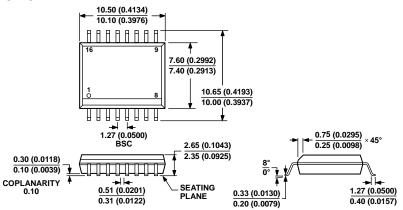
Note that the voltage presented in Figure 22 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.



AUTOMOTIVE PRODUCTS

The ADuM1400W, ADuM1401W, and ADuM1402W products are qualified per AEC-Q100 for use in automotive applications. Custom variants of these products may be available to meet stringent automotive performance and quality requirements. For more information, contact your local Analog Devices sales representative.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

032707-B

Figure 24. 16-Lead Standard Small Outline Package [SOIC_W] Wide Body (RW-16) Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Number of Inputs, V _{DD1} Side	Number of Inputs, V _{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Description	Package Option
ADuM1400ARW ¹	4	0	1	100	40	-40°C to +105°C	16-Lead SOIC_W	• RW-16
ADuM1400BRW ¹	4	0	10	50	3	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1400CRW ¹	4	0	90	32	2	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1400ARWZ ^{1, 2}	4	0	1	100	40	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1400BRWZ ^{1, 2}	4	0	10	50	3	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1400CRWZ ^{1,2}	4	0	90	32	2	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1400WSRWZ ^{1, 2}	4	0	1	100	40	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM1400WTRWZ ^{1, 2}	4	0	10	32	3	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM1401ARW ¹	3	1	1	100	40	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401BRW ¹	3	1	10	50	3	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401CRW ¹	3	1	90	32	2	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401ARWZ ^{1, 2}	3	1	1	100	40	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401BRWZ ^{1, 2}	3	1	10	50	3	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401CRWZ ^{1,2}	3	1	90	32	2	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1401WSRWZ ^{1, 2}	3	1	1	100	40	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM1401WTRWZ ^{1, 2}	3	1	10	32	3	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM1402ARW ¹	2	2	1	100	40	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402BRW ¹	2	2	10	50	3	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402CRW ¹	2	2	90	32	2	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402ARWZ ^{1, 2}	2	2	1	100	40	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402BRWZ ^{1, 2}	2	2	10	50	3	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402CRWZ ^{1,2}	2	2	90	32	2	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1402WSRWZ ^{1, 2}	2	2	1	100	40	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM1402WTRWZ ^{1, 2}	2	2	10	32	3	–40°C to +125°C	16-Lead SOIC_W	RW-16
EVAL-ADuM1402EBA	2	2	1	100	40		Evaluation Board	
EVAL-ADuM1402EBB	2	2	10	50	3		Evaluation Board	
EVAL-ADuM1402EBC	2	2	90	32	2		Evaluation Board	

¹ Tape and reel are available. The addition of an -RL suffix designates a 13" (1,000 units) tape and reel option.

 2 Z = RoHS Compliant Part.

NOTES

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Rev. G | Page 32 of 32

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