10-Bit Current output D to A Converter

DAC100

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. This brochure can be found at: http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/DAC100

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
DAC100-703Q	10-Bit Current output D to A Converter
DAC100-713Q	Radiation tested, 10-Bit Current output D to A Converter

2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
Q	GDIP1-T16	16-Lead ceramic dual-in-line package (CERDIP)

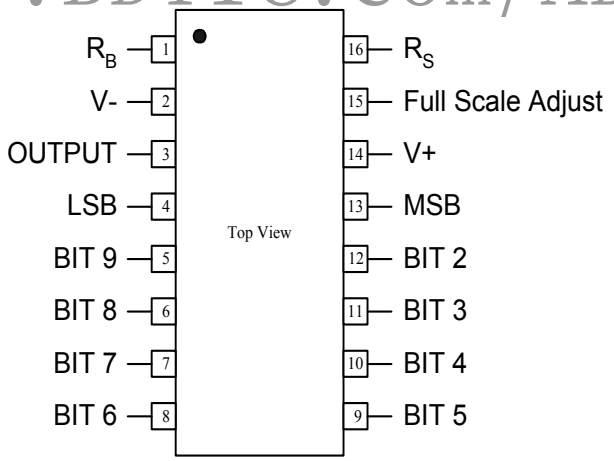

Figure 1 - Terminal connections.

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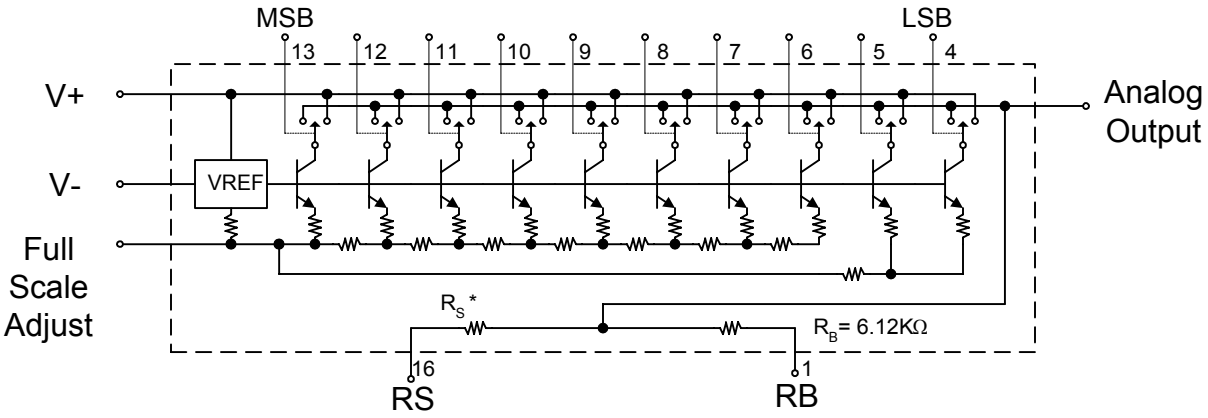

R_S = 4.88KΩ

Figure 1A: Simplified schematic

3.0 Absolute Maximum Ratings. (TA = 25°C, unless otherwise noted)

V+ supply to V- supply..... 0V to 36V
V+ supply to output..... 0V to +18V
V- supply to output..... 0V to –18V
Power dissipation 500mW
Logic inputs to outputs.....-1V to +6V
Operating temperature range.....-55°C to +125°C
Storage temperature range.....-65°C to +150°C
Lead temperature (soldering, 60 sec.) .....+300°C
Dice junction temperature (T_J).....+175°C

3.1 Thermal Characteristics:

Thermal resistance, CERDIP (Q) Package
Junction-to-case (Θ_{JC}) = 29°C/W Max
Junction-to-ambient (Θ_{JA}) = 91 °C/W Max
Thermal resistance, FLATPAK (N) Package
Junction-to-case (Θ_{JC}) = 22°C/W Max
Junction-to-ambient (Θ_{JA}) = 90 °C/W Max

4.0 Electrical Table: See notes at end of table

TABLE I

Parameter	Symbol	Conditions 1/	Sub-group	Limit Min	Limit Max	Units
Power supply current	I+	V_{IH} = 2.1V	1, 2, 3		8.33	mA
	I-	V_{IH} = 2.1V	1, 2, 3		8.33	
Full range output voltage	V_{FR}	V_{IL} = 0.7V, Full Adjust pin tied to V-	1, 2, 3	10.0	11.1	V
Zero scale output voltage	V_{ZS}	V_{IH} = 2.1V	1, 2, 3		±.013	%FS
Integral nonlinearity	NL	± ½ LSB – 9 Bits	1, 2, 3		±0.1	
Full scale temperature coefficient	TCV_{FR}	V_{IL} = 0.7V, Full Scale Adjust pin tied to V-	8		±60	ppm/° C
Logic inputs high	V_{IH}	V_{IN} = 2.1V to 3V (all inputs) Measured with respect to output pin allowing ≤ ±½ LSB change with ΔV_{IN}	1, 2, 3	2.1		V
Logic inputs low	V_{IL}	V_{IN} = 0.7V to 0V (all inputs) Measured with respect to output pin allowing ≤ ±½ LSB change with ΔV_{IN}	1, 2, 3		0.7	
Logic input current high	I_{IH}	V_{IH} = 6.0V, Each Input	1, 2, 3		5	µA
Logic input current low	I_{IL}	V_{IL} = 0V, Each Input	1, 2, 3		5	
Power supply sensitivity	PSS	V_{IL} = 0.7V (all inputs) V_S = ±6V to ±18V	1, 2, 3		±0.1	%/V
Monotonicity 2/	ΔI_O	Measured at each major carry code point	1	0		µA
Settling time 3/	T_{SHL}	R_L = 1KΩ, C_L ≤ 10pF	9		375	nS

Table I notes:

1/ V_S = ±15V, unless otherwise specified.

2/ The change in output current either increases or remains the same for an increasing digital input code.

3/ Output within ± ½ LSB of 10-bit accuracy final settled nominal value of V_{OUT}.

Input pulse characteristics:

Input frequency = 1MHz square wave, 50% duty cycle.

Input amplitude = 0V to 2.1V

Input signal = t_r, $t_f \leq 20$ nS

Measurement referenced to input High-to-Low Transition. DUT Settling Time to ±0.05 % FS

4.1 Electrical Test Requirements:

Table II	
MIL-STD-883 Test Requirements	Subgroups (see table I)
Interim electrical parameters (pre Burn-In)	1
Final Electrical Test Parameters	1, 2, 3, 8 1/ 2/
Group A Test Requirements	1, 2, 3, 8, 9
Group C Test Requirements	1 2/
Group D Test Requirements	1
* PDA applies to Subgroup 1 only. No other subgroups are included in PDA.	

1/ PDA applies to subgroup 1. Deltas not included in PDA
2/ See table III for deltas. See table I for test conditions.

4.2 Table III. Burn-in test delta limits.

Table III				
TEST TITLE	BURN-IN ENDPOINT	LIFETEST ENDPOINT	DELTA LIMIT	UNITS
V_{FR}	10.55 ± 0.55	10.55 ± 0.75	±0.2	V
V_{ZS}	±0.013	±0.018	±0.005	%FS
I+	8.33	8.33	±10%	mA
I-	8.33	8.33	±10%	mA

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	30-Jun-00
B	Update web address	Feb. 18, 2002
C	Update web address. Add Group C and D to table II. Add life test endpoint based on delta to table III.	Feb. 28, 2003
D	Delete Burn-In circuit	Aug. 5, 2003
E	Update header/footer & add to 1.0 Scope description	Feb. 21,2008
F	Remove minimum Dice Junction Temp. range in 3.0 Absolute Max. Ratings	March 31, 2008