Precision Low-Input Current Operational Amplifier (Internally Compensated)

OP12

1.0 SCOPE

This specification documents the detailed requirements for Analog Devices space qualified die including die qualification as described for Class K in MIL-PRF-38534, Appendix C, Table C-II except as modified herein.

The manufacturing flow described in the STANDARD DIE PRODUCTS PROGRAM brochure at http://www.analog.com/marketSolutions/militaryAerospace/pdf/Die_Broc.pdf is to be considered a part of this specification.

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/OP12

2.0 Part Number. The complete part number(s) of this specification follow:

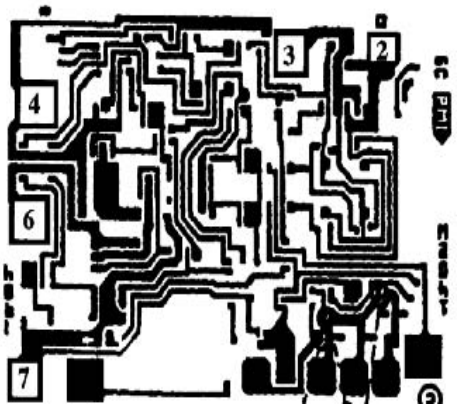
Part Number	Description
OP12-000C	Precision Low-Input Current Operational Amplifier (Internally Compensated)

3.0 Die Information

3.1 Die Dimensions

Die Size	Die Thickness	Bond Pad Metalization
43 mil x 59 mil	**19 mil ± 2 mil**	**Al/Cu**

3.2 Die Picture



1	NC
2	-IN
3	+IN
4	V-
5	NC
6	OUT
7	V+
8	NC

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3.3 Absolute Maximum Ratings 1/

Supply Voltage .....±20V
Differential Input Current 2/.....±10mA
Input Voltage 3/.....±15V
Output Short Circuit Duration .....Indefinite
Storage Temperature .....-65°C to +150°C
Operating Temperature Range .....-55°C to +125°C
Junction Temperature (T_J).....+150°C

Absolute Maximum Rating Notes:

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is provided.

3/ For supply voltages less than -15V, the absolute maximum input voltage is equal to the supply voltage.

4.0 Die Qualification

In accordance with class-K version of MIL-PRF-38534, Appendix C, Table C-II, except as modified herein.

(a) Qual Sample Size and Qual Acceptance Criteria – 10/0
(b) Qual Sample Package – DIP
(c) Pre-screen electrical test over temperature performed post-assembly prior to die qualification.

Table I - Dice Electrical Characteristics

Parameter	Symbol	Conditions 1/		Limit Min	Limit Max	Units
Input Offset Voltage	V_{OS}				0.15	mV
Input Offset Current	I_{OS}				0.2	nA
Input Bias Current	I_B				±2	nA
Input Voltage Range	IVR			±13		V
Common-Mode Rejection	CMR	V_{CM} = IVR		104		dB
Power Supply Rejection	PSRR	V_S = ±5V to±15V			7	µV/V
Output Voltage Swing	V_O	R_L = 10kΩ		±13		V
		R_L = 5kΩ		±10		
Large-Signal Voltage Gain	A_{VO}	V_O= ±10V	R_L = 10kΩ	80		V/mV
			R_L = 2kΩ	50		
Supply Current	I_{SY}	No Load	V_S = ±5V, ±15V		0.6	mA

Table I Notes:

1/ V_S = ±15V, R_S = 50Ω , and T_A = 25°C, unless otherwise specified.

Table II -Electrical Characteristics for Qual Samples							
Parameter	Symbol	Conditions 1/		Sub-groups	Limit Min	Limit Max	Units
Input Offset Voltage	V_{OS}			1		0.15	mV
				2, 3		0.35	
Input Offset Current	I_{OS}			1		0.2	nA
				2, 3		0.4	
Input Bias Current	I_B			1		±2	nA
				2, 3		±3	
Input Voltage Range	IVR			1, 2, 3	±13		V
Common-Mode Rejection	CMR	V_{CM} = IVR		1	104		dB
				2, 3	100		
Power Supply Rejection	PSRR	V_S = ±5V to ±15V		1		7	µV/V
				2, 3		10	
Output Voltage Swing	V_O	R_L =10kΩ		4, 5, 6	±13		V
		R_L =5kΩ		4, 5, 6	±10		
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V	R_L =10kΩ	4	80		V/mV
			R_L =2kΩ	4	50		
			R_L =5kΩ	5, 6	40		
Supply Current	I_{SY}	No Load	V_S = ±5V, ±15V	1		0.6	mA
			V_S = ±15V	2, 3		0.6	

Table II Notes:

1/ V_S = ±15V and RS = 50Ω , unless otherwise specified.

Table III - Life Test Endpoint and Delta Parameter
(Product is tested in accordance with Table II with the following exceptions)

Test Title	Symbol	Sub-groups	Post Burn In Limit		Post Life Test Limit		Life Test Delta	Units
			Min	Max	Min	Max		
Input Offset Voltage	V_{OS}	1		0.225		0.3	±0.075	mV
		2, 3				0.5		
Input Offset Current	I_{OS}	1		0.25		0.3		nA
		2, 3				0.5		
Input Bias Current	$\pm I_B$	1		±2.5		±3	±0.5	nA
		2, 3				±4		

5.0 Life Test/Burn-In Information

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B or C.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	8-OCT-01
B	Change package from Sidebrazed DIP to DIP Change from ±20V supply voltage to ±15V Supply voltage for V_{OS}, I_{OS}, and I_B on Table I and II. Change IOS from .4 to .5 nA at temp on table III	19-Dec-01
C	Update web address	Aug. 5, 2003
D	Update 1.0 Scope description.	16 Jul. 2007
E	Update header/footer & add to 1.0 Scope description.	14 Feb. 2008
F	Adjust header/footer and remove part description on pgs.2-5 header	28 Feb. 2008
G	Add Junction Temperature (T_J)….150°C to 3.3 Absolute Max. Ratings	March 28, 2008
H	Updated Section 4.0c note to indicate pre-screen temp testing being performed.	5-JUN-2009