ANALOG DEVICES

High-Speed, Dual Operational Amplifier

OP271

FEATURES

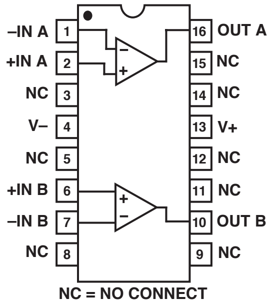
Excellent Speed: 8.5 V/μs Typ
Fast Settling (0.01%): 2 μs Typ
Unity-Gain Stable
High-Gain Bandwidth: 5 MHz Typ
Low Input Offset Voltage: 200 μV Max
Low Offset Voltage Drift: 21 μV/°C Max
High Gain: 400 V/mV Min
Outstanding CMR: 106 dB Min
Industry Standard 8-Pin Dual Pinout
Available in Die Form

GENERAL DESCRIPTION

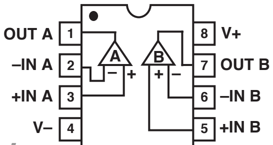
The OP271 is a unity-gain stable monolithic dual op amp featuring excellent speed, 8.5 V/μs typical, and fast settling time, 2 μs typical to 0. 01%. The OP271 has a gain bandwidth of 5 MHz with a high phase margin of 62°.

Input offset voltage of the OP271 is under 200 μV with input offset voltage drift below 2 μV/°C, guaranteed over the full military temperature range. Open-loop gain exceeds 400,000 into a 10 kΩ load ensuring outstanding gain accuracy and linearity. The input bias current is under 20 nA limiting errors due to source resistance. The OP271's outstanding CMR, over 106 dB, and low PSRR, under 5.6 μV/V, reduce errors caused by ground noise and power supply fluctuations. In addition, the OP27l exhibits high CMR and PSRR over a wide frequency range, further improving system accuracy.

PIN CONNECTIONS



16-Pin SOL
(S-Suffix)



Epoxy Mini-DIP
(P-Suffix)
8-Pin Hermetic DIP
(Z-Suffix)

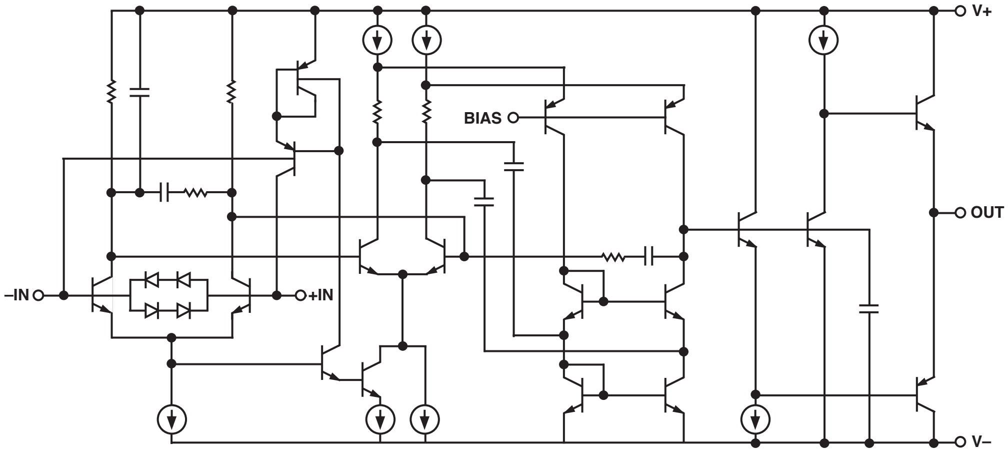


Figure 1. Simplified Schematic
(One of the two amplifiers is shown.)

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Tel: 781/329-4700
www.analog.com
Fax: 781/326-8703

OP271–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

			OP271A/E			OP271F			OP271G			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT OFFSET VOLTAGE	V_{OS}			75	200		150	300		200	400	µV
INPUT OFFSET CURRENT	I_{OS}	V_{CM} = 0 V		1	10		4	15		7	20	nA
INPUT BIAS CURRENT	I_B	V_{CM} = 0 V		4	20		6	40		12	60	nA
INPUT NOISE VOLTAGE DENSITY	e_n	f_O = 1 kHz		7.6			7.6			7.6		nV/Hz
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	V_O = ±10 V										
		R_L = 10 kΩ	400	650		300	500		250	400		V/mV
		R_L = 2 kΩ	300	500		200	300		175	250		V/mV
INPUT VOLTAGE RANGE	IVR		±12	±12.5		±12	±12.5		±12	±12.5		V
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±12	±13		±12	±13		±12	±13		V
COMMON-MODE REJECTION	CMR	V_{CM} = ±12 V	106	120		100	115		90	105		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V		0.6	3.2		1.8	5.6		2.4	7.0	µV/V
SLEW RATE	SR		5.5	8.5		5.5	8.5		5.5	8.5		V/µs
PHASE MARGIN	u_m	A_V = +1		62			62			62		degrees
SUPPLY CURRENT (ALL AMPLIFIERS)	I_{SY}	No Load		4 5	6.5		4.5	6.5		4.5	6.5	mA
GAIN BANDWIDTH PRODUCT	GBW			5			5			5		MHz
CHANNEL SEPARATION	CS	V_O = 20 V_{p-p}	125	175		125	175			175		dB
		f_O = 10 Hz	125	175		125	175			175		dB
INPUT CAPACITANCE	C_{IN}			3			3			3		pF
INPUT RESISTANCE DIFFERENTIAL-MODE	R_{IN}			0.4			0.4			0.4		MΩ
INPUT RESISTANCE COMMON MODE	R_{INCM}			20			20			20		GΩ
SETTLING TIME	t_S	AV = +1, 10 V Step to 0.01%		2			2			2		µs

NOTES

[1] Guaranteed by CMR test.

[2] Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, –55°C ≤ T_A ≤ 125°C for OP271A, unless otherwise noted.)

Parameter	Symbol	Conditions	OP271A Min	OP271A Typ	OP271A Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}			115	400	µV
AVERAGE INPUT OFFSET VOLTAGE DRIFT	TCV_{OS}			0.4	2	µV/°C
INPUT OFFSET CURRENT	I_{OS}	V_{CM} = 0 V		1.5	30	nA
INPUT BIAS CURRENT	IB	V_{CM} = 0 V		7	60	nA
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	V_O = ±10 V				
		R_L = 10 kΩ	300	600		V/mV
		R_L = 2 kΩ	200	500		V/mV
INPUT VOLTAGE RANGE[1]	IVR		±12	±12.5		V
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±12	±13		V
COMMON-MODE REJECTION	CMR	V_{CM} = ±12 V	100	120		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V		1.0	5.6	µV/V
SUPPLY CURRENT (ALL AMPLIFIERS)	I_{SY}	No Load		5.3	75	mA

NOTE

[1] Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP271A/E Min	OP271A/E Typ	OP271A/E Max	OP271F Min	OP271F Typ	OP271F Max	OP271G Min	OP271G Typ	OP271G Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}			100	330		215	560		300	700	µV
AVERAGE INPUT OFFSET VOLTAGE DRIFT	TCV_{OS}			0.4	2		1	4		2.0	5	µV/°C
INPUT OFFSET CURRENT	I_{OS}	V_{CM} = 0 V		1	30		5	40		15	50	nA
INPUT BIAS CURRENT	I_B	V_{CM} = 0 V		6	60		10	70		15	80	nA
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	V_O = ± 10 V										
		R_L = 10 kΩ	300	600		200	500		150	400		V/mV
		R_L = 2 kΩ	200	500		100	400		90	300		V/mV
INPUT VOLTAGE RANGE[1]	IVR		±12	±12.5		±12	±12.5		±12	±12.5		V
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±12	±13		±12	±13		±12	±13		V
COMMON-MODE REJECTION	CMR	V_{CM} = ±12 V	100	120		94	115		90	100		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V		0.7	5.6		51.8	10		2.0	15	µV/V
SUPPLY CURRENT (ALL AMPLIFIERS)	I_{SY}	No Load		5.2	7.2		5.2	7.2		5.2	7.2	mA

NOTE

[1] Guaranteed by CMR test.

(Continued from Page 1)

The OP271 offers outstanding dc and ac matching between channels. This is especially valuable for applications such as multiple gain blocks, high-speed instrumentation and amplifiers, buffers and active filters.

The OP271 conforms to the industry standard, 8-pin dual op amp pinout. It is pin compatible with the TL072, TL082, LF412, and 1458/1558 dual op amps and can be used to significantly improve systems using these devices.

For applications requiring lower voltage noise, see the OP270. For a quad version of the OP271, see the OP471.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Differential Input Voltage[2]	±1.0 V
Differential Input Current[2]	±25 mA
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature (Tj)	–65°C to +150°C
Operating Temperature Range	
OP271A	–55°C to +125°C
OP271E, OP271F, OP271G	–40°C to +85°C

Package Type	θ_{jA}[3]	θ_{jC}	Unit
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
8-Pin SOIC (S)	92	27	°C/W

NOTES

[1] Absolute maximum ratings apply to packaged parts, unless otherwise noted.

[2] The OP271's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low-noise performance. If differential voltage exceeds ±1.0 V, the input current should be limited to ±25 mA.

[3] θ_{jA} is specified for worst case mounting conditions, i.e., θ_{jA} is specified for device in socket for CERDIP and P-DIP packages; θ_{jA} is specified for device soldered to printed circuit board for SOIC package.

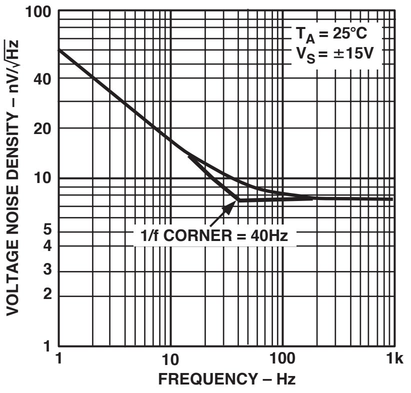
ORDERING GUIDE

T_A = 25°C V_{OS} Max (μV)	Package CERDIP 8-Pin	Package Plastic	Operating Temperature Range
200	*OP271AZ		MIL
200	*OP271EZ		XND
300	*OP271FZ		XND
400		OP271GP	XND
400		*OP271GS	XND

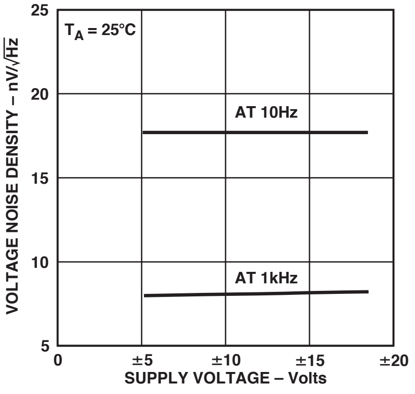
*Not for new design, obsolete April 2002.

CAUTION

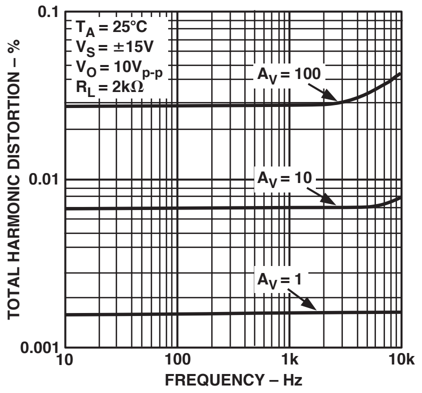
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP271 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



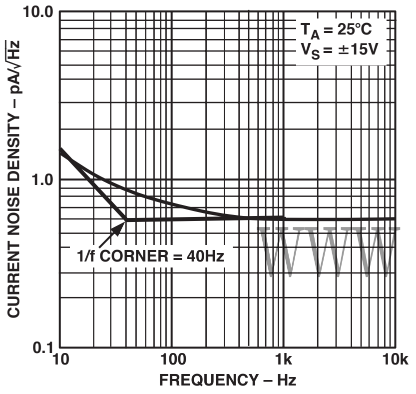
TPC 1. Voltage Noise Density vs. Frequency



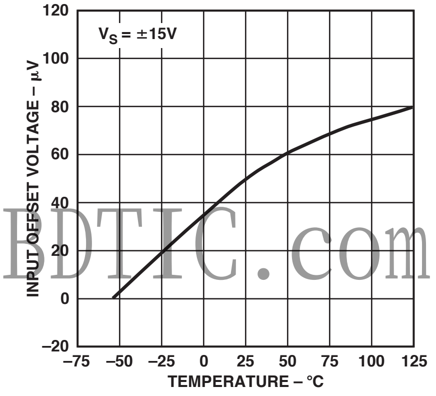
TPC 2. Voltage Noise Density vs. Supply Voltage



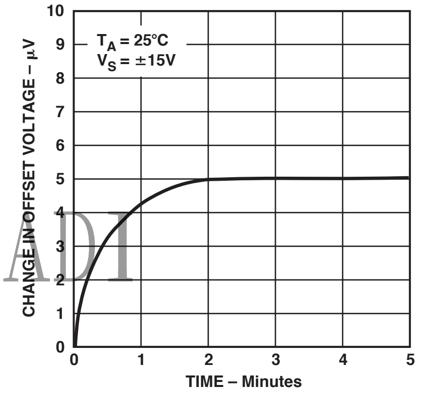
TPC 3. Total Harmonic Distortion vs. Frequency



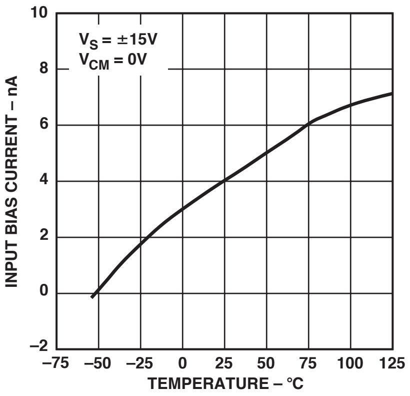
TPC 4. Current Noise Density vs. Frequency



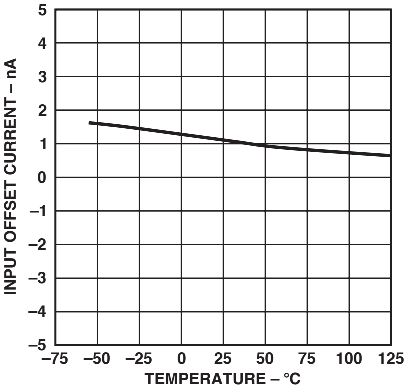
TPC 5. Input Offset Voltage vs. Temperature



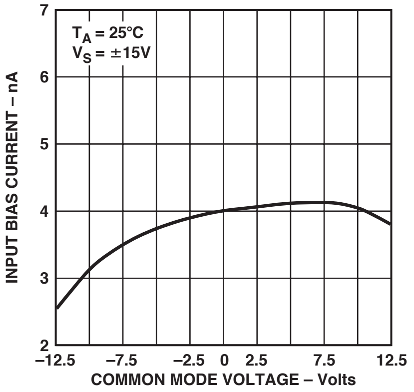
TPC 6. Warm-Up Offset Voltage Drift



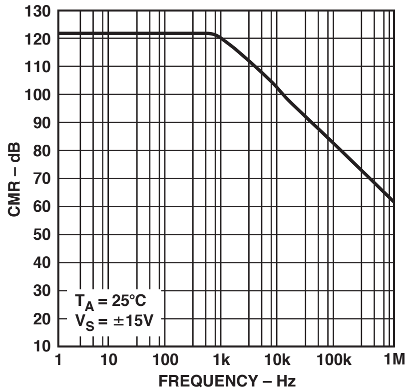
TPC 7. Input Bias Current vs. Temperature



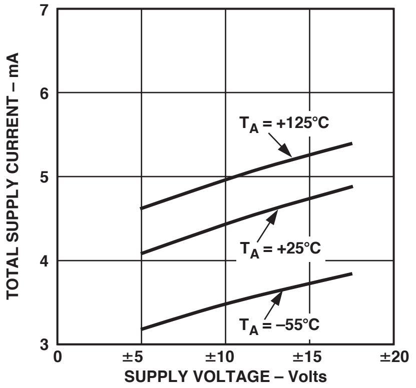
TPC 8. Input Offset Current vs. Temperature



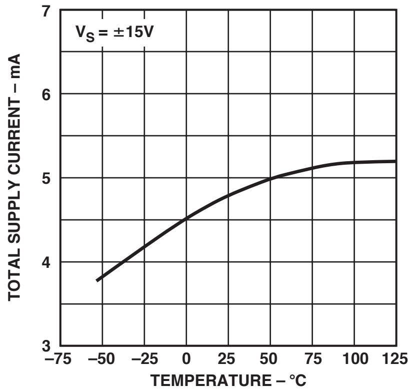
TPC 9. Input Bias Current vs. Common-Mode Voltage



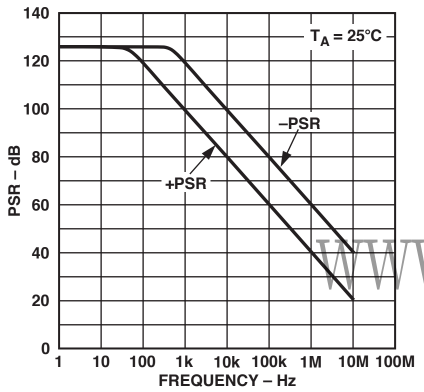
TPC 10. CMR vs. Frequency



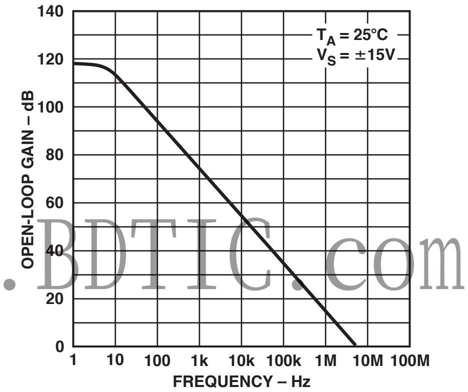
TPC 11. Total Supply Current vs. Supply Voltage



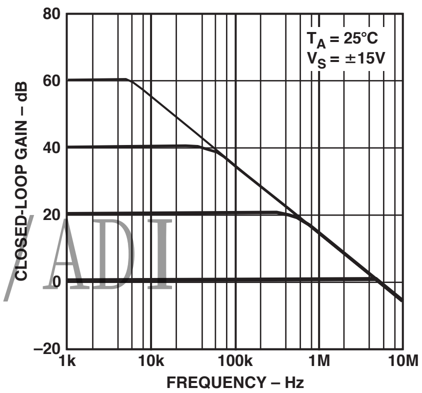
TPC 12. Total Supply Current vs. Temperature



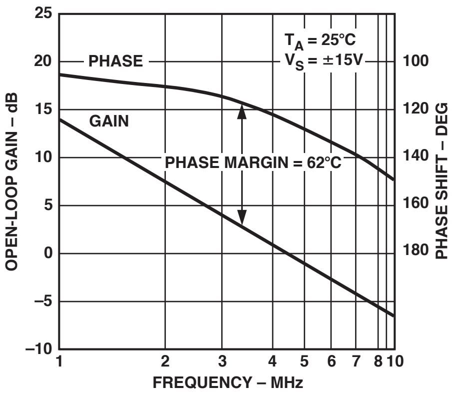
TPC 13. PSR vs. Frequency



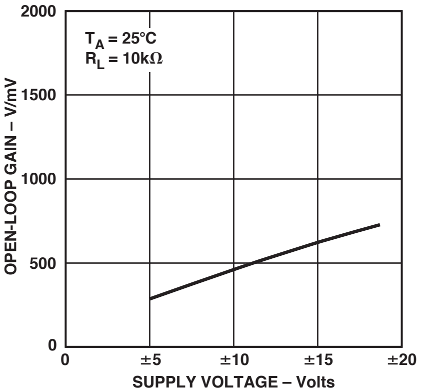
TPC 14. Open-Loop Gain vs. Frequency



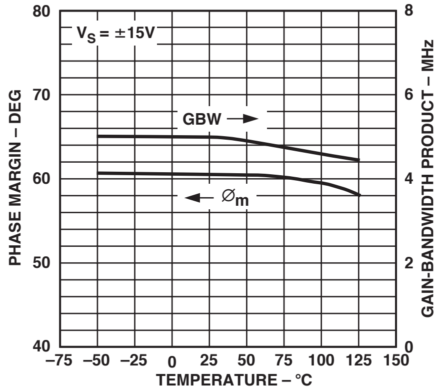
TPC 15. Closed-Loop Gain vs. Frequency



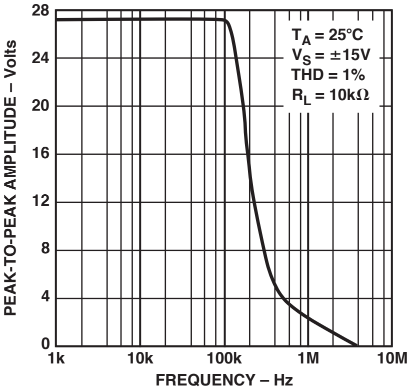
TPC 16. Open-Loop Gain, Phase Shift vs. Frequency



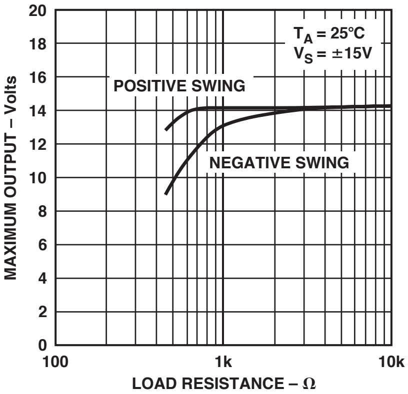
TPC 17. Open-Loop Gain vs. Supply Voltage



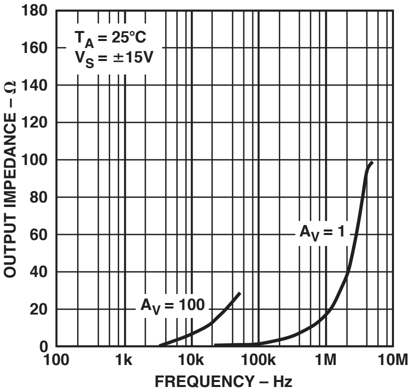
TPC 18. Gain-Bandwidth Product, Phase Margin vs. Temperature



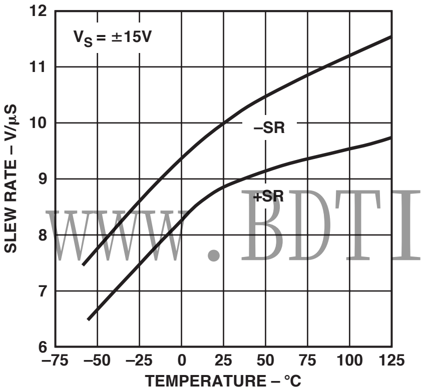
TPC 19. Maximum Output Swing vs. Frequency



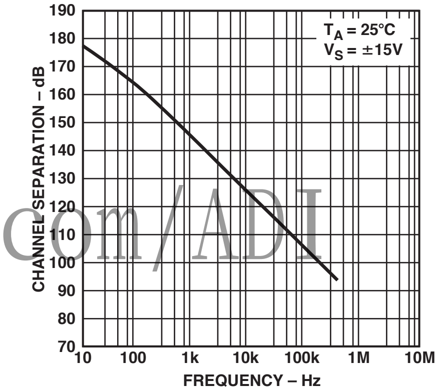
TPC 20. Maximum Output Voltage vs. Load Resistance



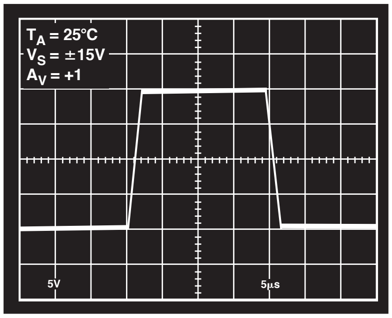
TPC 21. Output Impedance vs. Frequency



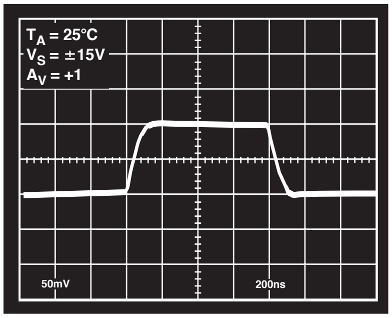
TPC 22. Slew Rate vs. Temperature



TPC 23. Channel Separation vs. Frequency



TPC 24. Large-Signal Transient Response



TPC 25. Small Signal Transient Response

APPLICATION INFORMATION

Capacitive Load Driving and Power Supply Considerations

The OP217 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP271.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 2. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000 pF when used with the OP271.

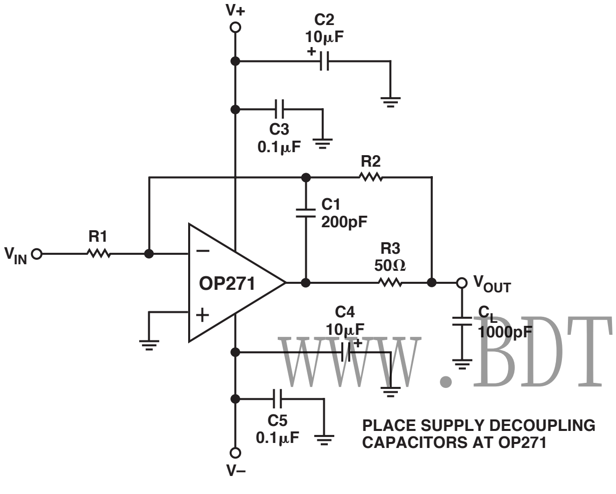


Figure 2. Driving Large Capacitive Loads

Unity-Gain Buffer Applications

When $R_f \leq 100\ \Omega$ and the input is driven with a fast, large-signal pulse (>1 V), the output waveform will look as shown in Figure 3.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\ \Omega$, the output is capable of handling the current requirements ($I_L \leq 20$ mA at 10 V); the amplifier will stay in its active mode and a smooth transition will occur.

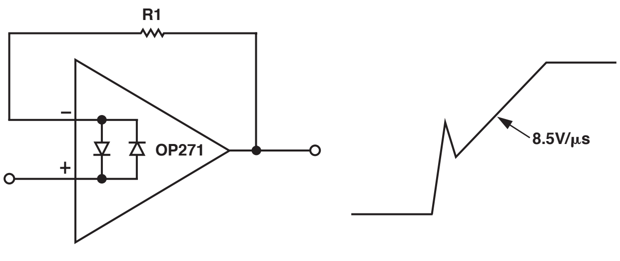


Figure 3. Pulsed Operation

When $R_f > 3\ k\Omega$, a pole created by R_f and the amplifier's input capacitance (3 pF) creates additional phase shift and reduces phase margin. A small capacitor in parallel with R_f helps eliminate this problem.

Computer Simulations

Many electronic design and analysis programs include models for op amps which calculate AC performance from the location of poles and zeros. As an aid to designers utilizing such a program, major poles and zeros of the OP271 are listed below. Their location will vary slightly between production lots. Typically, they will be within ±15% of the frequency listed. Use of this data will enable the designer to evaluate gross circuit performance quickly, but should not supplant rigorous characterization of a breadboard circuit.

POLES	ZEROS
15Hz	2.5 MHz
1.2 MHz	4 X 23 MHz
2 X 32 MHz	-
8 X 40 MHz	-

APPLICATIONS

Low Phase Error Amplifier

The simple amplifier depicted in Figure 4, utilizes a monolithic dual operational amplifier and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces $V_O/V_{IN} = K1 + 1$. The DC gain is determined by the resistor divider around A2. Note that, like a conventional single op amp amplifier, the DC gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

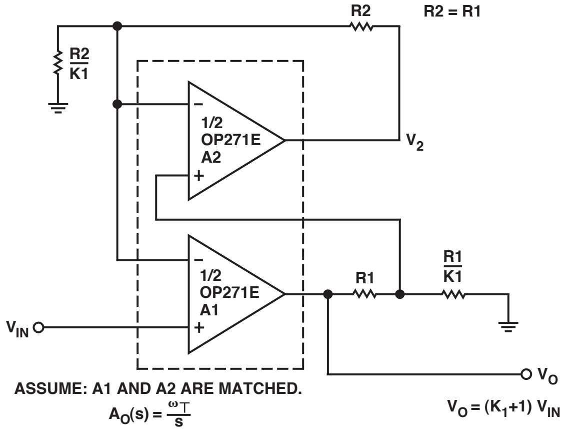


Figure 4. Low Phase Error Amplifier

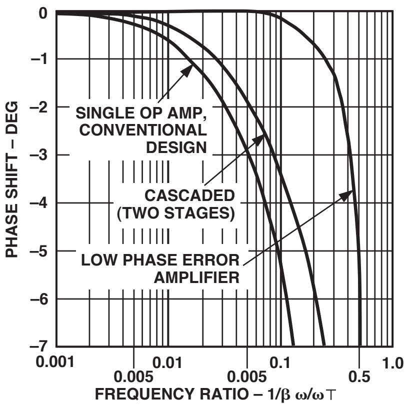


Figure 5. Phase Error Comparison

Figure 5 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/B\omega_T$<0.1. For example, phase error of -0.1° occurs at 0.002 $\omega/B\omega_T$ for the single op amplifier, but at 0.11 $\omega/B\omega_T$ for the low phase error amplifier.

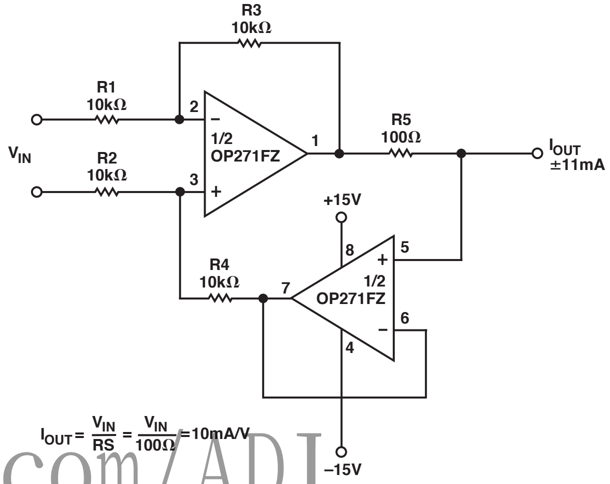
For more detailed information on the low phase error amplifier, see Application Note AN-107.

Dual 12-Bit Voltage Output DAC

The dual voltage output DAC shown in Figure 6 will settle to 12-bit accuracy from zero to full scale in 2 μs typically. The CMOS DAC-8222 utilizes a 12-bit, double-buffered input structure allowing faster digital throughput and minimizing digital feedback.

Fast Current Pump

Maximum output current of the fast current pump shown in Figure 7 is ±11 mA. Voltage compliance exceeds ±10 V with ±15 V supplies. The current pump has an output resistance of over 3 MΩ and maintains 12-bit linearity over its entire output range.



$I_{OUT} = \frac{V_{IN}}{RS} = \frac{V_{IN}}{100\Omega} = 10mA/V$

Figure 7. Fast Current Pump

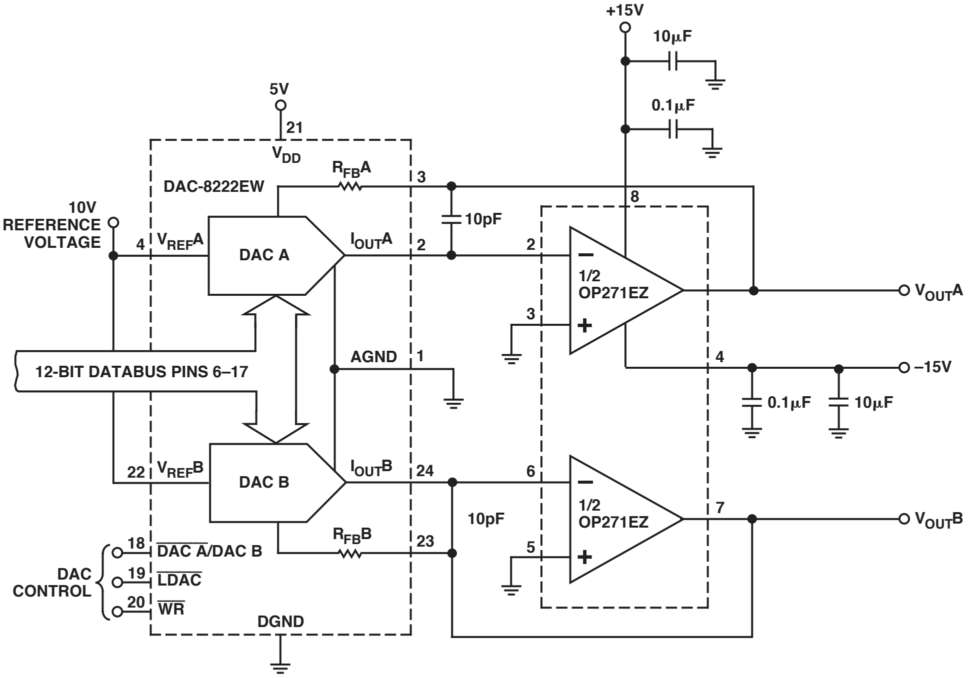
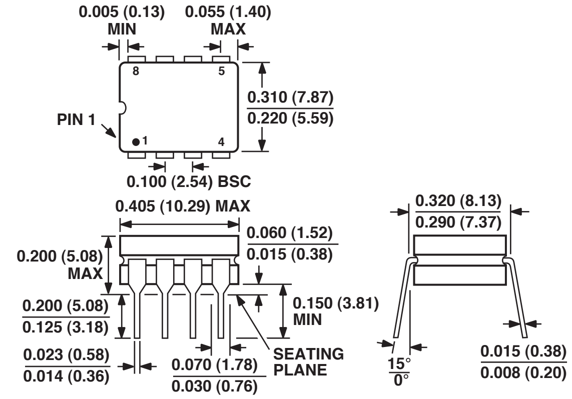


Figure 6. Dual 12-Bit Voltage Output DAC

OUTLINE DIMENSIONS

8-Lead Ceramic Dip-Glass Hermetic Seal [CERDIP]
(Q-8)

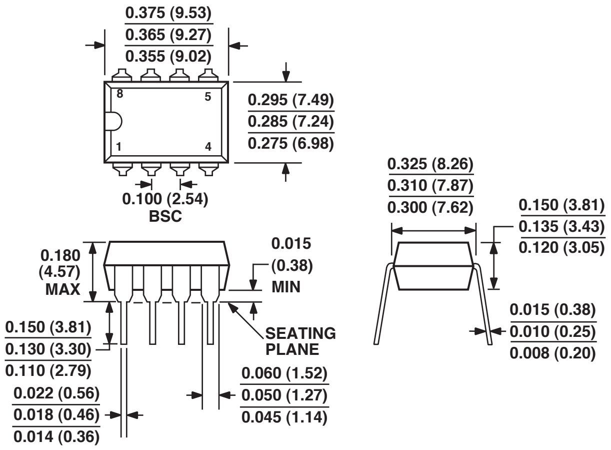
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCH; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Plastic Dual-in-Line Package [PDIP]
(N-8)

Dimensions shown in inches and (millimeters)

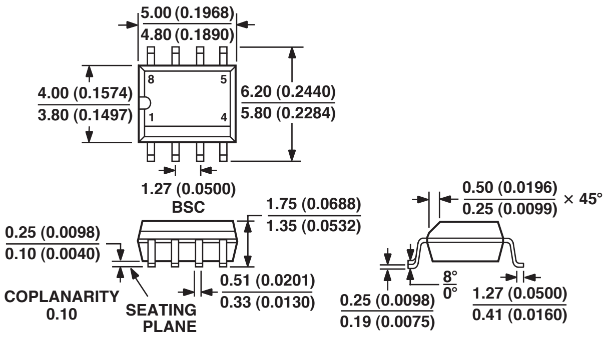


COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES)

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(RN-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

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10/02—Data Sheet changed from REV. 0 to REV. A.	
Deleted PIN CONNECTIONS Caption	1
Edits to ORDERING GUIDE	4
Edits to ABSOLUTE MAXIMUM RATINGS	4
Edits to Figure 6	9
Updated OUTLINE DIMENSIONS	10

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