

Features

- 400 MHz ARM926EJ-S™ ARM® Thumb® Processor
 - 32 KBytes Data Cache, 32 KBytes Instruction Cache, MMU
- Memories
 - 4-port, 4-bank DDR2/LPDDR Controller
 - External Bus Interface supporting 4-bank DDR2/LPDDR, SDR/LPSDR, Static Memories, CompactFlash, SLC NAND Flash with ECC
 - One 64-KByte internal SRAM, single-cycle access at system speed or processor speed through TCM interface
 - One 64-KByte internal ROM, embedding bootstrap routine
- Peripherals
 - LCD Controller supporting STN and TFT displays up to 1280*860
 - ITU-R BT. 601/656 Image Sensor Interface
 - Dual High Speed USB Host and a High Speed USB Device with On-Chip Transceivers
 - 10/100 Mbps Ethernet MAC Controller
 - Two High Speed Memory Card Hosts (SDIO, SDCard, e.MMC and CE ATA)
 - AC'97 controller
 - Two Master/Slave Serial Peripheral Interfaces
 - Two Three-channel 16-bit Timer/Counters
 - Two Synchronous Serial Controllers (I2S mode)
 - Four-channel 16-bit PWM Controller
 - Two Two-wire Interfaces
 - Four USARTs with ISO7816, IrDA, Manchester and SPI modes; one DBGU
 - 8-channel 10-bit ADC with 4-wire Touch Screen support
- Cryptography
 - TRNG True Random Number Generator
 - AES256-, 192-, 128-bit Key Algorithm,
 - TDES Compliant with FIPS PUB 46-3 Specifications
 - SHA (SHA1 and SHA256) Compliant with *FIPS Publication 180-2*
- System
 - 133 MHz twelve 32-bit layer AHB Bus Matrix
 - 39 DMA Channels
 - Boot from NAND Flash, SDCard, DataFlash® or serial DataFlash
 - Reset Controller with on-chip Power-on Reset
 - Selectable 32768 Hz Low-power and 12 MHz Crystal Oscillators
 - Internal Low-power 32 kHz RC Oscillator
 - One PLL for the system and one 480 MHz PLL optimized for USB High Speed
 - Two Programmable External Clock Signals
 - Advanced Interrupt Controller and Debug Unit
 - Periodic Interval Timer, Watchdog Timer, Real Time Timer and Real Time Clock
- I/O
 - Five 32-bit Parallel Input/Output Controllers
 - 160 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os with Schmitt trigger input
- Package
 - 324-ball TFBGA, pitch 0.8 mm



AT91SAM ARM-based Embedded MPU

SAM9G46

Summary

NOTE: This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

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1. Description

The ARM926EJ-S based SAM9G46 features the frequently requested combination of user interface functionality and high data rate connectivity, including LCD Controller, resistive touch-screen, camera interface, audio, Ethernet 10/100 and high speed USB and SDIO. With the processor running at 400MHz and multiple 100+ Mbps data rate peripherals, the SAM9G46 has the performance and bandwidth to the network or local storage media to provide an adequate user experience.

The SAM9G46 supports the latest generation of DDR2 and NAND Flash memory interfaces for program and data storage. An internal 133 MHz multi-layer bus architecture associated with 39 DMA channels, a dual external bus interface and distributed memory including a 64-KByte SRAM that can be configured as a tightly coupled memory (TCM) sustains the high bandwidth required by the processor and the high speed peripherals.

On-chip hardware accelerators with DMA support enable high-speed data encryption and authentication of the transferred data or application. Supported standards are up to 256-bit AES, FIPS PUB 46-3 compliant TDES and FIPS Publication 180-2 compliant SHA1 and SHA256. A True Random Number Generator is embedded for key generation and exchange protocols.

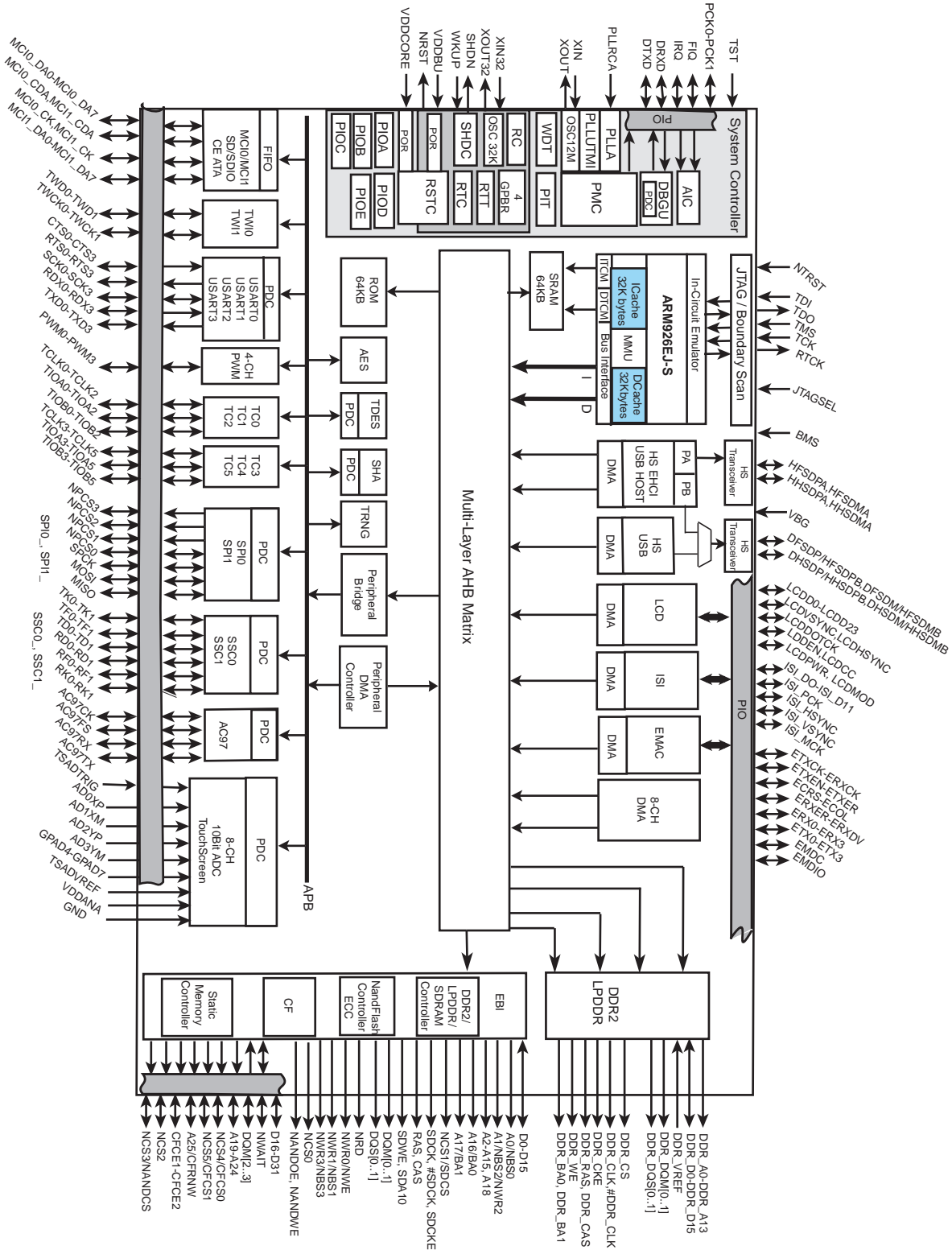
The I/Os support 1.8V or 3.3V operation, which are independently configurable for the memory interface and peripheral I/Os. This feature completely eliminates the need for any external level shifters. In addition it supports 0.8 ball pitch package for low cost PCB manufacturing.

The SAM9G46 power management controller features efficient clock gating and a battery backup section minimizing power consumption in active and standby modes.



2. Block Diagram

Figure 2-1. SAM9G46 Block Diagram





3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

| Signal Name | Function | Type | Active Level | Reference Voltage | Comments |
|-------------------------------------|---|--------|--------------|-------------------|--------------------------------|
| Power Supplies | | | | | |
| VDDIOM0 | DDR2 I/O Lines Power Supply | Power | | | 1.65V to 1.95V |
| VDDIOM1 | EBI I/O Lines Power Supply | Power | | | 1.65V to 1.95V or 3.0V to 3.6V |
| VDDIOP0 | Peripherals I/O Lines Power Supply | Power | | | 1.65V to 3.6V |
| VDDIOP1 | Peripherals I/O Lines Power Supply | Power | | | 1.65V to 3.6V |
| VDDIOP2 | ISI I/O Lines Power Supply | Power | | | 1.65V to 3.6V |
| VDDDBU | Backup I/O Lines Power Supply | Power | | | 1.8V to 3.6V |
| VDDANA | Analog Power Supply | Power | | | 3.0V to 3.6V |
| VDDPLLA | PLLA Power Supply | Power | | | 0.9V to 1.1V |
| VDDPLLUTMI | PLLUTMI Power Supply | Power | | | 0.9V to 1.1V |
| VDDOSC | Oscillator Power Supply | Power | | | 1.65V to 3.6V |
| VDDCORE | Core Chip Power Supply | Power | | | 0.9V to 1.1V |
| VDDUTMIC | UDPHS and UPHPS UTMI+ Core Power Supply | Power | | | 0.9V to 1.1V |
| VDDUTMII | UDPHS and UPHPS UTMI+ interface Power Supply | Power | | | 3.0V to 3.6V |
| GNDIOM | DDR2 and EBI I/O Lines Ground | Ground | | | |
| GNDIOP | Peripherals and ISI I/O lines Ground | Ground | | | |
| GNDCORE | Core Chip Ground | Ground | | | |
| GNDOSC | PLLA, PLLUTMI and Oscillator Ground | Ground | | | |
| GNDDBU | Backup Ground | Ground | | | |
| GNDUTMI | UDPHS and UPHPS UTMI+ Core and interface Ground | Ground | | | |
| GNDANA | Analog Ground | Ground | | | |
| Clocks, Oscillators and PLLs | | | | | |
| XIN | Main Oscillator Input | Input | | | |
| XOUT | Main Oscillator Output | Output | | | |
| XIN32 | Slow Clock Oscillator Input | Input | | | |
| XOUT32 | Slow Clock Oscillator Output | Output | | | |
| VBG | Bias Voltage Reference for USB | Analog | | | |
| PCK0 - PCK1 | Programmable Clock Output | Output | | (1) | |

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Reference Voltage | Comments |
|---|--------------------------------------|--------|--------------|-------------------|---|
| Shutdown, Wakeup Logic | | | | | |
| SHDN | Shut-Down Control | Output | | VDDDBU | Driven at 0V only. 0: The device is in backup mode 1: The device is running (not in backup mode). |
| WKUP | Wake-Up Input | Input | | VDDDBU | Accept between 0V and VDDDBU. |
| ICE and JTAG | | | | | |
| TCK | Test Clock | Input | | VDDIOP0 | No pull-up resistor, Schmitt trigger |
| TDI | Test Data In | Input | | VDDIOP0 | No pull-up resistor, Schmitt trigger |
| TDO | Test Data Out | Output | | VDDIOP0 | |
| TMS | Test Mode Select | Input | | VDDIOP0 | No pull-up resistor, Schmitt trigger |
| JTAGSEL | JTAG Selection | Input | | VDDDBU | Pull-down resistor (15 k Ω). |
| RTCK | Return Test Clock | Output | | VDDIOP0 | |
| Reset/Test | | | | | |
| NRST | Microcontroller Reset ⁽²⁾ | I/O | Low | VDDIOP0 | Open-drain output, Pull-Up resistor (100 k Ω), Schmitt trigger |
| TST | Test Mode Select | Input | | VDDDBU | Pull-down resistor (15 k Ω), Schmitt trigger |
| NTRST | Test Reset Signal | Input | | VDDIOP0 | Pull-Up resistor (100 k Ω), Schmitt trigger |
| BMS | Boot Mode Select | Input | | VDDIOP0 | must be connected to GND or VDDIOP. |
| Debug Unit - DBGU | | | | | |
| DRXD | Debug Receive Data | Input | | (1) | |
| DTXD | Debug Transmit Data | Output | | (1) | |
| Advanced Interrupt Controller - AIC | | | | | |
| IRQ | External Interrupt Input | Input | | (1) | |
| FIQ | Fast Interrupt Input | Input | | (1) | |
| PIO Controller - PIOA- PIOB - PIOC - PIOD - PIOE | | | | | |
| PA0 - PA31 | Parallel IO Controller A | I/O | | (1) | Pulled-up input at reset (100k Ω) ⁽³⁾ , Schmitt trigger |
| PB0 - PB31 | Parallel IO Controller B | I/O | | (1) | Pulled-up input at reset (100k Ω) ⁽³⁾ , Schmitt trigger |





Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Reference Voltage | Comments |
|--|------------------------------|--------|--------------|-------------------|---|
| PC0 - PC31 | Parallel IO Controller C | I/O | | (1) | Pulled-up input at reset (100kΩ) ⁽³⁾ , Schmitt trigger |
| PD0 - PD31 | Parallel IO Controller D | I/O | | (1) | Pulled-up input at reset (100kΩ) ⁽³⁾ , Schmitt trigger |
| PE0 - PE31 | Parallel IO Controller E | I/O | | (1) | Pulled-up input at reset (100kΩ) ⁽³⁾ , Schmitt trigger |
| DDR Memory Interface- DDR2/LPDDR Controller | | | | | |
| DDR_D0 - DDR_D15 | Data Bus | I/O | | VDDIOM0 | Pulled-up input at reset |
| DDR_A0 - DDR_A13 | Address Bus | Output | | VDDIOM0 | 0 at reset |
| DDR_CLK-#DDR_CLK | DDR differential clock input | Output | | VDDIOM0 | |
| DDR_CKE | DDR Clock Enable | Output | High | VDDIOM0 | |
| DDR_CS | DDR Chip Select | Output | Low | VDDIOM0 | |
| DDR_WE | DDR Write Enable | Output | Low | VDDIOM0 | |
| DDR_RAS- DDR_CAS | Row and Column Signal | Output | Low | VDDIOM0 | |
| DDR_DQM[0..1] | Write Data Mask | Output | | VDDIOM0 | |
| DDR_DQS[0..1] | Data Strobe | Output | | VDDIOM0 | |
| DDR_BA0 - DDR_BA1 | Bank Select | Output | | VDDIOM0 | |
| DDR_VREF | Reference Voltage | Input | | VDDIOM0 | |
| External Bus Interface - EBI | | | | | |
| D0 -D31 | Data Bus | I/O | | VDDIOM1 | Pulled-up input at reset |
| A0 - A25 | Address Bus | Output | | VDDIOM1 | 0 at reset |
| NWAIT | External Wait Signal | Input | Low | VDDIOM1 | |
| EBI - Static Memory Controller - SMC | | | | | |
| NCS0 - NCS5 | Chip Select Lines | Output | Low | VDDIOM1 | |
| NWR0 - NWR3 | Write Signal | Output | Low | VDDIOM1 | |
| NRD | Read Signal | Output | Low | VDDIOM1 | |
| NWE | Write Enable | Output | Low | VDDIOM1 | |
| NBS0 - NBS3 | Byte Mask Signal | Output | Low | VDDIOM1 | |
| EBI - CompactFlash Support | | | | | |
| CFCE1 - CFCE2 | CompactFlash Chip Enable | Output | Low | VDDIOM1 | |
| CFOE | CompactFlash Output Enable | Output | Low | VDDIOM1 | |
| CFWE | CompactFlash Write Enable | Output | Low | VDDIOM1 | |
| CFIOR | CompactFlash IO Read | Output | Low | VDDIOM1 | |

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Reference Voltage | Comments |
|---|-----------------------------------|--------|--------------|-------------------|----------|
| CFIOW | CompactFlash IO Write | Output | Low | VDDIOM1 | |
| CFRNW | CompactFlash Read Not Write | Output | | VDDIOM1 | |
| CFCS0 -CFCS1 | CompactFlash Chip Select Lines | Output | Low | VDDIOM1 | |
| EBI - NAND Flash Support | | | | | |
| NANDCS | NAND Flash Chip Select | Output | Low | VDDIOM1 | |
| NANDOE | NAND Flash Output Enable | Output | Low | VDDIOM1 | |
| NANDWE | NAND Flash Write Enable | Output | Low | VDDIOM1 | |
| EBI - DDR2/SDRAM/LPDDR Controller | | | | | |
| SDCK,#SDCK | DDR2/SDRAM differential clock | Output | | VDDIOM1 | |
| SDCKE | DDR2/SDRAM Clock Enable | Output | High | VDDIOM1 | |
| SDCS | DDR2/SDRAM Controller Chip Select | Output | Low | VDDIOM1 | |
| BA0 - BA1 | Bank Select | Output | | VDDIOM1 | |
| SDWE | DDR2/SDRAM Write Enable | Output | Low | VDDIOM1 | |
| RAS - CAS | Row and Column Signal | Output | Low | VDDIOM1 | |
| SDA10 | SDRAM Address 10 Line | Output | | VDDIOM1 | |
| DQS[0..1] | Data Strobe | Output | | VDDIOM1 | |
| DQM[0..3] | Write Data Mask | Output | | VDDIOM1 | |
| High Speed Multimedia Card Interface - HSMCIx | | | | | |
| MCIx_CK | Multimedia Card Clock | I/O | | (1) | |
| MCIx_CDA | Multimedia Card Slot A Command | I/O | | (1) | |
| MCIx_DA0 - MCIx_DA7 | Multimedia Card Slot A Data | I/O | | (1) | |
| Universal Synchronous Asynchronous Receiver Transmitter - USARTx | | | | | |
| SCKx | USARTx Serial Clock | I/O | | (1) | |
| TXDx | USARTx Transmit Data | Output | | (1) | |
| RXDx | USARTx Receive Data | Input | | (1) | |
| RTSx | USARTx Request To Send | Output | | (1) | |
| CTSx | USARTx Clear To Send | Input | | (1) | |
| Synchronous Serial Controller - SSCx | | | | | |
| TDx | SSC Transmit Data | Output | | (1) | |
| RDx | SSC Receive Data | Input | | (1) | |
| TKx | SSC Transmit Clock | I/O | | (1) | |
| RKx | SSC Receive Clock | I/O | | (1) | |
| TFx | SSC Transmit Frame Sync | I/O | | (1) | |
| RFx | SSC Receive Frame Sync | I/O | | (1) | |





Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Reference Voltage | Comments |
|--|-----------------------------------|--------|--------------|-------------------|------------------------|
| AC97 Controller - AC97C | | | | | |
| AC97RX | AC97 Receive Signal | Input | | (1) | |
| AC97TX | AC97 Transmit Signal | Output | | (1) | |
| AC97FS | AC97 Frame Synchronization Signal | Output | | (1) | |
| AC97CK | AC97 Clock signal | Input | | (1) | |
| Time Counter - TCx | | | | | |
| TCLKx | TC Channel x External Clock Input | Input | | (1) | |
| TIOAx | TC Channel x I/O Line A | I/O | | (1) | |
| TIOBx | TC Channel x I/O Line B | I/O | | (1) | |
| Pulse Width Modulation Controller - PWM | | | | | |
| PWMx | Pulse Width Modulation Output | Output | | (1) | |
| Serial Peripheral Interface - SPIx_ | | | | | |
| SPIx_MISO | Master In Slave Out | I/O | | (1) | |
| SPIx_MOSI | Master Out Slave In | I/O | | (1) | |
| SPIx_SPCK | SPI Serial Clock | I/O | | (1) | |
| SPIx_NPCS0 | SPI Peripheral Chip Select 0 | I/O | Low | (1) | |
| SPIx_NPCS1- SPIx_NPCS3 | SPI Peripheral Chip Select | Output | Low | (1) | |
| Two-Wire Interface | | | | | |
| TWDx | Two-wire Serial Data | I/O | | (1) | |
| TWCKx | Two-wire Serial Clock | I/O | | (1) | |
| USB Host High Speed Port - UHPHS | | | | | |
| HFSDPA | USB Host Port A Full Speed Data + | Analog | | VDDUTMII | |
| HFSDMA | USB Host Port A Full Speed Data - | Analog | | VDDUTMII | |
| HHSDPA | USB Host Port A High Speed Data + | Analog | | VDDUTMII | |
| HHSDMA | USB Host Port A High Speed Data - | Analog | | VDDUTMII | |
| HFSDPB | USB Host Port B Full Speed Data + | Analog | | VDDUTMII | Multiplexed with DFSDP |
| HFSDMB | USB Host Port B Full Speed Data - | Analog | | VDDUTMII | Multiplexed with DFSDM |
| HHSDPB | USB Host Port B High Speed Data + | Analog | | VDDUTMII | Multiplexed with DHSDP |
| HHSDMB | USB Host Port B High Speed Data - | Analog | | VDDUTMII | Multiplexed with DHSDM |
| USB Device High Speed Port - UDPHS | | | | | |
| DFSDM | USB Device Full Speed Data - | Analog | | VDDUTMII | |
| DFSDP | USB Device Full Speed Data + | Analog | | VDDUTMII | |
| DHSDM | USB Device High Speed Data - | Analog | | VDDUTMII | |
| DHSDP | USB Device High Speed Data + | Analog | | VDDUTMII | |

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Reference Voltage | Comments |
|---|---|--------|--------------|-------------------|----------------------------|
| Ethernet 10/100 | | | | | |
| ETXCK | Transmit Clock or Reference Clock | Input | | (1) | MII only, REFCK in RMII |
| ERXCK | Receive Clock | Input | | (1) | MII only |
| ETXEN | Transmit Enable | Output | | (1) | |
| ETX0-ETX3 | Transmit Data | Output | | (1) | ETX0-ETX1 only in RMII |
| ETXER | Transmit Coding Error | Output | | (1) | MII only |
| ERXDV | Receive Data Valid | Input | | (1) | RXDV in MII, CRSDV in RMII |
| ERX0-ERX3 | Receive Data | Input | | (1) | ERX0-ERX1 only in RMII |
| ERXER | Receive Error | Input | | (1) | |
| ECRS | Carrier Sense and Data Valid | Input | | (1) | MII only |
| ECOL | Collision Detect | Input | | (1) | MII only |
| EMDC | Management Data Clock | Output | | (1) | |
| EMDIO | Management Data Input/Output | I/O | | (1) | |
| Image Sensor Interface | | | | | |
| ISI_D0-ISI_D11 | Image Sensor Data | Input | | VDDIOP2 | |
| ISI_MCK | Image sensor Reference clock | output | | VDDIOP2 | |
| ISI_HSYNC | Image Sensor Horizontal Synchro | input | | VDDIOP2 | |
| ISI_VSYNC | Image Sensor Vertical Synchro | input | | VDDIOP2 | |
| ISI_PCK | Image Sensor Data clock | input | | VDDIOP2 | |
| LCD Controller - LCDC | | | | | |
| LCDD0 - LCDD23 | LCD Data Bus | Output | | VDDIOP1 | |
| LCDVSYNC | LCD Vertical Synchronization | Output | | VDDIOP1 | |
| LCDHSYNC | LCD Horizontal Synchronization | Output | | VDDIOP1 | |
| LCDDOTCK | LCD Dot Clock | Output | | VDDIOP1 | |
| LCDDEN | LCD Data Enable | Output | | VDDIOP1 | |
| LCDCC | LCD Contrast Control | Output | | VDDIOP1 | |
| LCDPWR | LCD panel Power enable control | Output | | VDDIOP1 | |
| LCDMOD | LCD Modulation signal | Output | | VDDIOP1 | |
| Touch Screen Analog-to-Digital Converter | | | | | |
| AD0X _p | Analog input channel 0 or Touch Screen Top channel | Analog | | VDDANA | Multiplexed with AD0 |
| AD1X _M | Analog input channel 1 or Touch Screen Bottom channel | Analog | | VDDANA | Multiplexed with AD1 |
| AD2Y _p | Analog input channel 2 or Touch Screen Right channel | Analog | | VDDANA | Multiplexed with AD2 |





Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Reference Voltage | Comments |
|-------------------|---|--------|--------------|-------------------|----------------------|
| AD3Y _M | Analog input channel 3 or Touch Screen Left channel | Analog | | VDDANA | Multiplexed with AD3 |
| GPAD4-GPAD7 | Analog Inputs | Analog | | VDDANA | |
| TSADTRG | ADC Trigger | Input | | VDDANA | |
| TSADVREF | ADC Reference | Analog | | VDDANA | |

- Notes:
1. Refer to peripheral multiplexing tables in [Section 9.4 “Peripheral Signals Multiplexing on I/O Lines”](#) for these signals.
 2. When configured as an input, the NRST pin enables asynchronous reset of the device when asserted low. This allows connection of a simple push button on the NRST pin as a system-user reset.
 3. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers. After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the peripheral multiplexing tables.

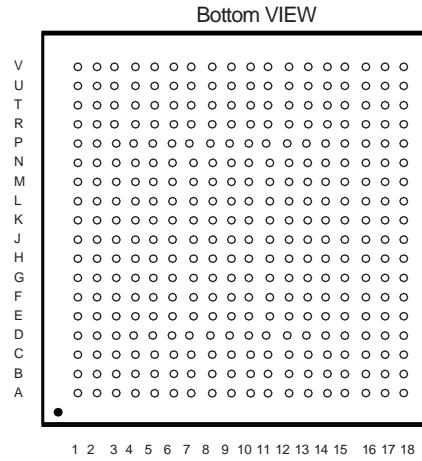
4. Package and Pinout

The SAM9G46 is delivered in a 324-ball TFBGA package.

4.1 Mechanical Overview of the 324-ball TFBGA Package

Figure 4-1 shows the orientation of the 324-ball TFBGA Package

Figure 4-1. Orientation of the 324-ball TFBGA Package





4.2 324-ball TFBGA Package Pinout

Table 4-1. SAM9G46 Pinout for 324-ball BGA Package

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|--------------|-----|-------------|-----|-------------|
| A1 | PC27 | E10 | NANDWE | K1 | PE21 | P10 | TMS |
| A2 | PC28 | E11 | DQS1 | K2 | PE23 | P11 | VDDPLLA |
| A3 | PC25 | E12 | D13 | K3 | PE26 | P12 | PB20 |
| A4 | PC20 | E13 | D11 | K4 | PE22 | P13 | PB31 |
| A5 | PC12 | E14 | A4 | K5 | PE24 | P14 | DDR_D7 |
| A6 | PC7 | E15 | A8 | K6 | PE25 | P15 | DDR_D3 |
| A7 | PC5 | E16 | A9 | K7 | PE27 | P16 | DDR_D4 |
| A8 | PC0 | E17 | A7 | K8 | PE28 | P17 | DDR_D5 |
| A9 | NWR3/NBS3 | E18 | VDDCORE | K9 | VDDIOP0 | P18 | DDR_D10 |
| A10 | NCS0 | F1 | PD22 | K10 | VDDIOP0 | R1 | PA18 |
| A11 | DQS0 | F2 | PD24 | K11 | GNDIOM | R2 | PA20 |
| A12 | RAS | F3 | SHDN | K12 | GNDIOM | R3 | PA24 |
| A13 | SDCK | F4 | PE1 | K13 | VDDIOM0 | R4 | PA30 |
| A14 | NSDCK | F5 | PE3 | K14 | DDR_A7 | R5 | PB4 |
| A15 | D7 | F6 | VDDIOM1 | K15 | DDR_A8 | R6 | PB13 |
| A16 | DDR_VREF | F7 | PC19 | K16 | DDR_A9 | R7 | PD0 |
| A17 | D0 | F8 | PC14 | K17 | DDR_A11 | R8 | PD9 |
| A18 | A14 | F9 | PC4 | K18 | DDR_A10 | R9 | PD18 |
| B1 | PC31 | F10 | NCS1/SDCS | L1 | PA0 | R10 | TDI |
| B2 | PC29 | F11 | NRD | L2 | PE30 | R11 | RTCK |
| B3 | PC30 | F12 | SDWE | L3 | PE29 | R12 | PB22 |
| B4 | PC22 | F13 | A0/NBS0 | L4 | PE31 | R13 | PB29 |
| B5 | PC17 | F14 | A1/NBS2/NWR2 | L5 | PA2 | R14 | DDR_D6 |
| B6 | PC10 | F15 | A3 | L6 | PA4 | R15 | DDR_D1 |
| B7 | PC11 | F16 | A6 | L7 | PA8 | R16 | DDR_D0 |
| B8 | PC2 | F17 | A5 | L8 | PD2 | R17 | HHSDMA |
| B9 | SDA10 | F18 | A2 | L9 | PD13 | R18 | HFSDMA |
| B10 | A17/BA1 | G1 | PD25 | L10 | PD29 | T1 | PA22 |
| B11 | DQM0 | G2 | PD23 | L11 | PD31 | T2 | PA25 |
| B12 | SDCKE | G3 | PE6 | L12 | VDDIOM0 | T3 | PA26 |
| B13 | D12 | G4 | PE0 | L13 | VDDIOM0 | T4 | PB0 |
| B14 | D8 | G5 | PE2 | L14 | DDR_A1 | T5 | PB6 |
| B15 | D4 | G6 | PE8 | L15 | DDR_A3 | T6 | PB16 |
| B16 | D3 | G7 | PE4 | L16 | DDR_A4 | T7 | PD1 |
| B17 | A15 | G8 | PE11 | L17 | DDR_A6 | T8 | PD11 |
| B18 | A13 | G9 | GNDCORE | L18 | DDR_A5 | T9 | PD19 |
| C1 | XIN32 | G10 | VDDIOM1 | M1 | PA1 | T10 | PD30 |
| C2 | GNDANA | G11 | VDDIOM1 | M2 | PA5 | T11 | BMS |
| C3 | WKUP | G12 | VDDCORE | M3 | PA6 | T12 | PB8 |
| C4 | PC26 | G13 | VDDCORE | M4 | PA7 | T13 | PB30 |
| C5 | PC21 | G14 | DDR_DQM0 | M5 | PA10 | T14 | DDR_D2 |
| C6 | PC15 | G15 | DDR_DQS1 | M6 | PA14 | T15 | PB21 |
| C7 | PC9 | G16 | DDR_BA1 | M7 | PB14 | T16 | PB23 |
| C8 | PC3 | G17 | DDR_BA0 | M8 | PD4 | T17 | HHSDPA |
| C9 | NWR0/NWE | G18 | DDR_DQS0 | M9 | PD15 | T18 | HFSDPA |
| C10 | A16/BA0 | H1 | PD26 | M10 | NRST | U1 | PA27 |
| C11 | CAS | H2 | PD27 | M11 | PB11 | U2 | PA29 |
| C12 | D15 | H3 | VDDIOP1 | M12 | PB25 | U3 | PA28 |

Table 4-1. SAM9G46 Pinout for 324-ball BGA Package (Continued)

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|-----|-------------|-----|---------------|
| C13 | D10 | H4 | PE13 | M13 | PB27 | U4 | PB3 |
| C14 | D6 | H5 | PE5 | M14 | VDDIOM0 | U5 | PB7 |
| C15 | D2 | H6 | PE7 | M15 | DDR_D14 | U6 | PB17 |
| C16 | GNDIOM | H7 | PE9 | M16 | DDR_D15 | U7 | PD7 |
| C17 | A18 | H8 | PE10 | M17 | DDR_A0 | U8 | PD10 |
| C18 | A12 | H9 | GNDCORE | M18 | DDR_A2 | U9 | PD14 |
| D1 | XOUT32 | H10 | GNDIOP | N1 | PA3 | U10 | TCK |
| D2 | PD20 | H11 | VDDCORE | N2 | PA9 | U11 | VDDOSC |
| D3 | GNDDBU | H12 | GNDIOM | N3 | PA12 | U12 | GNDOSC |
| D4 | VDDDBU | H13 | GNDIOM | N4 | PA15 | U13 | PB10 |
| D5 | PC24 | H14 | DDR_CS | N5 | PA16 | U14 | PB26 |
| D6 | PC18 | H15 | DDR_WE | N6 | PA17 | U15 | HHSDPB/DHSDP |
| D7 | PC13 | H16 | DDR_DQM1 | N7 | PB18 | U16 | HHSDMB/DHS DM |
| D8 | PC6 | H17 | DDR_CAS | N8 | PD6 | U17 | GNDUTMI |
| D9 | NWR1/NBS1 | H18 | DDR_NCLK | N9 | PD16 | U18 | VDDUTMIC |
| D10 | NANDOE | J1 | PE19 | N10 | NTRST | V1 | PA31 |
| D11 | DQM1 | J2 | PE16 | N11 | PB9 | V2 | PB1 |
| D12 | D14 | J3 | PE14 | N12 | PB24 | V3 | PB2 |
| D13 | D9 | J4 | PE15 | N13 | PB28 | V4 | PB5 |
| D14 | D5 | J5 | PE12 | N14 | DDR_D13 | V5 | PB15 |
| D15 | D1 | J6 | PE17 | N15 | DDR_D8 | V6 | PD3 |
| D16 | VDDIOM1 | J7 | PE18 | N16 | DDR_D9 | V7 | PD5 |
| D17 | A11 | J8 | PE20 | N17 | DDR_D11 | V8 | PD12 |
| D18 | A10 | J9 | GNDCORE | N18 | DDR_D12 | V9 | PD17 |
| E1 | PD21 | J10 | GNDCORE | P1 | PA11 | V10 | TDO |
| E2 | TSADVREF | J11 | GNDIOP | P2 | PA13 | V11 | XOUT |
| E3 | VDDANA | J12 | GNDIOM | P3 | PA19 | V12 | XIN |
| E4 | JTAGSEL | J13 | GNDIOM | P4 | PA21 | V13 | VDDPLLUTMI |
| E5 | TST | J14 | DDR_A12 | P5 | PA23 | V14 | VDDIOP2 |
| E6 | PC23 | J15 | DDR_A13 | P6 | PB12 | V15 | HFSDPB/DFSDP |
| E7 | PC16 | J16 | DDR_CKE | P7 | PB19 | V16 | HFSDMB/DFSDM |
| E8 | PC8 | J17 | DDR_RAS | P8 | PD8 | V17 | VDDUTMII |
| E9 | PC1 | J18 | DDR_CLK | P9 | PD28 | V18 | VBG |





5. Power Considerations

5.1 Power Supplies

The SAM9G46 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 0.9V to 1.1V, 1.0V typical.
- VDDIOM0 pins: Power the DDR2/LPDDR I/O lines; voltage ranges between 1.65V and 1.95V (1.8V typical).
- VDDIOM1 pins: Power the External Bus Interface 1 I/O lines; voltage ranges between 1.65V and 1.95V (1.8V typical) or between 3.0V and 3.6V (3.3V typical).
- VDDIOP0, VDDIOP1, VDDIOP2 pins: Power the Peripherals I/O lines; voltage ranges from 1.65V to 3.6V.
- VDDBU pin: Powers the Slow Clock oscillator, the internal RC oscillator and a part of the System Controller; voltage ranges from 1.8V to 3.6V.
- VDDPLLUTMI Powers the PLLUTMI cell; voltage range from 0.9V to 1.1V.
- VDDUTMIC pin: Powers the USB device and host UTMI+ core; voltage range from 0.9V to 1.1V, 1.0V typical.
- VDDUTMII pin: Powers the USB device and host UTMI+ interface; voltage range from 3.0V to 3.6V, 3.3V typical.
- VDDPLLA pin: Powers the PLLA cell; voltage ranges from 0.9V to 1.1V.
- VDDOSC pin: Powers the Main Oscillator cells; voltage ranges from 1.65V to 3.6V
- VDDANA pin: Powers the Analog to Digital Converter; voltage ranges from 3.0V to 3.6V, 3.3V typical.

Some supply pins share common ground (GND) pins whereas others have separate grounds.

The respective power/ground pin assignments are as follows:

| | |
|--|------------------|
| VDDCORE | GNDCORE |
| VDDIOM0, VDDIOM1 | GNDIOM |
| VDDIOP0, VDDIOP1, VDDIOP2 | GNDIOP |
| VDDBU | GNDDBU |
| VDDUTMIC, VDDUTMII | GNDUTMI |
| VDDPLLUTMI, VDDPLLA, VDDOSC, VDDANA | GNDOSC GNDANA |

6. Processor and Architecture

6.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with DSP Instruction Extensions and Jazelle® technology for Java® acceleration
- Two Instruction Sets
 - ARM High-performance 32-bit Instruction Set
 - Thumb High Code Density 16-bit Instruction Set
- 5-Stage Pipeline Architecture:
 - Instruction Fetch (F)
 - Instruction Decode (D)
 - Execute (E)
 - Data Memory (M)
 - Register Write (W)
- 32-KByte Data Cache, 32-KByte Instruction Cache
 - Virtually-addressed 4-way Associative Cache
 - Eight words per line
 - Write-through and Write-back Operation
 - Pseudo-random or Round-robin Replacement
- Write Buffer
 - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
 - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
 - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
 - Access Permission for Sections
 - Access Permission for large pages and small pages can be specified separately for each quarter of the page
 - 16 embedded domains
- Bus Interface Unit (BIU)
 - Arbitrates and Schedules AHB Requests
 - Separate Masters for both instruction and data access providing complete Matrix system flexibility
 - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
 - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)
- TCM Interface





6.2 Bus Matrix

- 12-layer Matrix, handling requests from 11 masters
- Programmable Arbitration strategy
 - Fixed-priority Arbitration
 - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
 - Breaking with Slot Cycle Limit Support
 - Undefined Burst Length Support
- One Address Decoder provided per Master
 - Three different slaves may be assigned to each decoded memory area: one for internal ROM boot, one for internal flash boot, one after remap
- Boot Mode Select
 - Non-volatile Boot Memory can be internal ROM or external memory on EBI_NCS0
 - Selection is made by General purpose NVM bit sampled at reset
- Remap Command
 - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory (ROM or External Flash)
 - Allows Handling of Dynamic Exception Vectors

6.2.1 Matrix Masters

The Bus Matrix of the SAM9G46 manages Masters, thus each master can perform an access concurrently with others, depending on whether the slave it accesses is available.

Each Master has its own decoder, which can be defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 6-1. List of Bus Matrix Masters

| | |
|-----------|---------------------------------|
| Master 0 | ARM926™ Instruction |
| Master 1 | ARM926 Data |
| Master 2 | Peripheral DMA Controller (PDC) |
| Master 3 | USB HOST OHCI |
| Master 4 | DMA |
| Master 5 | DMA |
| Master 6 | ISI Controller DMA |
| Master 7 | LCD DMA |
| Master 8 | Ethernet MAC DMA |
| Master 9 | USB Device High Speed DMA |
| Master 10 | USB Host High Speed EHCI DMA |

6.2.2 Matrix Slaves

Each Slave has its own arbiter, thus allowing a different arbitration per Slave to be programmed.

Table 6-2. List of Bus Matrix Slaves

| | |
|---------|------------------------|
| Slave 0 | Internal SRAM |
| Slave 1 | Internal ROM |
| | USB OHCI |
| | USB EHCI |
| | UDP High Speed RAM |
| | LCD User Interface |
| Slave 2 | DDR Port 0 |
| Slave 3 | DDR Port 1 |
| Slave 4 | DDR Port 2 |
| Slave 5 | DDR Port 3 |
| Slave 6 | External Bus Interface |
| Slave 7 | Internal Peripherals |

6.2.3 Masters to Slaves Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, such as allowing access from the Ethernet MAC to the internal peripherals. Thus, these paths are forbidden or simply not wired, and shown “-” in the following tables.

The four DDR ports are connected differently according to the application device.

The user can disable the DDR multi-port in the DDR multi-port Register (bit DDRMP_DIS) in the Chip Configuration User Interface.

- When the DDR multi-port is enabled (DDRMP_DIS=0), the ARM instruction and data are respectively connected to DDR Port 0 and DDR Port 1. The other masters share DDR Port 2 and DDR Port 3.
- When the DDR multi-port is disabled (DDRMP_DIS=1), DDR Port 1 is dedicated to the LCD controller. The remaining masters share DDR Port 2 and DDR Port 3.





Figure 6-1. DDR Multi-port

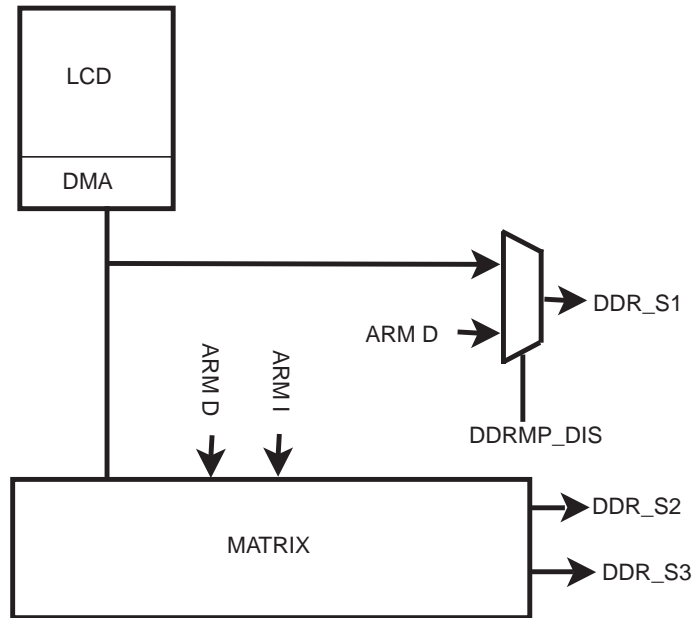


Table 6-3. SAM9G46 Masters to Slaves Access DDRMP_DIS = 0

| Master | 0 | 1 | 2 | 3 | 4 & 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|--------|------------------|--------------|-----|---------------|-------|---------|---------|--------------|---------------|---------------|----------|
| Slave | ARM 926 Instr. | ARM 926 Data | PDC | USB Host OHCI | DMA | ISI DMA | LCD DMA | Ethernet MAC | USB Device HS | USB Host EHCI | Reserved |
| 0 | Internal SRAM 0 | X | X | X | X | X | - | X | X | X | - |
| 1 | Internal ROM | X | X | X | - | - | - | - | - | X | - |
| | UHP OHCI | X | X | - | - | - | - | - | - | - | - |
| | UHP EHCI | X | X | - | - | - | - | - | - | - | - |
| | LCD User Int. | X | X | - | - | - | - | - | - | - | - |
| | UDPHS RAM | X | X | - | - | - | - | - | - | - | - |
| | Reserved | X | X | - | - | - | - | - | - | - | - |
| 2 | DDR Port 0 | X | - | - | - | - | - | - | - | - | - |
| 3 | DDR Port 1 | - | X | - | - | - | - | - | - | - | - |
| 4 | DDR Port 2 | - | - | X | X | X | X | - | X | X | X |
| 5 | DDR Port 3 | - | - | X | X | X | X | X | X | X | - |
| 6 | EBI | X | X | X | X | X | X | X | X | X | X |
| 7 | Internal Periph. | X | X | X | - | X | - | - | - | - | - |

Table 6-4. SAM9G46 Masters to Slaves Access with DDRMP_DIS = 1 (default)

| Master | | 0 | 1 | 2 | 3 | 4 & 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|--------|------------------|-------------------|-----------------|-----|---------------------|-------|------------|------------|-----------------|------------------|------------------|----------|
| Slave | | ARM 926 Instr. | ARM 926 Data | PDC | USB HOST OHCI | DMA | ISI DMA | LCD DMA | Ethernet MAC | USB Device HS | USB Host EHCI | Reserved |
| 0 | Internal SRAM 0 | X | X | X | X | X | X | - | X | X | X | - |
| 1 | Internal ROM | X | X | X | - | - | - | - | - | X | - | - |
| | UHP OHCI | X | X | - | - | - | - | - | - | - | - | - |
| | UHP EHCI | X | X | - | - | - | - | - | - | - | - | - |
| | LCD User Int. | X | X | - | - | - | - | - | - | - | - | - |
| | UDPHS RAM | X | X | - | - | - | - | - | - | - | - | - |
| | Reserved | X | X | - | - | - | - | - | - | - | - | - |
| 2 | DDR Port 0 | - | - | - | - | - | - | - | - | - | - | X |
| 3 | DDR Port 1 | - | - | - | - | - | - | X | - | - | - | - |
| 4 | DDR Port 2 | X | - | X | X | X | X | - | X | X | X | - |
| 5 | DDR Port 3 | - | X | X | X | X | X | - | X | X | X | - |
| 6 | EBI | X | X | X | X | X | X | X | X | X | X | X |
| 7 | Internal Periph. | X | X | X | - | X | - | - | - | - | - | - |

Table 6-5 summarizes the Slave Memory Mapping for each connected Master, depending on the Remap status (RCBx bit in Bus Matrix Master Remap Control Register MATRIX_MRCR) and the BMS state at reset.

Table 6-5. Internal Memory Mapping

| Slave Base Address | Master | | |
|-----------------------|--------------|----------|---------------|
| | RCBx = 0 | | RCBx = 1 |
| | BMS = 1 | BMS = 0 | |
| 0x0000 0000 | Internal ROM | EBI NCS0 | Internal SRAM |

6.3 Peripheral DMA Controller (PDC)

- Acting as one AHB Bus Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer support, prevents strong real-time constraints on buffer management.





The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Table 6-6. Peripheral DMA Controller

| Instance name | Channel T/R |
|---------------|-------------|
| DBGU | Transmit |
| USART3 | Transmit |
| USART2 | Transmit |
| USART1 | Transmit |
| USART0 | Transmit |
| AC97C | Transmit |
| TDES | Transmit |
| SHA | Transmit |
| SPI1 | Transmit |
| SPI0 | Transmit |
| SSC1 | Transmit |
| SSC0 | Transmit |
| TSADCC | Receive |
| DBGU | Receive |
| USART3 | Receive |
| USART2 | Receive |
| USART1 | Receive |
| USART0 | Receive |
| AC97C | Receive |
| TDES | Receive |
| SPI1 | Receive |
| SPI0 | Receive |
| SSC1 | Receive |
| SSC0 | Receive |

6.4 USB

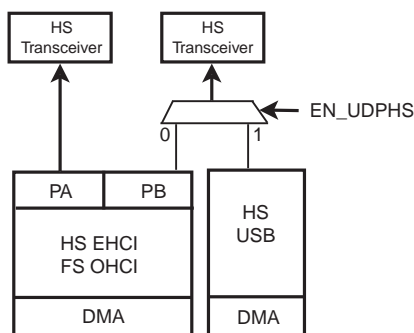
The SAM9G46 features USB communication ports as follows:

- 2 Ports USB Host full speed OHCI and High speed EHCI
- 1 Device High speed

USB Host Port A is directly connected to the first UTMI transceiver.

The Host Port B is multiplexed with the USB device High speed and connected to the second UTMI port. The selection between Host Port B and USB device high speed is controlled by a bit UDPHS enable bit located in the UDPHS_CTRL control register.

Figure 6-2. USB Selection



6.5 DMA Controller

- Two Masters
- Embeds 8 channels
- 64 bytes/FIFO for Channel Buffering
- Linked List support with Status Write Back operation at End of Transfer
- Word, HalfWord, Byte transfer support.
- memory to memory transfer
- Peripheral to memory
- Memory to peripheral

The DMA controller can handle the transfer between peripherals and memory and so receives the triggers from the peripherals below. The hardware interface numbers are also given below in [Table](#)

Table 6-7. DMA Channel Definition

| Instance Name | T/R | DMA Channel HW interface Number |
|---------------|-------|---------------------------------|
| MCI0 | TX/RX | 0 |
| SPI0 | TX | 1 |
| SPI0 | RX | 2 |
| SPI1 | TX | 3 |
| SPI1 | RX | 4 |
| SSC0 | TX | 5 |
| SSC0 | RX | 6 |
| SSC1 | TX | 7 |
| SSC1 | RX | 8 |
| AC97C | TX | 9 |
| AC97C | RX | 10 |
| AES | TX | 11 |
| AES | RX | 12 |
| MCI1 | TX/RX | 13 |





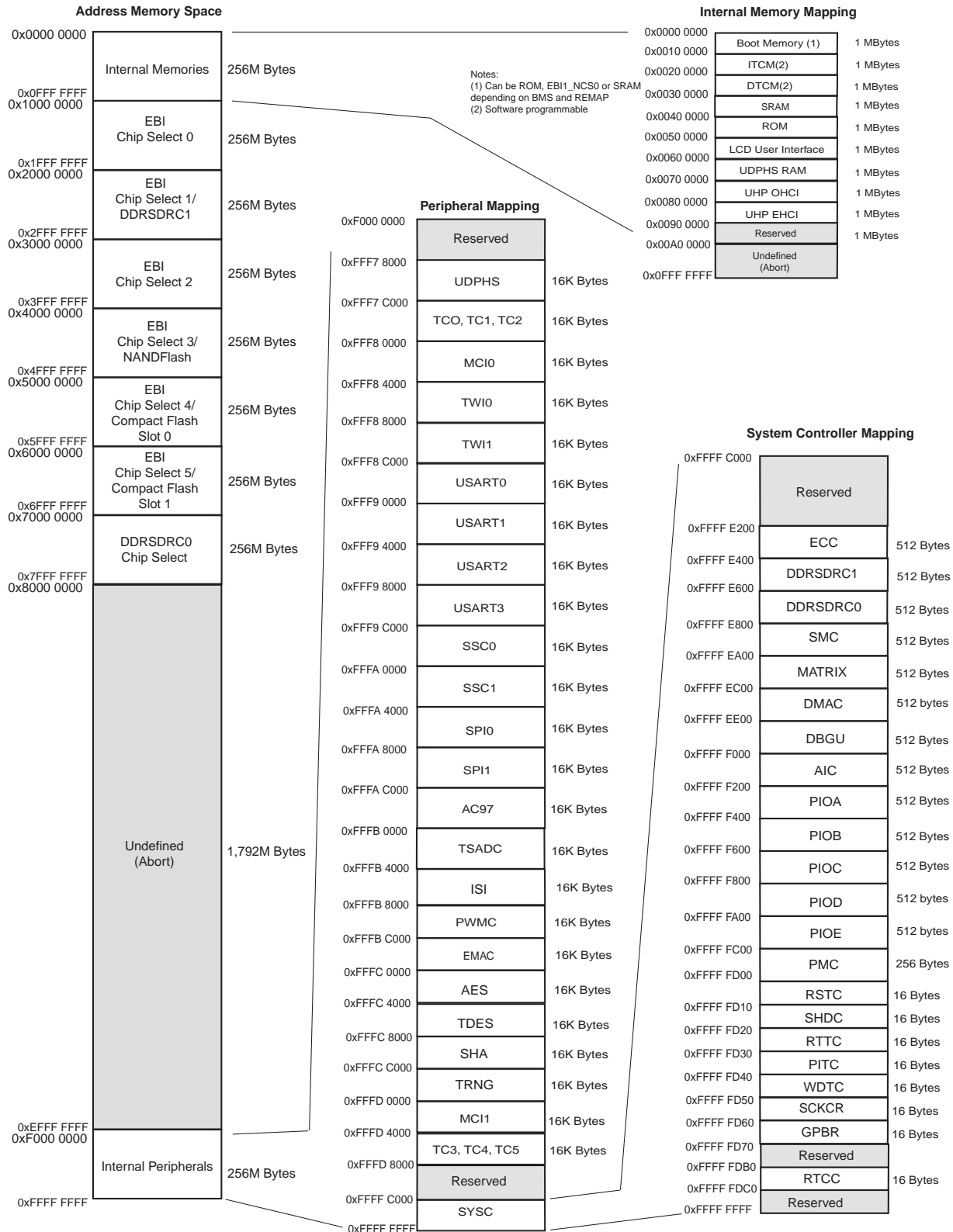
6.6 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
 - Two real-time Watchpoint Units
 - Two Independent Registers: Debug Control Register and Debug Status Register
 - Test Access Port Accessible through JTAG Protocol
 - Debug Communications Channel
- Debug Unit
 - Two-pin UART
 - Debug Communication Channel Interrupt Handling
 - Chip ID Register
- IEEE[®]1149.1 JTAG Boundary-scan on All Digital Pins.



7. Memories

Figure 7-1. SAM9G46 Memory Mapping





7.1 Memory Mapping

A first level of address decoding is performed by the AHB Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 Mbytes. The banks 1 to 6 are directed to the EBI that associates these banks to the external chip selects NCS0 to NCS5.

The bank 7 is directed to the DDRSDRC0 that associates this bank to DDR_NCS chip select and so dedicated to the 4-port DDR2/ LPDDR controller.

The bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. The bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

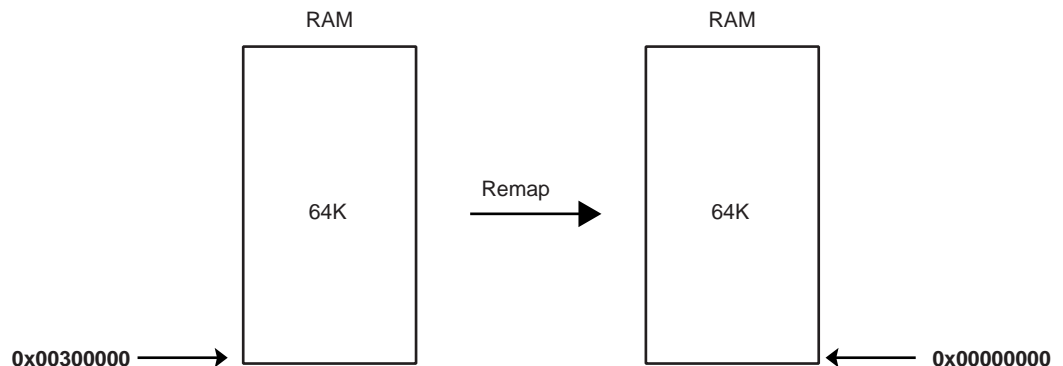
Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

7.2 Embedded Memories

7.2.1 Internal SRAM

The SAM9G46 product embeds a total of 64 Kbytes high-speed SRAM split in 4 blocks of 16 KBytes connected to one slave of the matrix. After reset and until the Remap Command is performed, the four SRAM blocks are contiguous and only accessible at address 0x00300000. After Remap, the SRAM also becomes available at address 0x0.

Figure 7-2. Internal SRAM Reset



The SAM9G46 device embeds two memory features. The processor Tightly Coupled Memory Interface (TCM) that allows the processor to access the memory up to processor speed (PCK) and the interface on the AHB side allowing masters to access the memory at AHB speed (MCK).

A wait state is necessary to access the TCM at 400 MHz. Setting the bit NWS_TCM in the bus Matrix TCM Configuration Register of the matrix inserts a wait state on the ITCM and DTCM accesses.

7.2.2 TCM Interface

On the processor side, this Internal SRAM can be allocated to two areas.

- Internal SRAM A is the ARM926EJ-S Instruction TCM. The user can map this SRAM block anywhere in the ARM926 instruction memory space using CP15 instructions and the TCR configuration register located in the Chip Configuration User Interface. This SRAM block is also accessible by the ARM926 Masters and by the AHB Masters through the AHB bus
- Internal SRAM B is the ARM926EJ-S Data TCM. The user can map this SRAM block anywhere in the ARM926 data memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus.
- Internal SRAM C is only accessible by all the AHB Masters. After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters. After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 64 Kbyte SRAM size available, the amount of memory assigned to each block is software programmable according to [Table 7-1](#).

Table 7-1. ITCM and DTCM Memory Configuration

| SRAM A ITCM size (KBytes) seen at 0x100000 through AHB | SRAM B DTCM size (KBytes) seen at 0x200000 through AHB | SRAM C (KBytes) seen at 0x300000 through AHB |
|---|---|---|
| 0 | 0 | 64 |
| 0 | 64 | 0 |
| 32 | 32 | 0 |

7.2.3 Internal ROM

The SAM9G46 embeds an Internal ROM, which contains the bootrom and SAM-BA program.

At any time, the ROM is mapped at address 0x0040 0000. It is also accessible at address 0x0 (BMS =1) after the reset and before the Remap Command.

7.2.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities the memory layout can be changed with two parameters.

REMAP allows the user to layout the internal SRAM bank to 0x0 to ease the development. This is done by software once the system has boot.

BMS allows the user to lay out to 0x0, when convenient, the ROM or an external memory. This is done by a hardware way at reset.

Note: All the memory blocks can always be seen at their specified base addresses that are not concerned by these parameters.

The SAM9G46 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.





7.2.4.1 *BMS = 1, boot on embedded ROM*

The system boots on Boot Program.

- Boot on on-chip RC
- Enable the 32768 Hz oscillator
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
 - SPI DataFlash/SerialFlash connected on NPCS0 of the SPI0
 - SDCard
 - NandFlash
 - EEPROM connected on TWI0
- SAM-BA Boot in case no valid program is detected in external NVM, supporting
 - Serial communication on a DBGU
 - USB Device HS Port

7.2.4.2 *BMS = 0, boot on external memory*

- Boot on on-chip RC
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

For optimization purpose, nothing else is done. To speed up the boot sequence user programmed software should perform a complete configuration:

- Enable the 32768 Hz oscillator if best accuracy needed
- Program the PMC (main oscillator enable or bypass mode)
- Program and Start the PLL
- Reprogram the SMC setup, cycle, hold, mode timings registers for EBI CS0 to adapt them to the new clock
- Switch the main clock to the new value

7.3 External Memories

The SAM99G46 features a Multi-port DDR2 Interface and an External Bus Interface allowing to connect to a wide range of external memories and to any parallel peripheral.

7.3.1 DDRSDRC0 Multi-port DDRSDR Controller

Four AHB Interfaces, Management of All Accesses Maximizes Memory Bandwidth and Minimizes Transaction Latency.

- Supports AHB Transfers:
 - Word, Half Word, Byte Access.
- Supports DDR2, LPDDR
- Numerous Configurations Supported
 - 2K, 4K, 8K, 16K Row Address Memory Parts
 - DDR2 with Four Internal Banks
 - DDR2/LPDDR with 16-bit Data Path
 - One Chip Select for DDR2/LPDDR Device (256 Mbytes Address Space)
- Programming Facilities
 - Multibank Ping-pong Access (Up to 4 Banks Opened at Same Time = Reduces Average Latency of Transactions)
 - Timing Parameters Specified by Software
 - Automatic Refresh Operation, Refresh Rate is Programmable
 - Automatic Update of DS, TCR and PASR Parameters
- Energy-saving Capabilities
 - Self-refresh, Power-down and Deep Power Modes Supported
- Power-up Initialization by Software
- CAS Latency of 2, 3 Supported
- Reset function supported (DDR2)
- Auto Precharge Command Not Used
- On Die Termination not supported
- OCD mode not supported

7.3.2 External Bus Interface

- Integrates Three External Memory Controllers:
 - Static Memory Controller
 - DDR2/SDRAM Controller
 - SLC Nand Flash ECC Controller
- Additional logic for NAND Flash and CompactFlash™
- Optional Full 32-bit External Data Bus
- Up to 26-bit Address Bus (up to 64MBytes linear per chip select)
- Up to 6 chip selects, Configurable Assignment:
 - Static Memory Controller on NCS0
 - DDR2/SDRAM Controller (SDCS) or Static Memory Controller on NCS1
 - Static Memory Controller on NCS2





- Static Memory Controller on NCS3, Optional NAND Flash support
- Static Memory Controller on NCS4 - NCS5, Optional CompactFlash^M support

7.3.2.1 *Static Memory Controller*

- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
 - Byte Write or Byte Select Lines
 - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
 - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
 - Programmable Wait State Generation
 - External Wait Request
 - Programmable Data Float Time
- Slow Clock mode supported

7.3.2.2 *DDR2/SDR Controller*

- Supports DDR2/LPDDR2, SDR-SDRAM and LPDDR
- Numerous Configurations Supported
 - 2K, 4K, 8K, 16K Row Address Memory Parts
 - SDRAM with Four Internal Banks
 - SDR-SDRAM with 16- or 32- bit Data Path
 - DDR2/LPDDR with 16- bit Data Path
 - One Chip Select for SDRAM Device (256 Mbyte Address Space)
- Programming Facilities
 - Multibank Ping-pong Access (Up to 4 Banks Opened at Same Time = Reduces Average Latency of Transactions)
 - Timing Parameters Specified by Software
 - Automatic Refresh Operation, Refresh Rate is Programmable
 - Automatic Update of DS, TCR and PASR Parameters (LPDDR)
- Energy-saving Capabilities
 - Self-refresh, Power-down and Deep Power Modes Supported
- SDRAM Power-up Initialization by Software
- CAS Latency of 2, 3 Supported
- Auto Precharge Command Not Used
- SDR-SDRAM with 16-bit Datapath and Eight Columns Not Supported
 - Clock Frequency Change in Precharge Power-down Mode Not Supported

7.3.2.3 *NAND Flash Error Corrected Code Controller*

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing

- ECC value available in a register
- Automatic Hamming Code Calculation while reading
 - Error Report, including error flag, correctable error flag and word address being detected erroneous
 - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-bytes pages.





8. System Controller

The System Controller is a set of peripherals that allows handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds the registers that configure the Matrix and a set of registers for the chip configuration. The chip configuration registers configure the EBI chip select assignment and voltage range for external memories.

8.1 System Controller Mapping

The System Controller's peripherals are all mapped within the highest 16 KBytes of address space, between addresses 0xFFFF E800 and 0xFFFF FFFF.

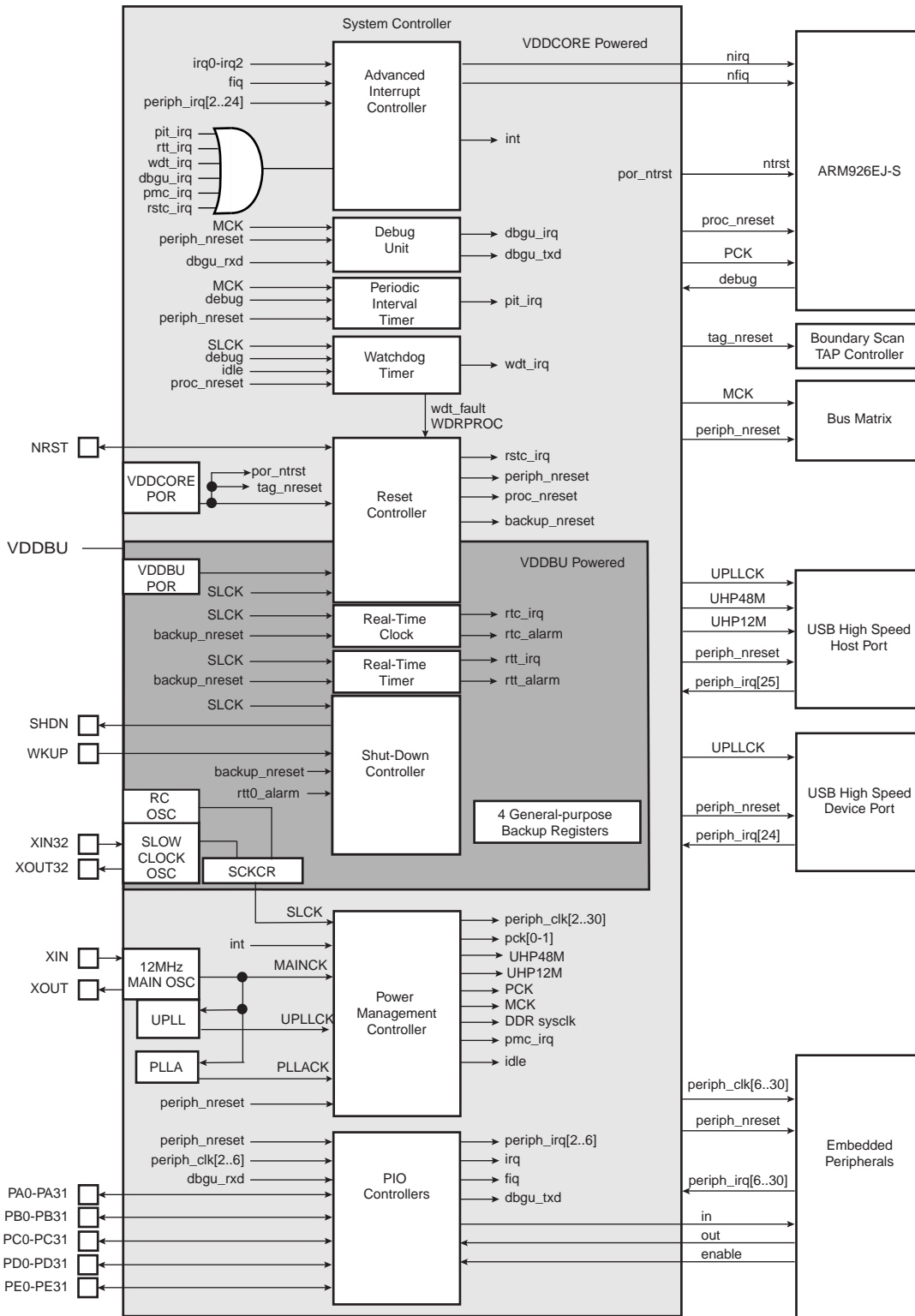
However, all the registers of the System Controller are mapped on the top of the address space. All the registers of the System Controller can be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instruction have an indexing mode of ± 4 KB.

[Figure 8-1 on page 31](#) shows the System Controller block diagram.

[Figure 7-1 on page 23](#) shows the mapping of the User Interfaces of the System Controller peripherals.

8.2 System Controller Block Diagram

Figure 8-1. SAM9G46 System Controller Block Diagram





8.3 Reset Controller

The Reset Controller is based on two Power-on-Reset cells, one on VDDBU and one on VDDCORE.

The Reset Controller is capable to return to the software the source of the last reset, either a general reset (VDDBU rising), a wake-up reset (VDDCORE rising), a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

The configuration of the Reset Controller is saved as supplied on VDDBU.

8.4 Shut Down Controller

The Shut Down Controller is supplied on VDDBU and allows a software-controllable shut down of the system through the pin SHDN. An input change of the WKUP pin or an alarm releases the SHDN pin, and thus wakes up the system power supply.

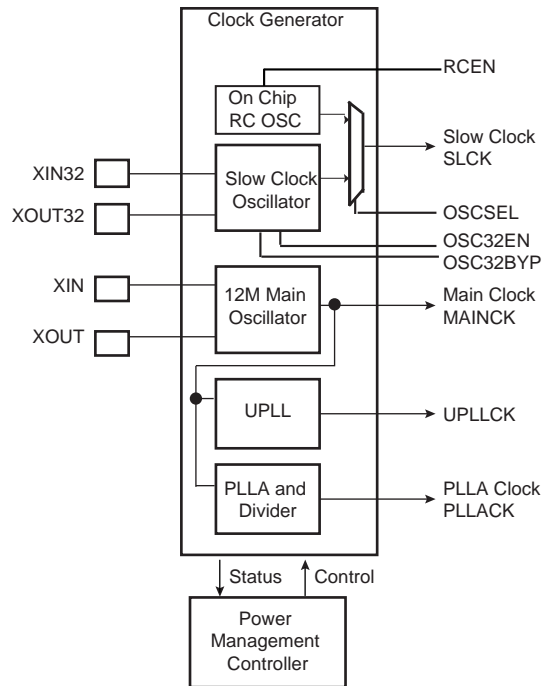
8.5 Clock Generator

The Clock Generator is made up of:

- One Low Power 32768 Hz Slow Clock Oscillator with bypass mode
- One Low-Power RC oscillator
- One 12 MHz Main Oscillator, which can be bypassed
- One 400 to 800 MHz programmable PLLA, capable to provide the clock MCK to the processor and to the peripherals. This PLL has an input divider to offer a wider range of output frequencies from the 12 MHz input, the only limitation being the lowest input frequency shall be higher or equal to 2 MHz.

The USB Device and Host HS Clocks are provided by a the dedicated UTMI PLL (UPLL) embedded in the UTMI macro.

Figure 8-2. Clock Generator Block Diagram



8.6 Slow Clock Selection

The SAM9G46 slow clock can be generated either by an external 32768Hz crystal or the on-chip RC oscillator. The 32768 Hz crystal oscillator can be bypassed, by setting the bit OSC32BYP, to accept an external slow clock on XIN32.

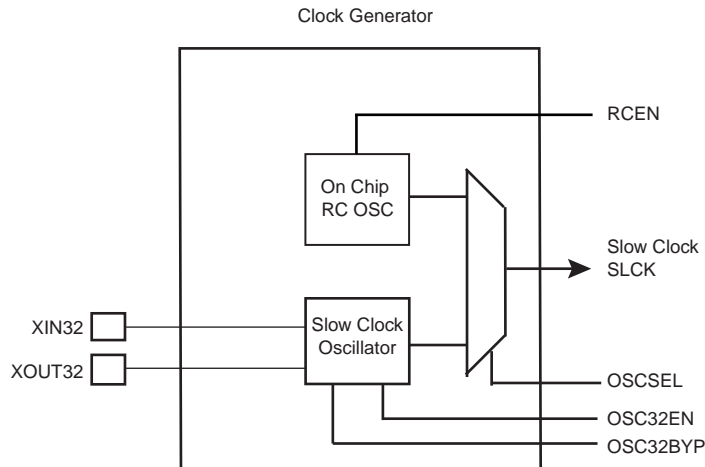
The internal RC oscillator and the 32768 Hz oscillator can be enabled by setting to 1 respectively RCEN bit and OSC32EN bit in the system controller user interface. OSCSEL command selects the slow clock source.

RCEN, OSC32EN, OSCSEL and OSC32BYP bits are located in the slow clock control register (SCKCR) located at address 0xFFFFD50 in the backup part of the system controller and so are preserved while VDDBU is present.





Figure 8-3. Slow Clock



After a VDDBU power on reset, the default configuration is RCEN = 1, OSC32EN = 0 and OSCSEL = 0 allowing the system to start on the internal RC oscillator.

The programmer controls by software the slow clock switching and so must take precautions during the switching phase.

8.6.1 Switch from Internal RC Oscillator to the 32768 Hz Crystal

To switch from internal RC oscillator to the 32768 Hz crystal, the programmer must execute the following sequence:

- Switch the master clock to a source different from slow clock (PLLA or PLLB or Main Oscillator) through the Power Management Controller.
- Enable the 32768 Hz oscillator by setting the bit OSCEN to 1.
- Wait 32768 Hz startup time for clock stabilization (software loop).
- Switch from internal RC to 32768 Hz by setting the bit OSCSEL to 1.
- Wait 5 slow clock cycles for internal resynchronization.
- Disable the RC oscillator by setting the bit RCEN to 0.

8.6.2 Bypass the 32768 Hz Oscillator

The following step must be added to bypass the 32768 Hz Oscillator.

- An external clock must be connected on XIN32.
- Enable the bypass path OSC32BYP bit set to 1.
- Disable the 32768 Hz oscillator by setting the bit OSC32EN to 0.

8.6.3 Switch from 32768 Hz Crystal to the Internal RC Oscillator

The same procedure must be followed to switch from 32768 Hz crystal to the internal RC oscillator.

- Switch the master clock to a source different from slow clock (PLLA or PLLB or Main Oscillator).
- Enable the internal RC oscillator by setting the bit RCEN to 1.
- Wait internal RC Startup Time for clock stabilization (software loop).

- Switch from 32768 Hz oscillator to internal RC oscillator by setting the bit OSCSEL to 0.
- Wait 5 slow clock cycles for internal resynchronization.
- Disable the 32768Hz oscillator by setting the bit OSC32EN to 0.

8.7 Power Management Controller

The Power Management Controller provides all the clock signals to the system.

PMC input clocks:

- UPLLCK: From UTMI PLL
- PLLACK From PLLA
- SLCK: slow clock from OSC32K or internal RC OSC
- MAINCK: from 12 MHz external oscillator

PMC output clocks

- Processor Clock PCK
- Master Clock MCK, in particular to the Matrix and the memory interfaces. The divider can be 1,2,3 or 4
- DDR system clock equal to 2xMCK

Note: DDR system clock is not available when Master Clock (MCK) equals Processor Clock (PCK).

- USB Host EHCI High speed clock (UPLLCK)
- USB OHCI clocks (UHP48M and UHP12M)
- Independent peripheral clocks, typically at the frequency of MCK
- Two programmable clock outputs: PCK0 and PCK1

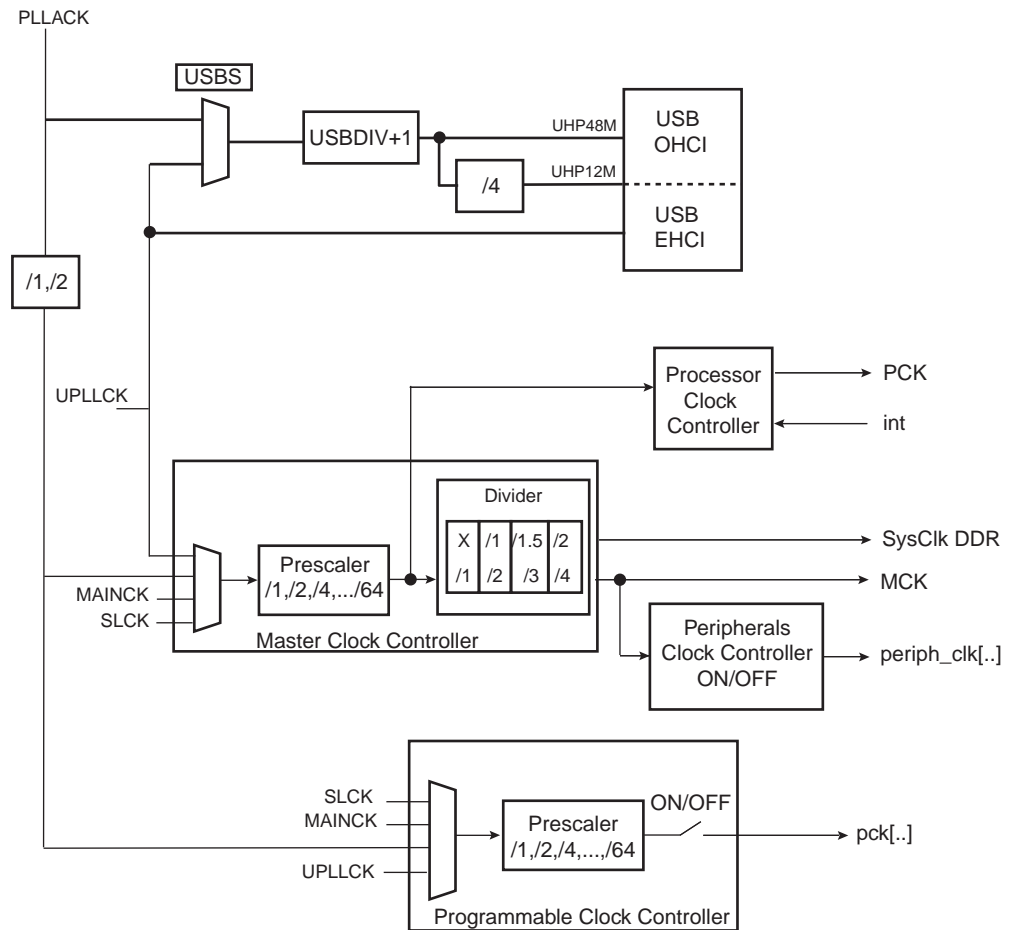
This allows the software control of five flexible operating modes:

- Normal Mode, processor and peripherals running at a programmable frequency
- Idle Mode, processor stopped waiting for an interrupt
- Slow Clock Mode, processor and peripherals running at low frequency
- Standby Mode, mix of Idle and Backup Mode, peripheral running at low frequency, processor stopped waiting for an interrupt
- Backup Mode, Main Power Supplies off, VDDBU powered by a battery





Figure 8-4. SAM9G46 Power Management Controller Block Diagram



8.7.1 Main Application Modes

The Power Management Controller provides 3 main application modes.

8.7.1.1 Normal Mode

- PLLA and UPLL are running respectively at 400 MHz and 480 MHz
- USB Device High Speed and Host EHCI High Speed operations are allowed
- Full Speed OHCI input clock is UPLLCK, USBDIV is 9 (division by 10)
- System Input clock is PLLACK, PCK is 400 MHz
- MDIV is '11', MCK is 133 MHz
- DDR2 can be used at up to 133 MHz

8.7.1.2 USB HS and LP-DDR Mode

- Only UPLL is running at 480 MHz, PLLA power consumption is saved
- USB Device High Speed and Host EHCI High Speed operations are allowed
- Full Speed OHCI input clock is UPLLCK, USBDIV is 9 (division by 10)
- System Input clock is UPLLCK, Prescaler is 2, PCK is 240 MHz
- MDIV is '01', MCK is 120 MHz
- Only LP-DDR can be used at up to 120 MHz

8.7.1.3 No UDP HS, UHP FS and DDR2 Mode

- Only PLLA is running at 384 MHz, UPLL power consumption is saved
- USB Device High Speed and Host EHCI High Speed operations are NOT allowed
- Full Speed OHCI input clock is PLLACK, USBDIV is 7 (division by 8)
- System Input clock is PLLACK, PCK is 384 MHz
- MDIV is '11', MCK is 128 MHz
- DDR2 can be used at up to 128 MHz

8.8 Periodic Interval Timer

- Includes a 20-bit Periodic Counter, with less than 1 μ s accuracy
- Includes a 12-bit Interval Overlay Counter
- Real Time OS or Linux/WinCE compliant tick generator

8.9 Watchdog Timer

- 16-bit key-protected only-once-Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

8.10 Real-Time Timer

- Real-Time Timer, allowing backup of time with different accuracies
 - 32-bit Free-running back-up Counter
 - Integrates a 16-bit programmable prescaler running on slow clock
 - Alarm Register capable to generate a wake-up of the system through the Shut Down Controller

8.11 Real Time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

8.12 General-Purpose Backup Registers

- Four 32-bit backup general-purpose registers

8.13 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of the ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
 - Source 0 is reserved for the Fast Interrupt Input (FIQ)
 - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, etc.)
 - Programmable Edge-triggered or Level-sensitive Internal Sources
 - Programmable Positive/Negative Edge-triggered or High/Low Level-sensitive





- One External Sources plus the Fast Interrupt signal
- 8-level Priority Controller
 - Drives the Normal Interrupt of the processor
 - Handles priority of the interrupt sources 1 to 31
 - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
 - Optimizes Interrupt Service Routine Branch and Execution
 - One 32-bit Vector Register per interrupt source
 - Interrupt Vector Register reads the corresponding current Interrupt Vector
- Protect Mode
 - Easy debugging by preventing automatic operations when protect modes are enabled
- Fast Forcing
 - Permits redirecting any normal interrupt source on the Fast Interrupt of the processor

8.14 Debug Unit

- Composed of two functions
 - Two-pin UART
 - Debug Communication Channel (DCC) support
- Two-pin UART
 - Implemented features are 100% compatible with the standard Atmel USART
 - Independent receiver and transmitter with a common programmable Baud Rate Generator
 - Even, Odd, Mark or Space Parity Generation
 - Parity, Framing and Overrun Error Detection
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
 - Support for two PDC channels with connection to receiver and transmitter
- Debug Communication Channel Support
 - Offers visibility of and interrupt trigger from COMMRX and COMMTX signals from the ARM Processor's ICE Interface

8.15 Chip Identification

The SAM9G46 Chip ID is defined in the Debug Unit Chip ID Register and Debug Unit Chip ID Extension Register.

- Chip ID: 0x819B05A2
- Ext ID: 0x00000003
- JTAG ID: 05B2_703F
- ARM926 TAP ID: 0x0792603F

8.16 PIO Controllers

- 5 PIO Controllers, PIOA, PIOB, PIOC, PIOD and PIOE, controlling a maximum of 160 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines
 - PIOA has 32 I/O Lines
 - PIOB has 32 I/O Lines
 - PIOC has 32 I/O Lines
 - PIOD has 32 I/O Lines
 - PIOE has 32 I/O Lines
- Fully programmable through Set/Clear Registers
- Multiplexing of two peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
 - Input change interrupt
 - Glitch filter
 - Multi-drive option enables driving in open drain
 - Programmable pull up on each I/O line
 - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write





9. Peripherals

9.1 Peripheral Mapping

As shown in [Figure 7-1](#), the Peripherals are mapped in the upper 256 Mbytes of the address space between the addresses 0xFFFF7 8000 and 0xFFFFC FFFF.

Each User Peripheral is allocated 16K bytes of address space.

9.2 Peripheral Identifiers

[Table 9-1](#) defines the Peripheral Identifiers of the SAM9G46. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 9-1. SAM9G46 Peripheral Identifiers

| Peripheral ID | Peripheral Mnemonic | Peripheral Name | External Interrupt |
|---------------|---------------------|--|--------------------|
| 0 | AIC | Advanced Interrupt Controller | FIQ |
| 1 | SYS | System Controller Interrupt | |
| 2 | PIOA | Parallel I/O Controller A, | |
| 3 | PIOB | Parallel I/O Controller B | |
| 4 | PIOC | Parallel I/O Controller C | |
| 5 | PIOD, PIOE | Parallel I/O Controller D, Parallel I/O Controller E | |
| 6 | TRNG | True Random Number Generator | |
| 7 | USART0 | USART 0 | |
| 8 | USART1 | USART 1 | |
| 9 | USART2 | USART 2 | |
| 10 | USART3 | USART 3 | |
| 11 | MCI0 | High Speed Multimedia Card Interface 0 | |
| 12 | TWI0 | Two-Wire Interface 0 | |
| 13 | TWI1 | Two-Wire Interface 1 | |
| 14 | SPI0 | Serial Peripheral Interface | |
| 15 | SPI1 | Serial Peripheral Interface | |
| 16 | SSC0 | Synchronous Serial Controller 0 | |
| 17 | SSC1 | Synchronous Serial Controller 1 | |
| 18 | TC0 .. TC5 | Timer Counter 0 .. Timer Counter 5 | |
| 19 | PWM | Pulse Width Modulation Controller | |
| 20 | TSADCC | Touch Screen ADC Controller | |
| 21 | DMAC | DMA Controller | |
| 22 | UHPHS | USB Host High Speed | |
| 23 | LCDC | LCD Controller | |
| 24 | AC97C | AC97 Controller | |
| 25 | EMAC | Ethernet MAC | |
| 26 | ISI | Image Sensor Interface | |
| 27 | UDPHS | USB Device High Speed | |
| 28 | AES, TDES, SHA | Advanced Encryption Standard, Triple Data Encryption Standard, Secure Hash Algorithm | |

Table 9-1. SAM9G46 Peripheral Identifiers (Continued)

| Peripheral ID | Peripheral Mnemonic | Peripheral Name | External Interrupt |
|---------------|---------------------|--|--------------------|
| 29 | MCI1 | High Speed Multimedia Card Interface 1 | |
| 30 | Reserved | | |
| 31 | AIC | Advanced Interrupt Controller | IRQ |

9.3 Peripheral Interrupts and Clock Control

9.3.1 System Interrupt

The System Interrupt in Source 1 is the wired-OR of the interrupt signals coming from:

- the DDR2/LPDDR Controller
- the Debug Unit
- the Periodic Interval Timer
- the Real-Time Timer
- the Real-Time Clock
- the Watchdog Timer
- the Reset Controller
- the Power Management Controller

The clock of these peripherals cannot be deactivated and Peripheral ID 1 can only be used within the Advanced Interrupt Controller.

9.3.2 External Interrupts

All external interrupt signals, i.e., the Fast Interrupt signal FIQ or the Interrupt signal IRQ, use a dedicated Peripheral ID. However, there is no clock control associated with these peripheral IDs.

9.4 Peripheral Signals Multiplexing on I/O Lines

The SAM9G46 features 5 PIO controllers, PIOA, PIOB, PIOC, PIOD and PIOE, which multiplexes the I/O lines of the peripheral set.

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers. The two columns “Function” and “Comments” have been inserted in this table for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral function which are output only, might be duplicated within the both tables.

The column “Reset State” indicates whether the PIO Line resets in I/O mode or in peripheral mode. If I/O is mentioned, the PIO Line resets in input with the pull-up enabled, so that the device is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is mentioned in the “Reset State” column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released. Note that the pull-up resistor is also enabled in this case.

To amend EMC, programmable delay has been inserted on PIO lines able to run at high speed.





9.4.1 PIO Controller A Multiplexing

Table 9-2. Multiplexing on PIO Controller A (PIOA)

| I/O Line | Peripheral A | Peripheral B | Reset State | Power Supply | Function | Comments |
|----------|--------------|--------------|-------------|--------------|----------|----------|
| PA0 | MCI0_CK | TCLK3 | I/O | VDDIOP0 | | |
| PA1 | MCI0_CDA | TIOA3 | I/O | VDDIOP0 | | |
| PA2 | MCI0_DA0 | TIOB3 | I/O | VDDIOP0 | | |
| PA3 | MCI0_DA1 | TCKL4 | I/O | VDDIOP0 | | |
| PA4 | MCI0_DA2 | TIOA4 | I/O | VDDIOP0 | | |
| PA5 | MCI0_DA3 | TIOB4 | I/O | VDDIOP0 | | |
| PA6 | MCI0_DA4 | ETX2 | I/O | VDDIOP0 | | |
| PA7 | MCI0_DA5 | ETX3 | I/O | VDDIOP0 | | |
| PA8 | MCI0_DA6 | ERX2 | I/O | VDDIOP0 | | |
| PA9 | MCI0_DA7 | ERX3 | I/O | VDDIOP0 | | |
| PA10 | ETX0 | | I/O | VDDIOP0 | | |
| PA11 | ETX1 | | I/O | VDDIOP0 | | |
| PA12 | ERX0 | | I/O | VDDIOP0 | | |
| PA13 | ERX1 | | I/O | VDDIOP0 | | |
| PA14 | ETXEN | | I/O | VDDIOP0 | | |
| PA15 | ERXDV | | I/O | VDDIOP0 | | |
| PA16 | ERXER | | I/O | VDDIOP0 | | |
| PA17 | ETXCK | | I/O | VDDIOP0 | | |
| PA18 | EMDC | | I/O | VDDIOP0 | | |
| PA19 | EMDIO | | I/O | VDDIOP0 | | |
| PA20 | TWD0 | | I/O | VDDIOP0 | | |
| PA21 | TWCK0 | | I/O | VDDIOP0 | | |
| PA22 | MCI1_CDA | SCK3 | I/O | VDDIOP0 | | |
| PA23 | MCI1_DA0 | RTS3 | I/O | VDDIOP0 | | |
| PA24 | MCI1_DA1 | CTS3 | I/O | VDDIOP0 | | |
| PA25 | MCI1_DA2 | PWM3 | I/O | VDDIOP0 | | |
| PA26 | MCI1_DA3 | TIOB2 | I/O | VDDIOP0 | | |
| PA27 | MCI1_DA4 | ETXER | I/O | VDDIOP0 | | |
| PA28 | MCI1_DA5 | ERXCK | I/O | VDDIOP0 | | |
| PA29 | MCI1_DA6 | ECRS | I/O | VDDIOP0 | | |
| PA30 | MCI1_DA7 | ECOL | I/O | VDDIOP0 | | |
| PA31 | MCI1_CK | PCK0 | I/O | VDDIOP0 | | |

9.4.2 PIO Controller B Multiplexing

Table 9-3. Multiplexing on PIO Controller B (PIOB)

| I/O Line | Peripheral A | Peripheral B | Reset State | Power Supply | Function | Comments |
|----------|--------------|--------------|-------------|--------------|----------|----------|
| PB0 | SPI0_MISO | | I/O | VDDIOP0 | | |
| PB1 | SPI0_MOSI | | I/O | VDDIOP0 | | |
| PB2 | SPI0_SPCK | | I/O | VDDIOP0 | | |
| PB3 | SPI0_NPCS0 | | I/O | VDDIOP0 | | |
| PB4 | TXD1 | | I/O | VDDIOP0 | | |
| PB5 | RXD1 | | I/O | VDDIOP0 | | |
| PB6 | TXD2 | | I/O | VDDIOP0 | | |
| PB7 | RXD2 | | I/O | VDDIOP0 | | |
| PB8 | TXD3 | ISI_D8 | I/O | VDDIOP2 | | |
| PB9 | RXD3 | ISI_D9 | I/O | VDDIOP2 | | |
| PB10 | TWD1 | ISI_D10 | I/O | VDDIOP2 | | |
| PB11 | TWCK1 | ISI_D11 | I/O | VDDIOP2 | | |
| PB12 | DRXD | | I/O | VDDIOP0 | | |
| PB13 | DTXD | | I/O | VDDIOP0 | | |
| PB14 | SPI1_MISO | | I/O | VDDIOP0 | | |
| PB15 | SPI1_MOSI | CTS0 | I/O | VDDIOP0 | | |
| PB16 | SPI1_SPCK | SCK0 | I/O | VDDIOP0 | | |
| PB17 | SPI1_NPCS0 | RTS0 | I/O | VDDIOP0 | | |
| PB18 | RXD0 | SPI0_NPCS1 | I/O | VDDIOP0 | | |
| PB19 | TXD0 | SPI0_NPCS2 | I/O | VDDIOP0 | | |
| PB20 | ISI_D0 | | I/O | VDDIOP2 | | |
| PB21 | ISI_D1 | | I/O | VDDIOP2 | | |
| PB22 | ISI_D2 | | I/O | VDDIOP2 | | |
| PB23 | ISI_D3 | | I/O | VDDIOP2 | | |
| PB24 | ISI_D4 | | I/O | VDDIOP2 | | |
| PB25 | ISI_D5 | | I/O | VDDIOP2 | | |
| PB26 | ISI_D6 | | I/O | VDDIOP2 | | |
| PB27 | ISI_D7 | | I/O | VDDIOP2 | | |
| PB28 | ISI_PCK | | I/O | VDDIOP2 | | |
| PB29 | ISI_VSYNC | | I/O | VDDIOP2 | | |
| PB30 | ISI_HSYNC | | I/O | VDDIOP2 | | |
| PB31 | ISI_MCK | PCK1 | I/O | VDDIOP2 | | |





9.4.3 PIO Controller C Multiplexing

Table 9-4. Multiplexing on PIO Controller C (PIOC)

| I/O Line | Peripheral A | Peripheral B | Reset State | Power Supply | Function | Comments |
|----------|--------------|--------------|-------------|--------------|----------|----------|
| PC0 | DQM2 | | DQM2 | VDDIOM1 | | |
| PC1 | DQM3 | | DQM3 | VDDIOM1 | | |
| PC2 | A19 | | A19 | VDDIOM1 | | |
| PC3 | A20 | | A20 | VDDIOM1 | | |
| PC4 | A21/NANDALE | | A21 | VDDIOM1 | | |
| PC5 | A22/NANDCLE | | A22 | VDDIOM1 | | |
| PC6 | A23 | | A23 | VDDIOM1 | | |
| PC7 | A24 | | A24 | VDDIOM1 | | |
| PC8 | CFCE1 | | I/O | VDDIOM1 | | |
| PC9 | CFCE2 | RTS2 | I/O | VDDIOM1 | | |
| PC10 | NCS4/CFCS0 | TCLK2 | I/O | VDDIOM1 | | |
| PC11 | NCS5/CFCS1 | CTS2 | I/O | VDDIOM1 | | |
| PC12 | A25/CFRNW | | A25 | VDDIOM1 | | |
| PC13 | NCS2 | | I/O | VDDIOM1 | | |
| PC14 | NCS3/NANDCS | | I/O | VDDIOM1 | | |
| PC15 | NWAIT | | I/O | VDDIOM1 | | |
| PC16 | D16 | | I/O | VDDIOM1 | | |
| PC17 | D17 | | I/O | VDDIOM1 | | |
| PC18 | D18 | | I/O | VDDIOM1 | | |
| PC19 | D19 | | I/O | VDDIOM1 | | |
| PC20 | D20 | | I/O | VDDIOM1 | | |
| PC21 | D21 | | I/O | VDDIOM1 | | |
| PC22 | D22 | | I/O | VDDIOM1 | | |
| PC23 | D23 | | I/O | VDDIOM1 | | |
| PC24 | D24 | | I/O | VDDIOM1 | | |
| PC25 | D25 | | I/O | VDDIOM1 | | |
| PC26 | D26 | | I/O | VDDIOM1 | | |
| PC27 | D27 | | I/O | VDDIOM1 | | |
| PC28 | D28 | | I/O | VDDIOM1 | | |
| PC29 | D29 | | I/O | VDDIOM1 | | |
| PC30 | D30 | | I/O | VDDIOM1 | | |
| PC31 | D31 | | I/O | VDDIOM1 | | |

9.4.4 PIO Controller D Multiplexing

Table 9-5. Multiplexing on PIO Controller D (PIOD)

| I/O Line | Peripheral A | Peripheral B | Reset State | Power Supply | Function | Comments |
|----------|--------------|--------------|-------------|--------------|----------|----------|
| PD0 | TK0 | PWM3 | I/O | VDDIOP0 | | |
| PD1 | TF0 | | I/O | VDDIOP0 | | |
| PD2 | TD0 | | I/O | VDDIOP0 | | |
| PD3 | RD0 | | I/O | VDDIOP0 | | |
| PD4 | RK0 | | I/O | VDDIOP0 | | |
| PD5 | RF0 | | I/O | VDDIOP0 | | |
| PD6 | AC97RX | | I/O | VDDIOP0 | | |
| PD7 | AC97TX | TIOA5 | I/O | VDDIOP0 | | |
| PD8 | AC97FS | TIOB5 | I/O | VDDIOP0 | | |
| PD9 | AC97CK | TCLK5 | I/O | VDDIOP0 | | |
| PD10 | TD1 | | I/O | VDDIOP0 | | |
| PD11 | RD1 | | I/O | VDDIOP0 | | |
| PD12 | TK1 | PCK0 | I/O | VDDIOP0 | | |
| PD13 | RK1 | | I/O | VDDIOP0 | | |
| PD14 | TF1 | | I/O | VDDIOP0 | | |
| PD15 | RF1 | | I/O | VDDIOP0 | | |
| PD16 | RTS1 | | I/O | VDDIOP0 | | |
| PD17 | CTS1 | | I/O | VDDIOP0 | | |
| PD18 | SPI1_NPCS2 | IRQ | I/O | VDDIOP0 | | |
| PD19 | SPI1_NPCS3 | FIQ | I/O | VDDIOP0 | | |
| PD20 | TIOA0 | | I/O | VDDANA | | TSAD0 |
| PD21 | TIOA1 | | I/O | VDDANA | | TSAD1 |
| PD22 | TIOA2 | | I/O | VDDANA | | TSAD2 |
| PD23 | TCLK0 | | I/O | VDDANA | | TSAD3 |
| PD24 | SPI0_NPCS1 | PWM0 | I/O | VDDANA | | GPAD4 |
| PD25 | SPI0_NPCS2 | PWM1 | I/O | VDDANA | | GPAD5 |
| PD26 | PCK0 | PWM2 | I/O | VDDANA | | GPAD6 |
| PD27 | PCK1 | SPI0_NPCS3 | I/O | VDDANA | | GPAD7 |
| PD28 | TSADTRG | SPI1_NPCS1 | I/O | VDDIOP0 | | |
| PD29 | TCLK1 | SCK1 | I/O | VDDIOP0 | | |
| PD30 | TIOB0 | SCK2 | I/O | VDDIOP0 | | |
| PD31 | TIOB1 | PWM1 | I/O | VDDIOP0 | | |





9.4.5 PIO Controller E Multiplexing

Table 9-6. Multiplexing on PIO Controller E (PIOE)

| I/O Line | Peripheral A | Peripheral B | Reset State | Power Supply | Function | Comments |
|----------|--------------|--------------|-------------|--------------|----------|----------|
| PE0 | LCDPWR | PCK0 | I/O | VDDIOP1 | | |
| PE1 | LCDDMOD | | I/O | VDDIOP1 | | |
| PE2 | LCDDCC | | I/O | VDDIOP1 | | |
| PE3 | LCDVSYNC | | I/O | VDDIOP1 | | |
| PE4 | LCDHSYNC | | I/O | VDDIOP1 | | |
| PE5 | LCDDOTCK | | I/O | VDDIOP1 | | |
| PE6 | LCDDEN | | I/O | VDDIOP1 | | |
| PE7 | LCDD0 | LCDD2 | I/O | VDDIOP1 | | |
| PE8 | LCDD1 | LCDD3 | I/O | VDDIOP1 | | |
| PE9 | LCDD2 | LCDD4 | I/O | VDDIOP1 | | |
| PE10 | LCDD3 | LCDD5 | I/O | VDDIOP1 | | |
| PE11 | LCDD4 | LCDD6 | I/O | VDDIOP1 | | |
| PE12 | LCDD5 | LCDD7 | I/O | VDDIOP1 | | |
| PE13 | LCDD6 | LCDD10 | I/O | VDDIOP1 | | |
| PE14 | LCDD7 | LCDD11 | I/O | VDDIOP1 | | |
| PE15 | LCDD8 | LCDD12 | I/O | VDDIOP1 | | |
| PE16 | LCDD9 | LCDD13 | I/O | VDDIOP1 | | |
| PE17 | LCDD10 | LCDD14 | I/O | VDDIOP1 | | |
| PE18 | LCDD11 | LCDD15 | I/O | VDDIOP1 | | |
| PE19 | LCDD12 | LCDD18 | I/O | VDDIOP1 | | |
| PE20 | LCDD13 | LCDD19 | I/O | VDDIOP1 | | |
| PE21 | LCDD14 | LCDD20 | I/O | VDDIOP1 | | |
| PE22 | LCDD15 | LCDD21 | I/O | VDDIOP1 | | |
| PE23 | LCDD16 | LCDD22 | I/O | VDDIOP1 | | |
| PE24 | LCDD17 | LCDD23 | I/O | VDDIOP1 | | |
| PE25 | LCDD18 | | I/O | VDDIOP1 | | |
| PE26 | LCDD19 | | I/O | VDDIOP1 | | |
| PE27 | LCDD20 | | I/O | VDDIOP1 | | |
| PE28 | LCDD21 | | I/O | VDDIOP1 | | |
| PE29 | LCDD22 | | I/O | VDDIOP1 | | |
| PE30 | LCDD23 | | I/O | VDDIOP1 | | |
| PE31 | PWM2 | PCK1 | I/O | VDDIOP1 | | |

10. Embedded Peripherals

10.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
 - Four chip selects with external decoder support allow communication with up to 15 peripherals
 - Serial memories, such as DataFlash and 3-wire EEPROMs
 - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
 - External co-processors
- Master or slave serial peripheral bus interface
 - 8- to 16-bit programmable data length per chip select
 - Programmable phase and polarity per chip select
 - Programmable transfer delays between consecutive transfers and between clock and data per chip select
 - Programmable delay between consecutive transfers
 - Selectable mode fault detection
- Very fast transfers supported
 - Transfers with baud rates up to MCK
 - The chip select line may be left active to speed up transfers on the same device

10.2 Two Wire Interface (TWI)

- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations
- Supports either master or slave modes
- Compatible with Standard Two-wire Serial Memories
- Master, Multi-master and Slave Mode Operation
- Bit Rate: Up to 400 Kbits
- General Call Supported in Slave mode

10.3 Universal Synchronous Asynchronous Receiver Transmitter (USART)

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
 - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
 - Parity generation and error detection
 - Framing error detection, overrun error detection
 - MSB- or LSB-first
 - Optional break generation and detection
 - By 8 or by-16 over-sampling receiver frequency
 - Hardware handshaking RTS-CTS





- Receiver time-out and transmitter timeguard
- Optional Multi-drop Mode with address generation and detection
- Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
 - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
 - Communication at up to 115.2 Kbps
- SPI Mode
 - Master or Slave
 - Serial Clock Programmable Phase and Polarity
 - SPI Serial Clock (SCK) Frequency up to Internal Clock Frequency MCK/4
- LIN Mode
 - Compliant with LIN 1.3 and LIN 2.0 specifications
 - Master or Slave
 - Processing of frames with up to 256 data bytes
 - Response Data length can be configurable or defined automatically by the Identifier
 - Self synchronization in Slave node configuration
 - Automatic processing and verification of the “Synch Break” and the “Synch Field”
 - The “Synch Break” is detected even if it is partially superimposed with a data byte
 - Automatic Identifier parity calculation/sending and verification
 - Parity sending and verification can be disabled
 - Automatic Checksum calculation/sending and verification
 - Checksum sending and verification can be disabled
 - Support both “Classic” and “Enhanced” checksum types
 - Full LIN error checking and reporting
 - Frame Slot Mode: the Master allocates slots to the scheduled frames automatically.
 - Generation of the Wakeup signal
- Test Modes
 - Remote Loopback, Local Loopback, Automatic Echo

10.4 Serial Synchronous Controller (SSC)

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I²S, TDM Buses, Magnetic Card Reader,...)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.5 AC97 Controller

- Compatible with AC97 Component Specification V2.2
- Capable to Interface with a Single Analog Front end
- Three independent RX Channels and three independent TX Channels
 - One RX and one TX channel dedicated to the AC97 Analog Front end control
 - One RX and one TX channel for data transfers, associated with a PDC
 - One RX and one TX channel for data transfers with no PDC
- Time Slot Assigner allowing to assign up to 12 time slots to a channel
- Channels support mono or stereo up to 20 bit sample length
 - Variable sampling rate AC97 Codec Interface (48KHz and below)

10.6 Timer Counter (TC)

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
 - Frequency Measurement
 - Event Counting
 - Interval Measurement
 - Pulse Generation
 - Delay Timing
 - Pulse Width Modulation
 - Up/down Capabilities
- Each channel is user-configurable and contains:
 - Three external clock inputs
 - Five internal clock inputs
 - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

10.7 Pulse Width Modulation Controller (PWM)

- Four channels, one 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
 - A Modulo n counter providing eleven clocks
 - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
 - Independent Enable Disable Commands
 - Independent Clock Selection
 - Independent Period and Duty Cycle, with Double Buffering
 - Programmable selection of the output waveform polarity
 - Programmable center or left aligned output waveform





10.8 High Speed Multimedia Card Interface (MCI)

- Compatibility with MultiMedia Card Specification Version 4.3
- Compatibility with SD Memory Card Specification Version 2.0
- Compatibility with SDIO Specification Version V2.0.
- Compatibility with Memory Stick PRO
- Compatibility with CE ATA

10.9 USB High Speed Host Port (UHPHS)

- Compliant with Enhanced HCI Rev 1.0 Specification
 - Compliant with USB V2.0 High-speed and Full-speed Specification
 - Supports Both High-speed 480Mbps and Full-speed 12 Mbps USB devices
- Compliant with Open HCI Rev 1.0 Specification
 - Compliant with USB V2.0 Full-speed and Low-speed Specification
 - Supports Both Low-speed 1.5 Mbps and Full-speed 12 Mbps USB devices
- Root Hub Integrated with 2 Downstream USB Ports
- Shared Embedded USB Transceivers

10.10 USB High Speed Device Port (UDPHS)

- USB V2.0 high-speed compliant, 480 Mbits per second
- Embedded USB V2.0 UTMI+ high-speed transceiver shared with UHP HS.
- Embedded 4-KByte dual-port RAM for endpoints
- Embedded 6 channels DMA controller
- Suspend/Resume logic
- Up to 2 or 3 banks for isochronous and bulk endpoints
- Seven endpoints:
 - Endpoint 0: 64 bytes, 1 bank mode
 - Endpoint 1 & 2: 1024 bytes, 2 banks mode, High Bandwidth, DMA
 - Endpoint 3 & 4: 1024 bytes, 3 banks mode, DMA
 - Endpoint 5 & 6: 1024 bytes, 3 banks mode, High Bandwidth, DMA

10.11 LCD Controller (LCDC)

- Single and Dual scan color and monochrome passive STN LCD panels supported
- Single scan active TFT LCD panels supported.
- 4-bit single scan, 8-bit single or dual scan, 16-bit dual scan STN interfaces supported
- Up to 24-bit single scan TFT interfaces supported
- Up to 16 gray levels for mono STN and up to 4096 colors for color STN displays
- 1, 2 bits per pixel (palletized), 4 bits per pixel (non-palletized) for mono STN
- 1, 2, 4, 8 bits per pixel (palletized), 16 bits per pixel (non-palletized) for color STN
- 1, 2, 4, 8 bits per pixel (palletized), 16, 24 bits per pixel (non-palletized) for TFT
- Single clock domain architecture
- Resolution supported up to 2048 x 2048

10.12 Touch Screen Analog-to-Digital Converter (TSADC)

- 8-channel ADC
- Support 4-wire resistive Touch Screen
- 10-bit 384 Ksamples/sec. Successive Approximation Register ADC
- -3/+3 LSB Integral Non Linearity, -2/+2 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
 - Hardware or software trigger
 - External trigger pin
- Sleep Mode and conversion sequencer
 - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

10.13 Ethernet 10/100 MAC (EMAC)

- Compatibility with IEEE® Standard 802.3
- 10 and 100 Mb/s per second data throughput capability
- Full- and half-duplex operations
- MII or RMI interface to the physical layer
- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 128-byte transmit and 128-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Supports promiscuous mode where all valid frames are copied to memory
- Supports physical layer management through MDIO interface
- Supports Wake On Lan. The receiver supports Wake on LAN by detecting the following events on incoming receive frames:
 - Magic packet
 - ARP request to the device IP address
 - Specific address 1 filter match
 - Multicast hash filter match

10.14 Image Sensor Interface (ISI)

- ITU-R BT. 601/656 8-bit mode external interface support
- Support for ITU-R BT.656-4 SAV and EAV synchronization
- Vertical and horizontal resolutions up to 2048 x 2048
- Preview Path up to 640*480
- Support for packed data formatting for YCbCr 4:2:2 formats





- Preview scaler to generate smaller size image

10.15 8-channel DMA (DMA)

- Acting as two Matrix Masters
- Embeds 8 unidirectional channels with programmable priority
- Address Generation
 - Source/Destination address programming
 - Address increment, decrement or no change
 - DMA chaining support for multiple non-contiguous data blocks through use of linked lists
 - Scatter support for placing fields into a system memory area from a contiguous transfer. Writing a stream of data into non-contiguous fields in system memory
 - Gather support for extracting fields from a system memory area into a contiguous transfer
 - User enabled auto-reloading of source, destination and control registers from initially programmed values at the end of a block transfer
 - Auto-loading of source, destination and control registers from system memory at end of block transfer in block chaining mode
 - Unaligned system address to data transfer width supported in hardware
- Channel Buffering
 - 16-word FIFO
 - Automatic packing/unpacking of data to fit FIFO width
- Channel Control
 - Programmable multiple transaction size for each channel
 - Support for cleanly disabling a channel without data loss
 - Suspend DMA operation
 - Programmable DMA lock transfer support
- Transfer Initiation
 - Support for Software handshaking interface. Memory mapped registers can be used to control the flow of a DMA transfer in place of a hardware handshaking interface
- Interrupt
 - Programmable Interrupt generation on DMA Transfer completion Block Transfer completion, Single/Multiple transaction completion or Error condition

10.16 True Random Number Generator (TRNG)

- Passed NIST Special Publication 800-22 Tests Suite
- Passed Diehard Random Tests Suite
- Provides a 32-bit Random Number Every 84 Clock Cycles
- For 133 MHz Clock Frequency, Throughput Close to 50 Mbits/s

10.17 Advanced Encryption Standard (AES)

- Compliant with FIPS Publication 197, Advanced Encryption Standard (AES)
- 256-bit Cryptographic Key
- 16 Clock Cycles Encryption/Decryption Processing Time with a 256-bit Cryptographic Key
- Support of the Five Standard Modes of Operation Specified in the NIST Special Publication 800-38A, Recommendation for Block Cipher Modes of Operation - Methods and Techniques:
 - Electronic Code Book (ECB)
 - Cipher Block Chaining (CBC)
 - Cipher Feedback (CFB)
 - Output Feedback (OFB)
 - Counter (CTR)
- 8-, 16-, 32-, 64- and 128-bit Data Sizes Possible in CFB Mode
- Last Output Data Mode Allows Optimized Message Authentication Code (MAC) Generation
- Hardware Counter Measures against Differential Power Analysis Attacks
- Connected to the DMA Controller to optimize Data Transfers for all Operating Modes
 - One Channel for the Receiver, One Channel for the Transmitter
 - Next Buffer Support

10.18 Triple Data Encryption Standard (TDES)

- Supports Single Data Encryption Standard (DES) and Triple Data Encryption Algorithm (TDEA or TDES)
- Compliant with FIPS Publication 46-3, Data Encryption Standard (DES)
- 64-bit Cryptographic Key for TDES
- Two-key or Three-key Algorithms for TDES
- 18-clock Cycles Encryption/Decryption Processing Time for DES
- 50-clock Cycles Encryption/Decryption Processing Time for TDES
- Support the Four Standard Modes of Operation specified in the FIPS Publication 81, DES Modes of Operation
 - Electronic Code Book (ECB)
 - Cipher Block Chaining (CBC)
 - Cipher Feedback (CFB)
 - Output Feedback (OFB)
- 8-, 16-, 32-, 64- and 128-bit Data Sizes Possible in CFB Mode
- Last Output Data Mode Allows Optimized Message (Data) Authentication Code (MAC) Generation
- Connection to PDC Channel Capabilities Optimizes Data Transfers for all Operating Modes
 - One Channel for the Receiver, One Channel for the Transmitter
 - Next Buffer Support





10.19 Secure Hash Algorithm (SHA)

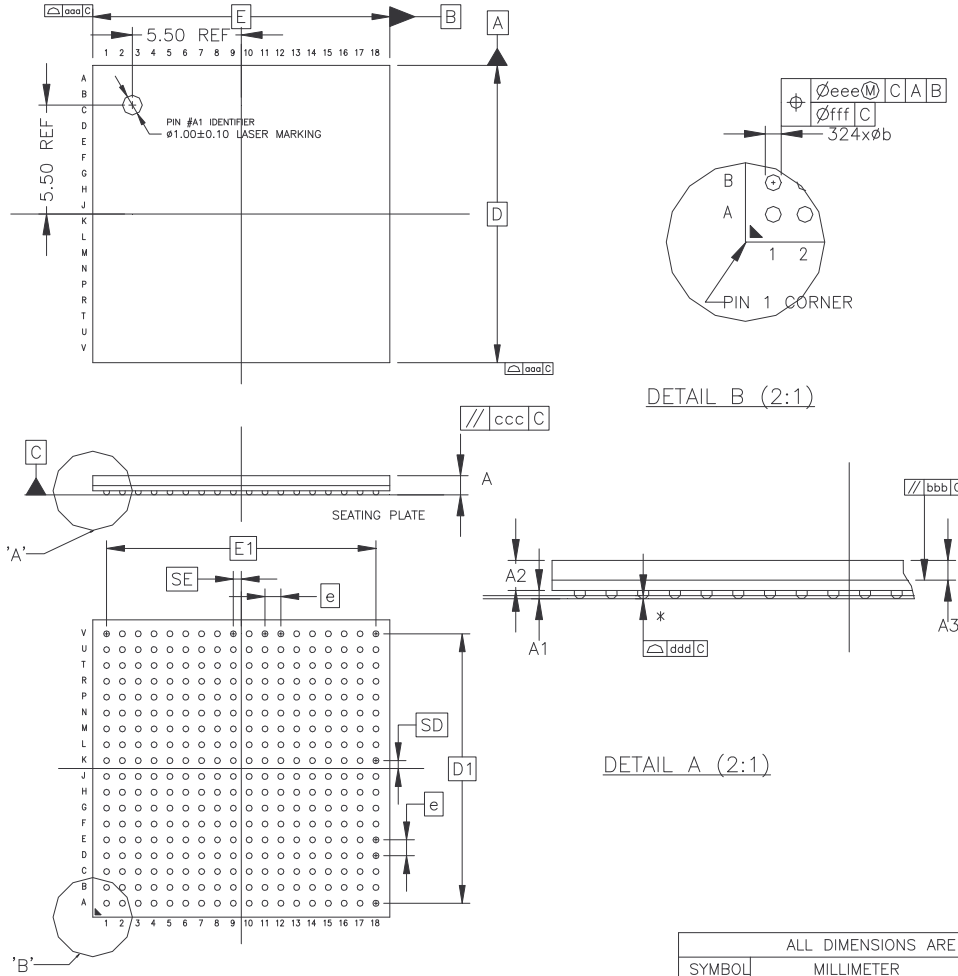
- Supports Secure Hash Algorithm (SHA1 and SHA256)
- Compliant with FIPS Publication 180-2
- Configurable Processing Period:
 - 85 Clock Cycles to Maximize the Bandwidth for SHA1 or 386 Clock Cycles or Other Applications in PDC (Peripheral DMA)
 - 72 Clock Cycles to Maximize the Bandwidth for SHA256 or 265 Clock Cycles or Other Applications in PDC (Peripheral DMA)
- Connection to PDC Channel Capabilities Optimizes Data Transfers
 - One Channel for the Transmitter
 - Next Buffer Support



11. Mechanical Characteristics

11.1 Package Drawings

Figure 11-1. 324-ball TFBGA Package Drawing



NOTES :

1. DIMENSIONS ARE IN MILLIMETERS.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
3. DIMENSION 'A' INCLUDES STANDOFF HEIGHT 'A1' , PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES.
4. DIMENSION 'b' IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| ALL DIMENSIONS ARE IN MILLIMETERS. | | | | | | |
|------------------------------------|-------------|-------|-------|--------------|--------|--------|
| SYMBOL | MILLIMETER | | | INCH | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 1.20 | --- | --- | 0.0472 |
| A1 | 0.16 | 0.21 | 0.26 | 0.0063 | 0.0083 | 0.0102 |
| A2 | 0.72 | 0.76 | 0.80 | 0.0283 | 0.0299 | 0.0315 |
| A3 | 0.50 BASIC | | | 0.0197 BASIC | | |
| D | 14.95 | 15.00 | 15.05 | 0.5886 | 0.5906 | 0.5926 |
| D1 | 13.60 BASIC | | | 0.5354 BASIC | | |
| E | 14.95 | 15.00 | 15.05 | 0.5866 | 0.5906 | 0.5926 |
| E1 | 13.60 BASIC | | | 0.5354 BASIC | | |
| SD | 0.40 BASIC | | | 0.0157 BASIC | | |
| SE | 0.40 BASIC | | | 0.0157 BASIC | | |
| e | 0.80 BASIC | | | 0.0315 | | |
| b | 0.25 | 0.30 | 0.35 | 0.0098 | 0.0118 | 0.0138 |
| aaa | 0.15 | | | 0.0059 | | |
| bbb | 0.20 | | | 0.0079 | | |
| ccc | 0.20 | | | 0.0079 | | |
| ddd | 0.08 | | | 0.0031 | | |
| eee | 0.15 | | | 0.0059 | | |
| fff | 0.08 | | | 0.0031 | | |





12. SAM9G46 Ordering Information

Table 12-1. AT91SAM9G46 Ordering Information

| Ordering Code | Package | Package Type | Temperature Operating Range |
|-----------------|----------|--------------|-----------------------------|
| AT91SAM9G46B-CU | TFBGA324 | Green | Industrial -40°C to 85°C |



Revision History

| Doc. Rev | Comments | Change Request Ref. |
|----------|--|------------------------|
| 11028DS | In "Features" on page 1 added mention of DBGU. In Section 12. "SAM9G46 Ordering Information" updated Table 12-1, "AT91SAM9G46 Ordering Information," on page 56 | rfo 8551 |
| 11028CS | Introduction Product Line/Product naming convention changed - AT91SAM ARM-based MPU / SAM9G46 Section 5.1 "Power Supplies", replaced ground pin names by GNDIOM, GNDCORE, GNDANA, GNDIOP, GNDBU, GNDOSC, GNDUTMI. Reorganized text describing GND association to power supply pins | rfo 7332 rfo |
| 11028BS | '11-layer --> '12-layer' in Section 6.2 "Bus Matrix". | 7172 |
| 11028AS | First issue | |





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