Errata on SAM3U Engineering Sample Devices

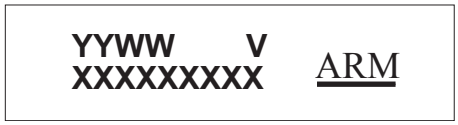
1. Scope

This document describes the known errata found on the SAM3U series engineering samples.

1.1 Marking

All devices are marked with the Atmel logo and the ordering code.

Additional marking is as follows:



where

- “YY”: manufactory year
- “WW”: manufactory week
- “V”: revision
- “XXXXXXXXX”: lot number

AT91 ARM Thumb-based Microcontrollers

ATSAM3U Series

Errata Sheet

6483C–ATARM–09-Aug-10

1.2 Errata: Device Identification (ES)

It applies to:

- AT91SAM3U4E (with Marking ES)
- AT91SAM3U2E (with Marking ES)
- AT91SAM3U1E (with Marking ES)
- AT91SAM3U4C (with Marking ES)
- AT91SAM3U2C (with Marking ES)
- AT91SAM3U1C (with Marking ES)

1.2.1 Flash Memory

1.2.1.1 Flash: Reading Flash in 64-bit mode

Flash access in 64-bit mode does not work.

Problem Fix/Workaround

Use 128-bit mode instead.

1.2.1.2 Flash: Flash Fetch issue running at frequency lower than 2.5 MHz

When the system clock (MCK) is lower than 2.5 MHz with 1 or 2 Wait States (WS) programmed in the EEFC Flash Mode Register (EEFC_FMR), the Cortex®-M3 fetches wrong instructions.

Problem Fix/Workaround

Do not use 1 or 2 WS when running at a frequency lower than 2.5 MHz.

1.2.1.3 Flash: Flash Programming

When writing data into the Flash memory plane (either through the EEFC, using the IAP function or FFPI), the data may not be correctly written (i.e the data written is not the one expected).

Problem Fix/Workaround

Set the number of Wait States (WS) at 6 (FWS = 6) during the programming.

1.2.2 12-bit ADC (ADC12B)

1.2.2.1 ADC12B: Single Ended Mode

When enabling a channel in single ended mode, AD12B0 (CH0) for example, the associated channel in differential mode, AD12B1 and its associated pin are also activated. If the application is using the PIO pin multiplexed with AD12B1 input, the PIO pin will switch to input Analog Mode when the channel is enabled. However, the conversion result on AD12B0 channel is not impacted.

Problem Fix/Workaround

None.

1.2.2.2 ADC12B: Differential Mode

When enabling a channel in differential mode, CH0 (AD12B0-AD12B1 inputs) for example, only the AD12B0 input will be set to input analog mode automatically by the ADC Controller.

Problem Fix/Workaround

The associated differential input channel, AD12B1 must be enabled by the user's software, i.e., CH1.

1.2.2.3 *ADC12B: Wrong Mode after reset*

After reset the ADC is not in Off Mode, but in Standby Mode leading to current consumption on VDDANA (1.4 mA. instead of 0.1 µA).

Problem Fix/Workaround

Configure the ADC in Off Mode in the ADC Extended Mode Register (ADC_EMR) after reset.

1.2.2.4 *ADC12B: Current Consumption in Backup Mode on VDDANA*

In Backup mode, the current consumption on VDDANA is around 1.0 mA instead of 0.1 µA

Problem Fix/Workaround

Three workarounds are possible:

1. Do not supply VDDANA and VDDIO in Backup mode using an external switch managed by SHDN pin.
2. Do not supply VDDANA in Backup mode using an external switch managed by the SHDN or any PIO line and set all PIOs with ADC inputs (PA22, PA30, PB3-PB8, PC15-PC18, PC28-C21) at low level (either externally or by software).
3. Use Wait mode instead of Backup mode

1.2.2.5 *ADC12B: Saturation*

When the ADC12B works in saturation (measurements below 0V or above ADREF) the results may be erratic, the value deviation can be around 30 LSB to the expected data.

Problem Fix/Workaround

None.

1.2.2.6 *ADC12B: ADC Gain Error*

The gain error of the ADC12B can up to ± 12%.

Problem Fix/Workaround

Calibrate the gain error by software.

1.2.3 Serial Wire and JTAG Debug Port (SWJ-DP)

1.2.3.1 *SWJ-DP: Asynchronous Trace (TRACESWO)*

Asynchronous Trace *(TRACESWO)* does not work.

Problem Fix/Workaround

None.

1.2.3.2 *SWJ-DP: Processor Reset*

A processor reset also asserts *SWJ-DP*. Connection issue in debug mode.

Problem Fix/Workaround

Workaround applied by Segger on SAM-ICE Firmware.

1.2.4 Supply Controller (SUPC)

1.2.4.1 SUPC: Bad behavior of SMS and SMOS bit in SUPC_SR in Sample mode

When the Supply Monitor is configured in sample mode (SMSMPL > 1), the SMS and SMOS bits of the supply controller status register (SUPC_SR) might not be reliable when polling SUPC_SR.

Problem Fix/Workaround

Use the Supply Monitor Interrupt instead of polling the status register. In the interrupt handler, set the Supply Monitor in Continuos mode to check the SMA and SMOS bits.

1.2.5 Power Management Controller (PMC)

1.2.5.1 PMC: SysTick does not work properly if MCK/8 is selected as clock source

The System Tick (SysTick) of the Cortex®-M3 has two sources of clock, either MCK or MCK/8 and is configured by the CLKSOURCE bit of the SysTick CTRL register.

When setting CLKSOURCE to 0 (MCK/8), SysTick does not work properly.

Problem Fix/Workaround

Set CLKSOURCE at 1 (MCK selected as SysTick source).

1.2.5.2 PMC: Main Oscillator Crystal Failure detection not functional

When the 32768 Hz Crystal Oscillator is selected as slow clock source and if the Main Oscillator Crystal Failure detection is enabled, the CFDEV, CFDS and FOS status bits in the PMC_SR register do not rise.

Problem Fix/Workaround

Use the Embedded 32 kHz RC Oscillator as slow clock source.

1.2.5.3 PMC: Main Oscillator Frequency selection if the Main On Chip RC Oscillator is off

When the 4/8/12 MHz RC Oscillator is off, the frequency selection (MOSCRCF in CKGR_MOR) can not be changed. The register can be written but the modification on MOSCRCF will not be taken into account.

Problem Fix/Workaround

Modify MOSCRCF when the 4/8/12 MHz RC Oscillator is on (MOSCRCEN =1).

1.2.6 SAM3U Matrix (MATRIX)

1.2.6.1 MATRIX: I/D default master for Flash after reset

The I/D Cortex-M3 bus is not set as default master for the Flash after reset. There is a minor impact in terms of performance when running the code from the Flash (about 5%).

Problem Fix/Workaround

Configure by software the I/D Cortex-M3 bus as default Master for the Flash.

1.2.7 PIO

1.2.7.1 PIO: NCS1 on PA16

The chip select 1 (NCS1) of the SMC on PA16 (Peripheral B) does not work.

Problem Fix/Workaround

Use NCS1 available on PC12 (Peripheral A) or use a another chip select or drive the chip select by software.

1.2.8 Backup Mode

1.2.8.1 Backup mode: VDDUTMI current consumption in Backup mode

In Backup mode, the current consumption measured on VDDUMTI can be around 500 µA instead of less than 0.1 µA.

Problem Fix/Workaround

Disable externally the voltage on VDDUTMI in Backup mode.

1.2.8.2 Backup mode: the PIO states are not kept

When entering in Backup mode with WFE command, the PIO states are not kept. All the PIOs go into input with pull-up state in Backup mode.

Problem Fix/Workaround

.Instead of using the WFE command to go into Backup mode, set the VROFF bit (SUPC_CR).

1.2.9 Wait Mode

1.2.9.1 Wait mode: VDDCORE current consumption

Some parts may show a higher current consumption than expected (50 µA instead of 5 µA) on VDDCORE.

Problem Fix/Workaround

None.

1.3 Errata: Device Identification (ES4)

It applies to:

- AT91SAM3U4E (with Marking ES4)
- AT91SAM3U2E (with Marking ES4)
- AT91SAM3U1E (with Marking ES4)
- AT91SAM3U4C (with Marking ES4)
- AT91SAM3U2C (with Marking ES4)
- AT91SAM3U1C (with Marking ES4)

1.3.1 Flash Memory

1.3.1.1 Flash: Reading Flash in 64-bit mode

Flash access in 64-bit mode does not work.

Problem Fix/Workaround

Use 128-bit mode instead.

1.3.1.2 Flash: Flash Fetch issue running at frequency lower than 2.5 MHz

When the system clock (MCK) is lower than 2.5 MHz with 1 or 2 Wait States (WS) programmed in the EEFC Flash Mode Register (EEFC_FMR), the Cortex-M3 fetches wrong instructions.

Problem Fix/Workaround

Do not use 1 or 2 WS when running at a frequency lower than 2.5 MHz.

1.3.1.3 Flash: Flash Programming

When writing data into the Flash memory plane (either through the EEFC, using the IAP function or FFPI), the data may not be correctly written (i.e the data written is not the one expected).

Problem Fix/Workaround

Set the number of Wait States (WS) at 6 (FWS = 6) during the programming.

1.3.2 12-bit Analog-to-Digital Converter (ADC12B)

1.3.2.1 ADC12B: Current Consumption in Backup Mode on VDDANA

In Backup mode, the current consumption on VDDANA is around 1.0 mA instead of 0.1 µA

Problem Fix/Workaround

Three workarounds are possible:

1. Do not supply VDDANA and VDDIO in Backup mode using an external switch managed by SHDN pin.
2. Do not supply VDDANA in Backup mode using an external switch managed by the SHDN or any PIO line and set all PIOs with ADC inputs (PA22, PA30, PB3-PB8, PC15-PC18, PC28-C21) at low level (either externally or by software).
3. Use Wait mode instead of Backup mode.

1.3.2.2 *ADC12B: Saturation*

When the ADC12B works in saturation (measurements below 0V or above ADREF) the results may be erratic, the value deviation can be around 30 LSB to the expected data.

Problem Fix/Workaround

None.

1.3.3 Power Management Controller (PMC)

1.3.3.1 *PMC: Main Oscillator Frequency selection if the Main On-chip RC Oscillator is OFF*

When the 4/8/12 MHz RC Oscillator is off, the frequency selection (MOSCRCF bitfield in CKGR_MOR) can not be changed. The register can be written but the modification to MOSCRCF will not be taken into account.

Problem Fix/Workaround

Modify MOSCRCF while 4/8/12 MHz RC Oscillator is on (MOSCREN = 1).

Revision History

In the table that follows, the most recent version of the document is referenced first.

Doc. Rev	Comments	Change Request Ref.
6438C	Section 1.2 “Errata: Device Identification (ES)” added Section 1.2.1.3 “Flash: Flash Programming” Section 1.2.2.6 “ADC12B: ADC Gain Error” Section 1.3 “Errata: Device Identification (ES4)” added Section 1.3.1.3 “Flash: Flash Programming”	7204
6483B	This document reorganized to accommodate errata on multiple chip versions. See: Section 1.2 “Errata: Device Identification (ES)” and Section 1.3 “Errata: Device Identification (ES4)” Stand alone “Problem Fix” to each errata removed from (ES) Errata. Section 1.2 “Errata: Device Identification (ES)” “ADC12B: Current Consumption in Backup Mode on VDDANA” on page 3, updated. “ADC12B: Saturation” on page 3, added to errata. Section 1.3 “Errata: Device Identification (ES4)”, Added errata for chips (with marking ES4)	7105
6483A	First issue	

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com
www.atmel.com/AT91SAM

Technical Support
AT91SAM Support
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