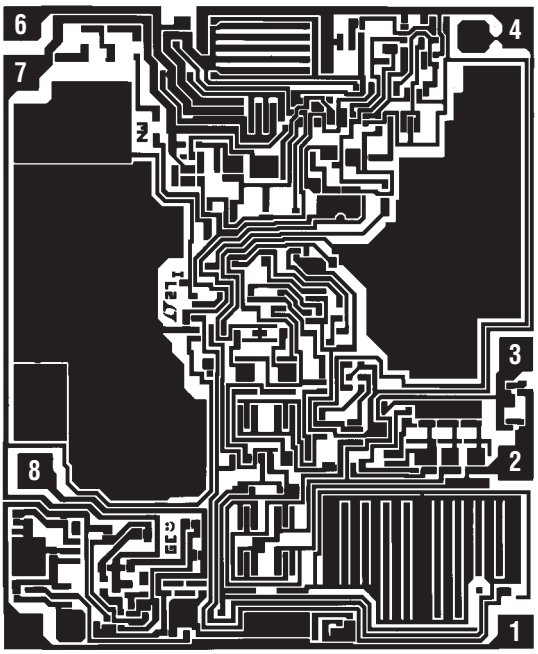
DICE/DWF SPECIFICATION

LT1007
Low Noise, High Speed Precision Op Amp



99mils × 83mils,
12mils thick

PAD FUNCTION

1. V_{OS} TRIM
2. –IN
3. +IN
4. V^-
5. NO CONNECT
6. OUT
7. V^+
8. V_{OS} TRIM

Backside (substrate) is an alloyed gold layer. Connect to V^-

DIE CROSS REFERENCE

LTC Finished Part Number	Order Part Number
LT1007C	LT1007CDICE
LT1007C	LT1007CDWF*

Please refer to LTC standard product data sheet for other applicable product information.
***DWF = DICE in wafer form.**

DICE/DWF ELECTRICAL TEST LIMITS $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = 25°C$.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		60	µV
I_{OS}	Input Offset Current			50	nA
I_B	Input Bias Current			±55	nA
	Input Voltage Range		±11.0		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11$	110		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	106		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2k$, $V_O = \pm12V$ $R_L \geq 1k$, $V_O = \pm10V$	5 3.5		V/µV V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k$ $R_L \geq 600\Omega$	±12.5 ±10.5		V V
SR	Slew Rate	$R_L \geq 2k$	1.7		V/µs
I_S	Supply Current			4.7	mA

Note 1: Input offset voltage measurements are performed by automatic equipment, approximately 0.5 seconds after application of power.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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