Monolithic 2A Step-Down Regulator Plus Linear Regulator/Controller

FEATURES

- **Wide Input Range: 3V to 36V Operating, 40V Maximum**
- **Short-Circuit Protected Over Full Input Range**
- **2A Output Current Capability**
- **Adjustable/Synchronizable Fixed Frequency Operation from 250kHz to 2.2MHz**
- **Soft-Start/Tracking Capability**
- **Output Adjustable Down to 0.8V**
- **Adjustable Linear Regulator/Driver with 13mA Output Capability**
- **Power Good Comparator with Complimentary Outputs**
- Low Shutdown Current: 12µA
- Thermally Enhanced 3mm × 3mm DFN or 16-Pin MSOP Package

APPLICATIONS

- Automotive Battery Regulation
- Industrial Control
- Wall Transformer Regulation
- Distributed Power Regulation

DESCRIPTION

The LT®3500 is a current mode PWM step-down DC/DC converter with an internal 2.3A switch. The wide input range of 3V to 40V makes the LT3500 suitable for regulating power from a wide variety of sources, including automotive batteries, 24V industrial supplies and unregulated wall adapters.

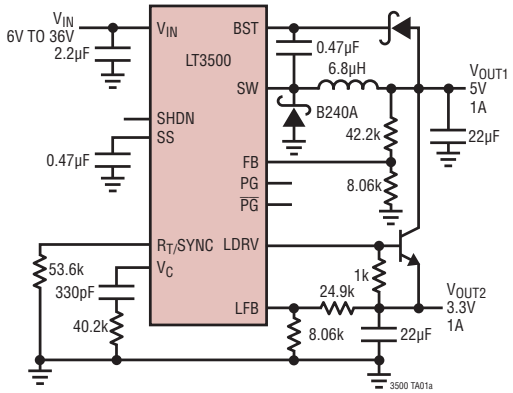
Resistor-programmable 250kHz to 2.2MHz frequency range and synchronization capability enable optimization between efficiency and external component size. Cycle-by-cycle current limit, frequency foldback and thermal shutdown provide protection against a shorted output. The soft-start feature controls the ramp rate of the output voltage, eliminating input current surge during start-up, and also provides output tracking.

The LT3500 contains an internal NPN transistor with feedback control which can be configured as a linear regulator or as a linear regulator controller.

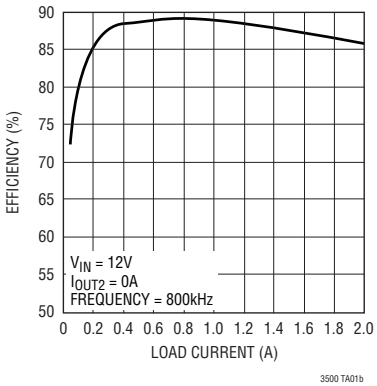
The LT3500's low current shutdown mode (<12µA) enables easy power management in battery-powered systems.

TYPICAL APPLICATION

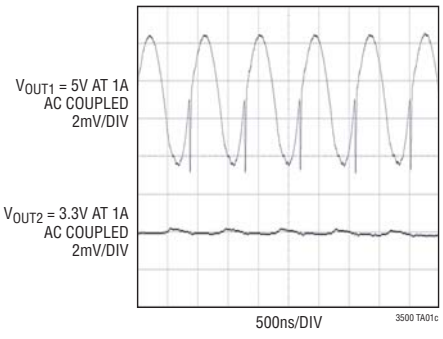
Dual Step-Down Converters



Switching Converter Efficiency



Output Voltage Ripple

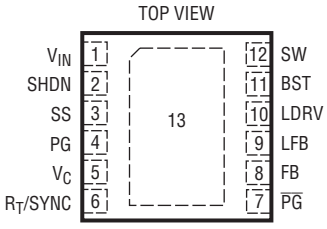


ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, PG, $\overline{PG}$ Operating 40V/–0.3V
SW ..... V_{IN}
BST 55V/–0.3V
BST Pin Above SW 25V
LDRV, SHDN 15V
FB, LFB, R_T/SYNC 5V
SS, V_C 2.5V

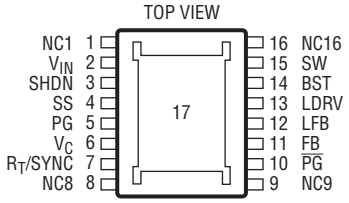
Operating Junction Temperature Range
LT3500EDD (Note 2) ..... –40°C to 125°C
LT3500IDD (Note 2) ..... –40°C to 125°C
LT3500HDD (Note 2) ..... –40°C to 150°C
LT3500EMSE (Note 2) ..... –40°C to 125°C
LT3500IMSE (Note 3) ..... –40°C to 125°C
LT3500HMSE (Note 2) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN

θ_{JA} = 45°C/W, $\theta_{JC(PAD)}$ = 10°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSE

θ_{JA} = 45°C/W, $\theta_{JC(PAD)}$ = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3500EDD#PBF	LT3500EDD#TRPBF	LCRN	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3500IDD#PBF	LT3500IDD#TRPBF	LCRN	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3500HDD#PBF	LT3500HDD#TRPBF	LDCY	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 150°C
LT3500EMSE#PBF	LT3500EMSE#TRPBF	3500	16-Lead Plastic MSE	–40°C to 125°C
LT3500IMSE#PBF	LT3500IMSE#TRPBF	3500	16-Lead Plastic MSE	–40°C to 125°C
LT3500HMSE#PBF	LT3500HMSE#TRPBF	3500	16-Lead Plastic MSE	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{VIN} = 15V, $V_{RT/SYNC}$ = 2V, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SHDN Threshold		●	710	760	780	mV
SHDN Source Current	V_{SHDN} = 0.62V		1.5	2.5	3.5	µA
SHDN Current Hysterisis			1.25	2	3.25	µA
Minimum Input Voltage (Note 3)	V_{FB} = 0V	●		2.4	2.8	V
Supply Shutdown Current	V_{SHDN} = 0V	●		12	30	µA
Supply Quiescent Current	V_{FB} = 0.9V			2.5	3.5	mA
FB Voltage	V_{VC} = 1V V_{VC} = 0.8V to 1.6V, V_{IN} = 3V to 40V	● ●	0.784 0.776	0.8 0.8	0.816 0.824	V V
FB Bias Current	V_{FB} = 0.8V, V_{VC} = 1V			50	150	nA
Error Amplifier g_m	V_{VC} = 1V, I_{VC} = ±10µA		150	250	350	µmho
Error Amplifier Source Current	V_{FB} = 0.6V, V_{VC} = 1V		12	16	20	µA
Error Amplifier Sink Current	V_{FB} = 1V, V_{VC} = 1V		14	18	22	µA
Error Amplifier High Clamp	V_{FB} = 0.6V		1.8	2.0	2.2	V
Error Amplifier Switching Threshold	V_{FB} = 0.6V		0.6	0.8	1.0	V
SS Source Current	V_{SS} = 0.4V, V_{FB} = 0.9V		2.25	2.75	3.75	µA
SS Sink Current	V_{FB} = 0V, V_{SS} = 2V		300	600	900	µA
SS POR Sink Current (Note 4)	V_{FB} = 0V, V_{SS} = 2V, Cycle SHDN		400	600	800	µA
SS POR Threshold			50	100	150	mV
SS to FB Offset (V_{SS} – V_{FB})	V_{VC} = V_{FS}, V_{SS} = 0.4V		70	100	120	mV
PG/$\overline{PG}$ Leakage	V_{FB} = 0.9V, V_{PG}/$V_{\overline{PG}}$ = 40V			0.1	1	µA
PG/$\overline{PG}$ Threshold (Rising)	V_{PG} = 0.4V		0.685	0.708	0.730	V
PG/$\overline{PG}$ Hysteresis (Falling)	V_{PG} = 0.4V		20	30	40	mV
PG Sink Current	V_{PG} = 0.4V, V_{FB} = 0.7V		250	500	750	µA
$\overline{PG}$ Sink Current	$V_{\overline{PG}}$ = 0.4V, V_{FB} = 0.9V		500	800	1100	µA
R_T/SYNC Reference Voltage	V_{FB} = 0.9V, $R_{RT/SYNC}$ = 15k		0.75	0.850	0.975	V
Switching Frequency	$R_{RT/SYNC}$ = 90.9k $R_{RT/SYNC}$ = 90.9k $R_{RT/SYNC}$ = 15k	 ● 	450 425 2	500 500 2.4	550 625 2.8	kHz kHz MHz
SYNC Frequency Range		●	250		2500	kHz
Minimum Switch On Time	V_{FB} = 0.7V, $R_{RT/SYNC}$ = 90.9k			140		ns
Minimum Switch Off Time	V_{FB} = 0.7V, $R_{RT/SYNC}$ = 90.9k			120		ns
Switch Leakage Current	V_{SW} = 0V			1	10	µA
Switch Saturation Voltage	I_{SW} = 2A, V_{BST} = 18V, V_{FB} = 0.7V			450		mV
Switch Peak Current DD Package	V_{BST} = 18V, V_{FB} = 0.7V	 ●	2.3 2.1	2.8 2.8	3.5 3.5	A A
Switch Peak Current MSE Package	V_{BST} = 18V, V_{FB} = 0.7V	 ●	2.3 2.1	2.9 2.9	3.5 3.7	A A
Boost Current	I_{SW} = 2A, V_{BST} = 20V, V_{FB} = 0.7V		20	30	45	mA
Minimum Boost Voltage (Note 5)	I_{SW} = 2A, V_{FB} = 0.7V			2.2	3	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{VIN} = 15V, $V_{RT/SYNC}$ = 2V, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LFB Voltage	$V_{LDRV} = V_{LFB}$	●	0.784	0.8	0.816	V
LFB Line/Load Regulation	V_{VIN} = 3V to 40V, $V_{LDRV} = V_{LFB}$	●	0.776	0.8	0.824	V
SS to LFB Offset ($V_{SS} - V_{LFB}$)	V_{SS} = 0.8V, $V_{LDRV} = V_{LFB}$		90	115	140	mV
LFB Bias Current	V_{LFB} = 0.8V			115	300	nA
LDRV Dropout ($V_{VIN} - V_{LDRV}$)	V_{LDRV} = 3V, I_{LDRV} = 5mA	●	0.8	1.2	1.6	V
LDRV Maximum Current	V_{LDRV} = 0V	●	9	13	18	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note2: The LT3500EDD/LT3500EMSE is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3500IDD/LT3500IMSE is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3500HDD/LT3500HMSE is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: Minimum input voltage is defined as the voltage where internal bias lines are regulated so that the reference voltage and oscillator remain constant. Actual minimum input voltage to maintain a regulated output will depend upon output voltage and load current. See Applications Information.

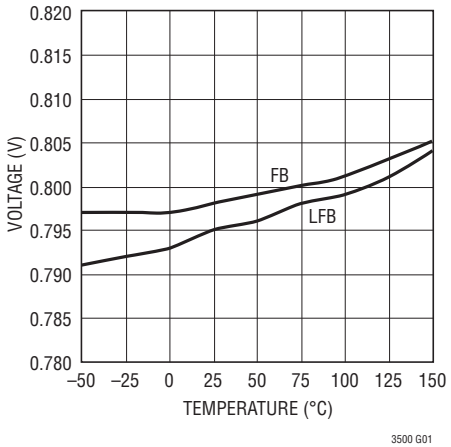
Note 4: An internal power-on reset (POR) latch is set on the positive transition of the SHDN pin through its threshold. The output of the latch activates a current source on the SS pin which typically sinks 600µA, discharging the SS capacitor. The latch is reset when the SS pin is driven below the soft-start POR threshold or the SHDN pin is taken below its threshold.

Note 5: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

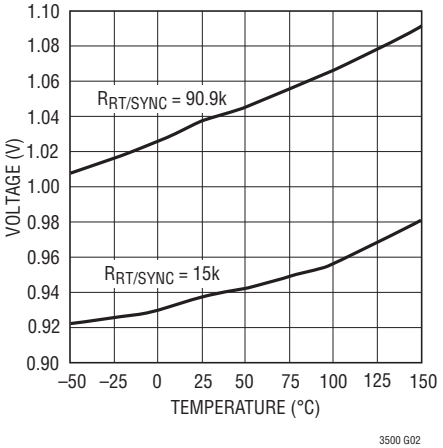
Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

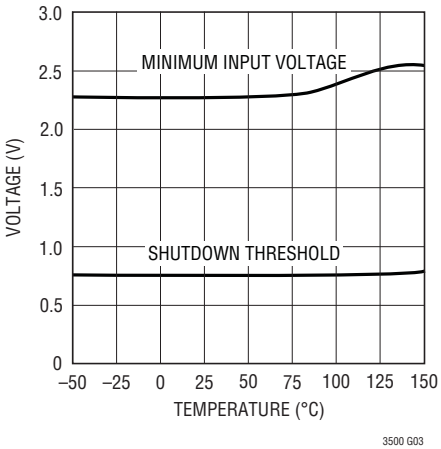
Feedback Voltage vs Temperature



R_T/SYNC Voltage vs Temperature

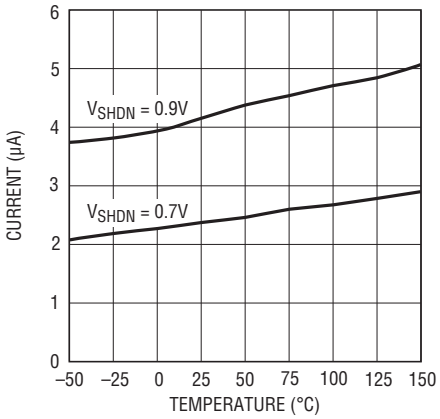


Shutdown Threshold and Minimum Input Voltage vs Temperature

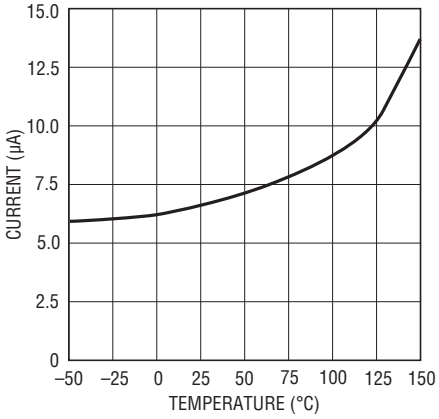


TYPICAL PERFORMANCE CHARACTERISTICS

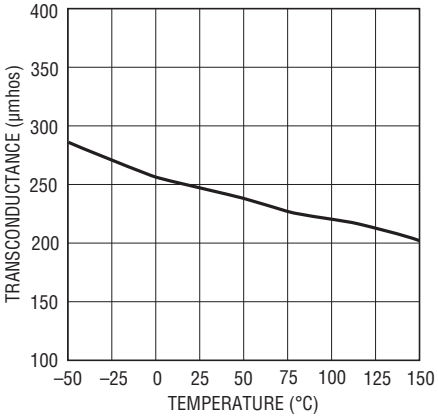
Shutdown Input Currents vs Temperature



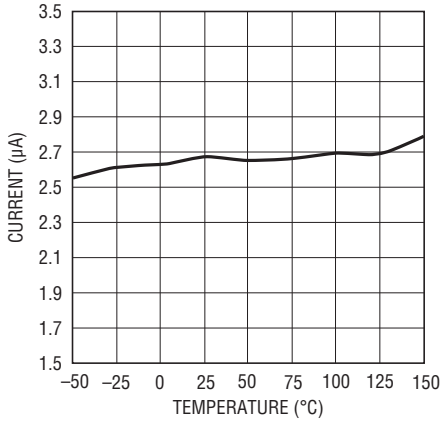
Shutdown Quiescent Current vs Temperature



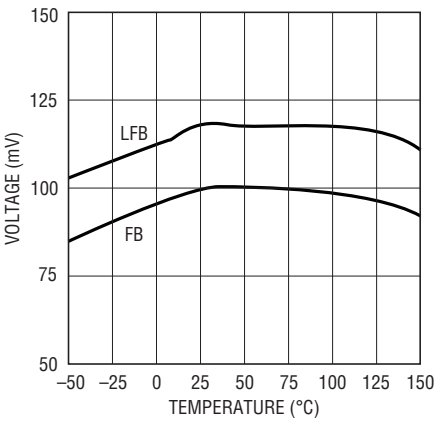
Error Amplifier g_m vs Temperature



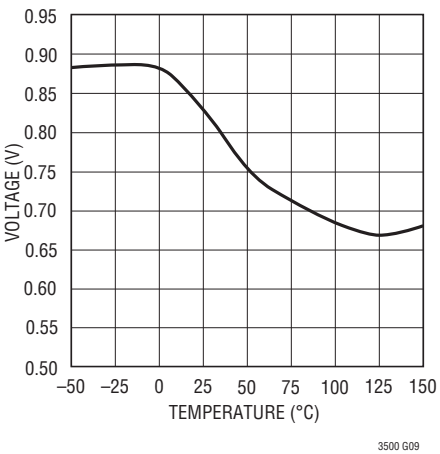
Soft-Start Source Current vs Temperature



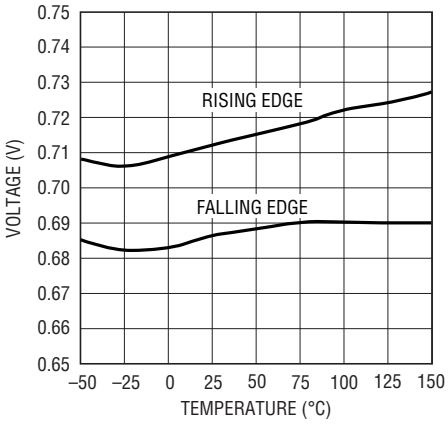
Soft-Start Feedback Offset vs Temperature



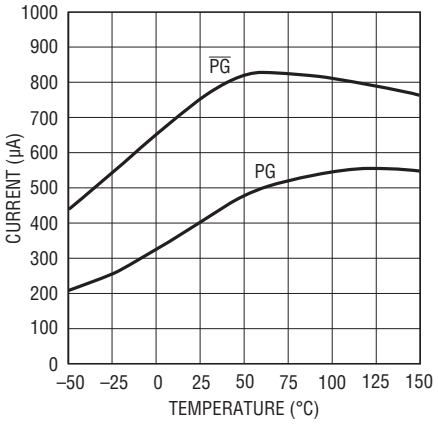
VC Switching Threshold vs Temperature



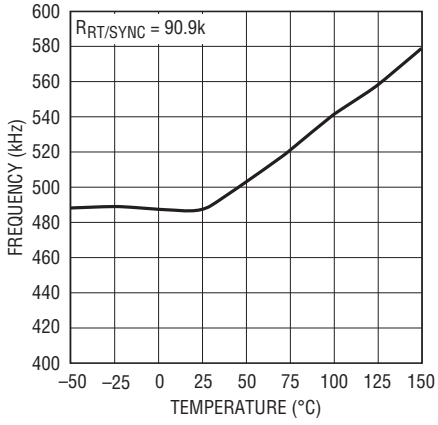
Power Good Thresholds vs Temperature



Power Good Sink Currents vs Temperature

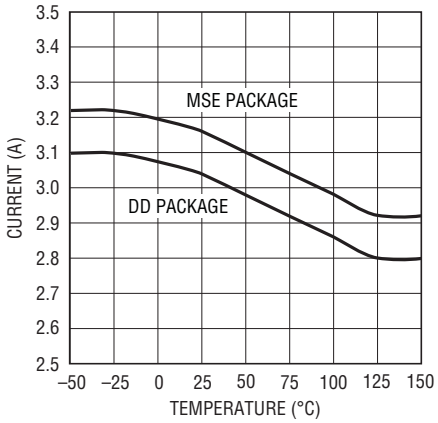


Frequency vs Temperature

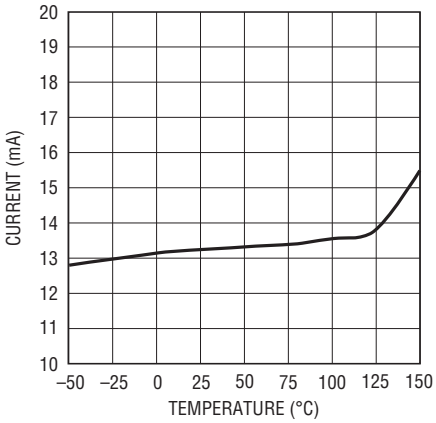


TYPICAL PERFORMANCE CHARACTERISTICS

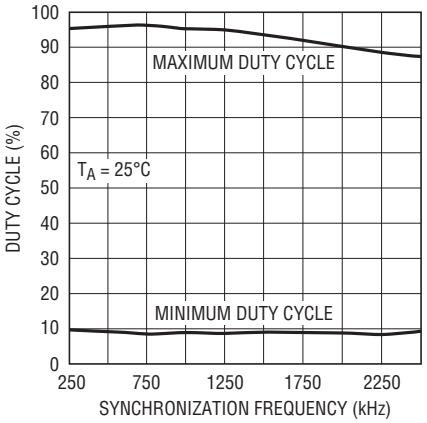
Peak Switch Current vs Temperature



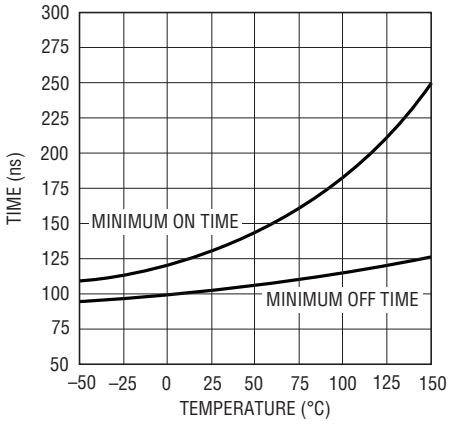
LDRV Short-Circuit Current vs Temperature



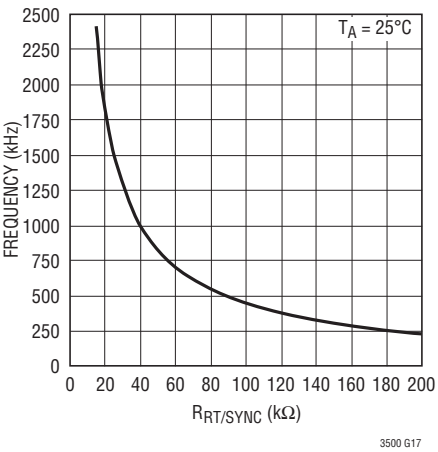
External Sync Duty Cycle Range vs External Sync Frequency



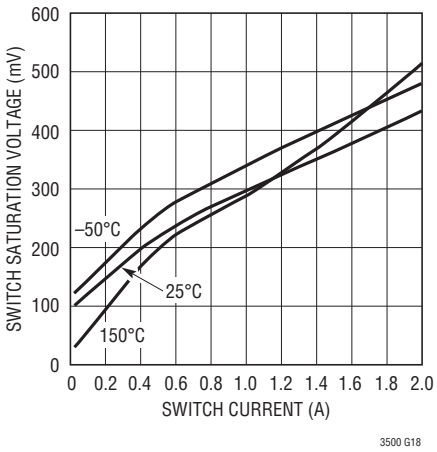
Minimum Switching Times



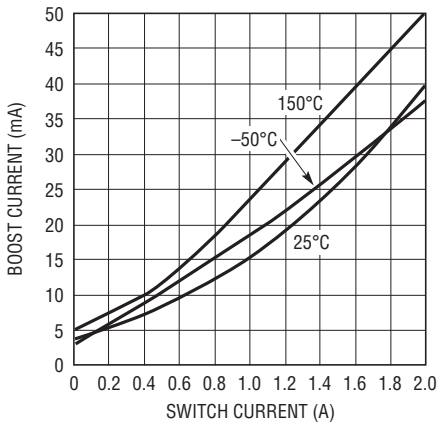
Frequency vs $R_{RT/SYNC}$



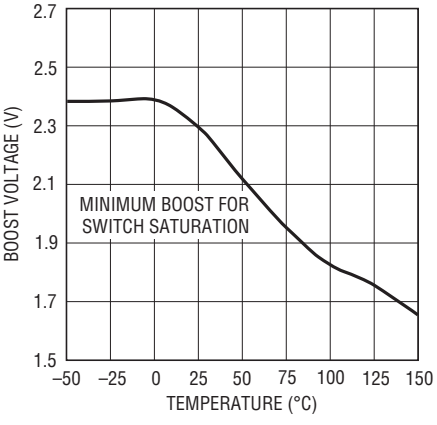
Switch Saturation Voltage vs Switch Current



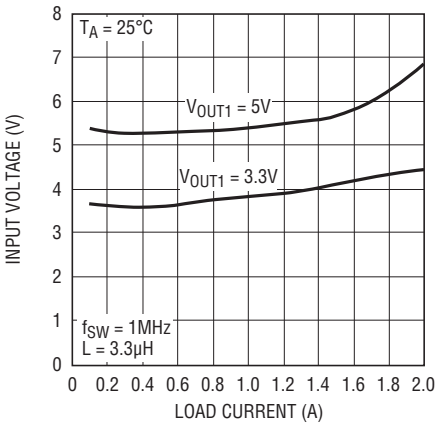
Boost Current vs Switch Current



Minimum Boost Voltages vs Temperature

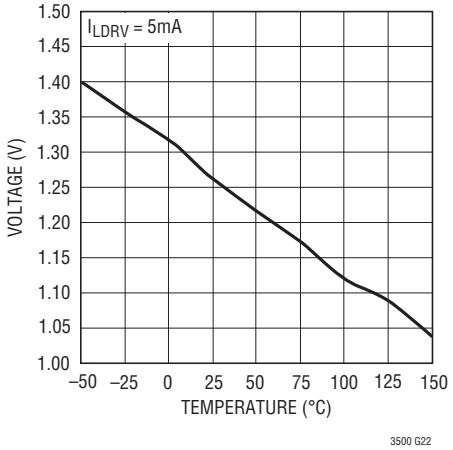


Minimum Input Voltage

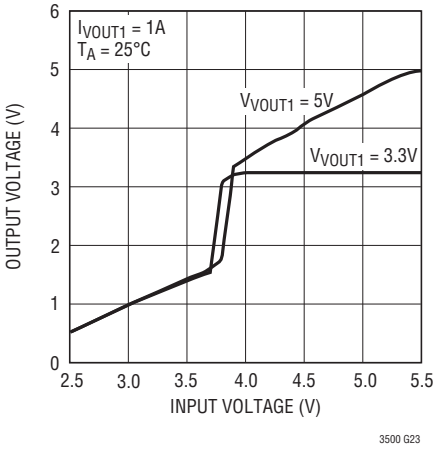


TYPICAL PERFORMANCE CHARACTERISTICS

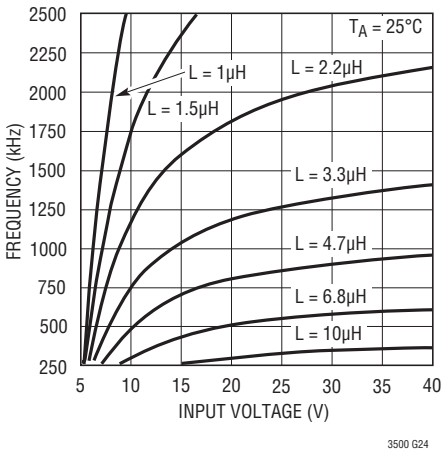
LDRV Dropout Voltage vs Temperature



Switcher Dropout Operation



Inductor Value for 2A Maximum Load Current (V_{OUT1} = 3.3V, I_{RIPPLE} = 250mA)



PIN FUNCTIONS

V_{IN}: The V_{IN} pin powers the internal control circuitry and is monitored by an undervoltage comparator. The V_{IN} pin is also connected to the collectors of the internal power NPN switch and linear output NPN. The V_{IN} pin has high dI/dt edges and must be decoupled to ground close to the pin of the device.

SHDN: The SHDN pin is used to shut down the LT3500 and reduce quiescent current to a typical value of 12µA. The accurate 0.76V threshold and input current hysteresis can be used as an undervoltage lockout, preventing the regulator from operating until the input voltage has reached a predetermined level. Force the SHDN pin above its threshold or let it float for normal operation.

SS: The SS pin is used to control the slew rate of the output of both the switching and linear regulators. A single capacitor from the SS pin to ground determines the regulators' ramp rate. For soft-start details see the Applications Information section.

PG: The power good pin is an open-collector output that sinks current when the FB or LFB falls below 90% of its nominal regulating voltage. For V_{IN} above 2V, its output state remains true, although during SHDN, V_{IN} undervoltage lockout, or thermal shutdown, its current sink capability is reduced

V_C: The V_C pin is the output of the error amplifier and the input to the peak switch current comparator. It is normally used for frequency compensation, but can also be used as a current clamp or control loop override. If the error amplifier drives V_C above the maximum switch current level, a voltage clamp activates. This indicates that the output is overloaded and current to be pulled from the SS pin reducing the regulation point.

R_T/SYNC: This R_T/SYNC pin provides two modes of setting the constant switch frequency.

Connecting a resistor from the R_T/SYNC pin to ground will set the R_T/SYNC pin to a typical value of 1V. The resultant switching frequency will be set by the resistor value. The minimum value of 15kΩ and maximum value of 200kΩ set the switching frequency to 2.5MHz and 250kHz respectively.

PIN FUNCTIONS

Driving the R_T/SYNC pin with an external clock signal will synchronize the switch to the applied frequency. Synchronization occurs on the rising edge of the clock signal after the clock signal is detected. Each rising clock edge initiates an oscillator ramp reset. A gain control loop servos the oscillator charging current to maintain a constant oscillator amplitude. Hence, the slope compensation remains unchanged. If the clock signal is removed, the oscillator reverts to resistor mode and reapplies the 1V bias to the R_T/SYNC pin after the synchronization detection circuitry times out. The clock source impedance should be set such that the current out of the R_T/SYNC pin in resistor mode generates a frequency roughly equivalent to the synchronization frequency. Floating or holding the R_T/SYNC pin above 1.1V will not damage the device, but will halt oscillation.

$\overline{PG}$: The power good bar pin is an open-collector output that sinks current when the FB or LFB rises above 90% of its nominal regulating voltage.

FB: The FB pin is the negative input to the switcher error amplifier. The output switches to regulate this pin to 0.8V with respect to the exposed ground pad. Bias current flows out of the FB pin.

LFB: The LFB pin is the negative input to the linear error amplifier. The L_{DRV} pin servo's to regulate this pin to 0.8V with respect to the exposed ground pad. Bias current flows out of the LFB pin.

LDRV: The LDRV pin is the emitter of an internal NPN that can be configured as an output of a linear regulator or as the drive for an external NPN high current regulator. Current flows out of the LDRV pin when the LFB pin voltage is below 0.8V. The LDRV pin has a typical maximum current capability of 13mA.

BST: The BST pin provides a higher than V_{IN} base drive to the power NPN to ensure a low switch drop. A comparator to V_{IN} imposes a minimum off time on the SW pin if the BST pin voltage drops too low. Forcing a SW off time allows the boost capacitor to recharge.

SW: The SW pin is the emitter of the on-chip power NPN. At switch off, the inductor will drive this pin below ground with a high dV/dt. An external catch diode to ground, close to the SW pin and respective V_{IN} decoupling capacitor's ground, must be used to prevent this pin from excessive negative voltages.

Exposed Pad: GND. The exposed pad is the only ground connection for the device. The exposed pad should be soldered to a large copper area to reduce thermal resistance. The GND pin also serves as small-signal ground. For ideal operation all small-signal ground paths should connect to the GND pin at a single point, avoiding any high current ground returns.

NC Pins (MSE Package Only): No Connection. The NC pins are electrically isolated from the LT3500. The NC pins may be connected to PCB traces to aid PCB layout.

BLOCK DIAGRAM

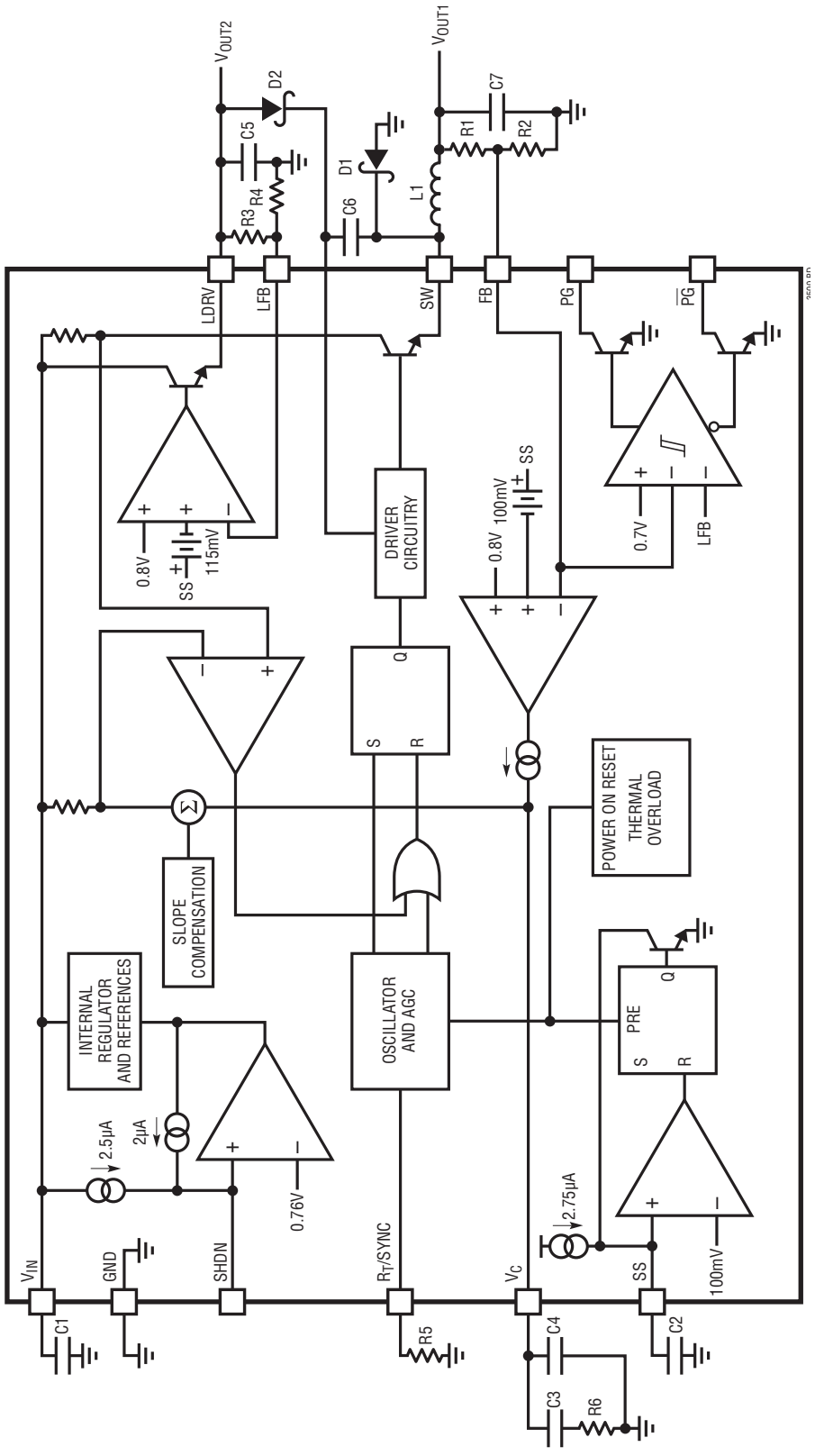


Figure 1. LT3500 Block Diagram

OPERATION

The LT3500 is a constant frequency, current mode buck converter with an internal 2.3A switch plus a linear regulator with 13mA output capability. Control of both outputs is achieved with a common SHDN pin, internal regulator, oscillator, undervoltage detect, soft-start, thermal shutdown and power-on reset.

If the SHDN pin is taken below its 0.8V threshold, the LT3500 will be placed in a low quiescent current mode. In this mode the LT3500 typically draws 12µA from the V_{IN} pin.

When the SHDN pin is floated or driven above 0.76V, the internal bias circuits turn on generating an internal regulated voltage, 0.8(V_{FB}) and 1V(R_T/SYNC) references, and a POR signal which sets the soft-start latch.

As the R_T/SYNC pin reaches its 1V regulation point, the internal oscillator will start generating a clock signal at a frequency determined by the resistor from the R_T/SYNC pin to ground. Alternatively, if a synchronization signal is detected by the LT3500 at the R_T/SYNC pin, a clock signal will be generated at the incoming frequency on the rising edge of the synchronization pulse. In addition, the internal slope compensation will be automatically adjusted to prevent subharmonic oscillation during synchronization.

The LT3500 is a constant frequency, current mode stepdown converter. Current mode regulators are controlled by an internal clock and two feedback loops that control the duty cycle of the power switch. In addition to the normal error amplifier, there is a current sense amplifier that monitors switch current on a cycle-by-cycle basis. This technique means that the error amplifier commands current to be delivered to the output rather than voltage.

A voltage fed system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180° shift will occur. The current fed system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and also gives much quicker transient response.

During power up, the POR signal sets the soft-start latch, which discharges the SS pin to ensure proper start-up operation. When the SS pin voltage drops below 100mV, the V_C pin is driven low disabling switching and the soft-start latch is reset. Once the latch is reset the soft-start capacitor starts to charge with a typical value of 2.75µA.

As the voltage rises above 100mV on the SS pin, the V_C pin will be driven high by the error amplifier. When the voltage on the V_C pin exceeds 0.8V, the clock set-pulse sets the driver flip-flop which turns on the internal power NPN switch. This causes current from V_{IN}, through the NPN switch, inductor and internal sense resistor, to increase. When the voltage drop across the internal sense resistor exceeds a predetermined level set by the voltage on the V_C pin, the flip-flop is reset and the internal NPN switch is turned off. Once the switch is turned off the inductor will drive the voltage at the SW pin low until the external Schottky diode starts to conduct, decreasing the current in the inductor. The cycle is repeated with the start of each clock cycle. However, if the internal sense resistor voltage exceeds the predetermined level at the start of a clock cycle, the flip-flop will not be set resulting in a further decrease in inductor current. Since the output current is controlled by the V_C voltage, output regulation is achieved by the error amplifier continually adjusting the V_C pin voltage.

The error amplifier is a transconductance amplifier that compares the FB voltage to either the SS pin voltage minus 100mV or an internally regulated 800mV, whichever is lowest. Compensation of the loop is easily achieved with a simple capacitor or series resistor/capacitor from the V_C pin to ground.

Since the SS pin is driven by a constant current source, a single capacitor on the soft-start pin will generate controlled linear ramp on the output voltage.

If the current demanded by the output exceeds the maximum current dictated by the V_C pin clamp, the SS pin will be discharged, lowering the regulation point until the output voltage can be supported by the maximum current. When overload is removed, the output will soft-start from the overload regulation point.

OPERATION

V_{IN} undervoltage detection or thermal shutdown will set the soft-start latch, resulting in a complete soft-start sequence.

The switch driver operates from either the V_{IN} or BST voltage. An external diode and capacitor are used to generate a drive voltage higher than V_{IN} to saturate the output NPN and maintain high efficiency.

In addition to the switching regulator, the LT3500 contains a NPN linear regulator with a 0.8V reference, and 13mA current capability. The 0.8 reference will track the SS pin in the same manner as the switching regulator. The linear output can also be configured to drive an external NPN to provide a linear regulator with higher current capability.

A power good comparator with 30mV of hysteresis trips when both FB and LFB are above 90% of the 0.8V reference. The PG output is an open collector NPN that is off when the output is in regulation allowing a resistor to pull the PG pin to a desired voltage. The $\overline{PG}$ output is an open-collector NPN that is on when the output is in regulation providing either drive for an output disconnect transistor or inverted power good logic.

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Choosing the Output Voltage

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the 1% resistors according to:

$$R1 = R2\left(\frac{V_{OUT1}}{0.8V} - 1\right)$$

R2 should be 10.0k or less to avoid bias current errors. Reference designators refer to the Block Diagram in Figure 1.

Choosing the Switching Frequency

The LT3500 switching frequency is set by resistor R5 in Figure 1. The R_T/SYNC pin is internally regulated at 1V. Setting resistor R5 sets the current in the R_T/SYNC pin which determines the oscillator frequency as illustrated in Figure 2.

The switching frequency is typically set as high as possible to reduce overall solution size. The LT3500 employs techniques to enhance dropout at high frequencies but efficiency and maximum input voltage decrease due to switching losses and minimum switch on times. The maximum recommended frequency can be approximated by the equation:

$$\text{Frequency (Hz)} = \frac{V_{OUT1} + V_D}{V_{IN} - V_{SW} + V_D} \bullet \frac{1}{t_{ON(MIN)}}$$

where V_D is the forward voltage drop of the catch diode (D1 Figure 1), V_{SW} is the voltage drop of the internal switch, and $t_{ON(MIN)}$ is the minimum on time of the switch, all at maximum load current.

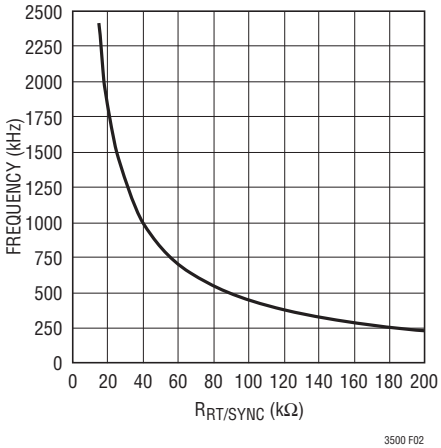

Figure 2. Frequency vs R_T/SYNC Resistance

APPLICATIONS INFORMATION

The following example along with the data in Table 1 illustrates the tradeoffs of switch frequency selection.

Example.

V_{IN} = 25V, V_{OUT1} = 3.3V, I_{OUT1} = 2.0A,

Temperature = 0°C to 85°C

$t_{ON(MIN)}$ = 185ns (85°C from Typical Characteristics graph), V_D = 0.6V, V_{SW} = 0.4V (85°C)

$$\text{Max Frequency} = \frac{3.3+0.6}{25-0.4+0.6} \bullet \frac{1}{185\text{ns}} \sim 835\text{kHz}$$

R_T/SYNC ~ 49.9k

Frequency ≅ 820kHz

Input Voltage Range

Once the switching frequency has been determined, the input voltage range of the regulator can be determined. The minimum input voltage is determined by either the LT3500's minimum operating voltage of ~2.8V or by its maximum duty cycle. The duty cycle is the fraction of time that the internal switch is on during a clock cycle. The maximum duty cycle can be determined from the clock frequency and the minimum off time from the typical characteristics graph.

This leads to a minimum input voltage of:

$$V_{IN(MIN)} = \frac{V_{OUT1} + V_D}{DC_{MAX}} - V_D + V_{SW}$$

where V_{SW} is the voltage drop of the internal switch, and

$DC_{MAX} = 1 - t_{OFF(MIN)} \bullet \text{Frequency}$.

Figure 3 shows a typical graph of minimum input voltage vs load current for 3.3V and 5V applications.

The maximum input voltage is determined by the absolute maximum ratings of the V_{IN} and BST pins and by the frequency and minimum duty cycle.

The minimum duty cycle is defined as:

$DC_{MIN} = t_{ON(MIN)} \bullet \text{Frequency}$

Maximum input voltage as:

$$V_{IN(MAX)} = \frac{V_{OUT1} + V_D}{DC_{MIN}} - V_D + V_{SW}$$

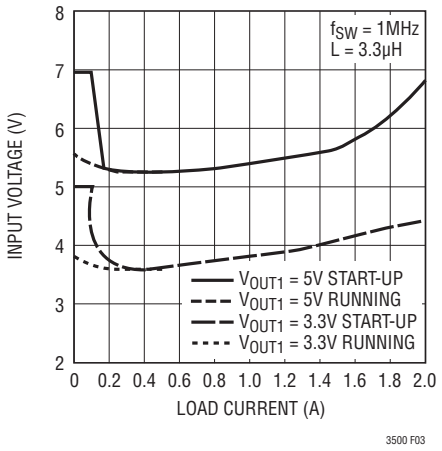

Figure 3. Minimum Input Voltage vs Load Current

Table 1. Efficiency and Size Comparisons for Different $R_{RT/SYNC}$ Values, V_{OUT1} = 3.3V

FREQUENCY	R_T/SYNC	EFFICIENCY	$V_{IN(MAX)}$	L	C	C + L AREA (mm^2)
2.5MHz	15k	73.6	12	1µ	10µ	24
2.0MHz	20k	81.5	14	1.5µ	10µ	24
1.5MHz	24.9k	84.5	18	2.2µ	10µ	24
1.0MHz	40.2k	87.3	28	3.3µ	22µ	34
500kHz	90.9k	88.9	36	4.7µ	47µ	40

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Note that the LT3500 will regulate if the input voltage is taken above the calculated maximum voltage as long as maximum ratings of the V_{IN} and BST pins are not violated. However operation in this region of input voltage will exhibit pulse skipping behavior.

Example:

V_{OUT1} = 3.3V, I_{OUT1} = 1A, Frequency = 1MHz,

Temperature = 25°C,

V_{SW} = 0.3V, V_D = 0.4V, $t_{ON(MIN)}$ = 150ns, $t_{OFF(MIN)}$ = 110ns

$$DC_{MAX} = 1 - (110ns)1MHz = 89\%$$

$$V_{IN(MIN)} = \frac{3.3 + 0.4}{0.89} - 0.4 + 0.3 = 4.06V$$

$$DC_{MIN} = t_{ON(MIN)} \bullet Frequency = 15\%$$

$$V_{IN(MAX)} = \frac{3.3 + 0.4}{0.15} - 0.4 + 0.3 = 24.57V$$

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = \frac{(V_{IN} - V_{OUT1}) \bullet V_{OUT1}}{V_{IN} \bullet f}$$

where f is frequency in MHz and L is in µH.

With this value the maximum load current will be ~2A, independent of input voltage. The inductor's RMS current rating must be greater than your maximum load current and its saturation current should be about 30% higher. To keep efficiency high, the series resistance (DCR) should be less than 0.05Ω.

For applications with a duty cycle of about 50%, the inductor value should be chosen to obtain an inductor ripple current less than 40% of peak switch current.

Of course, such a simple design guide will not always result in the optimum inductor for your application. A larger value provides a slightly higher maximum load current, and will reduce the output voltage ripple. If your load is lower than 1.5A, then you can decrease the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency.

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to peak inductor ripple current. The LT3500 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT3500 will deliver depends on the current limit, the inductor value, switch frequency, and the input and output voltages. The inductor is chosen based on output current requirements, output voltage ripple requirements, size restrictions and efficiency goals.

When the switch is off, the inductor sees the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = \frac{(1 - DC)(V_{OUT1} + V_D)}{L \bullet f}$$

where f is the switching frequency of the LT3500 and L is the value of the inductor. The peak inductor and switch current is:

$$I_{SW(PK)} = I_{LPK} = I_{OUT1} + \frac{\Delta I_L}{2}$$

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To maintain output regulation, this peak current must be less than the LT3500's switch current limit, I_{LIM}. I_{LIM} is guaranteed to be greater than 2.3A over the entire duty cycle range. The maximum output current is a function of the chosen inductor value:

$$I_{OUT1(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} = 2.3 - \frac{\Delta I_L}{2}$$

If the inductor value is chosen so that the ripple current is small, then the available output current will be near the switch current limit.

One approach to choosing the inductor is to start with the simple rule given above, look at the available inductors and choose one to meet cost or space goals. Then use these equations to check that the LT3500 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when I_{OUT1} is less than $I_L/2$ as calculated above.

Figure 4 illustrates the inductance value needed for a 3.3V output with a maximum load capability of 2A. Referring to Figure 4, an inductor value between 3.3µH and 4.7µH will be sufficient for a 15V input voltage and a switch frequency of 750kHz. There are several graphs in the Typical Performance Characteristics section of this data sheet that show inductor selection as a function of input voltage and switch frequency for several popular output voltages and output ripple currents. Also, low inductance may result in discontinuous mode operation, which is okay, but further reduces maximum load current. For details of maximum output current and discontinuous mode operation, see Linear Technology Application Note 44. Finally, for duty cycles greater than 50% (V_{OUT1}/V_{IN} > 0.5), there is a minimum inductance required to avoid subharmonic oscillations. See Application Note 19 for more information.

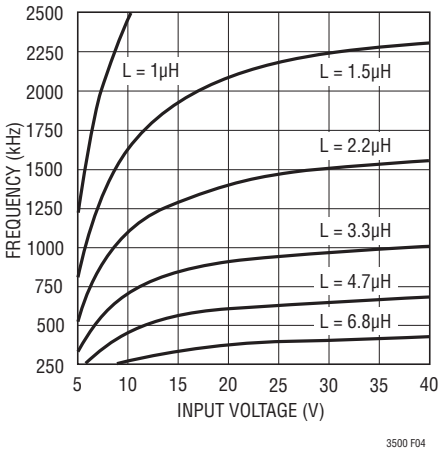

Figure 4. Inductor Values for 2A Maximum Load Current (V_{OUT1} = 3.3V, I_{RIPPLE} = 1A)

Input Capacitor Selection

Bypass the input of the LT3500 circuit with a 4.7µF or higher ceramic capacitor of X7R or X5R type. A lower value or a less expensive Y5V type can be used if there is additional bypassing provided by bulk electrolytic or tantalum capacitors. The following paragraphs describe the input capacitor considerations in more detail.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3500 and to force this very high frequency switching current into a tight local loop, minimizing EMI. The input capacitor must have low impedance at the switching frequency to do this effectively, and it must have an adequate ripple current rating.

A conservative value is the RMS input current is given by:

$$I_{CIN(RMS)} = \frac{I_{OUT1}\left[V_{OUT1} \bullet \left(V_{IN} - V_{OUT1}\right)\right]^{0.5}}{V_{IN}} < \frac{I_{OUT1}}{2}$$

and is largest when $V_{IN} = 2V_{OUT1}$ (50% duty cycle).

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The frequency, V_{IN} to V_{OUT1} ratio, and maximum load current requirement of the LT3500 along with the input supply source impedance, determine the energy storage requirements of the input capacitor. Determine the worst-case condition for input ripple current and then size the input capacitor such that it reduces input voltage ripple to an acceptable level. Typical values for input capacitors run from 10µF at low frequencies to 2.2µF at higher frequencies. The combination of small size and low impedance (low equivalent series resistance or ESR) of ceramic capacitors make them the preferred choice. The low ESR results in very low voltage ripple and the capacitors can handle plenty of ripple current. They are also comparatively robust and can be used in this application at their rated voltage. X5R and X7R types are stable over temperature and applied voltage, and give dependable service. Other types (Y5V and Z5U) have very large temperature and voltage coefficients of capacitance, so they may have only a small fraction of their nominal capacitance in your application. While they will still handle the RMS ripple current, the input voltage ripple may become fairly large, and the ripple current may end up flowing from your input supply or from other bypass capacitors in your system, as opposed to being fully sourced from the local input capacitor. An alternative to a high value ceramic capacitor is a lower value along with a larger electrolytic capacitor, for example a 1µF ceramic capacitor in parallel with a low ESR tantalum capacitor. For the electrolytic capacitor, a value larger than 10µF will be required to meet the ESR and ripple current requirements. Because the input capacitor is likely to see high surge currents when the input source is applied, tantalum capacitors should be surge rated. The manufacturer may also recommend operation below the rated voltage of the capacitor. Be sure to place the 1µF ceramic as close as possible to the V_{IN} and GND pins on the IC for optimal noise immunity.

A final caution regarding the use of ceramic capacitors for input bypassing. A ceramic input capacitor can combine with stray inductance to form a resonant tank circuit. If power is applied quickly (for example, by plugging the circuit into a live power source) this tank can ring, doubling the input voltage and damaging the LT3500. The solution is to either clamp the input voltage or dampen the tank circuit by adding a lossy capacitor in parallel with the ceramic capacitor. For details see Application Note 88.

Output Capacitor Selection

Typically step-down regulators are easily compensated with an output crossover frequency that is 1/10 of the switching frequency. This means that the time that the output capacitor must supply the output load during a transient step is ~2 or 3 switching periods. With an allowable 5% drop in output voltage during the step, a good starting value for the output capacitor can be expressed by:

$$C_{VOUT1} = \frac{\text{Max Load Step}}{\text{Frequency} \bullet 0.05 \bullet V_{OUT1}}$$

Example:

V_{OUT1} = 3.3V, Frequency = 1MHz, Max Load Step = 2A

$$C_{VOUT1} = \frac{2}{1\text{MHz} \bullet 0.05 \bullet 3.3} = 12\mu\text{F}$$

The calculated value is only a suggested starting value. Increase the value if transient response needs improvement or reduce the capacitance if size is a priority. The output capacitor filters the inductor current to generate an output with low voltage ripple. It also stores energy in order to satisfy transient loads and to stabilize the LT3500's control loop. The switching frequency of the LT3500 determines

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the value of output capacitance required. Also, the current mode control loop doesn't require the presence of output capacitor series resistance (ESR). For these reasons, you are free to use ceramic capacitors to achieve very low output ripple and small circuit size. Estimate output ripple with the following equations:

$$V_{RIPPLE} = \frac{\Delta I_L}{8 \bullet Frequency \bullet C_{OUT1}}$$

For ceramic capacitors and,

$V_{RIPPLE} = \Delta I_L \bullet ESR$

For electrolytic (tantalum and aluminum)

where ΔI_L is the peak-to-peak ripple current in the inductor.

The RMS content of this ripple is very low, and the RMS current rating of the output capacitor is usually not of concern.

Another constraint on the output capacitor is that it must have greater energy storage than the inductor; if the stored energy in the inductor is transferred to the output, you would like the resulting voltage step to be small compared to the regulation voltage. For a 5% overshoot, this requirement becomes:

$$C_{OUT1} > 10 \bullet L \left(\frac{I_{LIM}}{V_{OUT1}} \right)^2$$

Finally, there must be enough capacitance for good transient performance. The last equation gives a good starting point. Alternatively, you can start with one of the designs in this data sheet and experiment to get the desired performance. This topic is covered more thoroughly in the section on loop compensation.

The high performance (low ESR), small size and robustness of ceramic capacitors make them the preferred type for LT3500 applications. However, all ceramic capacitors are not the same. As mentioned above, many of the high value capacitors use poor dielectrics with high temperature and voltage coefficients. In particular, Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and temperature extremes. Because the loop stability and transient response depend on the value of C_{OUT1}, you may not be able to tolerate this loss. Use X7R and X5R types. You can also use electrolytic capacitors. The ESRs of most aluminum electrolytics are too large to deliver low output ripple. Tantalum and newer, lower ESR organic electrolytic capacitors intended for power supply use, are suitable and the manufacturers will specify the ESR. The choice of capacitor value will be based on the ESR required for low ripple. Because the volume of the capacitor determines its ESR, both the size and the value will be larger than a ceramic capacitor that would give you similar ripple performance. One benefit is that the larger capacitance may give better transient response for large changes in load current.

Catch Diode

The diode D1 conducts current only during switch off time. Use a Schottky diode to limit forward voltage drop to increase efficiency. The Schottky diode must have a peak reverse voltage that is equal to regulator input voltage and sized for average forward current in normal operation. Average forward current can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT1}}{V_{IN}} \bullet \left(V_{IN} - V_{OUT1} \right)$$

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The only reason to consider a larger diode is the worst-case condition of a high input voltage and shorted output. With a shorted condition, diode current will increase to a typical value of 3A, determined by the peak switch current limit of the LT3500. This is safe for short periods of time, but it would be prudent to check with the diode manufacturer if continuous operation under these conditions can be tolerated.

BST Pin Considerations

The capacitor and diode tied to the BST pin generate a voltage that is higher than the input voltage. In most cases a 0.47µF capacitor and fast switching diode (such as the CMDSH-3 or FMMD914) will work well. Almost any type of film or ceramic capacitor is suitable, but the ESR should be <1Ω to ensure it can be fully recharged during the off time of the switch. The capacitor value can be approximated by:

$$C_{BST} = \frac{I_{OUT1(MAX)} \bullet DC}{50 \bullet \left(V_{OUT1} - V_{BST(MIN)}\right) \bullet f}$$

where $I_{OUT1(MAX)}$ is the maximum load current, and $V_{BST(MIN)}$ is the minimum boost voltage to fully saturate the switch.

Figure 5 shows four ways to arrange the boost circuit. The BST pin must be more than 2.2V above the SW pin for full efficiency.

Generally, for outputs of 3.3V and higher the standard circuit (Figure 5a) is the best. For outputs between 2.8V and 3.3V, replace the D2 with a small Schottky diode such as the PMEG4005.

For lower output voltages the boost diode can be tied to the input (Figure 5b). The circuit in Figure 5a is more efficient because the BST pin current comes from a lower voltage source.

Figure 5c shows the boost voltage source from the linear output that is set to greater than 2.5V (any available DC sources that are greater than 2.5V is sufficient). The highest efficiency is attained by choosing the lowest boost voltage above 2.5V. You must also be sure that the maximum voltage at the BST pin is less than the maximum specified in the Absolute Maximum Ratings section.

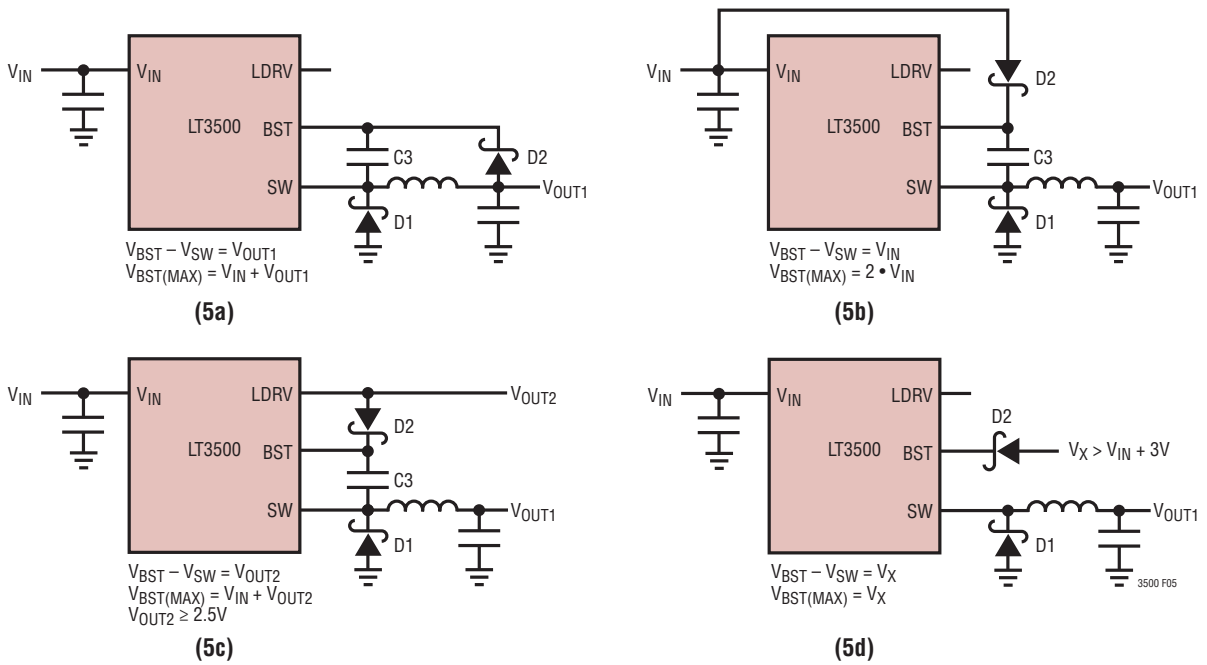

Figure 5. BST Pin Considerations

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The boost circuit can also run directly from a DC voltage that is higher than the input voltage by more than 2.5V, as in Figure 5d. The diode is used to prevent damage to the LT3500 in case V_X is held low while V_{IN} is present. The circuit eliminates a capacitor, but efficiency may be lower and dissipation in the LT3500 may be higher. Also, if V_X is absent, the LT3500 will still attempt to regulate the output, but will do so with very low efficiency and high dissipation because the switch will not be able to saturate, dropping 1.5V to 2V in conduction.

The minimum input voltage of an LT3500 application is limited by the minimum operating voltage (<2.8V) and by the maximum duty cycle as outlined above. For proper start-up, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, or the LT3500 is turned on with its SS pin when the output is already in regulation, then the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages and on the arrangement of the boost circuit.

The Typical Performance Characteristics section shows plots of the minimum load current to start and to run as a function of input voltage for 3.3V and 5V outputs. In many cases the discharged output capacitor will present a load to the switcher which will allow it to start. The plots show the worst-case situation where V_{IN} is ramping very slowly. Use a Schottky diode for the lowest start-up voltage.

Frequency Compensation

The LT3500 uses current mode control to regulate the output. This simplifies loop compensation. In particular, the LT3500 does not require the ESR of the output capacitor for stability so you are free to use ceramic capacitors to achieve low output ripple and small circuit size. Frequency compensation is provided by the components tied to the V_C pin. Generally a capacitor and a resistor in series to ground determine loop gain. In addition, there is a lower value capacitor in parallel. This capacitor is not part of the loop compensation but is used to filter noise at the switching frequency.

Loop compensation determines the stability and transient performance. Designing the compensation network is a bit complicated and the best values depend on the application and in particular the type of output capacitor. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature.

The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load.

Figure 6 shows an equivalent circuit for the LT3500 control loop. The error amp is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switch, and inductor, is modeled as a transconductance amplifier generating an output

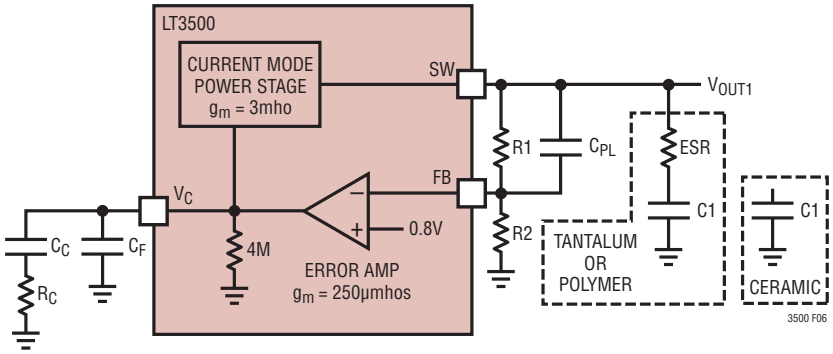

Figure 6. Model for Loop Response

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current proportional to the voltage at the V_C pin. Note that the output capacitor integrates this current, and that the capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. In most cases a zero is required and comes from either the output capacitor ESR or from a resistor in series with C_C. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor (C_{PL}) across the feedback divider may improve the transient response.

Synchronization

The R_T/SYNC pin can be used to synchronize the LT3500 to an external clock source. Driving the R_T/SYNC resistor with a clock source triggers the synchronization detection circuitry. Once synchronization is detected, the rising edge of SW will be synchronized to the rising edge of the R_T/SYNC pin signal. An AGC loop will adjust slope compensation to avoid subharmonic oscillation.

The synchronizing clock signal input to the LT3500 must have a frequency between 250kHz and 2.5MHz, a duty cycle between 20% and 80%, a low state below 0.5V and a high state above 1.6V. Synchronization signals outside of these parameters will cause erratic switching behavior. The R_T/SYNC resistor should be set such that the free running frequency ($(V_{RT/SYNC} – V_{SYNCLO})/R_{RT/SYNC}$) is approximately equal to the synchronization frequency. If the synchronization signal is halted, the synchronization detection circuitry will timeout in typically 10µs at which time the LT3500 reverts to the free-running frequency based on the current through R_T/SYNC. If the R_T/SYNC pin is held above 1.1V at any time, switching will be disabled.

If the synchronization signal is not present during regulator start-up (for example, the synchronization circuitry is powered from the regulator output) the R_T/SYNC pin must see an equivalent resistance to ground between 15k and 200k until the synchronization circuitry is active for proper start-up operation.

If the synchronization signal powers up in an undetermined state (V_{OL}, V_{OH}, Hi-Z), connect the synchronization clock to the LT3500 as shown in Figure 7. The circuit as shown will isolate the synchronization signal when the output voltage is below 90% of the regulated output. The LT3500 will start-up with a switching frequency determined by the resistor from the R_T/SYNC pin to ground.

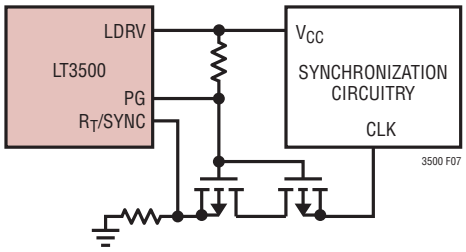


Figure 7. Synchronous Signal Powered from Regulator's Output

If the synchronization signal powers up in a low impedance state (V_{OL}), connect a resistor between the R_T/SYNC pin and the synchronizing clock. The equivalent resistance seen from the R_T/SYNC pin to ground will set the start-up frequency.

If the synchronization signal powers up in a high impedance state (Hi-Z), connect a resistor from the R_T/SYNC pin to ground. The equivalent resistance seen from the R_T/SYNC pin to ground will set the start-up frequency.

APPLICATIONS INFORMATION

If the synchronization signal changes between high and low impedance states during power up (V_{OL}, Hi-Z), connect the synchronization circuitry to the LT3500 as shown in the Typical Applications section. This will allow the LT3500 to start up with a switching frequency determined by the equivalent resistance from the R_T/SYNC pin to ground.

Shutdown and Undervoltage Lockout

Figure 8 shows how to add an undervoltage lockout (UVLO) to the LT3500. Typically, UVLO is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

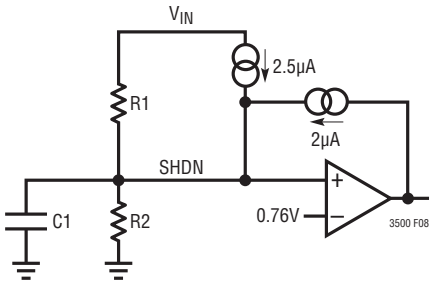


Figure 8. Undervoltage Lockout

An internal comparator will force the part into shutdown below the minimum V_{IN} of 2.8V. This feature can be used to prevent excessive discharge of battery-operated systems.

If an adjustable UVLO threshold is required, the SHDN pin can be used. The threshold voltage of the SHDN pin comparator is 0.76V. A 2.5µA internal current source defaults the open-pin condition to be operating (see Typical Performance Characteristics). Current hysteresis is added above the SHDN threshold. This can be used to set voltage hysteresis of the UVLO using the following:

$$R1 = \frac{V_H - V_L}{2\mu A}$$

$$R2 = \frac{0.76}{\frac{V_H - 0.76}{R1} + 2.5\mu A}$$

V_H = Turn-on threshold

V_L = Turn-off threshold

Example: switching should not start until the input is above 4.75V and is to stop if the input falls below 3.75V.

V_H = 4.75V

V_L = 3.75

$$R1 = \frac{4.75 - 3.75}{2\mu A} \sim 499k$$

$$R2 = \frac{0.76}{\frac{4.75 - 0.76}{499k} + 2.5\mu A} \sim 71.5k$$

Keep the connections from the resistors to the SHDN pin short and make sure that the interplane or surface capacitance to switching nodes is minimized. If high resistor values are used, the SHDN pin should be bypassed with a 1nF capacitor to prevent coupling problems from the switch node.

Soft-Start

The outputs of the LT3500 regulate to either the SS pin voltage minus 100mV or an internally regulated 800mV, whichever is lowest. A capacitor from the SS pin to ground is charged by an internal 2.75µA current source resulting in a linear output ramp from 0V to the regulated output whose duration is given by:

$$t_{RAMP} = \frac{C_{SS} \bullet 0.9V}{2.75\mu A}$$

APPLICATIONS INFORMATION

At power-up, a reset signal sets the soft-start latch and discharges the SS pin to approximately 0V to ensure proper start-up. When the SS pin is fully discharged the latch is reset and the internal 2.75µA current source starts to charge the SS pin.

When the SS pin voltage is below 100mV, the V_C pin is pulled low which disables switching. As the SS pin voltage rises above 100mV, the V_C pin is released and the outputs are regulated to the SS voltage. When the SS pin voltage minus 100mV exceeds the internal 0.8V reference, the outputs are regulated to the reference. The SS pin voltage will continue to rise until it is clamped at 2V.

In the event of a V_{IN} undervoltage lockout, the SHDN pin driven below 0.8V, or the internal die temperature exceeding its maximum rating during normal operation, the soft-start latch is set, triggering a start-up sequence.

In addition, if the load exceeds the maximum output switch current (switching regulator only), the output will start to drop causing the V_C pin clamp to be activated. As long as the V_C pin is clamped, the SS pin will be discharged. As a result, the output will be regulated to the highest voltage that the maximum output current can support. For example, if a 6V output is loaded by 1Ω the SS pin will drop to 0.5V, regulating the output at 3V (typical current limit time load, 3A • 1Ω). Once the overload condition is removed, the output will soft-start from the temporary voltage level to the normal regulation point.

Since the SS pin is clamped at 2V and has to discharge to 0.9V before taking control of regulation, momentary overload conditions will be tolerated without a soft-start recovery. The typical time before the SS pin takes control is:

$$t_{SS(CONTROL)} = \frac{C_{SS} \bullet 1.1V}{600\mu A}$$

Power Good Indicators

The PG and $\overline{PG}$ pins are collector outputs of an internal comparator. The comparator compares the voltages of the FB and LFB pins to 90% of the reference voltage with 30mV of hysterisis.

The PG pin has a sink capability of 400µA when the FB and LFB pins are below the threshold and can withstand 40V when the outputs are in regulation. The PG pin is typically connected to the output with a resistor and is used as an error flag. The resistor value should be chosen to allow the PG voltage to drop below 0.4V in an error condition.

Example:

V_{OUT1} = 5V, $PGSINK_{(MIN)}$ = 200µA

R_{PG} = (5 – 0.4)/200µA = 23kΩ

The $\overline{PG}$ pin has a sink capability of 800µA when the FB and LFB pins are above the threshold and can withstand 40V when the outputs are not in regulation. The $\overline{PG}$ pin is typically used as a drive signal for an output disconnect device. The $\overline{PG}$ pull-up resistor should be sized in the same manner as the PG pull-up resistor.

Linear Regulator

The LT3500 contains an error amplifier and a NPN output device which can be configured as a linear regulator or as a linear regulator controller.

With the LFB and LDRV pins configured as shown in Figure 1, the LDRV pin outputs a regulated voltage with a typical current limit of 13mA.

The LDRV voltage is programmed with a resistor divider between the output and the LFB pin. Choose the 1% resistors according to:

$$R3 = R4\left(\frac{V_{LDRV}}{0.8V} - 1\right)$$

R4 should be 10.0k or less to avoid bias current errors. Reference designators refer to the Block Diagram in Figure 1.

The reference voltage for the linear regulator (LFB pin) will track the SS pin in the same manner as the FB pin of the switching regulator.

APPLICATIONS INFORMATION

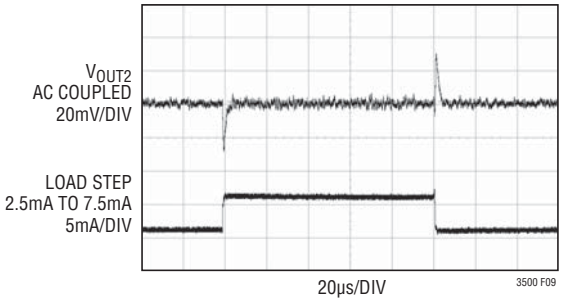


Figure 9. Linear Regulator Transient Response

To compensate the linear regulator, simply add a ceramic capacitor from the LDRV pin to ground. Typical values range from 0.01µF to 1µF. Figure 9 illustrates the transient response with a 0.47µF output capacitor.

Linear Controller

By adding an external follower (NPN or NMOS), the LFB and LDRV pins can be configured as a controller (Figure 10) for a low dropout regulator with increased output capability.

The output current capability of Figure 10's circuit is a product of the LDRV current limit and beta of the external NPN which is normally less than the current capability of the LT3500. The dropout voltage for the circuit is set by the saturation voltage of the external NPN, which is typically 300mV. The minimum V_{IN} for the circuit to function properly is 2V plus the base emitter drop of the external NPN.

Replacing the NPN in Figure 10 with a NMOS transistor can reduce the dropout voltage down to the $R_{DS(ON)}$ of the NMOS times the output current of the regulator. This also increases the overall efficiency of the system. However, the minimum V_{IN} increases to 2V plus the V_{GS} at full load of the transistor. Additionally, due to a lack of beta current limiting, a shorted output can cause the switcher output of the LT3500 to collapse.

Since the collector of the LDRV npn is connected internally to V_{IN}, you must consider the impact of LDRV current on efficiency and die temperature when configuring the linear regulator/controller. For example, with V_{IN} = 25V, LDRV = 3.3V and I_{LDRV} = 10mA, power dissipation on the die will be 217mW. For a typical 3.3V/1A switcher application, this represents an additional 7% efficiency loss and approximately 10 degrees rise in die temperature.

If the linear output of the LT3500 is not used, the LDRV pin should be shorted to the LFB Pin.

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board (PCB) layout. Figure 11 shows the high di/dt paths in the buck regulator circuit. Note that large switched currents flow in the power switch, the catch diode and the input capacitor. The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board and their connections should be made on that layer. Place a local, unbroken ground plane below these components, and tie this ground plane to system ground at one location, ideally at the ground terminal of the output

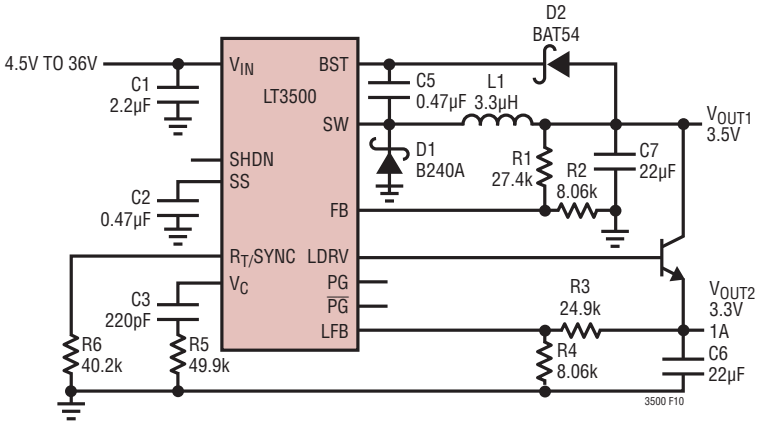
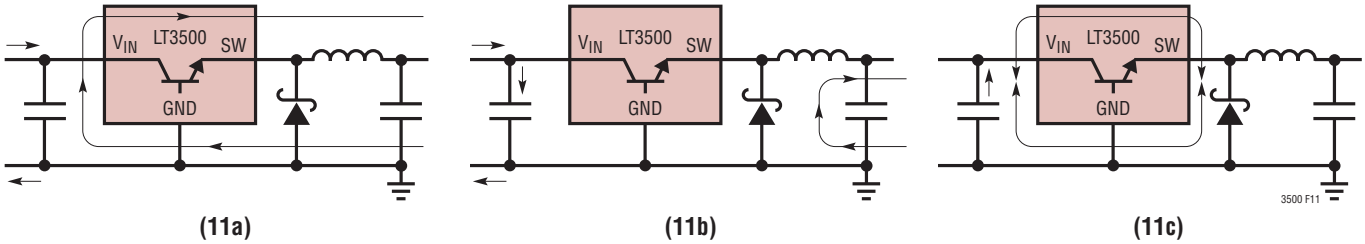


Figure 10. Linear Controller

APPLICATIONS INFORMATION



(11a) (11b) (11c)

Figure 11. Subtracting the Current when the Switch is On (11a) from the Current when the Switch is Off (11b) Reveals the Path of the High Frequency Switching Current (11c). Keep this Loop Small. The Voltage on the SW and BST Traces will Also be Switched; Keep These Traces as Short as Possible. Finally, Make Sure the Circuit is Shielded with a Local Ground Plane

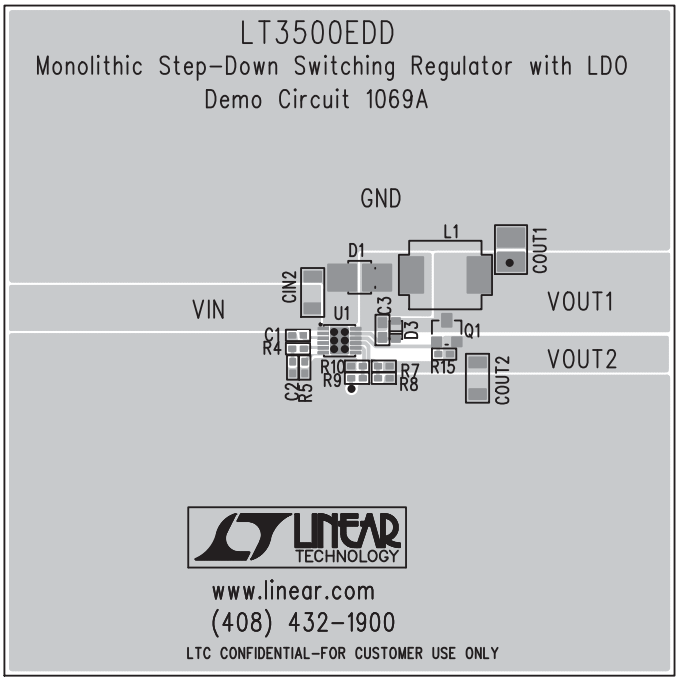


Figure 12. LT3500 Demonstration Circuit Board DC1069A

capacitor C2. Additionally, the SW and BST traces should be kept as short as possible. The topside metal from the DC1069A demonstration board in Figure 12 illustrates proper component placement and trace routing.

Thermal Considerations

The PCB must also provide heat sinking to keep the LT3500 cool. The exposed metal on the bottom of the package must be soldered to a ground plane. This ground should be tied to other copper layers below with thermal vias; these layers will spread the heat dissipated by the LT3500. Place additional vias near the catch diodes. Adding more copper to the top and bottom layers and tying this copper to the internal planes with vias can further reduce thermal resistance. With these steps, the thermal resistance from die (or junction) to ambient can be reduced to θ_{JA} = 45°C/W for the DD Package, and θ_{JA} = 45°C/W for the MSE Package.

Power dissipation within the LT3500 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the catch diode loss. The die temperature is calculated by multiplying the LT3500 power dissipation by the thermal resistance from junction to ambient.

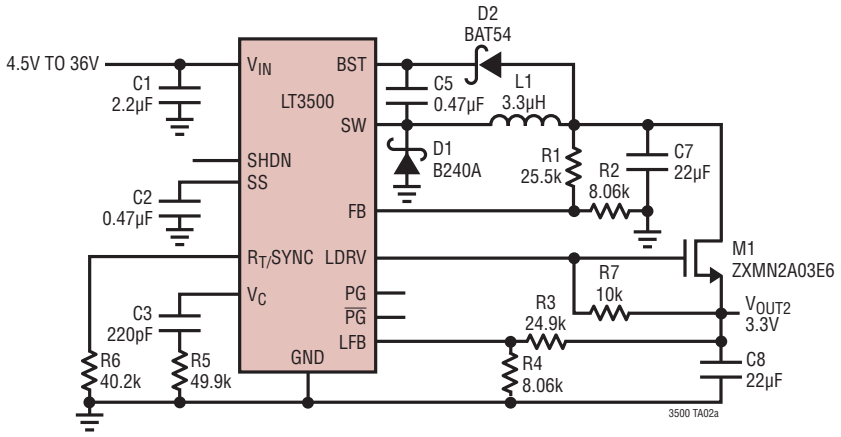
The power dissipation in the other power components such as catch diodes, boost diodes and inductors, cause additional copper heating and can further increase what the IC sees as ambient temperature. See the LT1767 data sheet's Thermal Considerations section.

Other Linear Technology Publications

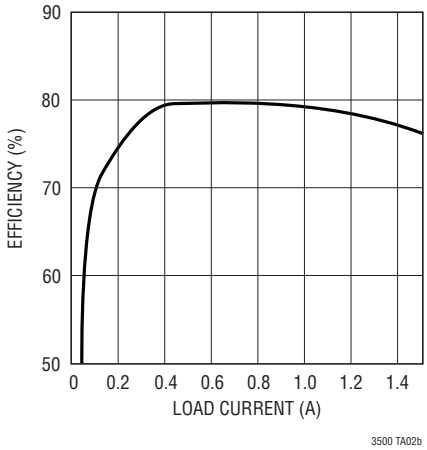
Application notes AN19, AN35 and AN44 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design note DN100 shows how to generate a dual (+ and –) output supply using a buck regulator.

TYPICAL APPLICATIONS

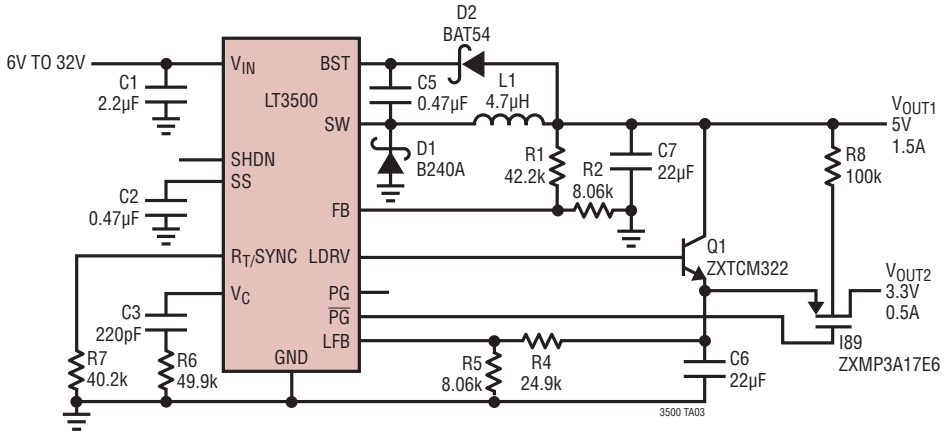
High Efficiency Linear Regulator



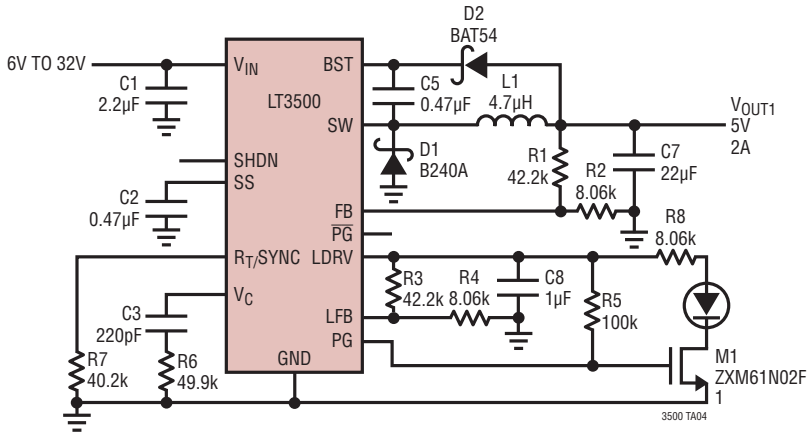
Efficiency vs Load Current



5V/1.5A, 3.3V/0.5A Step-Down with Output Disconnect

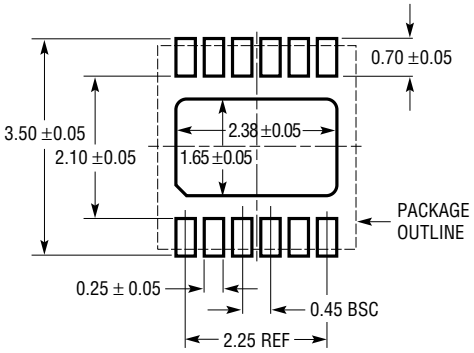


5V/2A Step-Down with Power Good LED

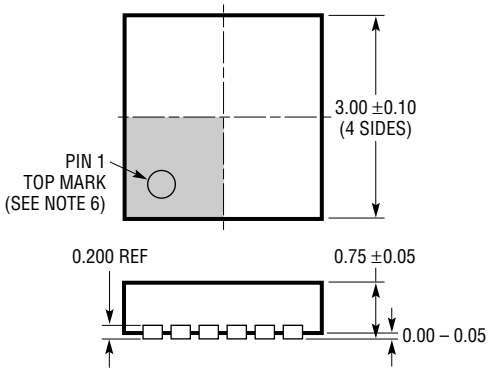


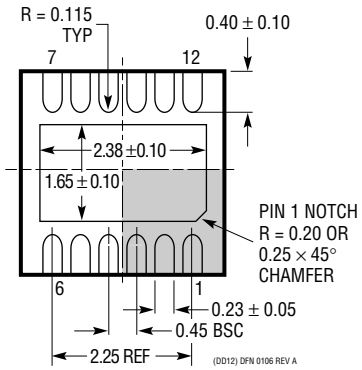
PACKAGE DESCRIPTION

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



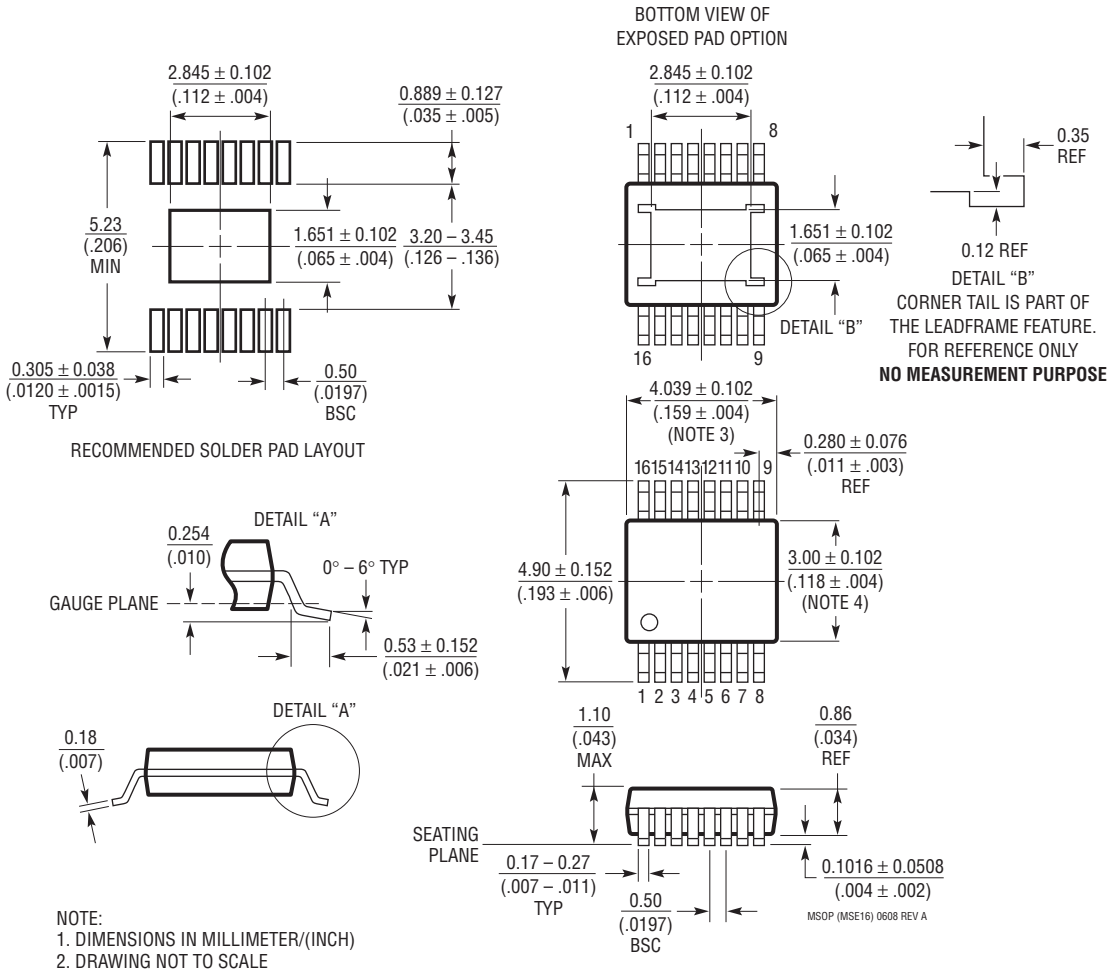


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev A)



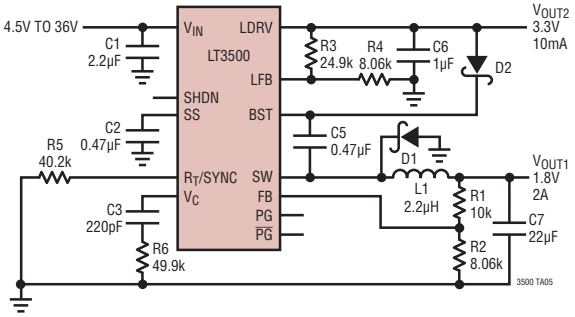
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	01/11	Corrected Pin Configuration for MSE package	2

TYPICAL APPLICATION

1.8V/2A Step-Down Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1766	60V, 1.2A (I_{OUT}), 200kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} = 25µA, 16-Lead TSSOPE Package
LT1933	36V, 500mA (I_{OUT}), 500kHz Step-Down Switching Regulator in SOT-23	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 1.6mA, I_{SD} < 1µA, ThinSOT™ Package
LT1936	36V, 1.4A (I_{OUT}), 500kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 1.9mA, I_{SD} < 1µA, 8-Lead MS8E Package
LT1940	Dual 25V, 1.4A (I_{OUT}), 1.1MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 25V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 3.8mA, I_{SD} < 30µA, 16-Lead TSSOPE Package
LTC3407/LTC3407-2	Dual 600mA/800mA, 1.5MHz/2.25MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, 3mm × 3mm DFN and 10-Lead MS10E Packages
LT3434/LT3435	60V, 2.4A (I_{OUT}), 200kHz/500kHz High Efficiency Step-Down DC/DC Converters with Burst Mode Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 100µA, I_{SD} < 1µA, 16-Lead TSSOPE Package
LT3437	60V, 400mA (I_{OUT}), Micropower Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.25V, I_Q = 100µA, I_{SD} < 1µA, 10-Lead 3mm × 3mm DFN, 16-Lead TSSOPE Package
LT3493	36V, 1.4A (I_{OUT}), 750kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.9mA, I_{SD} < 1µA, 6-Lead 2mm × 3mm DFN Package
LT3501	Dual 25V, 3A (I_{OUT}), 1.5MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.3V to 25V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 3.7mA, I_{SD} < 10µA, 20-Lead TSSOPE Package
LT3502/LT3502A	40V, 500mA (I_{OUT}), 1.1MHz/2.2MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 40V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.5mA, I_{SD} < 2µA, 8-Lead 2mm × 2mm DFN Package
LT3503	20V, 1A (I_{OUT}), 2.2MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 20V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 1.9mA, I_{SD} < 1µA, 6-Lead 2mm × 3mm DFN Package
LT3505	36V, 1.2A (I_{OUT}), 3MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 2mA, I_{SD} < 2µA, 8-Lead 3mm × 3mm DFN and MSE Packages
LT3506/LT3506A	Dual 25V, 1.6A (I_{OUT}), 575kHz/1.1MHz High Efficiency Step-Down DC/DC Converters	V_{IN}: 3.6V to 25V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 3.8mA, I_{SD} < 30µA, 16-Lead 4mm × 5mm DFN and TSSOPE Packages
LT3508	Dual 36V, 1.4A (I_{OUT}), 2.5MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 4.3mA, I_{SD} < 1µA, 24-Lead 4mm × 4mm QFN and 16-Lead TSSOPE Packages
LT3510	Dual 25V, 2A (I_{OUT}), 1.5MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.3V to 25V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 3.7mA, I_{SD} < 10µA, 20-Lead TSSOPE Package
LTC3548	Dual 400mA/800mA, 2.25MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, 3mm × 3mm DFN and 10-Lead MSE Packages
LT3680	36V, 3.5A (I_{OUT}), 2.4MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.79V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 3mm DFN and MS10E Packages

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