# 2MHz High Current 5-Output Regulator for TFT-LCD Panels

## FEATURES

- **4.5V to 30V Input Voltage Range**
- **Four Integrated Switches: 2.2A Buck, 1.5A Boost, 0.25A Boost, 0.25A Inverter (Guaranteed Minimum Current Limit)**
- **External NPN LDO Driver**
- **Fixed Frequency, Low Noise Outputs**
- **Inductor Current Sense for Buck**
- **Soft-Start for All Outputs**
- **Externally Programmable $V_{ON}$ Delay**
- Three Integrated Schottky Diodes
- $\overline{PGOOD}$ Pin for $AV_{DD}$ Output Disconnect
- PanelProtect™ Circuitry Disables $V_{ON}$ Upon Fault
- Thermally Enhanced 38-Lead 5mm × 7mm QFN Package

## APPLICATIONS

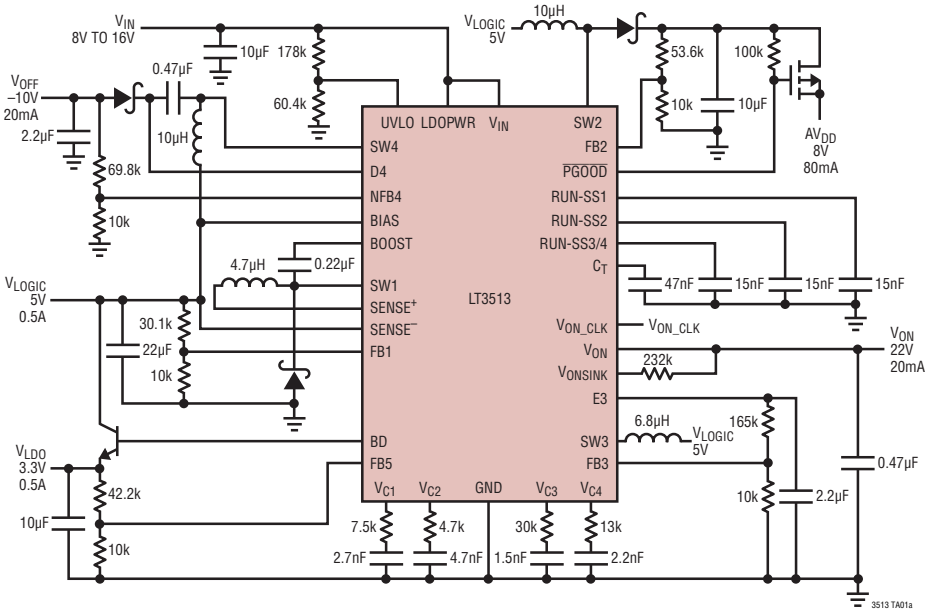
- Automotive TFT-LCD Displays
- Large TFT-LCD Desktop Monitors
- Flat Panel Televisions

## DESCRIPTION

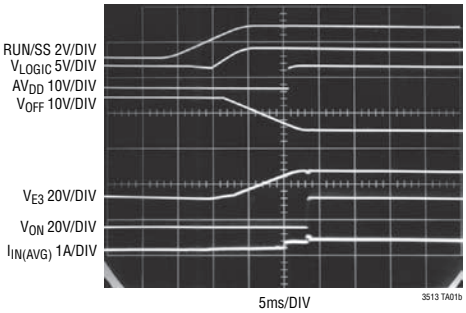
The LT®3513 5-output adjustable switching regulator provides power for large TFT-LCD panels. The 38-pin 5mm × 7mm QFN device can generate a 3.3V or 5V logic supply along with the triple output supply required for the TFT-LCD panel. A lower voltage secondary logic supply may also be generated with the addition of an external NPN driven by the internal linear regulator. A step-down regulator provides a low voltage output, $V_{LOGIC}$, with up to 1.2A of current while capable of operating from a wide input range of 4.5V to 30V. A high power step-up converter, a lower power step-up converter and an inverting converter provide the three independent output voltages: $AV_{DD}$, $V_{ON}$ and $V_{OFF}$ required by the LCD panel. A high-side PNP provides delayed turn-on of the $V_{ON}$ signal and can handle up to 30mA. Protection circuitry ensures that $V_{ON}$ is disabled if any of the four outputs are more than 10% below the programmed voltage.



## TYPICAL APPLICATION




**Start-Up Waveforms**

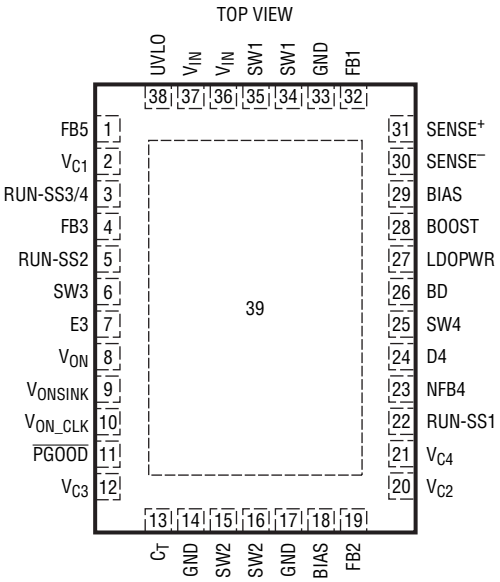


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$, LDOPWR Voltage ..... 32V
UVLO Voltage ..... 32V
SW2, SW3, SW4 Voltage ..... 40V
E3 Pin Voltage ..... 40V
$V_{ON}$, $V_{ONSINK}$ Voltage ..... 40V
PGOOD Voltage ..... 40V
D4 Voltage ..... 1V, –40V
BOOST Voltage ..... 37V
BOOST Over SW1 ..... 8V
SENSE+, SENSE– Voltage ..... 10V
$V_{ON\_CLK}$ Voltage ..... 10V
BIAS, BD Voltage ..... 10V
$C_T$ Pin Voltage ..... 5V
RUN-SS1, RUN-SS2, RUN-SS3/4 Voltage ..... 5V
FB1, FB2, FB3, FB5 Voltage ..... 5V
NFB4 Voltage ..... 5V, –5V
$V_{C1}$, $V_{C2}$, $V_{C3}$, $V_{C4}$ Voltage ..... 5V
Junction Temperature (Note 8) ..... 125°C
Operating Temperature Range (Note 2) .. –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C

## PIN CONFIGURATION




UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 34°C/W, $\theta_{JC}$ = 1°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LT3513EUHF#PBF | LT3513EUHF#TRPBF | 3513 | 38-Lead (5mm × 7mm) Plastic QFN | –40°C to 125°C |
| LT3513IUHF#PBF | LT3513IUHF#TRPBF | 3513 | 38-Lead (5mm × 7mm) Plastic QFN | –40°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 12V, BIAS = 3V, unless otherwise noted.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Minimum Input Voltage | | ● | | | 4.5 | V |
| Quiescent Current | Not Switching<br>$V_{RUNSS1}$ = 0V | | | 7.5<br>30 | 12<br>65 | mA<br>µA |
| RUN-SS1, RUN-SS2, RUN-SS3/4 Pin Current | RUN-SS1= RUN-SS2 = RUN-SS3 = RUN-SS4 = 0.4V | | | 2 | | µA |
| RUN-SS1, RUN-SS2, RUN-SS3/4 Threshold | | | | 0.8 | | V |
| BIAS Pin Voltage to Begin RUN-SS2, RUN-SS3/4 | | ● | | 2.25 | 2.7 | V |
| BIAS Pin Current | BIAS = 3.1V, All Switches Off | | | 16.5 | 20 | mA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 12V, BIAS = 3V, unless otherwise noted.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| FB Threshold Offset to Begin $C_T$ Charge | (Note 3) | | 90 | 125 | 160 | mV |
| $C_T$ Pin Current Source | All FB Pins = 1.5V, $C_T$ = 0.35V | | 16 | 20 | 25 | µA |
| $C_T$ Threshold to Power $V_{ON}$ | All FB Pins = 1.5V | | 1 | 1.1 | 1.2 | V |
| $V_{ON}$ Switch Drop | $V_{ON}$ Current = 30mA | | | 200 | 400 | mV |
| Maximum $V_{ON}$ Current | $V_{E3}$ = 30V | ● | 30 | 50 | | mA |
| $V_{ON\_CLK}$ Input Voltage High | | | 1.5 | | | V |
| $V_{ON\_CLK}$ Input Voltage Low | | | | | 0.3 | V |
| $V_{ONSINK}$ Voltage On | $V_{ONSINK}$ Current = 1µA | ● | | | 1.2 | V |
| Master Oscillator Frequency | | <br>● | 1.90<br>1.80 | 2 | 2.12<br>2.22 | MHz<br>MHz |
| Foldback Switching Frequency | FB2 = 0V, FB3 = 0V, NFB4 = 0V | | | 200 | | kHz |
| UVLO Pin Threshold | UVLO Pin Voltage Rising | | | 1.25 | | V |
| UVLO Pin Hysteresis Current | $V_{UVLO}$ = 1V | | 3.4 | 3.9 | 4.5 | µA |
| $\overline{PGOOD}$ Threshold Offset | | | 90 | 125 | 160 | mV |
| $\overline{PGOOD}$ Sink Current | $\overline{PGOOD}$ Connected to 40V Through 100k | | 4 | | | mA |
| $\overline{PGOOD}$ Pin Leakage | $V_{\overline{PGOOD}}$ = 40V | | | | 1 | µA |
| **Switch 1 (2.2A Buck)** | | | | | | |
| FB1 Voltage | | <br>● | 1.215<br>1.205 | 1.235 | 1.255<br>1.265 | V<br>V |
| FB1 Voltage Line Regulation | 4.5V < $V_{IN}$ < 30V | | | 0.01 | 0.03 | %/V |
| FB1 Pin Bias Current | (Note 4) | ● | | 30 | 200 | nA |
| Error Amplifier 1 Voltage Gain | | | | 250 | | V/V |
| Error Amplifier 1 Transconductance | ΔI = 10µA | | | 220 | | µmhos |
| Maximum Duty Cycle | | ● | 75 | 85 | | % |
| Switch 1 Current Limit | Duty Cycle = 35% (Note 6) | | 2.2 | 3 | 3.5 | A |
| Switch 1 $V_{CESAT}$ | $I_{SW}$ = 1.5A | | | 430 | | mV |
| Switch 1 Leakage Current | FB1 = 1.5V, RUN-SS1 = 0V | | | 0.1 | 10 | µA |
| Minimum BOOST Voltage Above SW1 Pin | $I_{SW}$ = 1.5A (Note 7) | | | 1.8 | 2.5 | V |
| BOOST Pin Current | $I_{SW}$ = 1.5A | | | 30 | 50 | mA |
| BOOST Schottky Diode Drop | I = 170mA | | | 700 | | mV |
| **Switch 2 (1.5A BOOST)** | | | | | | |
| FB2 Voltage | | <br>● | 1.20<br>1.19 | 1.22 | 1.24<br>1.25 | V<br>V |
| FB2 Voltage Line Regulation | 4.5V < $V_{IN}$ < 30V | | | 0.01 | 0.03 | %/V |
| FB2 Pin Bias Current | (Note 5) | ● | | 30 | 200 | nA |
| Error Amplifier 2 Voltage Gain | | | | 250 | | V/V |
| Error Amplifier 2 Transconductance | ΔI = 10µA | | | 220 | | µmhos |
| Switch 2 Current Limit | (Note 6) | | 1.5 | 1.85 | 2.4 | A |
| Switch 2 $V_{CESAT}$ | $I_{SW2}$ = 1.2A | | | 360 | | mV |
| Switch 2 Leakage Current | FB2 = 1.5V, RUN-SS1 = 0V | | | 0.1 | 1 | µA |
| BIAS Pin Current Due to SW2 | $I_{SW2}$ = 1.2A | | | 45 | | mA |
| Maximum Duty Cycle (SW2) | | ● | 75 | 90 | | % |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 12V, BIAS = 3V, unless otherwise noted.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Switch 3 (250mA BOOST)** | | | | | | |
| FB3 Voltage | | <br>● | 1.20<br>1.19 | 1.22 | 1.24<br>1.25 | V<br>V |
| FB3 Voltage Line Regulation | 4.5V < $V_{IN}$ < 30V | | | 0.01 | 0.03 | %/V |
| FB3 Pin Bias Current | (Note 4) | ● | | 30 | 200 | nA |
| Error Amplifier 3 Voltage Gain | | | | 250 | | V/V |
| Error Amplifier 3 Transconductance | ΔI = 10µA | | | 220 | | µmhos |
| Switch 3 Current Limit | (Note 6) | | 0.25 | 0.3 | 0.38 | A |
| Switch 3 $V_{CESAT}$ | $I_{SW3}$ = 0.2A | | | 200 | | mV |
| Switch 3 Leakage Current | FB3 = 1.5V, RUN-SS1 = 0V | | | 0.1 | 1 | µA |
| BIAS Pin Current Due to SW3 | $I_{SW3}$ = 0.2A | | | 18 | | mA |
| Maximum Duty Cycle (SW3) | | ● | 84 | 88 | | % |
| Schottky Diode Drop | I = 170mA | | | 900 | | mV |
| **Switch 4 (250mA Inverter)** | | | | | | |
| NFB4 Voltage | | <br>● | –1.205<br>–1.215 | –1.180 | –1.155<br>–1.145 | V<br>V |
| NFB4 Voltage Line Regulation | 4.5V < $V_{IN}$ < 30V | | | 0.01 | 0.03 | %/V |
| NFB4 Pin Bias Current | (Note 4) | ● | | 5 | 16 | µA |
| Error Amplifier 4 Voltage Gain | | | | 200 | | V/V |
| Error Amplifier 4 Transconductance | ΔI = 10µA | | | 220 | | µmhos |
| Switch 4 Current Limit | (Note 6) | | 0.25 | 0.3 | 0.40 | A |
| Switch 4 $V_{CESAT}$ | $I_{SW4}$ = 0.2A | | | 200 | | mV |
| Switch 4 Leakage Current | NFB4 = –1.5V, RUN-SS1 = 0V | | | 0.1 | 1 | µA |
| BIAS Pin Current Due to SW4 | $I_{SW4}$ = 0.2A | | | 18 | | mA |
| Maximum Duty Cycle (SW4) | | | 84 | 88 | | % |
| Schottky Diode Drop (D4) | I = 170mA | | | 700 | | mV |
| **NPN LDO** | | | | | | |
| FB5 Voltage | | <br>● | 0.61<br>0.6 | 0.625 | 0.63<br>0.65 | V<br>V |
| FB5 Pin Bias Current | (Note 4) | ● | | 30 | 200 | nA |
| Base Drive Current | FB5 = 0.5V | | 6 | 8 | 10 | mA |
| LDOPWR Minimum Voltage | BD = 3.5V | | 4.5 | | | V |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LT3513E is guaranteed to meet specified performance from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3513I is guarenteed over the full –40°C to 125°C operating junction temperature range.

**Note 3:** The $C_T$ pin is held low until FB1, FB2, FB3 and NFB4 all ramp above the FB threshold offset.

**Note 4:** Current flows out of FB1, FB3, NFB4 and FB5.

**Note 5:** Current may flow in or out of FB2. The absolute value of this test is used.

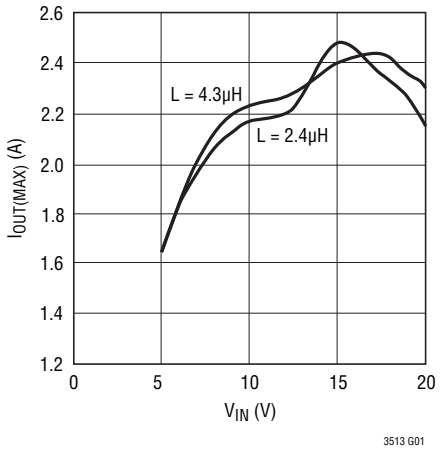
**Note 6:** Current limit is guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles.

**Note 7:** This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

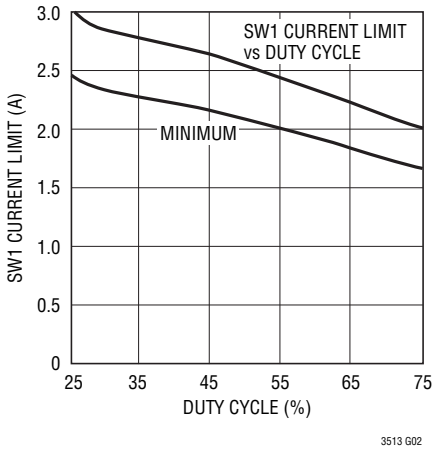
**Note 8:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature range when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

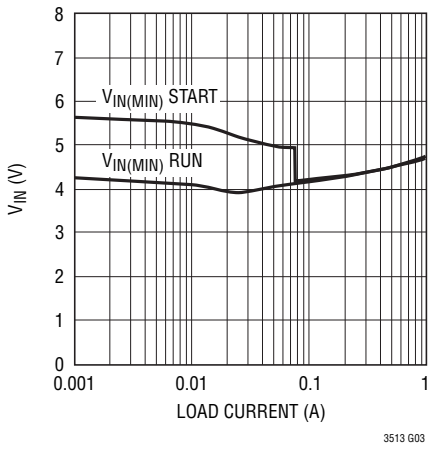
### Maximum Output Current for $V_{LOGIC}$ = 3.3V



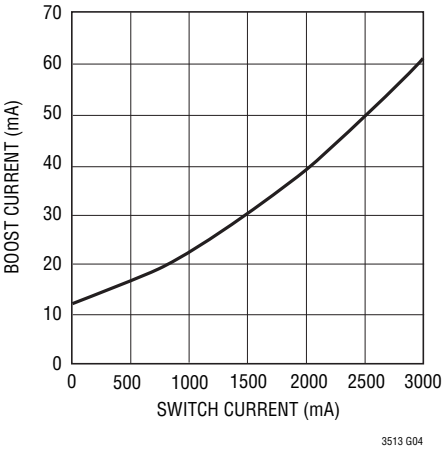

### SW1 Current Limit vs Duty Cycle



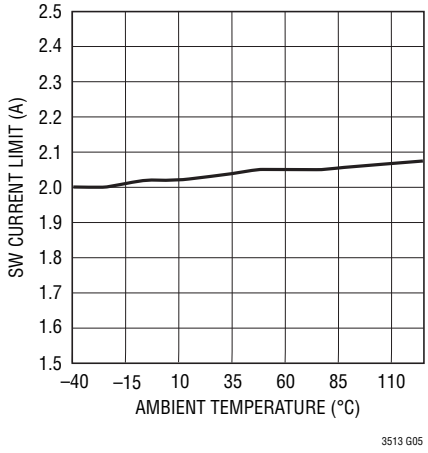

### Start and Run $V_{LOGIC}$ = 3.3V



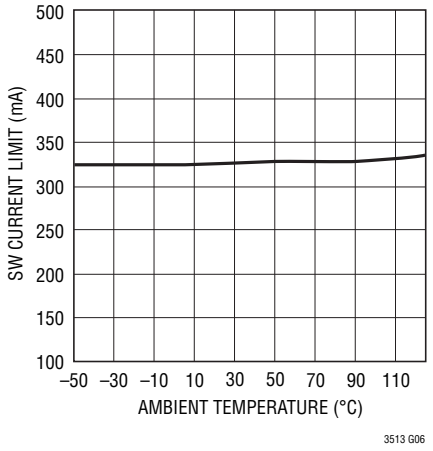

### BOOST Pin Current



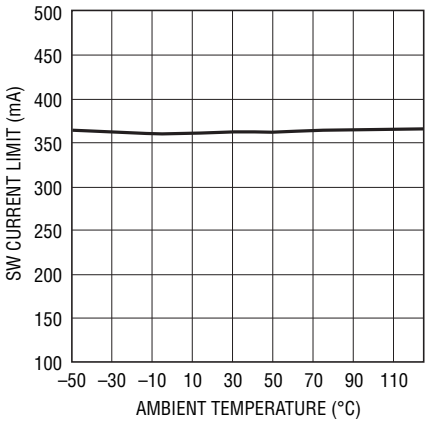

### SW2 Current Limit



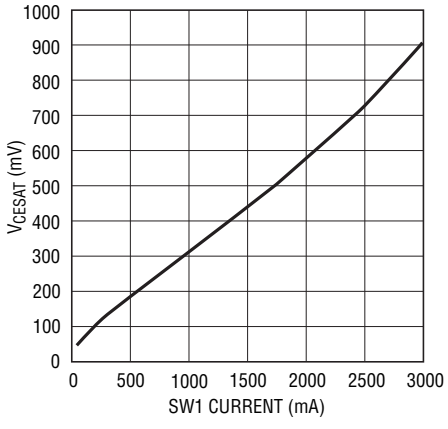

### SW3 Current Limit



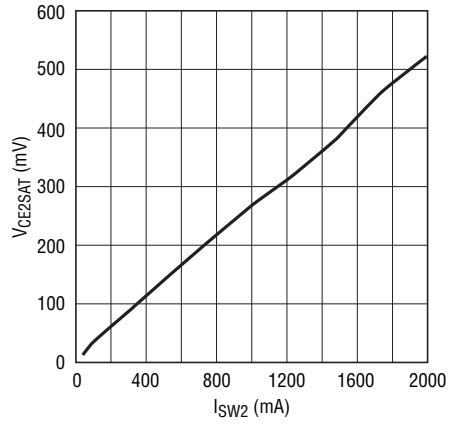

### SW4 Current Limit




### SW1 $V_{CESAT}$

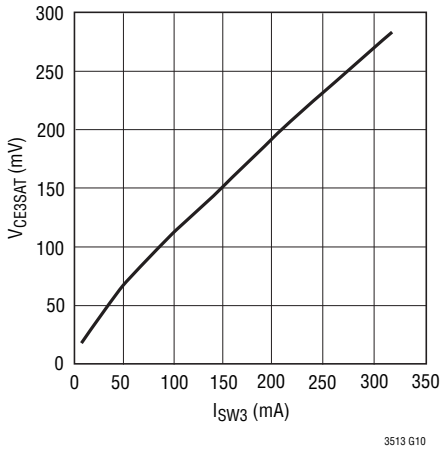



### SW2 $V_{CESAT}$

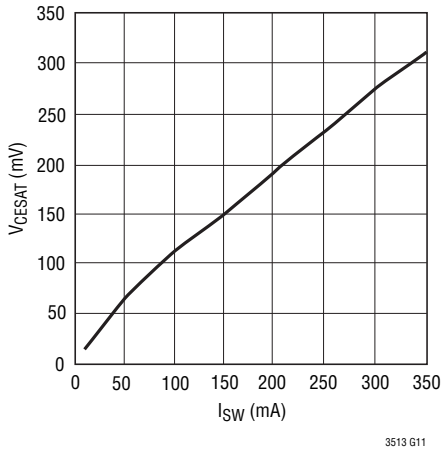


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

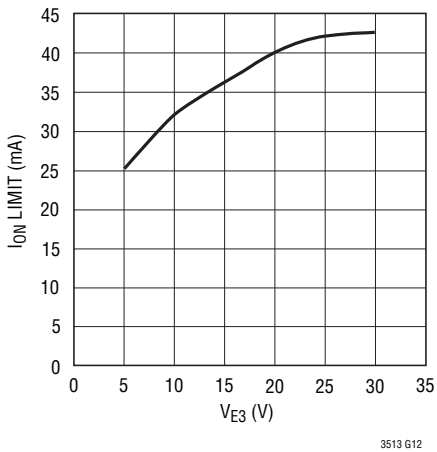
**SW3 $V_{CESAT}$**



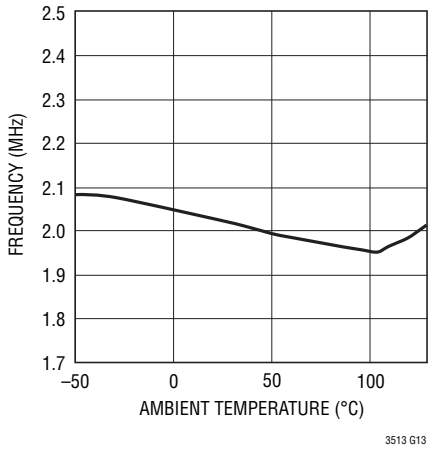

**SW4 $V_{CESAT}$**



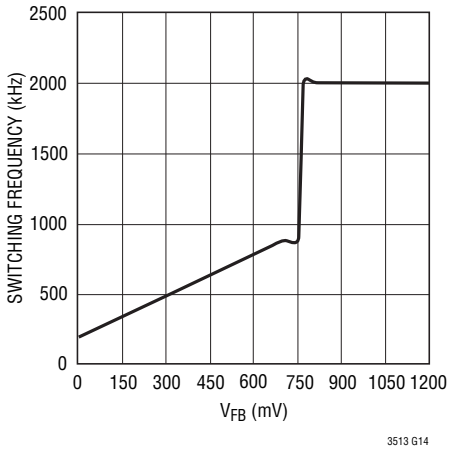

**$V_{ON}$ Current Limit**



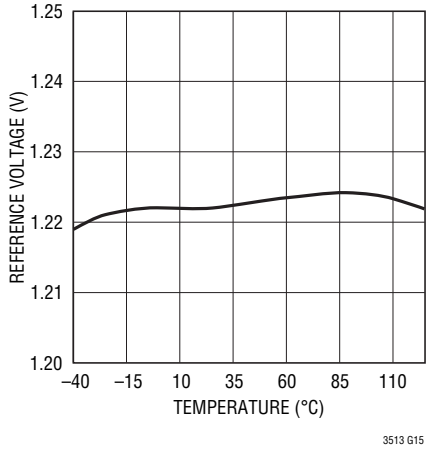

**Oscillator Frequency**




**Frequency Foldback**



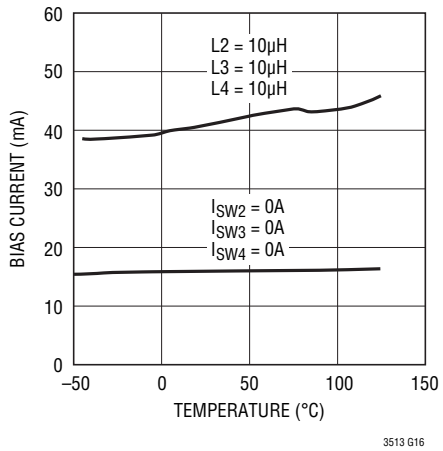

**Reference Voltage**



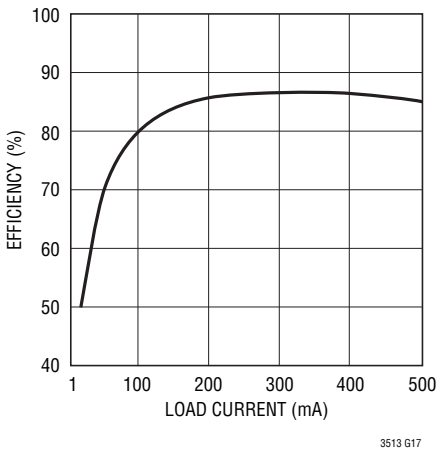
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

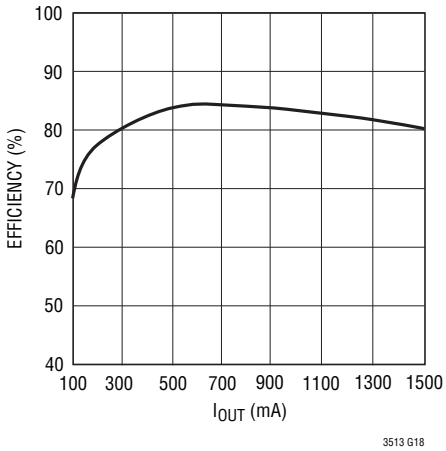
### BIAS Pin Current



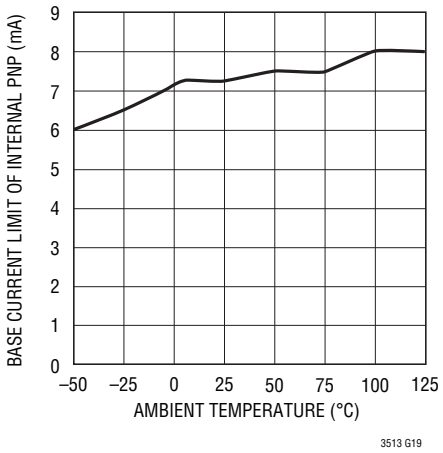

### Efficiency, $AV_{DD}$ = 13V



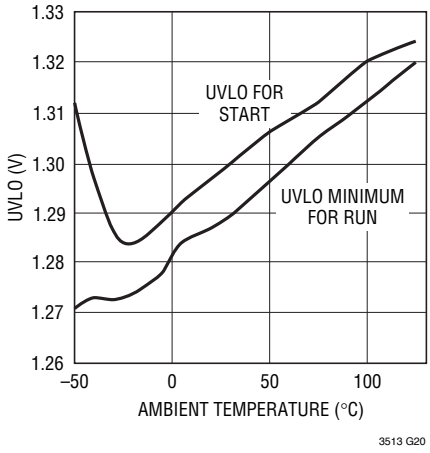

### Efficiency, $V_{LOGIC}$ = 5V



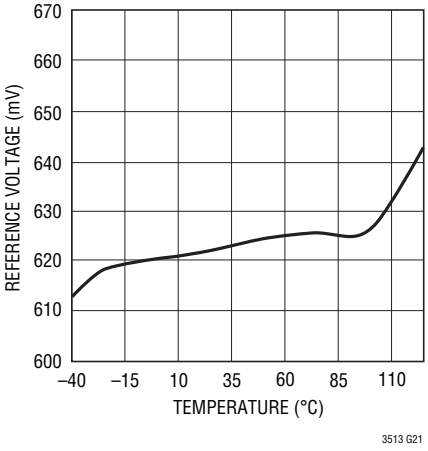

### LDO Current Limit vs Temperature




### $V_{UVLO}$ vs Temperature




### Reference Voltage for FB5, LDO



## PIN FUNCTIONS

**FB5 (Pin 1):** Feedback Pin. Tie the resistor tap to this pin and set the output of the LDO according to $V_{LDO}$ = 0.625 • (1 + R14/R15). Reference designators refer to Figure 1.

**$V_{C1}$ (Pin 2):** Control Voltage and Compensation Pin for Internal Error Amplifier. Connect a series RC from this pin to ground to compensate switching regulator 1.

**RUN-SS3/4 (Pin 3):** Run/Soft-Start Pin. This is the soft-start pin for switching regulators 3 and 4. Place a soft-start capacitor here to limit start-up inrush current and output voltage ramp rate. When the BIAS pin reaches 2.25V, a 2µA current source charges the capacitor. When the voltage at this pin reaches 0.8V, switches 3 and 4 turn on and begin switching. For slower start-up use a larger capacitor. For complete shutdown tie RUN-SS3/4 to ground.

**FB3 (Pin 4):** Feedback Pin. Tie the resistor tap to this pin and set $V_{ON}$ according to $V_{ON}$ = 1.22V • (1 + R8/R9) – 150mV. Reference designators refer to Figure 1.

**RUN-SS2 (Pin 5):** Run/Soft-Start Pin. This is the soft-start pin for switching regulator 2. Place a soft-start capacitor here to limit start-up inrush current and output voltage ramp rate. When the BIAS pin reaches 2.25V, a 2µA current source charges the capacitor. When the voltage at this pin reaches 0.8V, switch 2 turns on and begins switching. For slower start-up use a larger capacitor. For complete shutdown tie RUN-SS2 to ground.

**SW3 (Pin 6):** Switch Node. The SW3 pin is the collector of the internal NPN bipolar transistor for switching regulator 3. Minimize trace area at this pin to keep EMI down.

**E3 (Pin 7):** This is switching regulator 3's output and the emitter of the output disconnect PNP. Tie the output capacitor and resistor divider here.

**$V_{ON}$ (Pin 8):** This is the delayed output for switching regulator 3. $V_{ON}$ reaches its programmed voltage after the internal $C_T$ timer times out. Protection circuitry ensures $V_{ON}$ is disabled if any of the four outputs are more than 10% below normal voltage. This output is also disabled when $V_{ON\_CLK}$ is high.

**$V_{ONSINK}$ (Pin 9):** This is an open-collector output controlled by the $V_{ON\_CLK}$ pin. When $V_{ON\_CLK}$ is low, this pin draws no current and when $V_{ON\_CLK}$ is high, this pin draws current.

**$V_{ON\_CLK}$ (Pin 10):** This pin controls the output disconnect device and the open collector of $V_{ONSINK}$. When this pin is low, the $V_{ON}$ pin is enabled and the $V_{ONSINK}$ pin is a high impedance. When this pin is high, the $V_{ON}$ pin is disabled and the $V_{ONSINK}$ pin sinks current to ground.

**$\overline{\text{PGOOD}}$ (Pin 11):** Power Good Comparator Output. This is the open collector output of the power good comparator and can be used in conjunction with an external P-channel MOSFET to provide output disconnect for $AV_{DD}$ as shown in Figure 2. When switcher 2's output reaches approximately 90% of its programmed voltage, $\overline{\text{PGOOD}}$ will be pulled to ground. This will pull down on the gate of the MOSFET, connecting $AV_{DD}$. A 100k pull-up resistor between the source and the gate of the P-channel MOSFET keeps it off when switcher 2's output is low.

**$V_{C3}$ (Pin 12):** Control Voltage and Compensation Pin for Internal Error Amplifier. Connect a series RC from this pin to ground to compensate switching regulator 3.

**$C_T$ (Pin 13):** Timing Capacitor Pin. This is the input to the $V_{ON}$ timer and programs the time delay from all four feedback pins reaching 1.125V to $V_{ON}$ turning on. The $C_T$ capacitor value can be set using the equation C = (20µA • $t_{DELAY}$)/1.1V.

**GND (Pins 14, 17, 33):** Ground.

**SW2 (Pins 15, 16):** Switch Node. The SW2 pin is the collector of the internal NPN bipolar transistor for switching regulator 2. Minimize trace area at this pin to keep EMI down.

**BIAS (Pins 18, 29):** The BIAS pin is used to improve efficiency when operating at higher input voltages. Connecting this pin to the output of switching regulator 1 forces most of the internal circuitry to draw its operating current from $V_{LOGIC}$ rather than $V_{IN}$. The drivers of switches 2, 3 and 4 and the LDO are supplied by BIAS. Switches 2, 3 and 4 and the LDO will not function until the BIAS pin reaches approximately 2.7V. Both BIAS pins must be tied to $V_{LOGIC}$.

**FB2 (Pin 19):** Feedback Pin. Tie the resistor divider tap to this pin and set $AV_{DD}$ according to $AV_{DD}$ = 1.22V • (1 + R5/R6). Reference designators refer to Figure 2.

## PIN FUNCTIONS

**$V_{C2}$ (Pin 20):** Control Voltage and Compensation Pin for Internal Error Amplifier. Connect a series RC from this pin to ground to compensate switching regulator 2.

**$V_{C4}$ (Pin 21):** Control Voltage and Compensation Pin for Internal Error Amplifier. Connect a series RC from this pin to ground to compensate switching regulator 4.

**RUN-SS1 (Pin 22):** Run/Soft-Start Pin. This is the soft-start pin for switching regulator 1. Place a soft-start capacitor here to limit start-up inrush current and output voltage ramp rate. When power is applied to the $V_{IN}$ pin, a 2µA current source charges the capacitor. When the voltage at this pin reaches 0.8V, switch 1 turns on and begins switching. For slower start-up use a larger capacitor. For complete shutdown tie RUN-SS1 to ground.

**NFB4 (Pin 23):** Negative Feedback Pin. Tie the resistor divider tap to this pin and set $V_{OFF}$ according to $V_{OFF} = -1.18 \bullet (1 + R3/R4)$. Reference designators refer to Figure 2.

**D4 (Pin 24):** Internal Schottky Diode Pin. This pin is the anode of an internal Schottky diode with the other end connected to ground. This Schottky diode is used in generating the $V_{OFF}$ output.

**SW4 (Pin 25):** Switch Node. The SW4 pin is the collector of the internal NPN bipolar transistor for switching regulator 4. Minimize trace area at this pin to keep EMI down.

**BD (Note 26):** NPN LDO Base Drive. This pin controls the base of the external NPN LDO transistor.

**LDOPWR (Pin 27):** Input Voltage for LDO Driver. This pin supplies the current for the NPN LDO base. This pin can be connected to $V_{IN}$. To save power at high $V_{IN}$ voltages, the pin can alternatively be connected to the $AV_{DD}$ supply.

**BOOST (Pin 28):** The BOOST pin is used to provide a drive voltage higher than $V_{IN}$ to the switch 1 drive circuit. An internal Schottky diode is connected between BIAS and BOOST. A capacitor needs to be connected between BOOST and SW1.

**$SENSE^-$ (Pin 30)** Negative Current Sense Input. This pin (along with the $SENSE^+$ pin) is used to sense the inductor current for the buck switching regulator.

**$SENSE^+$ (Pin 31)** Positive Current Sense Input. This pin (along with the $SENSE^-$ pin) is used to sense the inductor current for the buck switching regulator.

**FB1 (Pin 32):** Feedback Pin. Tie the resistor divider tap to this pin and set $V_{LOGIC}$ according to $V_{LOGIC} = 1.235V \bullet (1 + R1/R2)$. Reference designators refer to Figure 2.

**SW1 (Pins 34, 35):** Switch Node. The SW1 pins are the emitter of the internal NPN bipolar power transistor for switching regulator 1. These points must be tied together for proper operation. Connect these pins to the inductor, catch diode and boost capacitor.

**$V_{IN}$ (Pins 36, 37):** Input Voltage. This pin supplies current to the internal circuitry of the LT3513. This pin must be locally bypassed with a capacitor.

**UVLO (Pin 38):** Undervoltage Lockout. A resistor divider connected to $V_{IN}$ is tied to this pin to program the minimum input voltage at which the LT3513 will operate. This pin is compared to the internal 1.25V reference. When UVLO is less than 1.25V, the switching regulators are not allowed to operate (the RUN/SS pins are still used to turn on each switching regulator). When this pin falls below 1.25V, 3.9µA will be pulled from the pin to provide programmable hysteresis for UVLO.

**Exposed Pad (Pin 39):** Ground. The Exposed Pad of the package provides both electrical contact to ground and good thermal contact to the printed circuit board. The Exposed Pad must be soldered to the circuit board for proper operation.

## BLOCK DIAGRAM

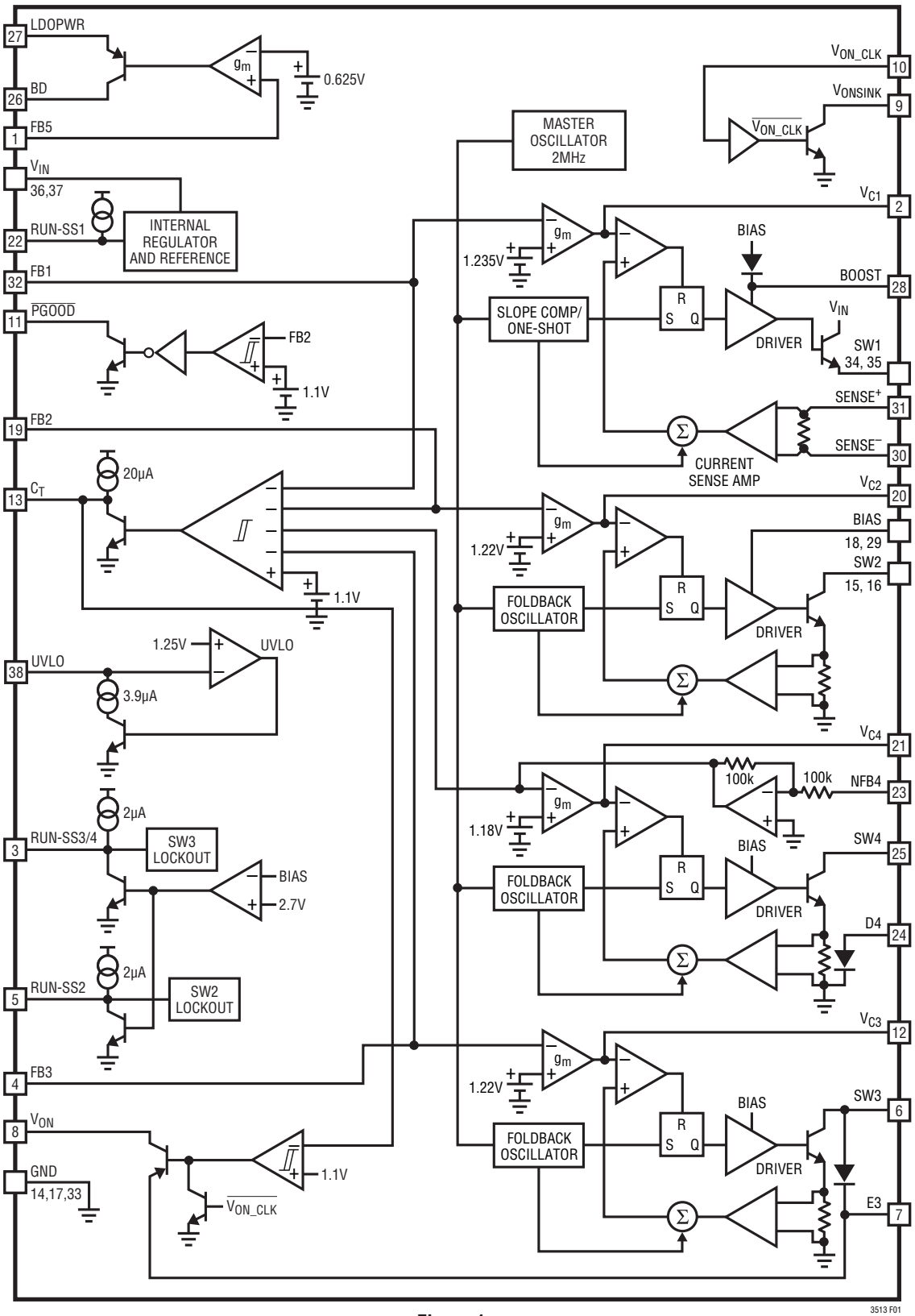
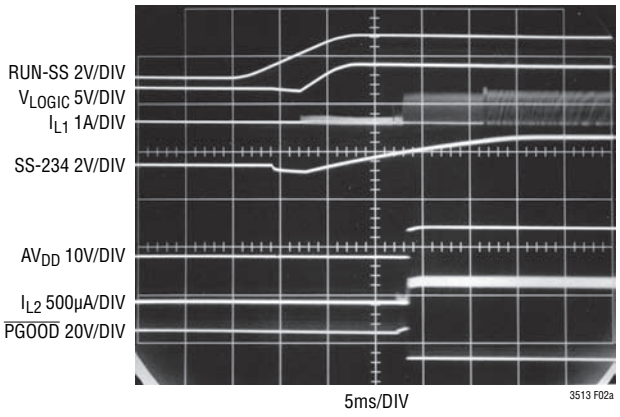



**Figure 1**

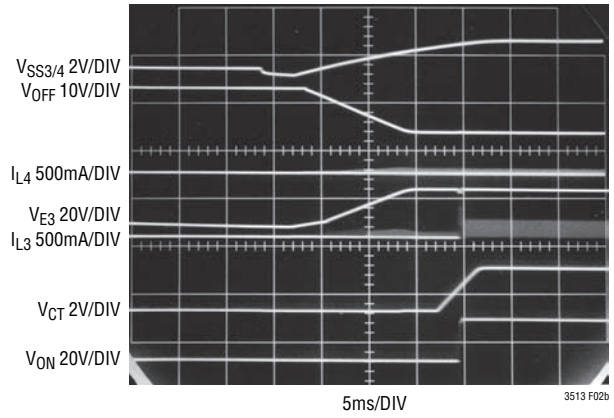
## OPERATION

The LT3513 is a highly integrated power supply IC containing four separate switching regulators and a low dropout linear regulator (LDO). Switching regulator 1 is a step-down 2.2A regulator with inductor current sense and an integrated boost Schottky diode. Switching regulator 2 can be configured as a step-up or SEPIC converter and has a 1.5A switch. Switching regulator 3 consists of a step-up regulator with a 0.25A switch as well as an integrated Schottky diode. Switching regulator 4 is a negative regulator with a switch current limit of 0.25A and an integrated Schottky diode. Linear regulator 5 is capable of providing 8mA of current to the base of an external NPN transistor. The regulators share common circuitry including input source, voltage reference and master oscillator. Operation can be best understood by referring to the Block Diagram as shown in Figure 1.

If the RUN-SS1 pin is pulled to ground, the LT3513 is shut down and draws 30µA from the input source tied to $V_{IN}$. An internal 2µA current source charges the external soft-start capacitor, generating a voltage ramp at this pin. If the RUN-SS1 pin exceeds 0.8V, the internal bias circuits turn on, including the internal regulator, reference and 2MHz master oscillator. The master oscillator generates four clock signals, one for each of the switching regulators. Switching regulator 1 will only begin to operate when the RUN-SS1 pin reaches 0.8V. Switcher 1 generates $V_{LOGIC}$, which must be tied to the BIAS pin. When BIAS reaches 2.8V, the NPNs pulling down on the RUN-SS2 and RUN-SS3/4 pins turns off, allowing an internal 2µA current source to charge the external capacitors tied to RUN-SS2 and RUN-SS3/4 pins. When the voltage on RUN-SS2 reaches 0.8V, switcher 2 is enabled. Correspondingly, when the voltage on RUN-SS3/4 reaches 0.8V, switchers 3 and 4 are enabled. $AV_{DD}$, E3 and $V_{OFF}$ will then begin rising at a rate determined by the capacitors tied to the RUN-SS2 and RUN-SS3/4 pins. When all four switching outputs reach 90% of their programmed voltages, the NPN pulling down on the $C_T$ pin will turn off, and an internal 20µA current source will charge the external capacitor tied to the $C_T$ pin. When the $C_T$ pin reaches 1.1V, the output disconnect PNP turns on, connecting $V_{ON}$ to E3. In the event of any of the four outputs dropping below 90% of their programmed voltage, PanelProtect circuitry pulls the $C_T$ pin to GND, disabling $V_{ON}$.




**(2a)**




**(2b)**

**Figure 2. LT3513 Power-Up Sequence. (Traces from Both Photos are Synchnonized to the Same Trigger)**

## OPERATION

A power good comparator monitors $AV_{DD}$ and turns on when FB2 is at or above 90% of its regulated value. The output is an open-collector transistor that is off when the output is out of regulation, allowing an external resistor to pull the pin high. This pin can be used with a P-channel MOSFET that functions as an output disconnect for $AV_{DD}$.

The four switchers are current mode regulators. Instead of directly modulating the duty cycle of the power switch, the feedback loop controls the peak current in the switch during each cycle. Compared to voltage mode control, current mode control improves loop dynamics and provides cycle-by-cycle current limit.

All four switchers employ a constant-frequency current mode control scheme. Switcher 1, the step-down regulator, differs slightly from the others with inductor current sense. Instead of monitoring the current at the switch, current nodes are used to measure the current through the inductor. Inductor current sense does not suffer from minimum on-time problems, therefore always keeping the switch current limited with any input-to-output voltage ratio. Switcher 1 is always synchronized to the master oscillator. The other three switchers each have their own slave oscillator. The slave oscillator reduces the frequency when the feedback voltage dips below 0.75V and decreases linearly below the threshold as shown in the Performance Characteristics' Frequency Foldback plot. Other than these two differences, the control loop is similar in all four switchers. A pulse from the master oscillator for switcher 1 or a pulse from the slave oscillator for the other three switchers sets the RS latch and turns on the internal NPN bipolar power switch. Current in the switch and the external inductor begins to increase. When this current exceeds a level determined by the voltage at $V_C$, the current comparator resets the latch, turning off the switch. The current in the inductor flows through the Schottky diode and begins to decrease. The cycle begins again at the next pulse from the oscillator. In this way, the voltage on the $V_C$ pin controls the current through the inductor to the output. The internal error amplifier regulates the output by continually adjusting the $V_C$ pin voltage. The threshold for switching on the $V_C$ pin is 0.8V, and an active clamp of 1.8V limits the $V_C$ voltage. Switchers 2, 3 and 4 also contain an independent current limit not dependent on $V_C$ or duty cycle. Switcher 1's current limit is controlled by the $V_C$ voltage and varies with duty cycle. All four switchers also use slope compensation to ensure stability with the current mode scheme at duty cycles above 50%. The RUN-SS1, RUN-SS2 and RUN-SS3/4 pins control the rate of rise of the feedback pins.

The switch driver for SW1 operates either from $V_{IN}$ or from the BOOST pin. An external capacitor and an integrated Schottky diode are used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to saturate the internal bipolar NPN power switch for efficient operation.

### INPUT VOLTAGE RANGE STEP-DOWN CONSIDERATION

The minimum operating voltage of switcher 1 is determined either by the LT3513's undervoltage lockout of ~4V or by its maximum duty cycle. A user defined undervoltage lockout may be set with the UVLO pin at a voltage higher than the internal undervoltage lockout. The duty cycle is the fraction of time that the internal switch is on and is determined by the input and output voltages:

$$DC = \frac{V_{OUT} + V_F}{V_{IN} - V_{SW} + V_F}$$

where $V_F$ is the forward voltage drop of the catch diode (~0.4V) and $V_{SW}$ is the voltage drop of the internal switch

## OPERATION

(~0.3V at maximum load). This leads to a minimum input voltage of:

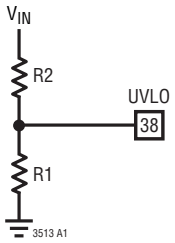
$$V_{IN(MIN)} = \frac{V_{OUT} + V_F}{DC_{MAX} - V_F + V_{SW}}$$

with $DC_{MAX}$ = 0.75.

The user defined undervoltage is set by a resistor divider connected to the UVLO pin. The comparator pulls 3µA from the pin when the UVLO pin is higher than 1.25V. The hysteresis and minimum input voltage equations are as follows:

$$V_{HYS} = (R2 + 2k) \bullet 3.9\mu A$$

$$V_{IN(MIN)} = 1.25V \frac{R1 + R2}{R1}$$




### INDUCTOR SELECTION AND MAXIMUM OUTPUT CURRENT

A good first choice for the inductor value is:

$$L = \frac{V_{OUT} + V_F}{1.8}$$

where $V_F$ is the voltage drop of the catch diode (~0.4V) and L is in µH. The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be at least 30% higher. For highest efficiency, the series resistance (DCR) should be less than 0.1Ω. Table 1 lists several vendors and types that are suitable.

**Table 1. Inductor Vendors**

| VENDOR | URL | PART SERIES | TYPE |
|---|---|---|---|
| Coilcraft | www.coilcraft.com | MSS7341 | Shielded |
| Murata | www.murata.com | LQH55D | Open |
| TDK | www.component.tdk.com | SLF7045<br>SLF10145 | Shielded<br>Shielded |
| Toko | www.toko.com | DC62CB<br>D63CB<br>D75C<br>D75F | Shielded<br>Shielded<br>Shielded<br>Open |
| Sumida | www.sumida.com | CR54<br>CDRH74<br>CDRH6D38<br>CR75 | Open<br>Shielded<br>Shielded<br>Open |

The optimum inductor for a given application may differ from the one indicated by this simple design guide. A larger value inductor provides a higher maximum load current, and reduces the output voltage ripple. If your load is lower than the maximum load current, then you can relax the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor or one with a lower DCR resulting in higher efficiency. Be aware that the maximum load current depends on input voltage. A graph in the Typical Performance Characteristics section of this data sheet shows the maximum load current as a function of input voltage and inductor value for $V_{OUT}$ = 3.3V. In addition, low inductance may result in discontinuous mode operation, which further reduces maximum load current. For details of maximum output current and discontinuous mode operation, see Linear Technology's Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN}$ > 0.5), a minimum inductance is required to avoid subharmonic oscillations, see Application Note 19.

## OPERATION

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to-peak inductor ripple current. The LT3513 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT3513 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = \frac{(1-DC)(V_{OUT}+V_F)}{L \bullet f}$$

where f is the switching frequency of the LT3513 and L is the value of the inductor. The peak inductor and switch current is:

$$I_{SW(PK)} = I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2}$$

To maintain output regulation, this peak current must be less than the LT3513's switch current limit of $I_{LIM}$. For SW1, $I_{LIM}$ is at least 2A at DC = 0.35, and decreases linearly to 1.5A at DC = 0.75 as shown in the Typical Performance Characteristics section. The maximum output current is a function of the chosen inductor value:

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} = 2.5A \bullet (1-0.57 \bullet DC) - \frac{\Delta I_L}{2}$$

Choosing an inductor value so that the ripple current is small will allow a maximum output current near the switch current limit. One approach to choosing the inductor is to start with the simple rule given above, look at the available inductors and choose one to meet cost or space goals. Then use these equations to check that the LT3513 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when $I_{OUT}$ is less than $\Delta I_L/2$.

### OUTPUT CAPACITOR SELECTION

For 5V and 3.3V outputs, a 10µF 6.3V ceramic capacitor (X5R or X7R) at the output results in very low output voltage ripple and good transient response. Other types and values will also work; the following discussion explores tradeoffs in output ripple and transient performance.

The output capacitor filters the inductor current to generate an output with low voltage ripple. It also stores energy in order satisfy transient loads and stabilizes the LT3513's control loop. Because the LT3513 operates at a high frequency, minimal output capacitance is necessary. In addition, the control loop operates well with or without the presence of output capacitor series resistance (ESR). Ceramic capacitors, which achieve very low output ripple and small circuit size, are therefore an option.

You can estimate output ripple with the following equations:

$$V_{RIPPLE} = \frac{\Delta I_L}{8 \bullet f \bullet C_{OUT}}$$ for ceramic capacitors, and

$V_{RIPPLE} = \Delta I_L \bullet ESR$ for electrolytic capacitors (tantalum and aluminum)

where $\Delta I_L$ is the peak-to-peak ripple current in the inductor. The RMS content of this ripple is very low so the RMS current rating of the output capacitor is usually not of concern. It can be estimated with the formula:

$$I_{C(RMS)} = \frac{\Delta I_L}{\sqrt{12}}$$

Another constraint on the output capacitor is that it must have greater energy storage than the inductor; if the stored energy in the inductor transfers to the output, the resulting voltage step should be small compared to the regulation voltage. For a 5% overshoot, this requirement indicates:

$$C_{OUT} > 10 \bullet L \bullet \left(\frac{I_{LIM}}{V_{OUT}}\right)^2$$

## OPERATION

The low ESR and small size of ceramic capacitors make them the preferred type for LT3513 applications. However, not all ceramic capacitors are the same. Many of the higher value capacitors use poor dielectrics with high temperature and voltage coefficients. In particular, Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and at temperature extremes.

Because loop stability and transient response depend on the value of $C_{OUT}$, this loss may be unacceptable. Use X7R and X5R types. Electrolytic capacitors are also an option. The ESRs of most aluminum electrolytic capacitors are too large to deliver low output ripple. Tantalum and newer, lower ESR organic electrolytic capacitors intended for power supply use are suitable, and the manufacturers will specify the ESR. Chose a capacitor with a low enough ESR for the required output ripple. Because the volume of the capacitor determines its ESR, both the size and the value will be larger than a ceramic capacitor that would give similar ripple performance. One benefit is that the larger capacitance may give better transient response for large changes in load current. Table 2 lists several capacitor vendors.

**Table 2. Low ESR Surface Mount Capacitors**

| VENDOR | TYPE | SERIES |
|---|---|---|
| Taiyo Yuden | Ceramic | X5R, X7R |
| AVX | Ceramic<br>Tantalum | X5R, X7R<br>TPS |
| Kemet | Tantalum<br>Ta Organic<br>Al Organic | T491, T494, T495<br>T520<br>A700 |
| Sanyo | Ta or Al Organic | POSCAP |
| Panasonic | Al Organic | SP CAP |
| TDK | Ceramic | X5R, X7R |

### DIODE SELECTION

The catch diode (D1 from Figure 1) conducts current only during switch-off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{OUT} \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The only reason to consider a diode with a larger current rating than necessary for nominal operation is for the worst-case condition of shorted output. The diode current will then increase to the typical peak switch current. Peak reverse voltage is equal to the regulator input voltage. Use a diode with a reverse voltage rating greater than the input voltage. Table 3 lists several Schottky diodes and their manufacturers.

**Table 3. Schottky Diodes**

| PART NUMBER | $V_R$ (V) | $I_{AVE}$ (A) | $V_{FAT}$ 1A (mV) | $V_F$ at 2A (mV) |
|---|---|---|---|---|
| **On Semiconductor** | | | | |
| MBRM120E | 20 | 1 | 530 | |
| MBRM140 | 40 | 1 | 550 | |
| MBRS240 | 40 | 2 | | |
| MBRA340 | 40 | 3 | | 450 |
| **Diodes Inc.** | | | | |
| B120 | 20 | 1 | 500 | |
| B240 | 40 | 2 | | 500 |
| B340A | 40 | 3 | | 450 |

### BOOST PIN CONSIDERATIONS

The minimum operating voltage of an LT3513 application is limited by the undervoltage lockout ~4V and by the maximum duty cycle. The boost circuit also limits the minimum input voltage for proper start-up. If the input voltage ramps slowly or the LT3513 turns on when the output is already in regulation, the boost capacitor may not be fully charged. Because the boost capacitor charges with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages. The Typical Performance Characteristics section shows a plot of the minimum load current to start as a function of input voltage for a 3.3V

## OPERATION

output. The minimum load current generally goes to zero once the circuit has started. Even without an output load current, in many cases the discharged output capacitor will present a load to the switcher that will allow it to start.

### INVERTER/STEP-UP CONSIDERATIONS

#### Regulating Positive Output Voltages

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistors according to:

$$R3 = R4\left(\frac{V_{OUT}}{1.25} - 1\right)$$

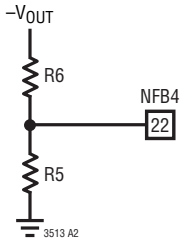
R4 should be 10k or less to avoid bias current errors.

#### Regulating Negative Output Voltages

The LT3513 contains an inverting op amp with a gain of 1. The NFB4 pin works just as the other FB pins. Choose the resistors according to:

$$R6 = \frac{V_{OUT} \bullet R5}{1.25} - R5$$

R5 should be 2.5kΩ or less to avoid bias current errors.




#### Duty Cycle Range

The maximum duty cycle (DC) of the LT3513 switching regulator is 75% for SW2, and 84% for SW3 and SW4. The duty cycle for a given application using the step-up or charge pump topology is:

$$DC = \frac{|V_{OUT}| - V_{IN}}{|V_{OUT}|}$$

The duty cycle for a given application using the inverter or SEPIC is:

$$DC = \frac{|V_{OUT}|}{V_{IN} + |V_{OUT}|}$$

The LT3513 can still be used in applications where the duty cycle, as calculated above, is greater than the maximum. However, the part must be operated in discontinuous mode so that the actual duty cycle is reduced.

#### Inductor Selection

Table 1 lists several inductor vendors and types that are suitable to use with the LT3513. Consult each manufacturer for detailed information and for their entire selection of related parts. Use ferrite core inductors to obtain the best efficiency, as core losses at frequencies above 1MHz are much lower for ferrite cores than for powdered-iron units. A 10µH to 22µH inductor will be the best choice for most LT3513 step-up and charge pump designs. Choose an inductor that can carry the entire switch current without saturating. For inverting and SEPIC regulators, a coupled inductor, or two separate inductors is an option. When using coupled inductors, choose one that can handle at least the switch current without saturating. If using uncoupled inductors, each inductor need only handle approximately one-half of the total switch current. A 4.7µH to 15µH coupled inductor or two 10µH to 22µH uncoupled inductors will usually be the best choice for most LT3513 inverting and SEPIC designs.

## OPERATION

### Output Capacitor Selection

Use low ESR (equivalent series resistance) capacitors at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have an extremely low ESR and are available in very small packages. X7R dielectrics are preferred, followed by X5R, as these materials retain their capacitance over wide voltage and temperature ranges. A 10µF to 22µF output capacitor is sufficient for most LT3513 applications. Even less capacitance is required for outputs with $|V_{OUT}| > 20V$ or $|I_{OUT}| < 100mA$. Solid tantalum or OS-CON capacitors will also work, but they will occupy more board area and will have a higher ESR than a ceramic capacitor. Always use a capacitor with a sufficient voltage rating.

### Diode Selection

A Schottky diode is recommended for use with the LT3513 switcher 2 and switcher 4. The Schottky diode for switcher 3 is integrated inside the LT3513. Choose diodes for switcher 2 and switcher 4 rated to handle an average current greater than the load current and rated to handle the maximum diode voltage. The average diode current in the step-up and SEPIC is equal to the load current. Each of the two diodes in the charge pump configurations carries an average diode current equal to the load current. The ground connected diode in the charge pump is integrated into the LT3513. The maximum diode voltage in the step-up and charge pump configurations is equal to $|V_{OUT}|$. The maximum diode voltage in the SEPIC and inverting configurations is $V_{IN} + |V_{OUT}|$.

### Input Capacitor Selection

Bypass the input of the LT3513 circuit with a 4.7µF or higher ceramic capacitor of X7R or X5R type. A lower value or a less expensive Y5V type will work if there is additional bypassing provided by bulk electrolytic capacitors or if the input source impedance is low. The following paragraphs describe the input capacitor considerations in more detail. Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3513 input and to force this switching current into a tight local loop, minimizing EMI. The input capacitor must have low impedance at the switching frequency to do this effectively and it must have an adequate ripple current rating. The input capacitor RMS current can be calculated from the step-down output voltage and current, and the input voltage:

$$C_{IN(RMS)} = I_{OUT} \frac{\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}} < \frac{I_{OUT}}{2}$$

and is largest when $V_{IN} = 2V_{OUT}$ (50% duty cycle). The ripple current contribution from the other channels will be minimal. Considering that the maximum load current from switcher 1 is ~3A, RMS ripple current will always be less than 1.5A. The high frequency of the LT3513 reduces the energy storage requirements of the input capacitor, so that the capacitance required is less than 10µF. The combination of small size and low impedance (low equivalent series resistance or ESR) of ceramic capacitors makes them the preferred choice. The low ESR results in very low voltage ripple. Ceramic capacitors can handle larger magnitudes of ripple current than other capacitor types of the same value. Use X5R and X7R types. An alternative to a high value ceramic capacitor is a lower value along with a larger electrolytic capacitor, for example a 1µF ceramic capacitor in parallel with a low ESR tantalum capacitor. For the electrolytic capacitor, a value larger than 10µF will be required to meet the ESR and ripple current requirements. Because the input capacitor is likely to see high surge currents when the input source is applied, only consider a tantalum capacitor if it has the appropriate surge current rating. The manufacturer may also recommend operation

## OPERATION

below the rated voltage of the capacitor. Be sure to place the 1µF ceramic as close as possible to the $V_{IN}$ and GND pins on the IC for optimal noise immunity.

A final caution is in order regarding the use of ceramic capacitors at the input. A ceramic input capacitor can combine with stray inductance to form a resonant tank circuit. If power is applied quickly (for example by plugging the circuit into a live power source), this tank can ring, doubling the input voltage and damaging the LT3513. The solution is to either clamp the input voltage or dampen the tank circuit by adding a lossy capacitor (an electrolytic) in parallel with the ceramic capacitor. For details, see Application Note 88.

### Soft-Start and Shutdown

The RUN-SS1(Run/Soft-Start) pin is used to place the switching regulators and the internal bias circuits in shutdown mode. It also provides a soft-start function, along with RUN-SS2 and RUN-SS3/4. If the RUN-SS1 pin is pulled to ground, the LT3513 enters its shutdown mode with all regulators off and quiescent current reduced to ~30µA. An internal 2µA current source pulls up on the RUN-SS1, RUN-SS2, and RUN-SS3/4 pins. If the RUN-SS1 pin reaches ~0.6V, the internal bias circuits start and the quiescent currents increase to their nominal levels.

If a capacitor is tied from the RUN-SS1, RUN-SS2 or RUN-SS3/4 pins to ground, then the internal pull-up current will generate a voltage ramp on these pins. This voltage clamps the $V_C$ pin, limiting the peak switch current and therefore input current during start-up. The RUN-SS1 pin clamps $V_{C1}$, the RUN-SS2 pin clamps $V_{C1}$ and the RUN-SS3/4 pin clamps the $V_{C3}$ and $V_{C4}$ pins. A good value for the soft-start capacitors is $C_{OUT}$/10,000, where $C_{OUT}$ is the value of the largest output capacitor.

### $V_{ON}$ Pin Considerations

The $V_{ON}$ pin is the delayed output for switching regulator 3. When the $C_T$ pin reaches 1.1V, the output disconnect PNP turns on, connecting $V_{ON}$ to E3. The $V_{ON}$ pin is current limited and will protect the LT3513 and input source from a shorted output.

The $V_{ON}$ pin output is also controlled from the $V_{ON\_CLK}$ pin. When $V_{ON\_CLK}$ is low, the $V_{ON}$ output will turn on if the $C_T$ pin is greater than 1.1V. When $V_{ON\_CLK}$ is high, greater than 1.5V, the $V_{ON}$ output is disabled and the $V_{ONSINK}$ open collector device turns on. If the $V_{ONSINK}$ pin is connected to $V_{ON}$ through a resistor, the $V_{ON}$ voltage will decay with a high $V_{ON\_CLK}$. $V_{ON\_CLK}$ may be synced to the horizontal scanning frequency to improve LCD image quality.

### Low Voltage Dropout Linear Regulator

The LT3513 features an output to drive an external NPN transistor LDO to provide a lower voltage logic supply voltage. The output is capable of providing 10mA of current to the base of the NPN. The output of the LDO is controlled by the FB5 pin. Choose the resistor values according to:

$$R8 = R7\left(\frac{V_{LDO}}{0.625V} - 1\right)$$

R8 should be 10k or less to avoid bias current errors.

The internal compensation of the LDO relies on a low ESR ceramic capacitor between the values of 2.2µF and 20µF. X7R dielectrics are preferred, followed by X5R, as these materials retain their capacitance over wide voltage and temperature ranges.

### Printed Circuit Board Layout

For proper operation and minimum EMI, care must be taken during printed circuit board (PCB) layout. Figure 3 shows the high current paths in the step-down regulator circuit. Note that in the step-down regulators, large, switched currents flow in the power switch, the catch diode and the input capacitor. In the step-up regulators, large, switched currents flow through the power switch, the switching diode and the output capacitor. In SEPIC and

## OPERATION

inverting regulators, the switched currents flow through the power switch, the switching diode and the tank capacitor. The loop formed by the components in the switched current path should be as small as possible. Place these components, along with the inductor and output capacitor, on the same side of the circuit board, and connect them on that layer. Place a local, unbroken ground plane below these components, and tie this ground plane to system ground at one location, ideally at the ground terminal of the output capacitor C2. Additionally, keep the SW and BOOST nodes as small as possible.

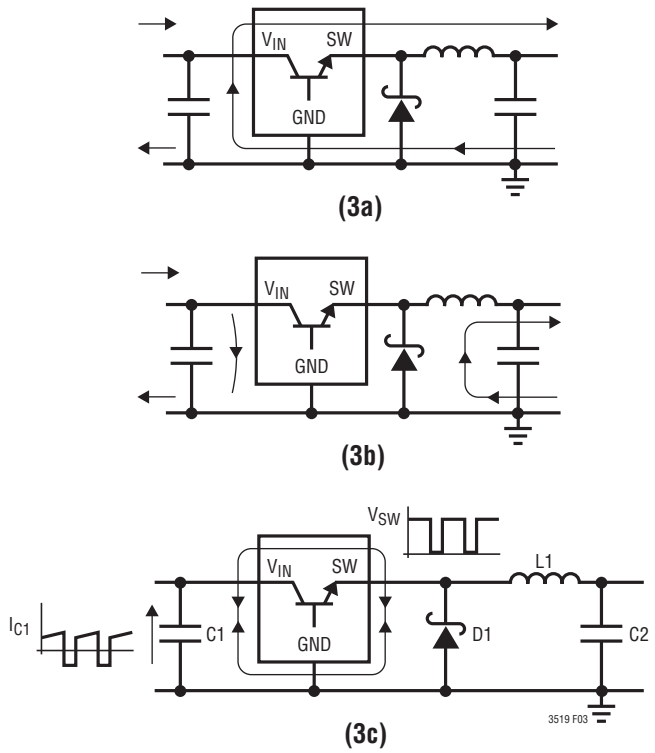



**Figure 3. Subtracting the Current When the Switch is On (3a) from the Current When the Switch is Off (3b) Reveals the Path of the High Frequency Switching Current (3c) Keep this Loop Small. The Voltage on the SW and BOOST Nodes Will Also Be Switched; Keep These Nodes as Small as Possible. Finally, Make Sure the Circuit is Shielded with a Local Ground Plane**

### Thermal Considerations

The PCB must provide heat sinking to keep the LT3513 cool. The Exposed Pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to other copper layers below with thermal vias; these layers will spread the heat dissipated by the LT3513. Place additional vias near the catch diodes. Adding more copper to the top and bottom layers and tying this copper to the internal planes with vias can reduce thermal resistance further. With these steps, the thermal resistance from die (or junction) to ambient can be reduced to $\theta_{JA}$ = 25°C or less. With 100LFPM airflow, this resistance can fall by another 25%. Further increases in airflow will lead to lower thermal resistance.

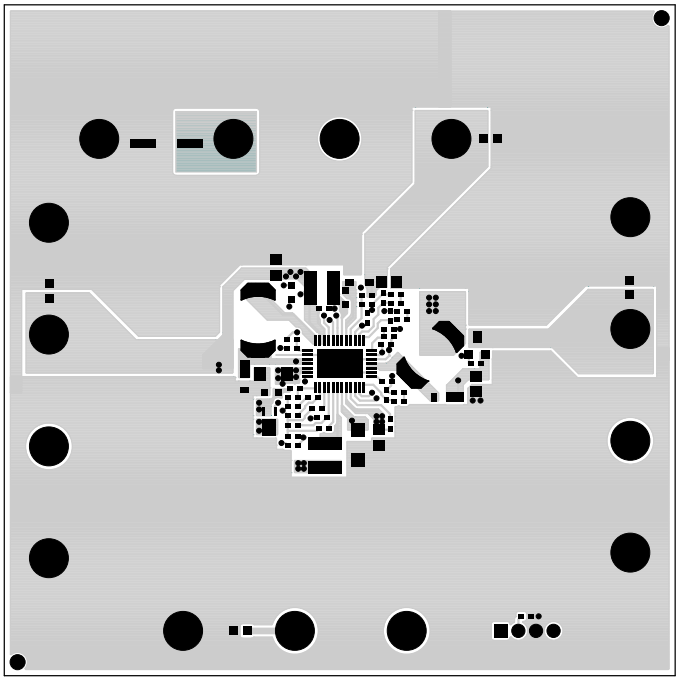
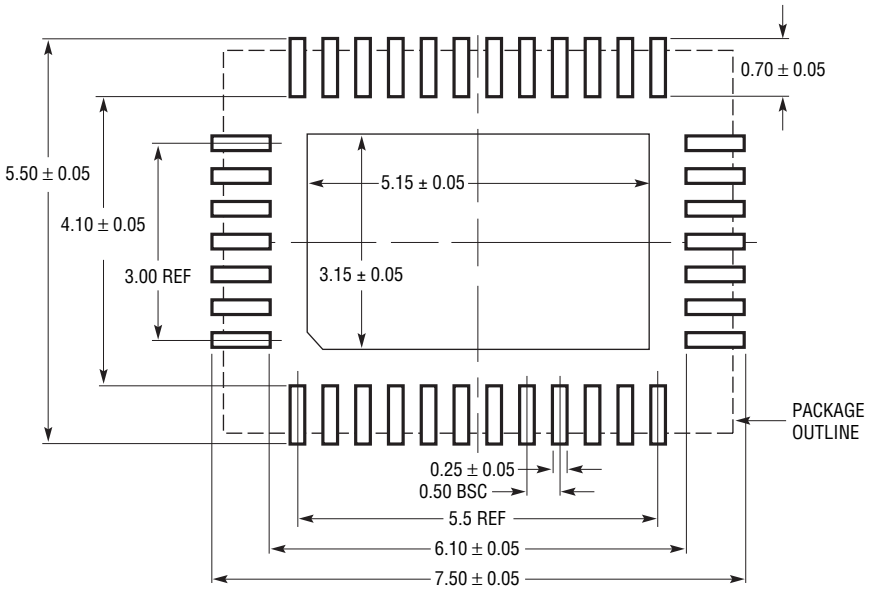


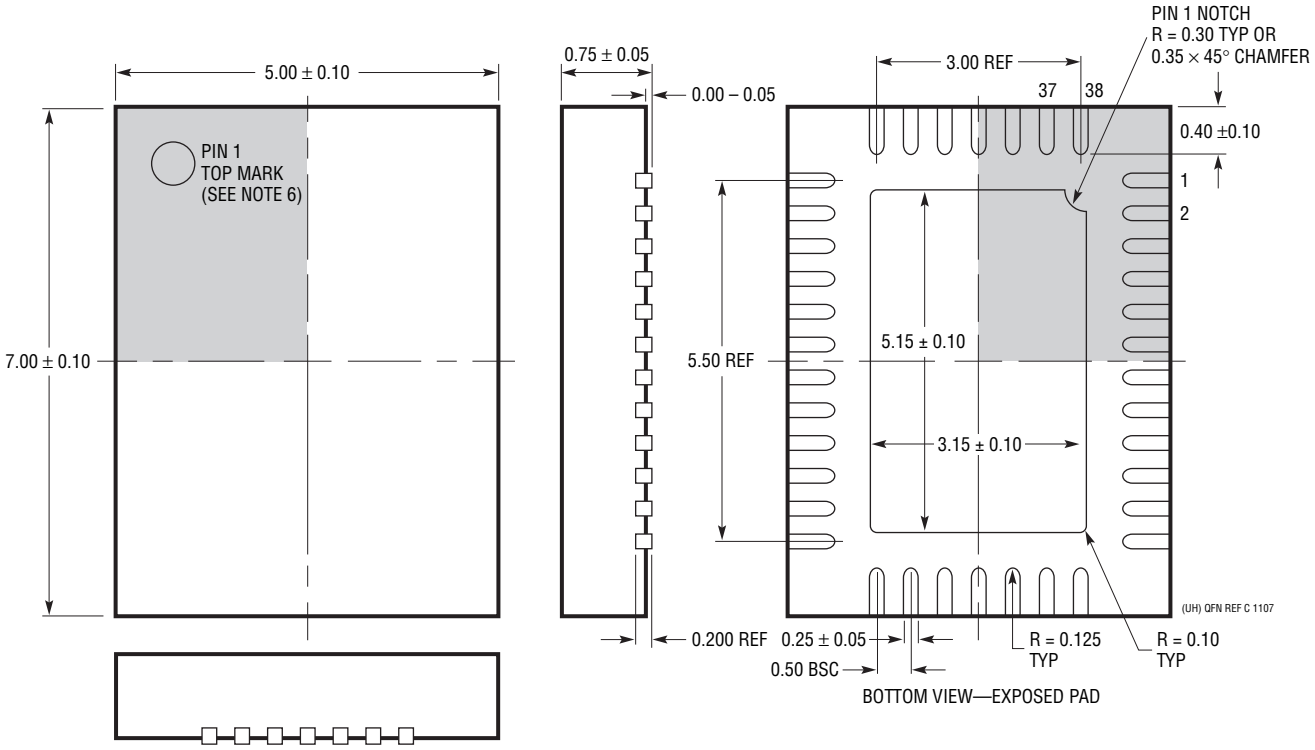
**Figure 4. Topside PCB Layout**

# PACKAGE DESCRIPTION

**UHF Package**
**38-Lead Plastic QFN (5mm × 7mm)**
(Reference LTC DWG # 05-08-1701 Rev C)




RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED




NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY (Revision history begins at Rev C)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| C | 01/11 | Revised UVLO Pin Hysteresis Current and Switch 2 Current Limit Max values in Electrical Characteristics section | 3 |

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LT3003 | 3-Channel LED Ballaster with PWM Dimming | $V_{IN}$: 3V to 48V, $I_Q$ = 3,000:1 True Color PWM™, $I_{SD}$ < 5µA, MSOP10 Package |
| LT3465/LT3465A | Constant Current, 1.2MHz/2.7MHz, High Efficiency White LED Boost Regulators with Integrated Schottky Diode | $V_{IN}$: 2.7V to 16V, $V_{OUT(MAX)}$ = 34V, $I_Q$ = 1.9mA, $I_{SD}$ < 1µA, ThinSOT™ Package |
| LT3466/LT3466-1 | Dual Constant Current, 2MHz High Efficiency White LED Boost Regulators with Integrated Schottky Diode | $V_{IN}$: 2.7V to 24V, $V_{OUT(MAX)}$ = 40V, $I_Q$ = 5mA, $I_{SD}$ < 16µA, 3mm × 3mm DFN10 Package |
| LT3474 | 36V, 1A ($I_{LED}$), 2MHz Step-Down LED Driver | $V_{IN}$: 4V to 36V, $V_{OUT(MAX)}$ = 13.5V, $I_Q$ = 400:1 True Color PWM, $I_{SD}$ < 16µA, TSSOP16E Package |
| LT3475 | Dual 1.5A ($I_{LED}$), 36V, 2MHz Step-Down LED Driver | $V_{IN}$: 4V to 36V, $V_{OUT(MAX)}$ = 13.5V, $I_Q$ = 3,000:1 True Color PWM, $I_{SD}$ < 1µA, TSSOP20E Package |
| LT3476 | Quad Output 1.5A, 2MHz High Current LED Driver with 1,000:1 Dimming | $V_{IN}$: 2.8V to 16V, $V_{OUT(MAX)}$ = 36V, $I_Q$ = 1,000:1 True Color PWM, $I_{SD}$ < 10µA, 5mm × 7mm QFN10 Package |
| LT3478/LT3478-1 | 42V, 4.5A ($I_{SW}$), 2.25MHz, LED Drivers with 3,000:1 True Color PWM Dimming | $V_{IN}$: 2.8V to 36V, $V_{OUT(MAX)}$ = 42V, $I_Q$ = 6.1mA, $I_{SD}$ < 3µA, TSSOP16E Package |
| LT3486 | Dual 1.3A, 2MHz High Current LED Driver | $V_{IN}$: 2.5V to 24V, $V_{OUT(MAX)}$ = 36V, $I_Q$ = 1,000:1 True Color PWM, $I_{SD}$ < 1µA, 5mm × 3mm DFN, TSSOP16E Packages |
| LT3491 | Constant Current, 2.3MHz, High Efficiency White LED Boost Regulator with Integrated Schottky Diode | $V_{IN}$: 2.5V to 12V, $V_{OUT(MAX)}$ = 27V, $I_Q$ = 2.6mA, $I_{SD}$ < 8µA, 2mm × 2mm DFN6, SC70 Packages |
| LT3494/LT3494A | 40V, 180mA/350mA Micropower Low Noise Boost Converters with Output Disconnect | $V_{IN}$: 2.3V to 16V, $V_{OUT(MAX)}$ = 40V, $I_Q$ = 65µA, $I_{SD}$ < 1µA, 3mm × 2mm DFN8 Package |
| LT3497 | Dual 2.3MHz, Full Function LED Driver with Integrated Schottkys and 250:1 True Color PWM Dimming | $V_{IN}$: 2.5V to 10V, $V_{OUT(MAX)}$ = 32V, $I_Q$ = 6mA, $I_{SD}$ < 12µA, 3mm × 2mm DFN10 Package |
| LT3498 | 2.3MHz, 20mA LED Driver and OLED Driver with Integrated Schottkys | $V_{IN}$: 2.5V to 12V, $V_{OUT(MAX)}$ = 32V, $I_Q$ = 1.65mA, $I_{SD}$ < 9µA, 3mm × 2mm DFN12 Package |
| LT3591 | Constant Current, 1MHz, High Efficiency White LED Boost Regulator with Integrated Schottky Diode and 80:1 True Color PWM Dimming | $V_{IN}$: 2.5V to 12V, $V_{OUT(MAX)}$ = 40V, $I_Q$ = 4mA, $I_{SD}$ < 9µA, 3mm × 2mm DFN8 Package |
| LT3595 | 16-Channel 48V, 2MHz Buck Mode LED Driver with 3000:1 True Color PWM Dimming | $V_{IN}$: 4.5V to 50V, $I_Q$ = 3,000:1 True Color PWM, $I_{SD}$ < 3µA, 5mm × 9mm QFN56 Package |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