36V, 2A, 2.8MHz Step-Down Switching Regulator with Integrated Power Schottky Diode

FEATURES

- **Wide Input Voltage Range: 3.6V to 34V Operating, 36V Maximum**
- **2A Maximum Output Current**
- **Low Ripple Burst Mode® Operation**
  50µA I_Q at 12V_{IN} to 3.3V_{OUT}
  Output Ripple < 15mV_{P-P}
- **Adjustable Switching Frequency: 300kHz to 2.8MHz**
- **Low Shutdown Current: I_Q < 1µA**
- **Integrated Boost Diode**
- **Integrated Power Schottky Diode**
- Power Good Flag
- Saturating Switch Design: 0.18Ω On-Resistance
- 1.265V Feedback Reference Voltage
- Output Voltage: 1.265V to 20V
- Soft-Start Capability
- Small 14-Pin Thermally Enhanced (4mm x 3mm) DFN Package

APPLICATIONS

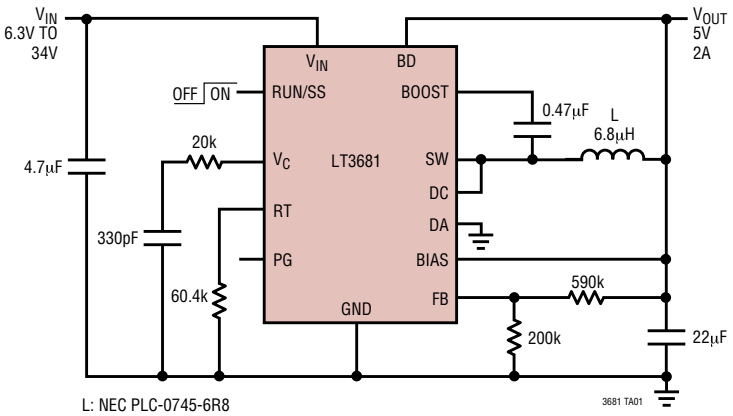
- Automotive Battery Regulation
- Power for Portable Products
- Distributed Supply Regulation
- Industrial Supplies
- Wall Transformer Regulation

DESCRIPTION

The LT®3681 is an adjustable frequency (300kHz to 2.8MHz) monolithic buck switching regulator that accepts input voltages up to 34V (36V maximum). A high efficiency 0.18Ω switch is included on the die along with a boost Schottky diode and the necessary oscillator, control, and logic circuitry. An undedicated power Schottky diode is integrated into the LT3681 to minimize the solution size. Current mode topology is used for fast transient response and good loop stability. Low ripple Burst Mode operation maintains high efficiency at low output currents while keeping output ripple below 15mV in a typical application. In addition, the LT3681 can further enhance low output current efficiency by drawing bias current from the output when V_{OUT} is above 3V. Shutdown reduces input supply current to less than 1µA while a resistor and capacitor on the RUN/SS pin provide a controlled output voltage ramp (soft-start). A power good flag signals when V_{OUT} reaches 90% of the programmed output voltage. The LT3681 is available in 14-Pin 4mm x 3mm DFN package with exposed pads for low thermal resistance.

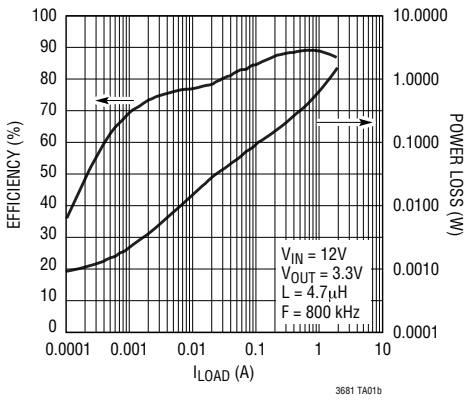
TYPICAL APPLICATION

5V Step-Down Converter



L: NEC PLC-0745-6R8

Efficiency

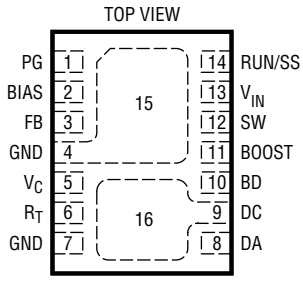


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, RUN/SS Voltage 36V
BOOST Pin Voltage 56V
BOOST Pin Above SW Pin 30V
FB, RT, V_C Voltage 5V
BIAS, PG, BD Voltage 30V
Maximum Junction Temperature ..... 125°C
DC above DA 40V
Operating Temperature Range (Note 2)
LT3681E ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

PACKAGE/ORDER INFORMATION



DE14MA PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB
EXPOSED PAD PIN 16 IS DC

ORDER PART NUMBER	DE PART MARKING
LT3681EDE	3681

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, $V_{RUNS/SS}$ = 10V, V_{BOOST} = 15V, V_{BIAS} = 3.3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●		3	3.6	V
Quiescent Current from V_{IN}	$V_{RUN/SS}$ = 0.2V			0.01	0.5	µA
	V_{BIAS} = 3V, Not Switching	●		22	60	µA
	V_{BIAS} = 0, Not Switching			75	120	µA
Quiescent Current from BIAS	$V_{RUN/SS}$ = 0.2V			0.01	0.5	µA
	V_{BIAS} = 3V, Not Switching	●		50	120	µA
	V_{BIAS} = 0, Not Switching			0	5	µA
Minimum Bias Voltage				2.7	3	V
Feedback Voltage		 ●	1.25 1.24	1.265 1.265	1.29 1.3	V V
FB Pin Bias Current (Note 3)	V_{FB} = 1.25V, V_C = 0.4V	●		30	100	nA
FB Voltage Line Regulation	4V < V_{IN} < 34V			0.002	0.02	%/V
Error Amp GM				330		µMho
Error Amp Gain				800		
V_C Source Current				65		µA
V_C Sink Current				85		µA
V_C Pin to Switch Current Gain				3.5		A/V
V_C Clamp Voltage				2		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, $V_{RUNS/SS}$ = 10V V_{BOOST} = 15V, V_{BIAS} = 3.3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Schottky Diode Forward Voltage	I_{DA} = 1A I_{DA} = 2A			0.50 0.56		V V
Power Schottky Diode Leakage Current	V_{DC-DA} = 40V				100	µA
Switching Frequency	RT = 8.66k RT = 29.4k RT = 187k		2.5 1.25 250	2.8 1.4 300	3.1 1.55 350	MHz MHz kHz
Minimum Switch Off-Time		●		130	200	nS
Switch Current Limit	Duty Cycle = 5%		3.2	3.8	4.4	A
Switch V_{CESAT}	I_{SW} = 2A			360		mV
Boost Schottky Reverse Leakage	V_{SW} = 10V, V_{BIAS} = 0V			0.02	2	µA
Minimum Boost Voltage (Note 4)		●		1.5	2.1	V
BOOST Pin Current	I_{SW} = 1A			18	35	mA
RUN/SS Pin Current	$V_{RUN/SS}$ = 2.5V			5	10	µA
RUN/SS Input Voltage High			2.5			V
RUN/SS Input Voltage Low					0.2	V
PG Threshold Offset from Feedback Voltage	V_{FB} Rising			122		mV
PG Hysteresis				5		mV
PG Leakage	V_{PG} = 5V			0.1	1	µA
PG Sink Current	V_{PG} = 3V	●	100	600		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

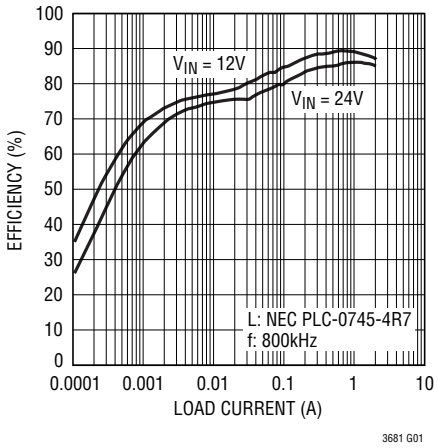
Note 2: The LT3681E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Bias current flows into the FB pin.

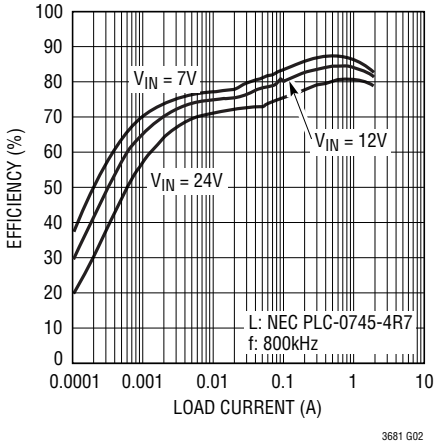
Note 4: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the switch.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

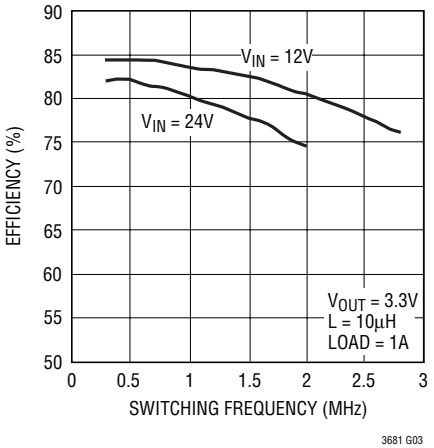
Efficiency (V_{OUT} = 5.0V)



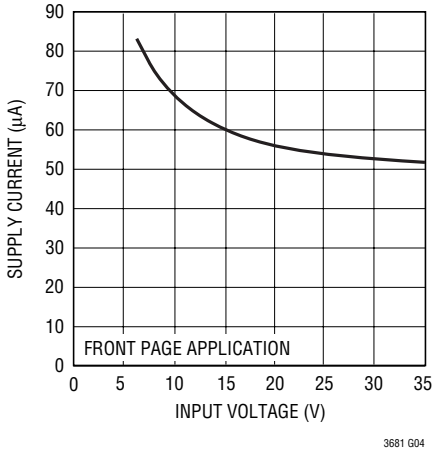
Efficiency (V_{OUT} = 3.3V)



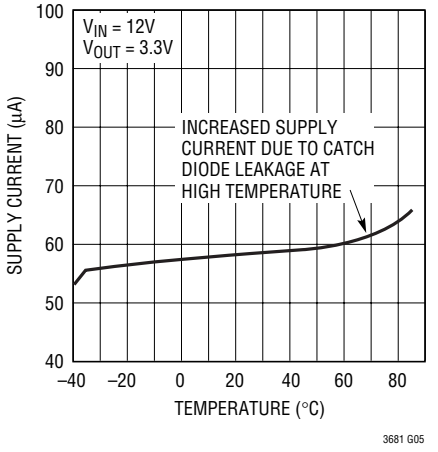
Efficiency vs Switching Frequency



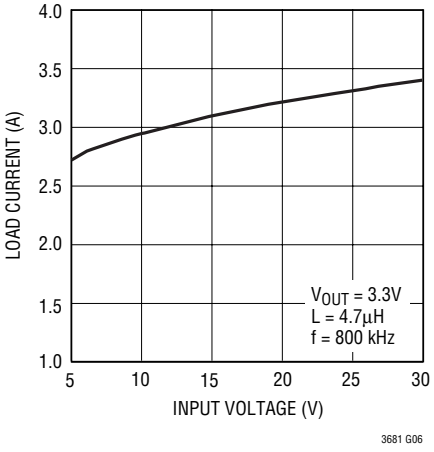
No Load Supply Current



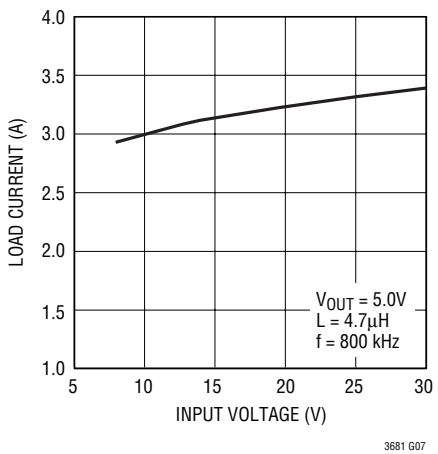
No Load Supply Current vs Temperature



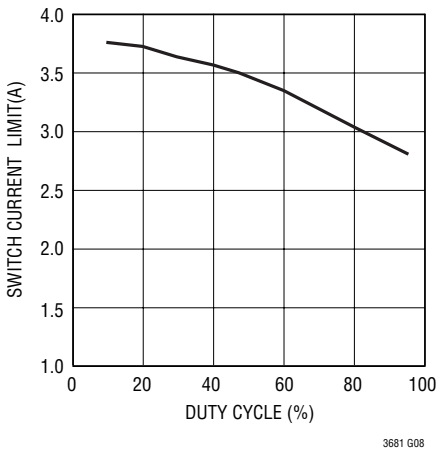
Maximum Load Current



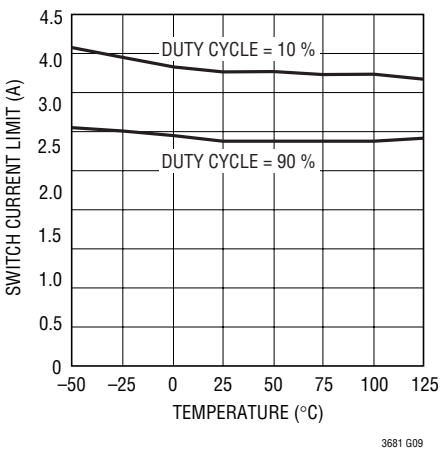
Maximum Load Current



Switch Current Limit

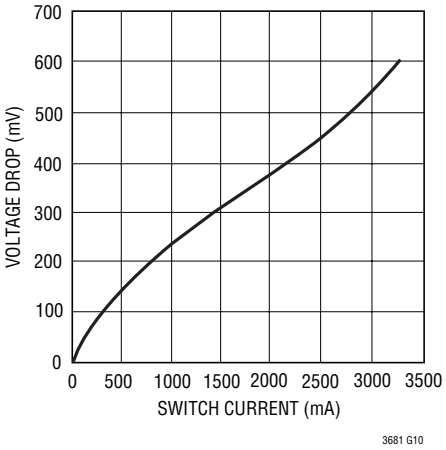


Switch Current Limit



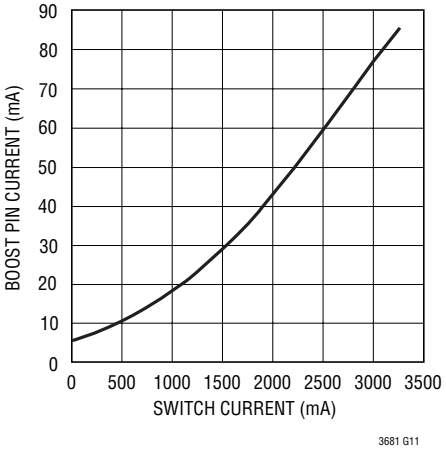
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Switch Voltage Drop



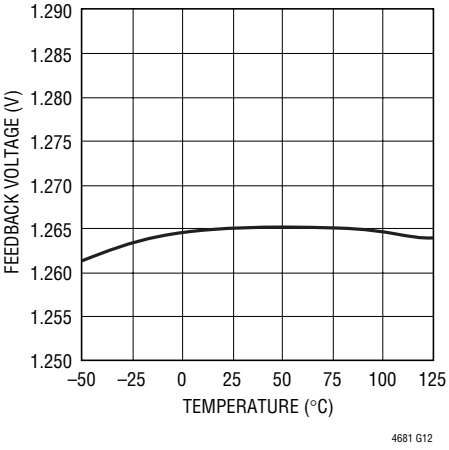
3681 G10

Boost Pin Current



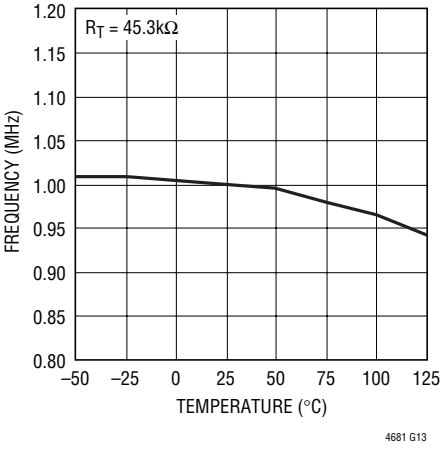
3681 G11

Feedback Voltage



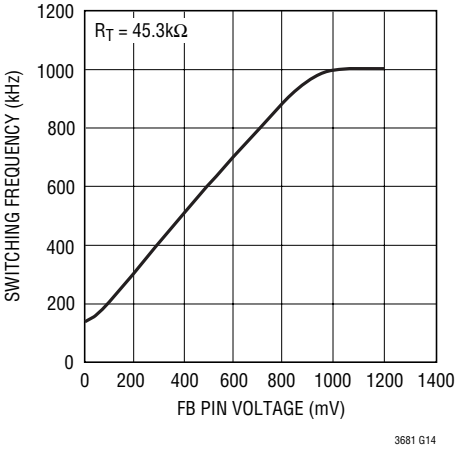
4681 G12

Switching Frequency



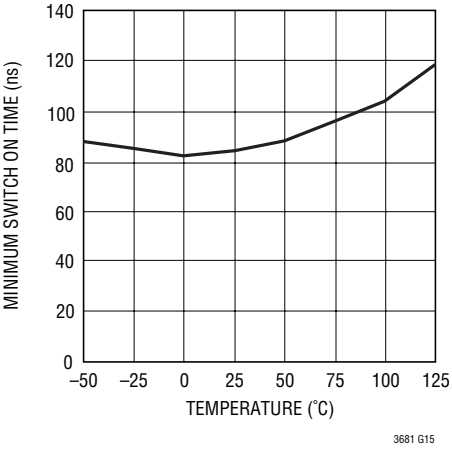
4681 G13

Frequency Foldback



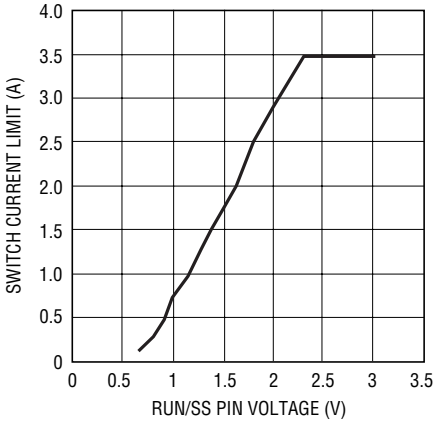
3681 G14

Minimum Switch On-Time



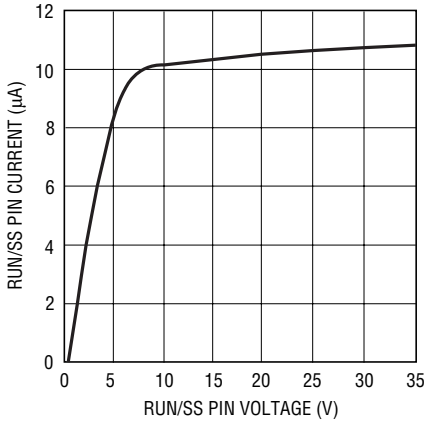
3681 G15

Soft Start



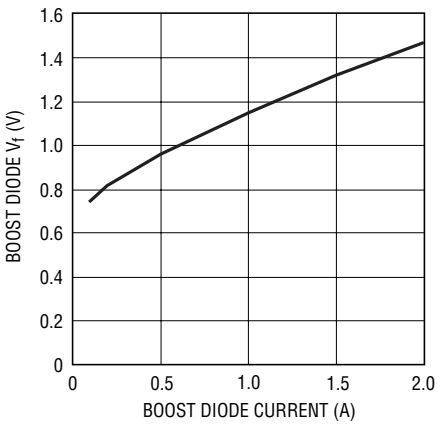
3681 G16

RUN/SS Pin Current



3681 G17

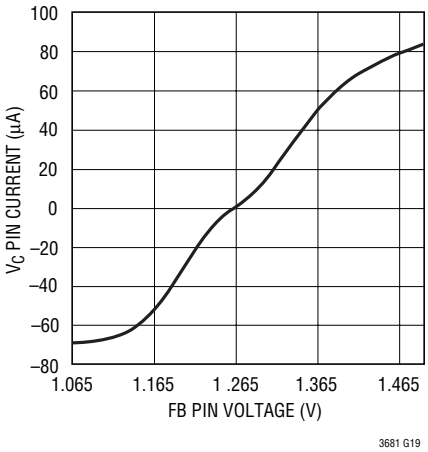
Boost Diode



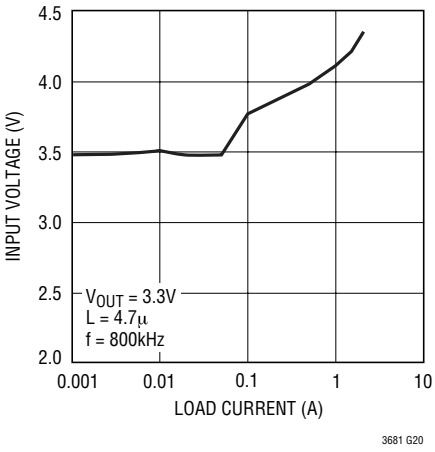
3681 G18

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

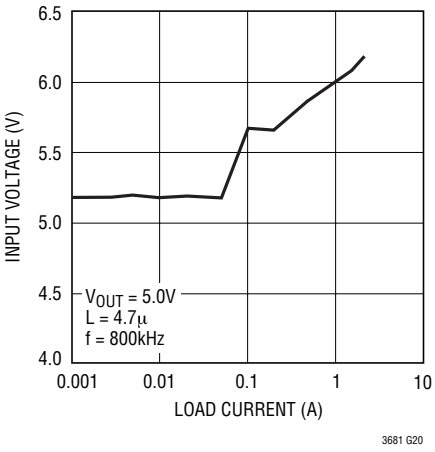
Error Amp Output Current



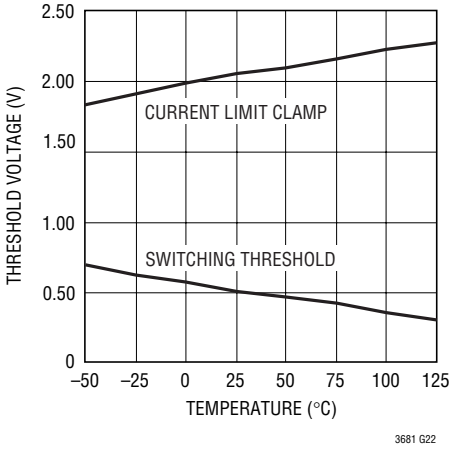
Minimum Input Voltage



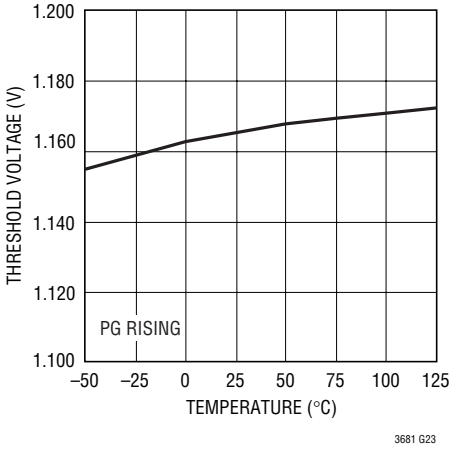
Minimum Input Voltage



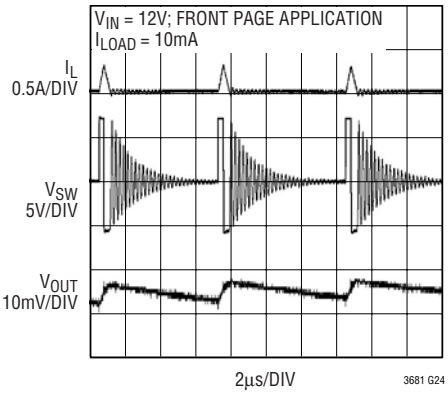
V_C Voltages



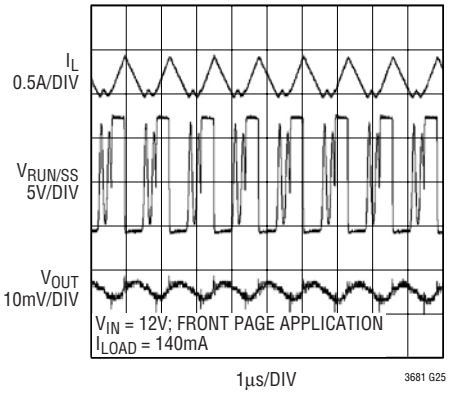
Power Good Threshold



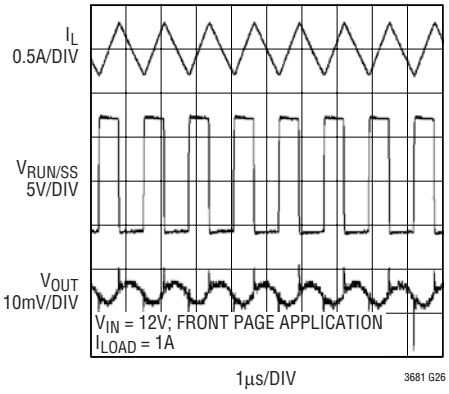
Switching Waveforms; Burst Mode



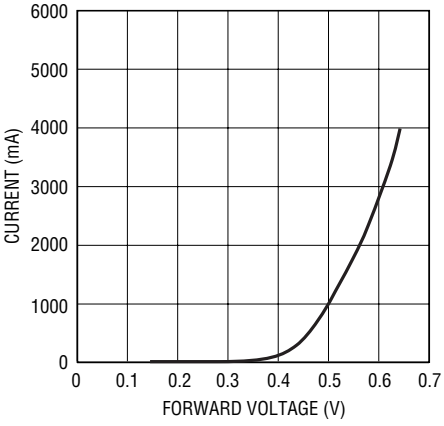
Switching Waveforms; Transition from Burst Mode to Full Frequency



Switching Waveforms; Full Frequency Continuous Operation



Power Schottky Diode Forward Voltage vs Current



PIN FUNCTIONS

PG (Pin 1): The PG pin is the open collector output of an internal comparator. PG remains low until the FB pin is within 10% of the final regulation voltage. PG output is valid when V_{IN} is above 3.5V and RUN/SS is high.

BIAS (Pin 2): The BIAS pin supplies the current to the LT3681's internal regulator. Tie this pin to the lowest available voltage source above 3V (typically V_{OUT}). This architecture increases efficiency especially when the input voltage is much higher than the output.

FB (Pin 3): The LT3681 regulates the FB pin to 1.265V. Connect the feedback resistor divider tap to this pin.

V_C (Pin 5): The V_C pin is the output of the internal error amplifier. The voltage on this pin controls the peak switch current. Tie an RC network from this pin to ground to compensate the control loop.

RT (Pin 6): Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency.

DA (Pin 8): This is the anode of the integrated power Schottky diode. High frequency, large amplitude currents flow through this pin, so tie it to ground through a low impedance connection.

DC (Pin 9, Exposed Pad 16): These pins connect to the cathode of the integrated power Schottky diode. High frequency, large amplitude currents flow through these pins, so tie them to SW through a low impedance connection.

BD (Pin 10): This pin connects to the anode of the internal boost Schottky diode.

BOOST (Pin 11): This pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch. Connect a capacitor between this pin and SW.

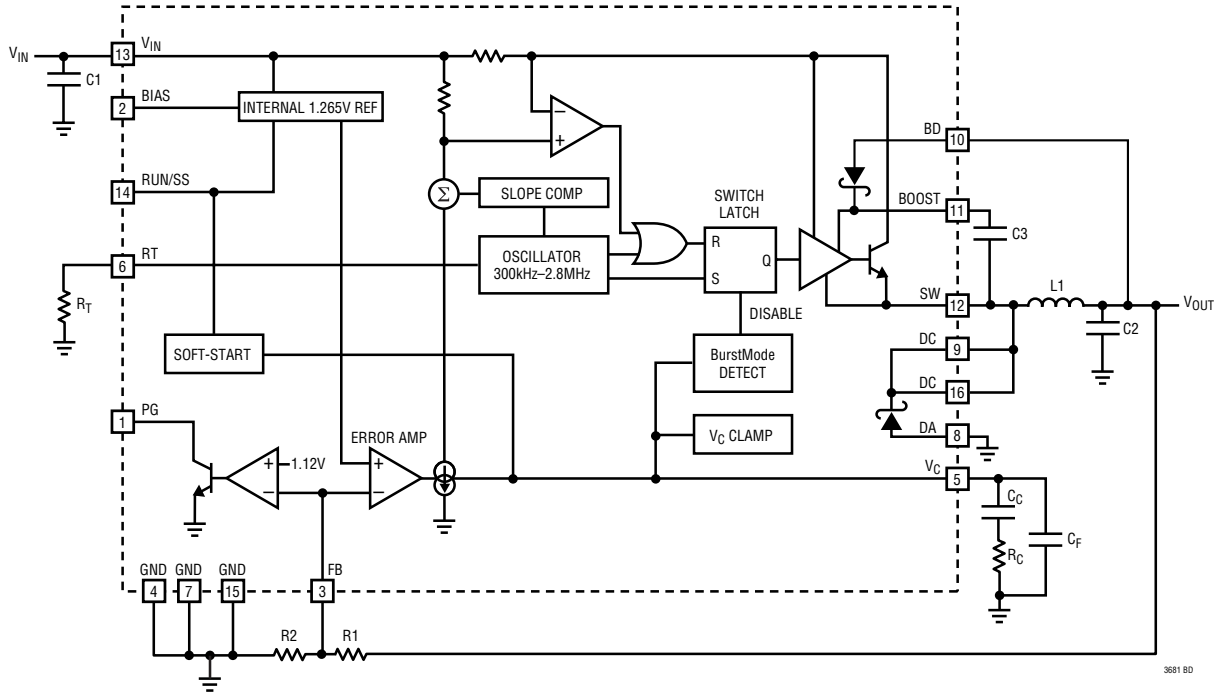
SW (Pin 12): The SW pin is the output of the internal power switch. Connect this pin to the inductor, DC and boost capacitor.

V_{IN} (Pin 13): The V_{IN} pin supplies current to the LT3681's internal regulator and to the internal power switch. This pin must be locally bypassed.

RUN/SS (Pin 14): The RUN/SS pin is used to put the LT3681 in shutdown mode. Tie to ground to shut down the LT3681. Tie to 2.3V or more for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin. RUN/SS also provides a soft-start function; see the Applications Information section.

GND (Pins 4, 7, Exposed Pad 15): All three of these terminals internally connect to the LT3681 control IC's signal return, while exposed pad 15 performs the added function of providing a low thermal resistance heat flow path between the IC and the system heatsink. Tie all of these terminals to a copper pour on the top layer of the printed circuit board. Please refer to the Applications Information section for more details.

BLOCK DIAGRAM



OPERATION

The LT3681 is a constant frequency, current mode step-down regulator. An oscillator, with frequency set by RT, sets an RS flip-flop, turning on the internal power switch. An amplifier and comparator monitor the current flowing between the V_{IN} and SW pins, turning the switch off when this current reaches a level determined by the voltage at V_C. An error amplifier measures the output voltage through an external resistor divider tied to the FB pin and servos the V_C pin. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. An active clamp on the V_C pin provides current limit. The V_C pin is also clamped to the voltage on the RUN/SS pin; soft-start is implemented by generating a voltage ramp at the RUN/SS pin using an external resistor and capacitor.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 3V bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN/SS pin is used to place the LT3681 in shutdown, disconnecting the output and reducing the input current to less than 1µA.

The switch driver operates from either the input or from the BOOST pin. An external capacitor is used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to fully saturate the internal bipolar NPN power switch for efficient operation.

To further optimize efficiency, the LT3681 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 55µA in a typical application.

The oscillator reduces the LT3681's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the output current during startup and overload.

The LT3681 contains a power good comparator which trips when the FB pin is at 91% of its regulated value. The PG output is an open-collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. Power good is valid when the LT3681 is enabled and V_{IN} is above 3.6V.

The LT3681 integrates a high quality, 36V, 2A power Schottky diode to reduce the overall solution size.

APPLICATIONS INFORMATION

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the 1% resistors according to:

$$R1 = R2\left(\frac{V_{OUT}}{1.265} - 1\right)$$

Reference designators refer to the Block Diagram.

Setting the Switching Frequency

The LT3681 uses a constant frequency PWM architecture that can be programmed to switch from 300kHz to 2.8MHz by using a resistor tied from the RT pin to ground. A table showing the necessary RT value for a desired switching frequency is in Figure 1.

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.3	187
0.4	133
0.6	84.5
0.8	60.4
1.0	45.3
1.2	36.5
1.4	29.4
1.6	23.7
1.8	20.5
2.0	16.9
2.2	14.3
2.4	12.1
2.6	10.2
2.8	8.66

Figure 1. Switching Frequency vs. RT Value

Operating Frequency Tradeoffs

Selection of the operating frequency is a tradeoff between efficiency, component size, minimum dropout voltage, and maximum input voltage. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency, lower maximum input voltage, and higher dropout voltage. The highest acceptable switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_D + V_{OUT}}{t_{ON(MIN)}\left(V_D + V_{IN} - V_{SW}\right)}$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, V_D is the power Schottky catch diode drop (~0.55V), V_{SW} is the internal switch drop (~0.5V at max load). This equation shows that slower switching frequency is necessary to safely accommodate high V_{IN}/V_{OUT} ratio. Also, as shown in the next section, lower frequency allows a lower dropout voltage. The reason input voltage range depends on the switching frequency is because the LT3681 switch has finite minimum on and off times. The switch can turn on for a minimum of ~150ns and turn off for a minimum of ~150ns. This means that the minimum and maximum duty cycles are:

$$DC_{MIN} = f_{SW}\, t_{ON(MIN)}$$

$$DC_{MAX} = 1 - f_{SW}\, t_{OFF(MIN)}$$

where f_{SW} is the switching frequency, the $t_{ON(MIN)}$ is the minimum switch on time (~150ns), and the $t_{OFF(MIN)}$ is the minimum switch off time (~150ns). These equations show that duty cycle range increases when switching frequency is decreased.

A good choice of switching frequency should allow adequate input voltage range (see next section) and keep the inductor and capacitor values small.

Input Voltage Range

The maximum input voltage for LT3681 applications depends on switching frequency, the Absolute Maximum Ratings on V_{IN} and BOOST pins, and on operating mode.

If the output is in start-up or short-circuit operating modes, then V_{IN} must be below 34V and below the result of the following equation:

$$V_{IN(MAX)} = \frac{V_{OUT} + V_D}{f_{SW}\, t_{ON(MIN)}} - V_D + V_{SW}$$

where $V_{IN(MAX)}$ is the maximum operating input voltage, V_{OUT} is the output voltage, V_D is the catch diode drop (~0.55V), V_{SW} is the internal switch drop (~0.5V at max load), f_{SW} is the switching frequency (set by R_T), and $t_{ON(MIN)}$ is the minimum switch on time (~150ns). Note that a higher switching frequency will depress the maximum operating input voltage. Conversely, a lower switching

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frequency will be necessary to achieve safe operation at high input voltages.

If the output is in regulation and no short-circuit or start-up events are expected, then input voltage transients of up to 36V are acceptable regardless of the switching frequency. In this mode, the LT3681 may enter pulse skipping operation where some switching pulses are skipped to maintain output regulation. In this mode the output voltage ripple and inductor current ripple will be higher than in normal operation.

The minimum input voltage is determined by either the LT3681's minimum operating voltage of ~3.6V or by its maximum duty cycle (see equation in previous section). The minimum input voltage due to duty cycle is:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_D}{1 - f_{SW} t_{OFF(MIN)}} - V_D + V_{SW}$$

where $V_{IN(MIN)}$ is the minimum input voltage, and $t_{OFF(MIN)}$ is the minimum switch off time (150ns). Note that higher switching frequency will increase the minimum input voltage. If a lower dropout voltage is desired, a lower switching frequency should be used.

Inductor Selection

For a given input and output voltage, the inductor value and switching frequency will determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} or V_{OUT} and decreases with higher inductance and faster switching frequency. A reasonable starting point for selecting the ripple current is:

$$\Delta I_L = 0.4(I_{OUT(MAX)})$$

where $I_{OUT(MAX)}$ is the maximum output load current. To guarantee sufficient output current, peak inductor current must be lower than the LT3681's switch current limit (I_{LIM}). The peak inductor current is:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \Delta I_L/2$$

where $I_{L(PEAK)}$ is the peak inductor current, $I_{OUT(MAX)}$ is the maximum output load current, and ΔI_L is the inductor ripple current. The LT3681's switch current limit (I_{LIM}) is at least 3.5A at low duty cycles and decreases linearly to 2.5A at DC = 0.8. The maximum output current is a function of the inductor ripple current:

$$I_{OUT(MAX)} = I_{LIM} - \Delta I_L/2$$

Be sure to pick an inductor ripple current that provides sufficient maximum output current ($I_{OUT(MAX)}$).

The largest inductor ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT} + V_D}{f\Delta I_L}\right)\left(1 - \frac{V_{OUT} + V_D}{V_{IN(MAX)}}\right)$$

where V_D is the voltage drop of the integrated Schottky diode (~0.55V), $V_{IN(MAX)}$ is the maximum input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency (set by RT), and L is in the inductor value.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be about 30% higher. For robust operation in fault conditions (start-up or short circuit) and high input voltage (>30V), the saturation current should be above 3.5A. To keep the efficiency high, the series resistance (DCR) should be less than 0.1Ω, and the core material should be intended for high frequency applications. Table 1 lists several vendors and suitable types.

Table 1. Inductor Vendors

VENDOR	URL	PART SERIES	TYPE
Murata	www.murata.com	LQH55D	Open
TDK	www.componenttdk.com	SLF7045 SLF10145	Shielded Shielded
Toko	www.toko.com	D75C D75F FDV0620	Shielded Open Shielded
Sumida	www.sumida.com	CDRH74 CDRH6D38 CR75 CDRH8D43	Shielded Shielded Open Shielded
NEC	www.nec.tokin.com	PLC-0745	Shielded

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Of course, such a simple design guide will not always result in the optimum inductor for your application. A larger value inductor provides a slightly higher maximum load current and will reduce the output voltage ripple. If your load is lower than 2A, then you can decrease the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. There are several graphs in the Typical Performance Characteristics section of this data sheet that show the maximum load current as a function of input voltage and inductor value for several popular output voltages. Low inductance may result in discontinuous mode operation, which is okay but further reduces maximum load current. For details of maximum output current and discontinuous mode operation, see Linear Technology Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), there is a minimum inductance required to avoid subharmonic oscillations. See Application Note 19.

Input Capacitor

Bypass the input of the LT3681 circuit with a ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT3681 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3681 and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 4.7µF capacitor is capable of this task, but only if it is placed close to the LT3681 and the catch diode (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3681. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3681 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3681's voltage rating. This situation is easily avoided (see the Hot Plugging Safely section).

For space sensitive applications, a 2.2µF ceramic capacitor can be used for local bypassing of the LT3681 input. However, the lower input capacitance will result in increased input current ripple and input voltage ripple, and may couple noise into other circuitry. Also, the increased voltage ripple will raise the minimum operating voltage of the LT3681 to ~3.7V.

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3681 to produce the DC output. In this role it determines the output ripple, and low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT3681's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{100}{V_{OUT} f_{SW}}$$

where f_{SW} is in MHz, and C_{OUT} is the recommended output capacitance in µF. Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value capacitor if the compensation network is also adjusted to maintain the loop bandwidth. A lower value of output capacitor can be used to save space and cost but transient performance will suffer. See the Frequency Compensation section to choose an appropriate compensation network.

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Table 2. Capacitor Vendors

VENDOR	PHONE	URL	PART SERIES	COMMENTS
Panasonic	(714) 373-7366	www.panasonic.com	Ceramic, Polymer, Tantalum	EEF Series
Kemet	(864) 963-6300	www.kemet.com	Ceramic, Tantalum	T494, T495
Sanyo	(408) 749-9714	www.sanyovideo.com	Ceramic, Polymer, Tantalum	POSCAP
Murata	(408) 436-1300	www.murata.com	Ceramic	
AVX		www.avxcorp.com	Ceramic, Tantalum	TPS Series
Taiyo Yuden	(864) 963-6300	www.taiyo-yuden.com	Ceramic	

When choosing a capacitor, look carefully through the data sheet to find out what the actual capacitance is under operating conditions (applied voltage and temperature). A physically larger capacitor, or one with a higher voltage rating, may be required. High performance tantalum or electrolytic capacitors can be used for the output capacitor. Low ESR is important, so choose one that is intended for use in switching regulators. The ESR should be specified by the supplier, and should be 0.05Ω or less. Such a capacitor will be larger than a ceramic capacitor and will have a larger capacitance, because the capacitor must be large to achieve low ESR. Table 2 lists several capacitor vendors.

Catch Diode

The integral power Schottky catch diode conducts current only during switch off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{OUT} (V_{IN} – V_{OUT})/V_{IN}$$

where I_{OUT} is the output load current.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT3681 due to their piezoelectric nature. When in Burst Mode operation, the LT3681's switching frequency depends on the load current, and at very light loads the LT3681 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT3681 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT3681. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3681 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3681's rating. This situation is easily avoided (see the Hot Plugging Safely section).

Frequency Compensation

The LT3681 uses current mode control to regulate the output. This simplifies loop compensation. In particular, the LT3681 does not require the ESR of the output capacitor for stability, so you are free to use ceramic capacitors to achieve low output ripple and small circuit size. Frequency compensation is provided by the components tied to the V_C pin, as shown in Figure 2. Generally a capacitor (C_C) and a resistor (R_C) in series to ground are used. In addition, there may be a lower value capacitor in parallel. This capacitor (C_F) is not part of the loop compensation but is used to filter noise at the switching frequency, and is required only if a phase-lead capacitor is used or if the output capacitor has high ESR.

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Loop compensation determines the stability and transient performance. Designing the compensation network is a bit complicated and the best values depend on the application and in particular the type of output capacitor. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load. Figure 2 shows an equivalent circuit for the LT3681 control loop. The error amplifier is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switch and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C pin. Note that the output capacitor integrates this current, and that the capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. In most cases a zero is required and comes from either the output capacitor ESR or from a resistor R_C in series with C_C. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor (C_{PL}) across the feedback divider may improve the transient response. Figure 3 shows the transient response when the load current is stepped from 500mA to 1500mA and back to 500mA.

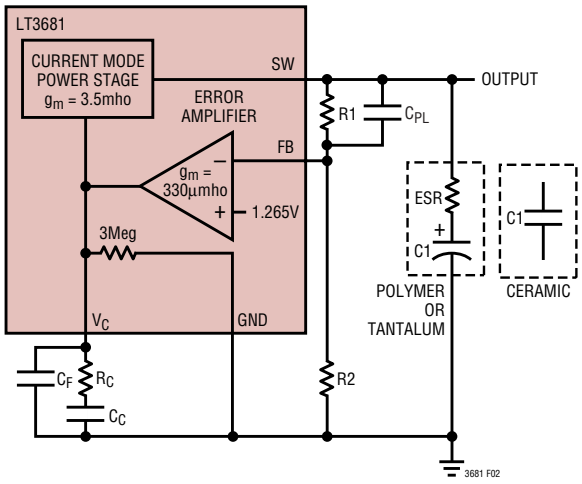

Figure 2. Model for Loop Response

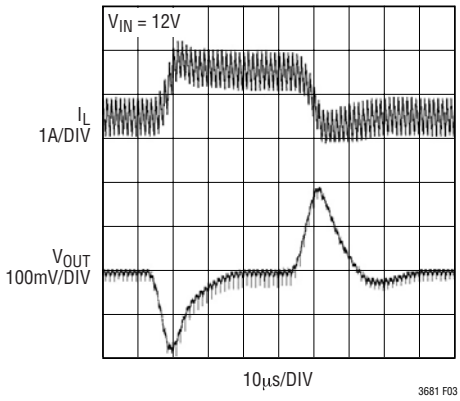

Figure 3. Transient Load Response of the LT3681 3.3V Application as the Load Current is Stepped from 500mA to 1500mA.

Burst Mode Operation

To enhance efficiency at light loads, the LT3681 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LT3681 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. In addition, V_{IN} and BIAS quiescent currents are reduced to typically 20µA and 50µA respectively during the sleep time. As the load current decreases towards a no load condition, the percentage of time that the LT3681 operates in sleep mode increases and the average input current is greatly reduced resulting in higher efficiency. See Figure 4.

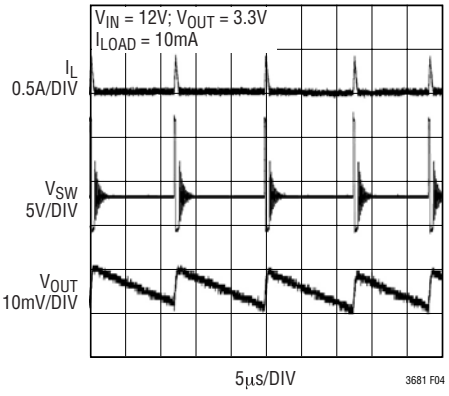

Figure 4. Burst Mode Operation

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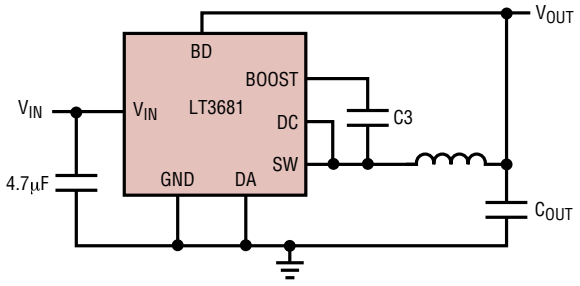
BOOST and BIAS Pin Considerations

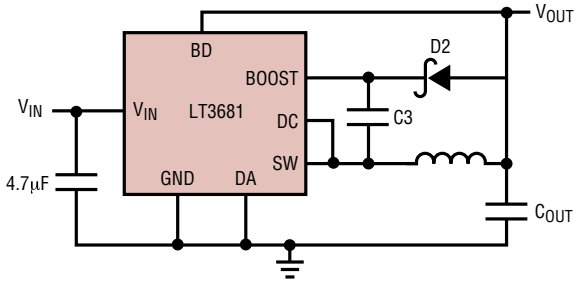
Capacitor C3 and the internal boost Schottky diode (see the Block Diagram) are used to generate a boost voltage that is higher than the input voltage. In most cases a 0.22µF capacitor will work well. Figure 5 shows three ways to arrange the boost circuit. The BOOST pin must be more than 2.3V above the SW pin for best efficiency. For outputs of 2.8V and above, the standard circuit (Figure 5a) is best. For outputs between 2.8V and 3V, use a 1µF boost capacitor. A 2.5V output presents a special case because it is marginally adequate to support the boosted drive stage while using the internal boost diode. For reliable BOOST pin operation with 2.5V outputs use a good external Schottky diode (such as the ON Semi MBR0540), and a 1µF boost capacitor (see Figure 5b). For lower output voltages the boost diode can be tied to the input (Figure 5c), or to another supply greater than 2.8V. The circuit in Figure 5a is more efficient because the BOOST pin current and BIAS pin quiescent current comes from a lower voltage source. You must also be sure that the maximum voltage ratings of the BOOST and BIAS pins are not exceeded.

The minimum operating voltage of an LT3681 application is limited by the minimum input voltage (3.6V) and by the maximum duty cycle as outlined in a previous section. For proper startup, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, or the LT3681 is turned on with its RUN/SS pin when the output is already in regulation, then the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages, and on the arrangement of the boost circuit. The minimum load generally goes to zero once the circuit has started. If, however, the LT3681 is started by the RUN/SS pin and the output is discharged, the discharged output capacitance will often present enough of a load to allow the circuit to start. Figure 6 gives plots of the input voltage required for three different situations: the worst case situation where RUN/SS is tied to V_{IN} and V_{IN} is ramped up very slowly, the minimum input voltage at which the circuit will regulate when start-up is controlled by RUN/SS, and the minimum input voltage required to maintain output regulation. For lower start-up voltage, the boost diode can be tied to V_{IN}; however, this restricts the input range to one-half of the absolute maximum rating of the BOOST pin.

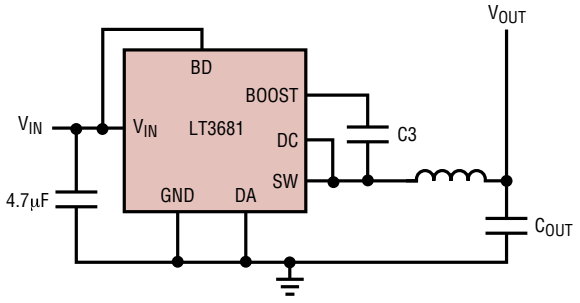
At light loads, the inductor current becomes discontinuous and the effective duty cycle at the BOOST pin (not the SW pin) can be very high. This reduces the minimum input voltage to approximately 300mV above V_{OUT}. At higher load currents, the inductor current is continuous and the duty cycle is limited by the maximum duty cycle of the LT3681, requiring a higher input voltage to maintain regulation.



(5a) For V_{OUT} > 2.8V



(5b) For 2.5V < V_{OUT} < 2.8V



(5c) For V_{OUT} < 2.5V

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Figure 5. Three Circuits For Generating The Boost Voltage

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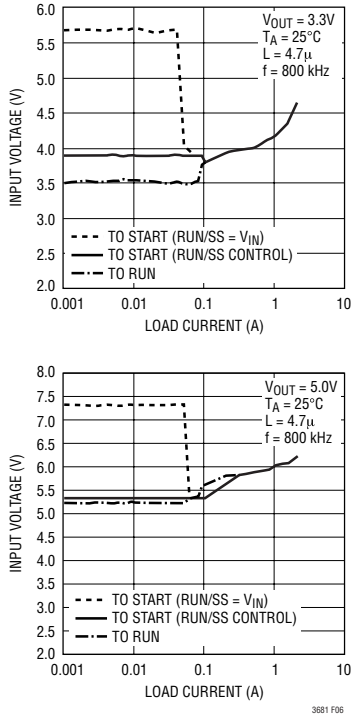

Figure 6. The Minimum Input Voltage Depends on Output Voltage, Load Current and Boost Circuit

Soft-Start

The RUN/SS pin can be used to soft-start the LT3681, reducing the maximum input current during start-up. The RUN/SS pin is driven through an external RC filter to create a voltage ramp at this pin. Figure 7 shows the start-up and shut-down waveforms with the soft-start circuit. By choosing a large RC time constant, the peak start-up current can be reduced to the current that is required to regulate the output, with no overshoot. Choose the value of the resistor so that it can supply 20µA when the RUN/SS pin reaches 2.3V.

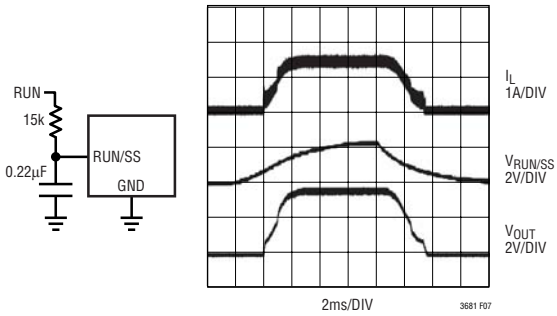

Figure 7. To Soft-Start the LT3681, Add a Resistor and Capacitor to the RUN/SS Pin

Synchronization

The internal oscillator of the LT3681 can be synchronized to an external 275kHz to 475kHz clock by using a 5pF to 20pF capacitor to connect the clock signal to the RT pin. The resistor tying the RT pin to ground should be chosen such that the LT3681 oscillates 20% lower than the intended synchronization frequency (see Setting the Switching Frequency section).

The LT3681 should not be synchronized until its output is near regulation as indicated by the PG flag. This can be done with the system microcontroller/microprocessor or with a discrete circuit by using the PG output. If a sync signal is applied while the PG is low, the LT3681 may exhibit erratic operation.

When applying a sync signal, positive clock transitions reset LT3681's internal clock and negative transitions initiate a switch cycle. The amplitude of the sync signal must be at least 2V. The sync signal duty cycle can range from 5% up to a maximum value given by the following equation:

$$DC_{SYNC(MAX)} = \left(1 - \frac{V_{OUT} + V_D}{V_{IN} - V_{SW} + V_D}\right) - f_{SW} \bullet 600ns$$

where V_{OUT} is the programmed output voltage, V_D is the diode forward drop, V_{IN} is the typical input voltage, V_{SW} is the switch drop, and f_{SW} is the desired switching frequency. For example, a 24V input to 5V output at 300kHz can be synchronized to a square wave with a maximum duty cycle of 60%. For some applications, such as $12V_{IN}$ to $5V_{OUT}$ at 350kHz, the maximum allowable sync duty cycle will be less than 50%. If a low duty cycle clock cannot be obtained from the system, then a one-shot should be used between the sync signal and the LT3681. The value of the coupling capacitor which connects the clock signal to the RT pin should be chosen based on the clock signal amplitude. Good starting values for 3.3V and 5V clock signals are 10pF and 5pF, respectively. These values should be tested and adjusted for each individual application to assure reliable operation.

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Caution should be used when synchronizing more than 50% above the initial switching frequency (as set by the RT resistor) because at higher clock frequencies the amplitude of the internal slope compensation used to prevent subharmonic switching is reduced. This type of subharmonic switching only occurs at input voltages less than twice output voltage. Higher inductor values will tend to reduce this problem.

Reversed Input Protection

In some systems, the output may be held high when the input to the LT3681 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LT3681's output. If the V_{IN} pin is allowed to float and the RUN/SS pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT3681's internal circuitry will pull its quiescent current through its SW pin. This is fine if your system can tolerate a few mA in this state. If you ground the RUN/SS pin, the SW pin current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LT3681 can pull large currents from the output through the SW pin and the V_{IN} pin. Figure 8 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

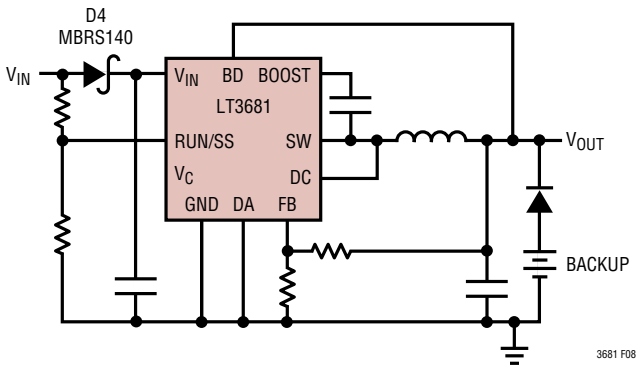

Figure 8. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LT3681 Runs Only When the Input is Present

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PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 9 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT3681's V_{IN} and SW pins, the integrated Schottky diode the input capacitor (C_{IN}) and the output capacitor (C_{OUT}). The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and V_C nodes small so that the ground traces will shield them from the SW and BOOST nodes. Each of the Exposed Pads on the bottom of the package must be soldered to copper pours so that the pad acts as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT3681 to additional ground planes within the circuit board and on the bottom side. Keep in mind that the thermal design must keep the junctions of the IC and power diode below the specified absolute maximum temperature of 125°C.

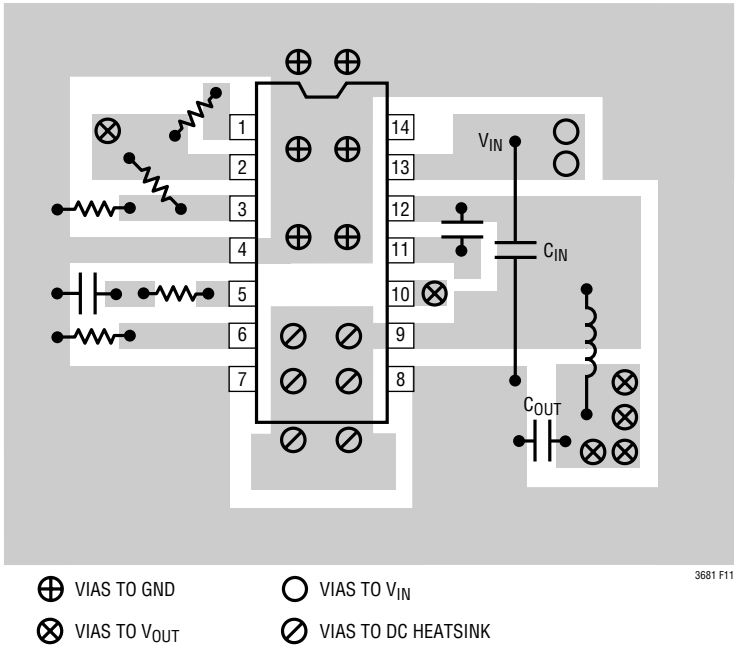

Figure 9. A Good PCB Layout Ensures Proper, Low EMI Operation

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Hot Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LT3681 circuits. However, these capacitors can cause problems if the LT3681 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor, combined with stray inductance in series with the power source, forms an under damped tank circuit, and the voltage at the V_{IN} pin of the LT3681 can ring to twice the nominal input voltage, possibly exceeding the LT3681's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LT3681 into an energized supply, the input network should be designed to prevent this overshoot. Figure 10 shows the waveforms that result when an LT3681 circuit is connected to a 24V supply through six feet of 24-gauge twisted pair. The first plot (10a) is the response with a 4.7µF ceramic capacitor at the input. The input voltage rings as high as 50V and the input current peaks at 26A. A good solution is shown in Figure 10b. A 0.7Ω resistor is added in series with the input to eliminate the voltage overshoot (it also reduces the peak inrush current). A 0.1µF capacitor improves high frequency filtering. For high input voltages its impact on efficiency is minor, reducing efficiency by 1.5 percent for a 5V output at full load operating from 24V. Another effective method of reducing the overshoot is to add a 22µF aluminum electrolytic capacitor, as shown in Figure 10c.

High Temperature Considerations

The PCB must provide heat sinking to keep the LT3681 cool. The Exposed Pads on the bottom of the package must be soldered to copper pours, which in turn should be tied to large copper layers below with thermal vias; these layers will spread the heat dissipated by the LT3681. Place additional vias to reduce thermal resistance further. With these steps, the thermal resistance from die (or junction) to ambient can be reduced to θ_{JA} = 35°C/W or less. With 100 LFPM airflow, this resistance can fall by another 25%. Further increases in airflow will lead to lower thermal resistance. Because of the large output current capability of the LT3681, it is possible to dissipate enough power to raise the junction temperature beyond the absolute maximum of 125°C. When operating at high ambient temperatures, the maximum load current should be derated as the ambient temperature approaches 125°C.

Power dissipation within the LT3681 can be estimated by calculating the total power loss from an efficiency measurement. The die temperature is calculated by multiplying the LT3681 power dissipation by the thermal resistance from junction to ambient.

Also keep in mind that the leakage current of the integrated power Schottky diode, like all Schottky diodes, goes up with junction temperature. The curves in Figure 11 show how the leakage current in the power Schottky diode varies with temperature and reverse voltage. When the power switch is closed, the power Schottky diode is in parallel with the power converter's output filter stage. As a result, an increase in a diode's leakage current results in an effective increase in the load, and a corresponding increase in input power.

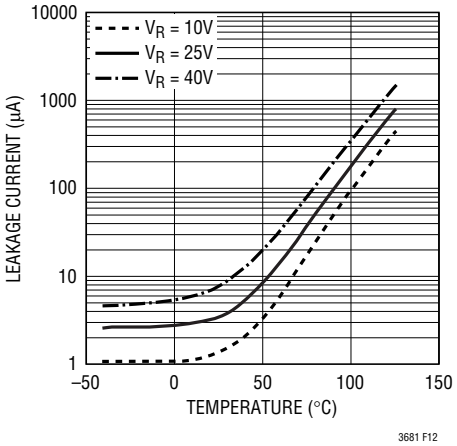


Figure 11. Like all Schottky Diodes, the LT3681 Integrated Power Diode Leakage Current Varies with Temperature and Applied Reverse Voltage V_R.

Other Linear Technology Publications

Application Notes 19, 35, 44 and 76 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design Note 100 shows how to generate a bipolar output supply using a buck regulator.

APPLICATIONS INFORMATION

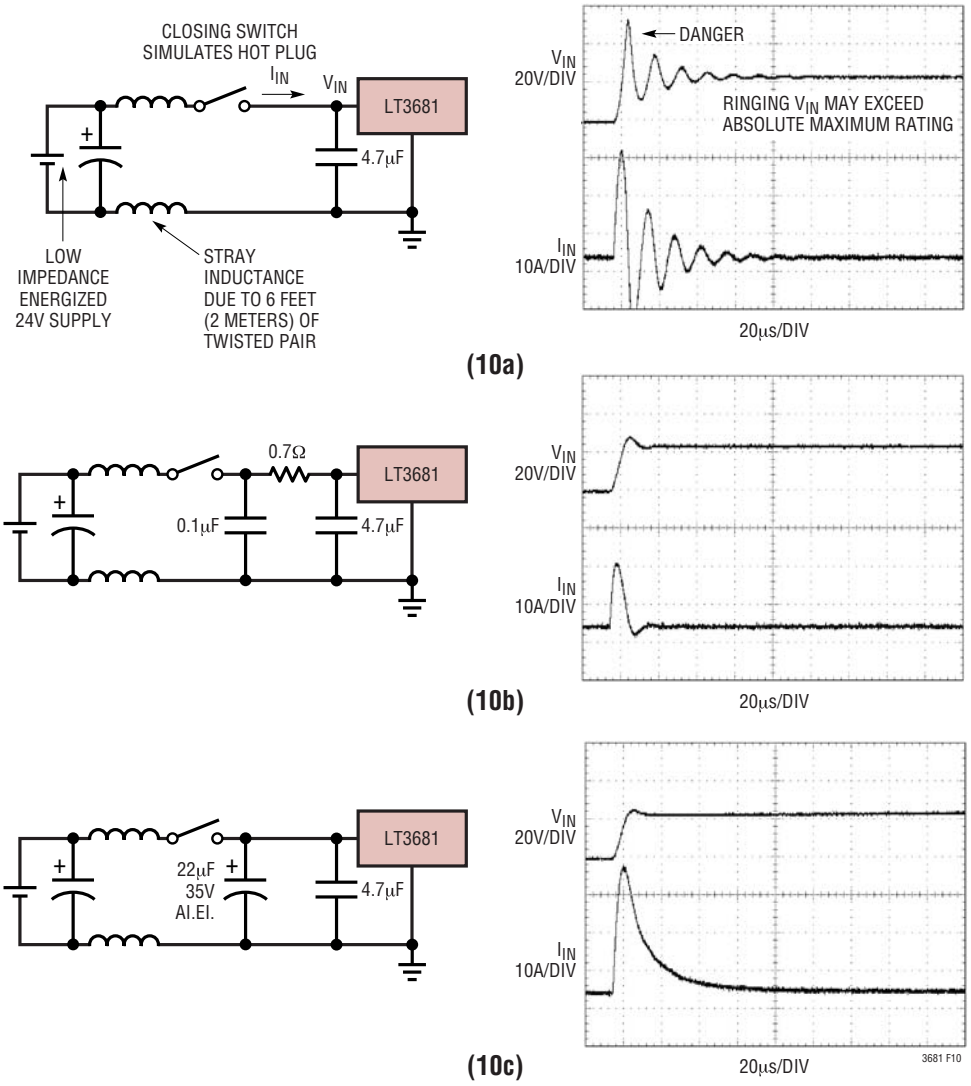
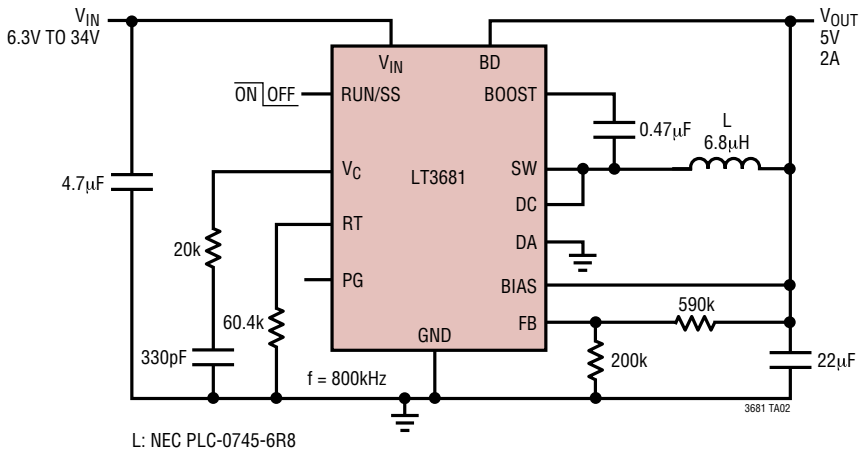


Figure 10. A Well Chosen Input Network Prevents Input Voltage Overshoot and Ensures Reliable Operation when the LT3681 is Connected to a Live Supply

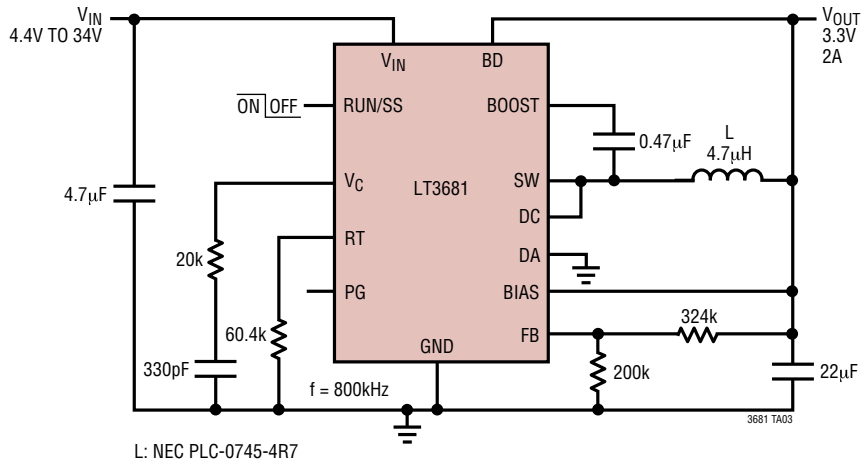
TYPICAL APPLICATIONS

5V Step-Down Converter



L: NEC PLC-0745-6R8

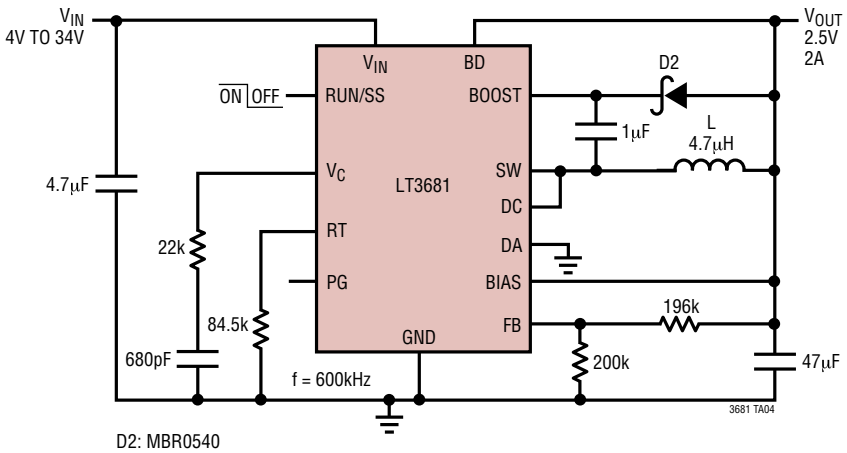
3.3V Step-Down Converter



L: NEC PLC-0745-4R7

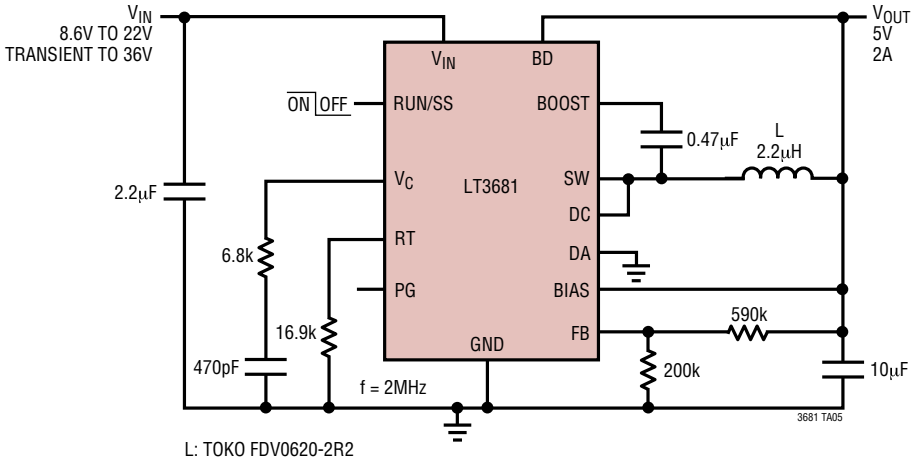
TYPICAL APPLICATIONS

2.5V Step-Down Converter



D2: MBR0540
L: SUMIDA CDRH8D43-4R7

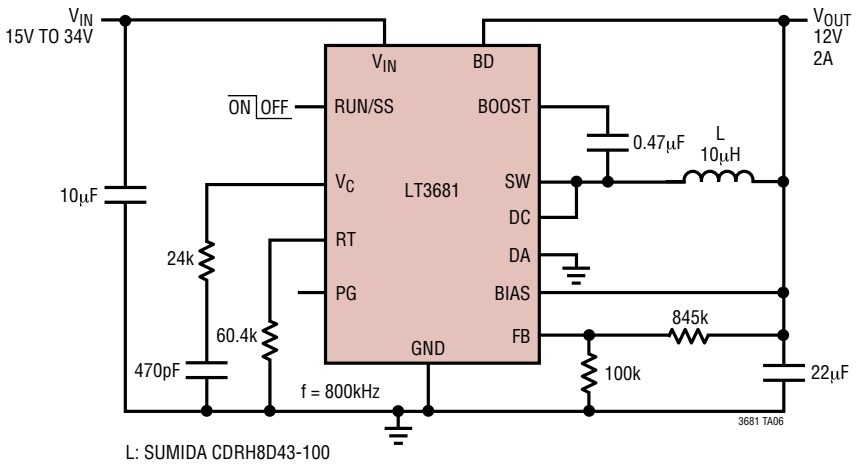
5V, 2MHz Step-Down Converter



L: TOKO FDV0620-2R2

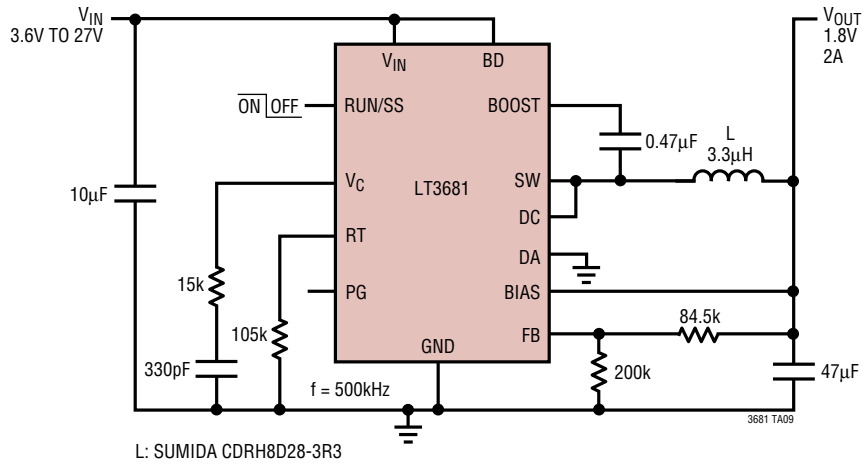
TYPICAL APPLICATIONS

12V Step-Down Converter



L: SUMIDA CDRH8D43-100

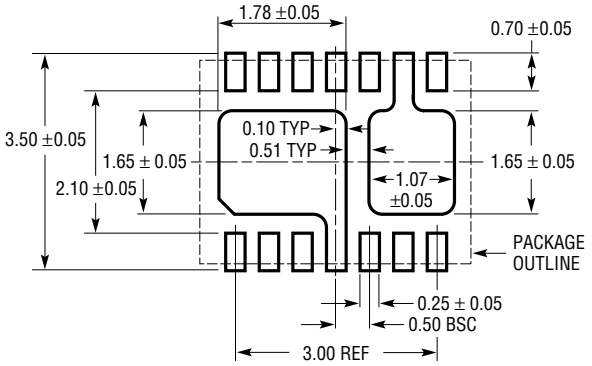
1.8V Step-Down Converter



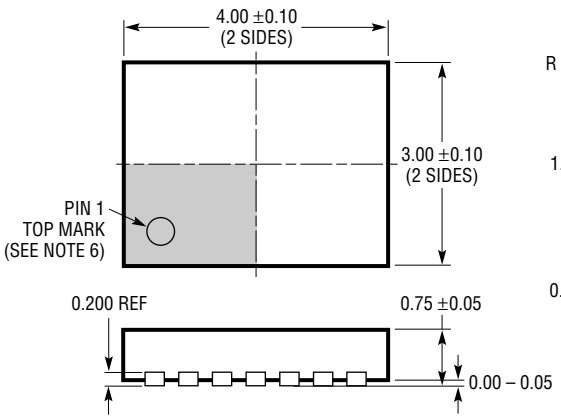
L: SUMIDA CDRH8D28-3R3

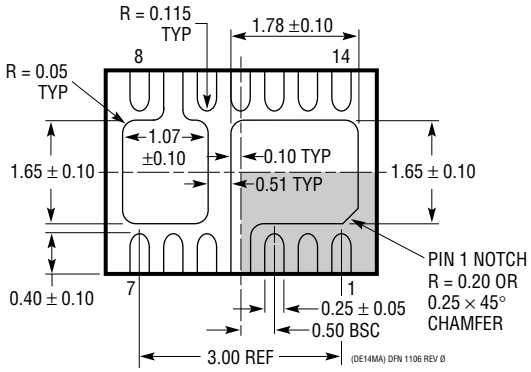
PACKAGE DESCRIPTION

DE14MA Package
14-Lead Plastic DFN, Multichip (4mm × 3mm)
(Reference LTC DWG # 05-08-1731 Rev 0)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



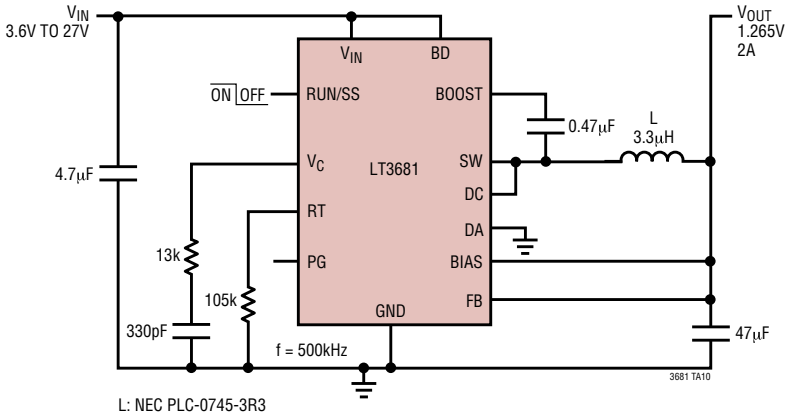


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

1.265V Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1766	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 5.5V to 60V, V_{OUT} = 1.20V, I_Q = 2.5mA, I_{SD} 25µA TSSOP16E Package
LT1767	25V, 1.2A (I_{OUT}), 1.2MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.0V to 25V, V_{OUT} = 1.20V, I_Q = 1mA, I_{SD} < 6µA MS8E Package
LT1933	500mA (I_{OUT}), 500kHz Step-Down Switching Regulator in SOT-23	V_{IN} = 3.6V to 36V, V_{OUT} = 1.2V, I_Q = 1.6mA, I_{SD} < 1µA ThinSOT Package
LT1936	36V, 1.4A (I_{OUT}), 500kHz High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 36V, V_{OUT} = 1.2V, I_Q = 1.9mA, I_{SD} < 1µA MS8E Package
LT1940	Dual 25V, 1.4A (I_{OUT}), 1.1MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 25V, V_{OUT} = 1.20V, I_Q = 3.8mA, I_{SD} < 30µA TSSOP16E Package
LT1976/LT1977	60V, 1.2A (I_{OUT}), 200kHz/500kHz, High Efficiency Step-Down DC/DC Converter with Burst Mode	V_{IN} = 3.3V to 60V, V_{OUT} = 1.20V, I_Q = 100µA, I_{SD} < 1µA TSSOP16E Package
LT3434/LT3435	60V, 2.4A (I_{OUT}), 200/500kHz, High Efficiency Step-Down DC/DC Converter with Burst Mode	V_{IN} = 3.3V to 60V, V_{OUT} = 1.20V, I_Q = 100µA, I_{SD} < 1µA TSSOP16E Package
LT3437	60V, 400mA (I_{OUT}), MicroPower Step-Down DC/DC Converter with Burst Mode	V_{IN} = 3.3V to 60V, V_{OUT} = 1.25V, I_Q = 100µA, I_{SD} < 1µA (3mm × 3mm) DFN-10 TSSOP16E Package
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} = 3.6V to 38V, V_{OUT} = 0.78V, I_Q = 70µA, I_{SD} < 1µA (3mm × 3mm) DFN-10 MSOP10E Package
LT3481	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} = 3.6V to 34V, V_{OUT} = 1.265V, I_Q = 50µA, I_{SD} < 1µA (3mm × 3mm) DFN-10 MSOP10E Package
LT3493	36V, 1.4A (I_{OUT}), 750kHz High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 36V, V_{OUT} = 0.8V, I_Q = 1.9mA, I_{SD} < 1µA (2mm × 3mm)DFN-6 Package
LT3505	36V with Transient Protection to 40V, 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 34V, V_{OUT} = 0.78V, I_Q = 2mA, I_{SD} < 2µA (3mm × 3mm) DFN-8 MSOP8E Package
LT3508	36V with Transient Protection to 40V, Dual 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.7V to 37V, V_{OUT} = 0.8V, I_Q = 4.6mA, I_{SD} < 1µA (4mm × 4mm) QFN-24 TSSOP16E Package
LT3684	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 34V, V_{OUT} = 01.26V, I_Q = 850mA, I_{SD} < 1µA (3mm × 3mm) DFN-10 MSOP10E Package
LT3685	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 38V, V_{OUT} = 0.78V, I_Q = 70mA, I_{SD} < 1µA (3mm × 3mm) DFN-10 MSOP10E Package

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