High Speed Comparator

FEATURES

- Ultrafast (5.5ns typ)
- Complementary ECL Output
- 50Ω Line Driving Capability
- Low Offset Voltage
- Output Latch Capability
- External Hysteresis Control
- Pin Compatible with Am685

APPLICATIONS

- High Speed A-to-D Converters
- High Speed Sampling Circuits
- Oscillators

DESCRIPTION

The LT®685 is an ultrafast comparator with differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving transmission lines terminated in 50Ω. The low input offset and high resolution make this comparator ideally suited for analog-to-digital signal processing applications.

A latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the comparator outputs are locked in their existing logical states. If the latch function is not used, the latch enable must be connected to ground or ECL high.

The device is pin-compatible with the Am685. Hysteresis has been added to improve switching time with slow input signals as well as to minimize oscillation. A single resistor between the hysteresis pin and V^- adds input hysteresis voltage as more current is drawn. If hysteresis is not required, the pin can be left unconnected.

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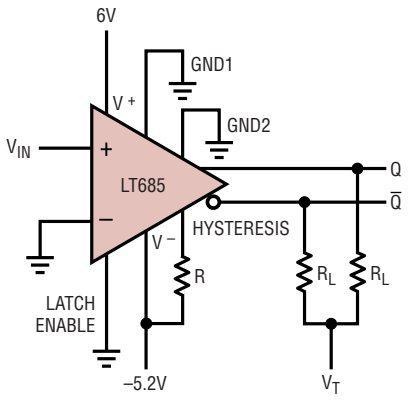
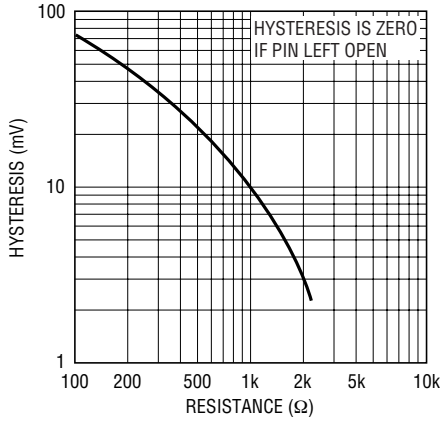
TYPICAL APPLICATION

Comparator with Hysteresis



LT685 • TA01

Hysteresis



LT685 • TA02

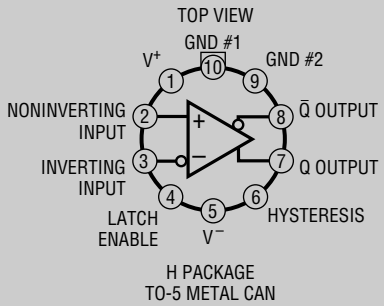
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Positive Supply Voltage 7V
Negative Supply Voltage ..... –7V
Input Voltage ..... ±4V
Differential Input Voltage ..... ±6V
Latch Pin Voltage ..... 2V to V^-
Hysteresis Pin Voltage ..... 0V to V^-

Output Current 30mA
Power Dissipation (Note 2) 500mW
Operating Temperature
LT685C ..... $-30°C \le T_A \le 85°C$
LT685M **(OBSOLETE)** ..... $-55°C \le T_A \le 125°C$

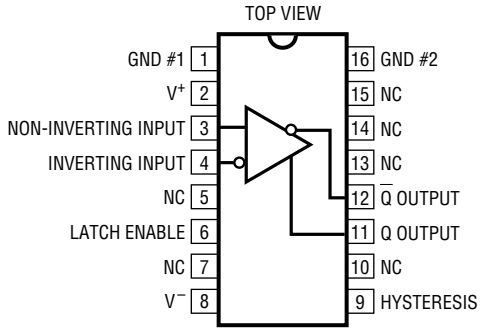
PACKAGE/ORDER INFORMATION



H PACKAGE
TO-5 METAL CAN

OBSOLETE PACKAGE
Consider the N16 Package as an Alternate Source

ORDER PART NUMBER
LT685CH
LT685MH



N16 PACKAGE
16-LEAD CERDIP

ORDER PART NUMBER
LT685CN

J16 PACKAGE (HERMETIC)
16-LEAD PDIP

OBSOLETE PACKAGE
Consider the N16 Package as an Alternate Source

ORDER PART NUMBER
LT685CJ
LT685MJ

LT685 • POI01

Consult LTC Marketing for parts specified with wider operating temperature ranges.

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ELECTRICAL CHARACTERISTICS

V^+ = 6.0V, V^- = –5.2V, V_T = –2V, R_L = 50Ω, R = ∞ over the operating temperature ranges, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT685C MIN	LT685C TYP	LT685C MAX	LT685M MIN	LT685M TYP	LT685M MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C		1.0	±2.0 ±2.5		1.0	±2.0 ±3.0	mV mV
dV_{OS}/dT	Input Offset Voltage Drift	(Note 3)			±10			±10	µV/°C
I_{OS}	Input Offset Current	T_A = 25°C		0.3	±1.0 ±1.3		0.3	±1.0 ±1.6	µA µA
I_B	Input Bias Current	T_A= 25°C		5	10 13		5	10 16	µA µA
R_{IN}	Input Resistance	T_A = 25°C (Note 3)	6.0			6.0			kΩ
C_{IN}	Input Capacitance	T_A = 25°C (Note 3)			3.0			3.0	pF
V_{CM}	Input Voltage Range				±3.3			±3.3	V
CMRR	Common Mode Rejection		80			80			dB
SVRR	Supply Voltage Rejection		70			70			dB
V_{OH}	Output High Voltage	T_A = 25°C $T_A = T_{MIN}$ $T_A = T_{MAX}$	–0.960 –1.060 –0.890		–0.810 –0.890 –0.700	–0.960 –1.100 –0.850		–0.810 –0.920 –0.620	V V V
V_{OL}	Output Low Voltage	T_A = 25°C $T_A = T_{MIN}$ $T_A = T_{MAX}$	–1.850 –1.890 –1.825		–1.650 –1.675 –1.625	–1.850 –1.910 –1.810		–1.650 –1.690 –1.575	V V V
I^+	Positive Supply Current				22			22	mA
I^-	Negative Supply Current				26			26	mA
P_{DISS}	Power Dissipation				300			300	mW

LINEAR TECHNOLOGY

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SWITCHING CHARACTERISTICS (V_{IN} = 100mV step, 5mV overdrive)

SYMBOL	PARAMETER	CONDITIONS	LT685C MIN	LT685C TYP	LT685C MAX	LT685M MIN	LT685M TYP	LT685M MAX	UNITS
t_{PD}	Propagation Delay (Note 4)	T_A = 25°C $T_A = T_{MAX}$ $T_A = T_{MIN}$	4.5 5.0 4.0	5.5	6.5 9.5 6.5	4.5 5.5 3.5	5.5	6.5 12 6.5	ns ns ns
$t_{PD(E)}$	Latch Enable to Output Delay (Note 3)	T_A = 25°C $T_A = T_{MAX}$ $T_A = T_{MIN}$	4.5 5.0 4.0	5.5	6.5 9.5 6.5	4.5 5.5 3.5	5.5	6.5 12 6.5	ns ns ns
t_S	Minimum Set-Up Time (Note 3)	$T_{MIN} \le T_A \le$ 25°C $T_A = T_{MAX}$			3.0 4.0			3.0 6.0	ns ns
t_H	Minimum Hold Time (Note 3)	$T_{MIN} \le T_A \le T_{MAX}$			1.0			1.0	ns
$t_{PW(E)}$	Minimum Latch Enable Pulse Width (Note 3)	$T_{MIN} \le T_A \le$ 25°C $T_A = T_{MAX}$			3.0 4.0			3.0 5.0	ns ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: For the metal can package, derate at 6.8mW/°C for operation at ambient temperatures above 100°C; for the hermetic dual-in-line package, derate at 9mW/°C for operation at ambient temperatures above 105°C.

Note 3: Guaranteed by design, but not tested.

Note 4: Sample tested at 25°C only.

Definitions:

t_{PD}: The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of the output transition.

$t_{PD(E)}$: The propagation delay measured from the 50% point of the latch enable signal positive transition to the 50% point of the output transition.

t_S: The minimum time before the negative transition of the latch enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_H: The minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{PW\ (E)}$: The minimum time that the latch enable signal must be HIGH in order to acquire and hold an input signal change.

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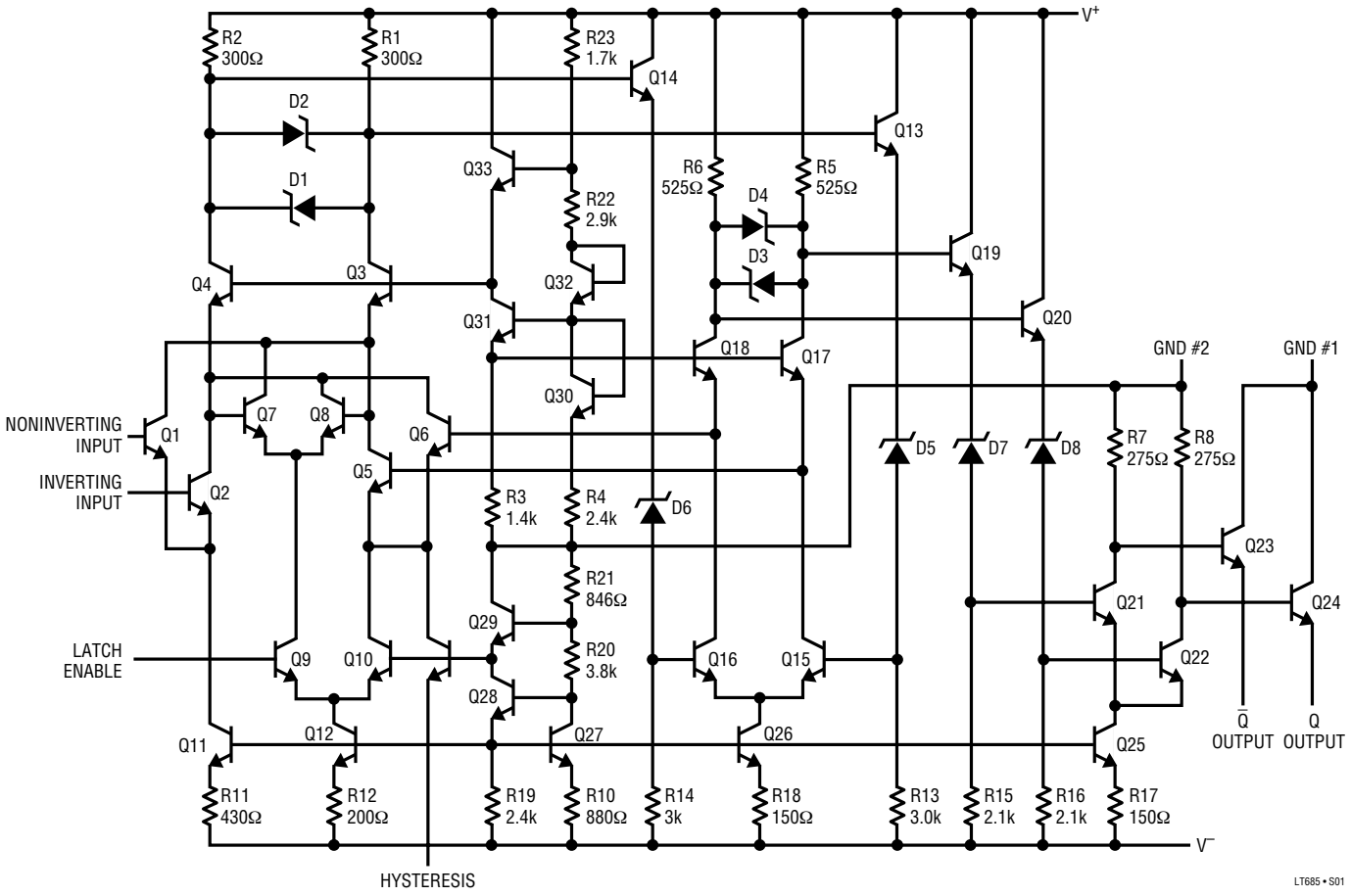
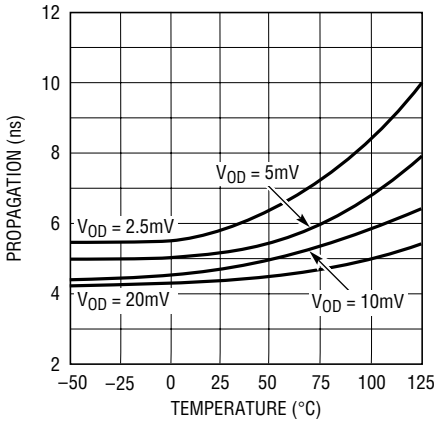
SCHEMATIC DIAGRAM



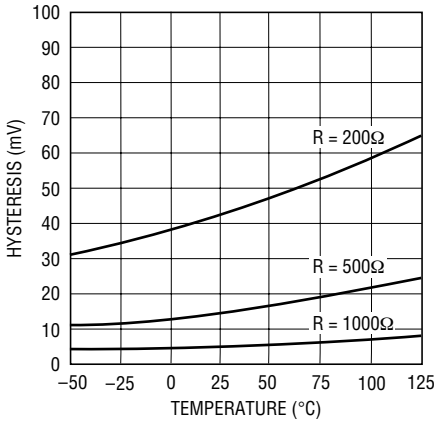
TYPICAL PERFORMANCE CHARACTERISTICS

Propagation Delays as a Function of Temperature



LTC685 • TPC01

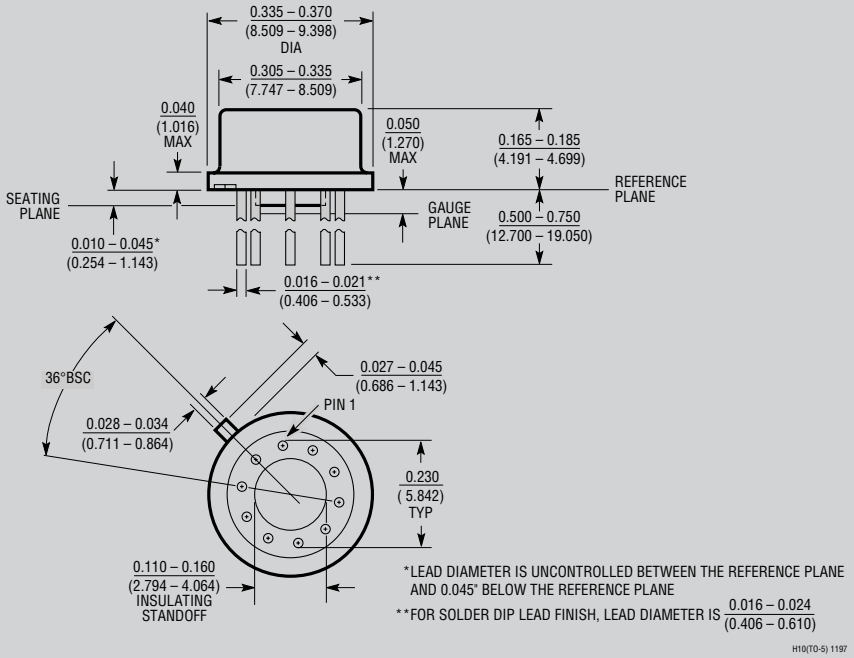
Hysteresis as a Function of Temperature



LTC685 • TPC02

PACKAGE DESCRIPTION

H Package
10-Lead TO-5 Metal Can
(Reference LTC DWG # 05-08-1322)



*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

H10(TO-5) 1197

OBSOLETE PACKAGE

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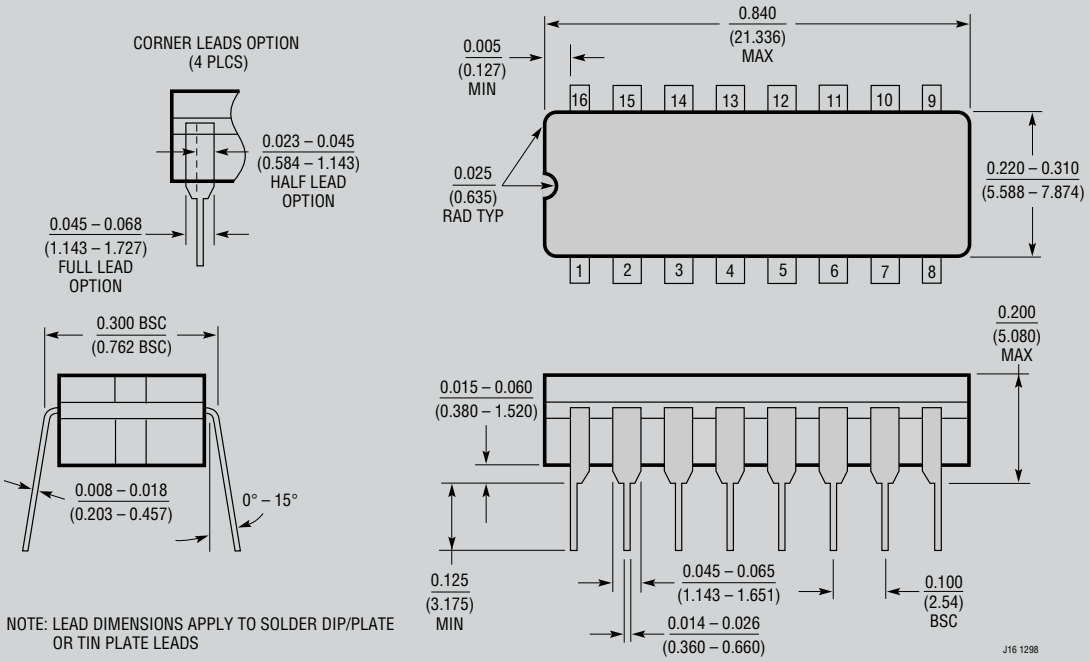
PACKAGE DESCRIPTION

J Package
16-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

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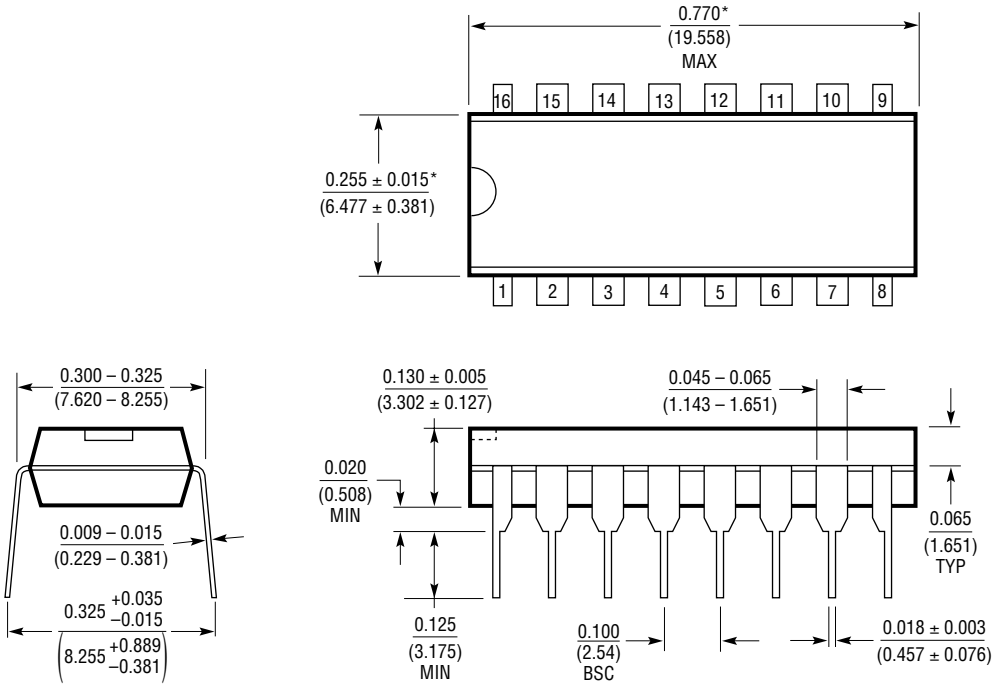
PACKAGE DESCRIPTION

N Package
16-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N16 1098

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