LTC1064-3

Low Noise, High Frequency, 8th Order Linear Phase Lowpass Filter

FEATURES

- 8th Order Filter in a 14-Pin Package
- 95kHz Maximum Corner Frequency
- No External Components
- 75:1, 150:1 and 120:1 Clock to Cutoff Frequency Ratio
- $60\mu V_{RMS}$ Total Wideband Noise
- 0.03% THD or Better
- Operates from ±2.37V to ±8V Power Supplies
- Low Total Output DC Offset

APPLICATIONS

- Antialiasing Filters
- Smoothing Filters
- Tracking High Frequency Lowpass Filters

DESCRIPTION

The LTC®1064-3 is a monolithic 8th order lowpass Bessel filter, which provides a linear phase response over its entire passband. An external TTL or CMOS clock programs the filter's cutoff frequency. The clock to cutoff frequency ratio is 75:1 (Pin 10 at V^+) or 150:1 (Pin 10 at V^-) or 120:1 (Pin 10 at GND). The maximum cutoff frequency is 95kHz. No external components are needed.

The LTC1064-3 features low wideband noise and low harmonic distortion even for input voltages up to $3V_{RMS}$. In fact the LTC1064-3 overall performance competes with equivalent multiple op amp RC active realizations. The LTC1064-3 is available in a 14-pin DIP or 16-pin surface mounted SOL package. The LTC1064-3 is fabricated using LTC's enhanced analog CMOS Si-gate process.

The LTC1064-3 is pin compatible with the LTC1064-1, LTC1064-2 and LTC1064-4.

*LT*, LTC and LT are registered trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

8th Order Clock Sweepable Lowpass Bessel Filter
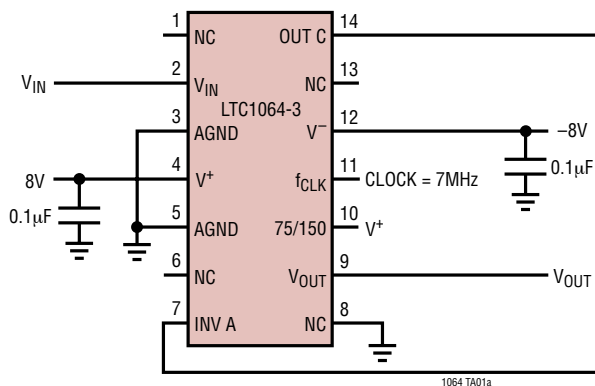
NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1μF OR LARGER CAPACITOR CLOSE TO THE PACKAGE. THE CONNECTION BETWEEN PIN 7 AND PIN 14 SHOULD BE MADE UNDER THE IC PACKAGE.

Measured Frequency Response

$V_S = \pm7.5V$, $f_{CLK} = 7MHz$, PIN 10 TO V^+, $f_{-3dB} = 95kHz$, GROUP DELAY = 6μs

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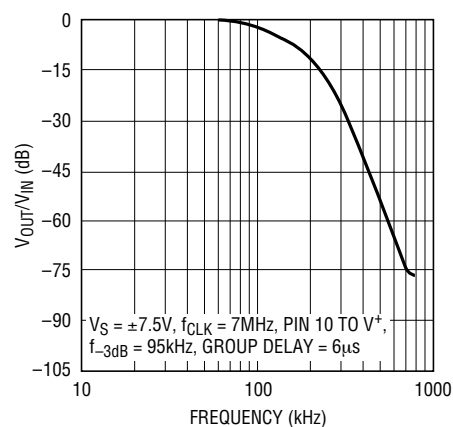
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V⁺ to V⁻) 16.5V
Power Dissipation 400mW
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

Operating Temperature Range
   LTC1064-3M **(OBSOLETE)** .... −55°C to 125°C
   LTC1064-3C .... −40°C to 85°C
Input Voltage .... (V⁺ +0.3V) to V⁻ −0.3V
Burn-In Voltage 15V

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER
NC [1] ... [14] OUT C V$_{IN}$ [2] ... [13] NC AGND [3] ... [12] V⁻ V⁺ [4] ... [11] f$_{CLK}$ AGND [5] ... [10] 75/150 NC [6] ... [9] V$_{OUT}$ R$_{IN}$ A [7] ... [8] NC N PACKAGE 14-LEAD PDIP T$_{JMAX}$ = 110°C, θ$_{JA}$ = 70°C/W	LTC1064-3CN
J PACKAGE 14-LEAD CERDIP **OBSOLETE PACKAGE** Consider the N 14 Package for Alternate Source	LTC1064-3MJ LTC1064-3CJ

TOP VIEW	ORDER PART NUMBER
NC [1] ... [16] OUT C V$_{IN}$ [2] ... [15] NC AGND [3] ... [14] V⁻ V⁺ [4] ... [13] NC AGND [5] ... [12] f$_{CLK}$ NC [6] ... [11] 75/150 NC [7] ... [10] NC R$_{IN}$ A [8] ... [9] V$_{OUT}$ SW PACKAGE 16-LEAD PLASTIC (WIDE) SO T$_{JMAX}$ = 150°C, θ$_{JA}$ = 90°C/W	LTC1064-3CSW

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T$_A$ = 25°C. V$_S$ = ±7.5V, 75:1, f$_{CLK}$ = 2MHz, R1 = 10k, TTL or CMOS clock input level unless otherwise specified.

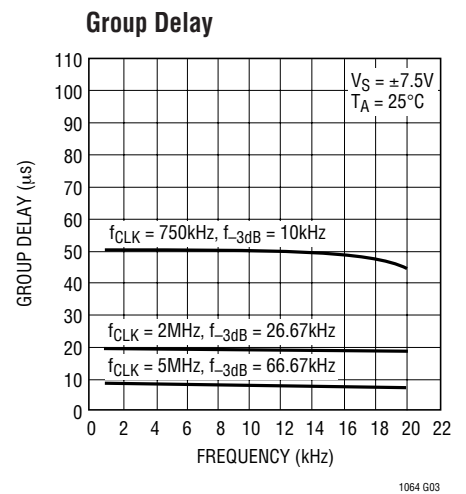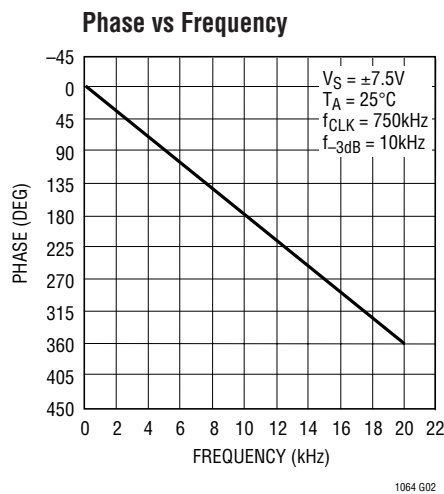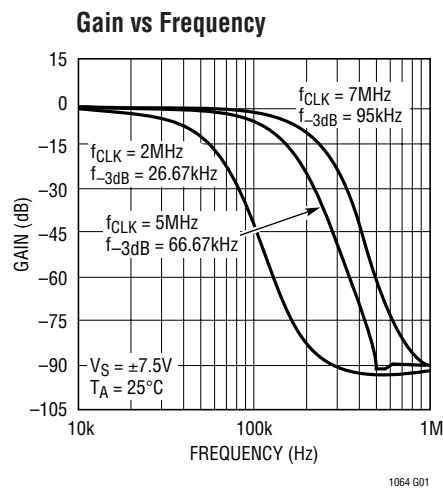| PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	Referenced to 0dB, 1Hz to 1kHz	●	−0.5		0.15	dB
Gain TempCo				0.0002		dB/°C
−3dB Frequency	50:1 (f$_{CLK}$ /f$_{−3dB}$ = 75)			26.67		kHz
	100:1 (f$_{CLK}$ /f$_{−3dB}$ = 150)			13.34		kHz
Gain at −3dB Frequency	Referenced to 0dB, f$_{IN}$ = 26.67/13.34kHz	●	−3.8		−2.75	dB
Stopband Attenuation	At 3f$_{−3dB}$	●	−25	−29		dB
Stopband Attenuation	At 5f$_{−3dB}$	●	−56	−60		dB
Stopband Attenuation	At 7f$_{−3dB}$			−84		dB
Input Frequency Range	100:1		0		<f$_{CLK}$/2	kHz
	50:1		0		<f$_{CLK}$	kHz
Output Voltage Swing and	V$_S$ = ±2.37V	●	±1.1			V
Operating Input Voltage Range	V$_S$ = ±5V	●	±3.1			V
	V$_S$ = ±7.5V	●	±5			V
Total Harmonic Distortion	V$_S$ = ±5V, Input = 1V$_{RMS}$ at 1kHz			0.015		%
	V$_S$ = ±7.5V, Input = 3V$_{RMS}$ at 1kHz			0.03		%
Wideband Noise	V$_S$ = ±5V, Input = GND 1Hz − 1.99MHz			55		μV$_{RMS}$
	V$_S$ = ±7.5V, Input = GND 1Hz − 1.99MHz			60		μV$_{RMS}$

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ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±7.5V, 75:1, f_{CLK} = 2MHz, R1 = 10k, TTL or CMOS clock input level unless otherwise specified.

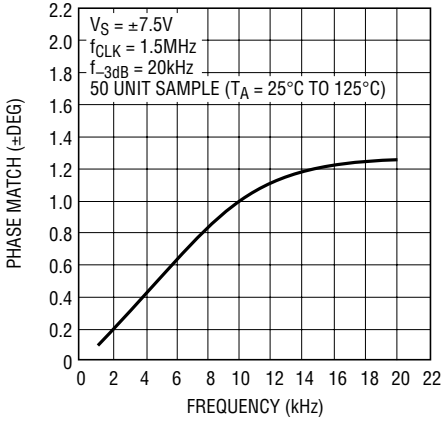| PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output DC Offset	V_S = ±7.5V			±30	±150	mV
Output DC Offset TempCo	V_S = ±5V			±20		μV/°C
	V_S = ±7.5V			±50		μV/°C
Input Impedance			14	22		kΩ
Output Impedance	f_{OUT} = 10kHz			2		Ω
Output Short-Circuit Current	Source/Sink			3/1		mA
Clock Feedthrough				200		μV$_{RMS}$
Maximum Clock Frequency	V_S ≥ ±7V, 50% Duty Cycle				5	MHz
	V_S ≥ ±7V, 50% Duty Cycle, T_A = <55°C				7	MHz
Power Supply Current	V_S = ±2.37V, f_{CLK} = 1MHz	●		10	22	mA
	V_S = ±5V, f_{CLK} = 1MHz			12	23	mA
		●			26	mA
	V_S = ±7.5V, f_{CLK} = 1MHz			16	28	mA
		●			32	mA
Power Supply Voltage Range		●	±2.37		±8	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
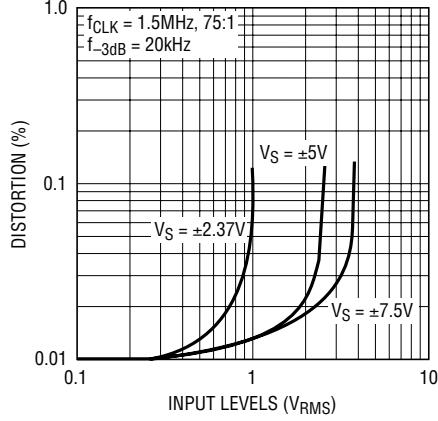
TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency

Phase vs Frequency

Group Delay

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TYPICAL PERFORMANCE CHARACTERISTICS

Phase Matching

$V_S = \pm7.5V$
$f_{CLK} = 1.5MHz$
$f_{-3dB} = 20kHz$
50 UNIT SAMPLE ($T_A = 25°C$ TO $125°C$)

PHASE MATCH (±DEG) vs FREQUENCY (kHz)

1064 G04

Total Harmonic Distortion

$f_{CLK} = 1.5MHz$, 75:1
$f_{-3dB} = 20kHz$

$V_S = \pm5V$
$V_S = \pm2.37V$
$V_S = \pm7.5V$

DISTORTION (%) vs INPUT LEVELS (V_{RMS})

1064 G05

Power Supply Current vs Power Supply Voltage

$f_{CLK} = 1MHz$

$T_A = -55°C$
$T_A = 25°C$
$T_A = 125°C$

POWER SUPPLY CURRENT (mA) vs TOTAL POWER SUPPLY VOLTAGE (V)
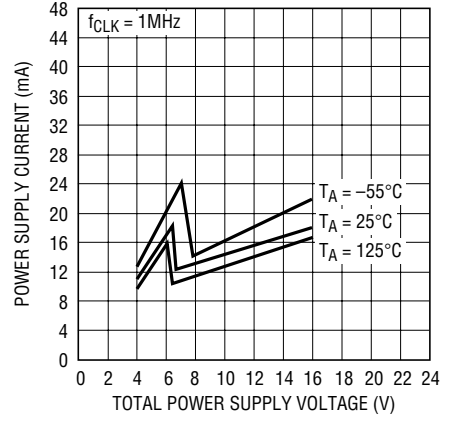
1064 G06

Transient Response
Input $10V_{P-P}$ Square Wave
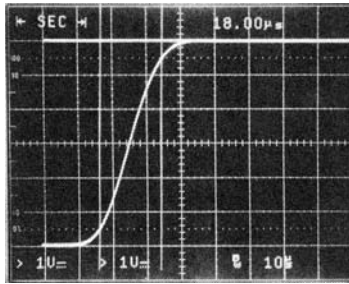$V_S = \pm7.5V$, Pin 10 to V^+,
$f_{CLK} = 1.5MHz$

Table 1. Wideband Noise (μV_{RMS})

Pin 10 to	f_{CLK}/f_{-3dB}	$V_S = \pm2.37V$ Noise μV_{RMS}	$V_S = \pm5V$ Noise μV_{RMS}	$V_S = \pm7.5V$ Noise μV_{RMS}
V^+	75/1	50	55	60
V^-	150/1	52	58	62
GND	120/1	45	50	54

TYPICAL PERFORMANCE CHARACTERISTICS

Table 2. Gain/Phase, f$_{-3dB}$ = 1kHz, LTC1064-3 Typical Response
V$_S$ = ±5V, T$_A$ = 25°C, f$_{CLK}$ = 75kHz, Pin 10 at V$^+$ (fltr 75:1)

FREQUENCY (kHz)	GAIN (dB)	PHASE (deg)
0.500	−0.858	−90.430
1.000	−2.990	179.200
1.500	−6.840	89.600
2.000	−12.780	3.800
2.500	−20.800	−71.000
3.000	−29.900	−129.600
3.500	−38.800	−173.700
4.000	−47.100	152.600
4.500	−54.700	126.000
5.000	−61.600	103.300
5.500	−68.000	85.190
6.000	−73.840	69.060
6.500	−79.250	54.780
7.000	−84.230	42.440
7.500	−88.940	30.060
8.000	−93.360	21.300
8.500	−97.510	10.000
9.000	−100.880	1.520
9.500	−105.780	−7.820

Table 3. Gain/Delay, f$_{-3dB}$ = 1kHz, LTC1064-3 Typical Response
V$_S$ = ±5V, T$_A$ = 25°C, f$_{CLK}$ = 75kHz, Pin 10 at V$^+$ (fltr 75:1)

FREQUENCY (kHz)	GAIN (dB)	DELAY (ms)
0.200	−0.281	0.502
0.300	−0.420	0.503
0.400	−0.610	0.503
0.500	−0.860	0.502
0.600	−1.160	0.502
0.700	−1.530	0.502
0.800	−1.950	0.503
0.900	−2.430	0.503
1.000	−2.990	0.500
1.100	−3.610	0.500
1.200	−4.300	0.500
1.300	−5.060	0.498
1.400	−5.920	0.495
1.500	−6.830	0.491
1.600	−7.840	0.489
1.700	−8.930	0.481
1.800	−10.130	0.473
1.900	−11.410	0.465
2.000	−12.780	0.454

Table 4. Gain/Phase, f$_{-3dB}$ = 1kHz, LTC1064-3 Typical Response
V$_S$ = ±5V, T$_A$ = 25°C, f$_{CLK}$ = 150kHz, Pin 10 at V$^-$ (fltr 150:1)

FREQUENCY (kHz)	GAIN (dB)	PHASE (deg)
0.500	−0.955	−88.100
1.000	−3.380	−175.300
1.500	−7.570	99.700
2.000	−13.770	20.100
2.500	−21.800	−48.000
3.000	−30.700	−100.700
3.500	−39.400	−139.900
4.000	−47.600	−169.200
4.500	−55.100	168.300
5.000	−61.900	150.300
5.500	−68.260	135.830
6.000	−74.050	123.660
6.500	−79.450	113.440
7.000	−84.330	104.440
7.500	−89.010	97.670
8.000	−93.250	91.580
8.500	−97.340	84.670
9.000	−101.390	74.600
9.500	−104.980	75.990

Table 5. Gain/Delay, f$_{-3dB}$ = 1kHz, LTC1064-3 Typical Response
V$_S$ = ±5V, T$_A$ = 25°C, f$_{CLK}$ = 150kHz, Pin 10 at V$^-$ (fltr 150:1)

FREQUENCY	GAIN (dB)	DELAY (ms)
0.200	−0.284	0.490
0.300	−0.450	0.489
0.400	−0.670	0.489
0.500	−0.960	0.487
0.600	−1.310	0.487
0.700	−1.730	0.485
0.800	−2.210	0.484
0.900	−2.750	0.482
1.000	−3.380	0.478
1.100	−4.070	0.478
1.200	−4.820	0.475
1.300	−5.660	0.470
1.400	−6.580	0.467
1.500	−7.570	0.463
1.600	−8.640	0.456
1.700	−9.790	0.448
1.800	−11.050	0.438
1.900	−12.360	0.428
2.000	−13.770	0.417

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LTC1064-3

TYPICAL PERFORMANCE CHARACTERISTICS

Table 6. Gain/Phase, f_{-3dB} = 1kHz, LTC1064-3 Typical Response $V_S = \pm 5V$, $T_A = 25°C$, f_{CLK} = 120kHz, Pin 10 at GND (fltr 120:1)

FREQUENCY (kHz)	GAIN (dB)	PHASE (deg)
0.500	−0.994d	−82.210
1.000	−3.050	−162.800
1.500	−6.520	116.700
2.000	−12.180	40.200
2.500	−19.460	−23.600
3.000	−27.200	−74.000
3.500	−34.700	−114.200
4.000	−41.900	−146.800
4.500	−48.700	−173.300
5.000	−55.100	164.700
5.500	−60.900	145.800
6.000	−66.500	130.610
6.500	−71.660	117.130
7.000	−76.390	105.880
7.500	−80.910	96.140
8.000	−84.900	87.510
8.500	−88.750	81.380
9.000	−92.410	78.190
9.500	−98.290	52.860

Table 7. Gain/Delay, f_{-3dB} = 1kHz, LTC1064-3 Typical Response $V_S = \pm 5V$, $T_A = 25°C$, f_{CLK} = 120kHz, Pin 10 at GND (fltr 120:1)

FREQUENCY (kHz)	GAIN (dB)	DELAY (ms)
0.200	−0.354	0.458
0.300	−0.520	0.456
0.400	−0.730	0.454
0.500	−1.000	0.452
0.600	−1.320	0.449
0.700	−1.670	0.448
0.800	−2.090	0.446
0.900	−2.540	0.446
1.000	−3.050	0.445
1.100	−3.600	0.446
1.200	−4.220	0.449
1.300	−4.900	0.448
1.400	−5.670	0.447
1.500	−6.520	0.446
1.600	−7.470	0.441
1.700	−8.500	0.432
1.800	−9.650	0.422
1.900	−10.870	0.409
2.000	−12.180	0.395

Table 8. Gain/Phase, f_{-3dB} = 20kHz, LTC1064-3 Typical Response $V_S = \pm 7.5V$, f_{CLK} = 1.5MHz, Pin 10 at V⁺(fltr 75:1)

$T_A = 25°C$			$T_A = 125°C$		
FREQUENCY (kHz)	GAIN (dB)	PHASE (deg)	FREQUENCY (kHz)	GAIN (dB)	PHASE (deg)
10.000	−0.912	−92.270	10.000	−0.944	−92.880
20.000	−3.090	176.000	20.000	−3.170	175.500
30.000	−6.910	85.500	30.000	−6.910	85.700
40.000	−12.710	−1.200	40.000	−12.450	−0.600
50.000	−20.500	−77.800	50.000	−19.920	−78.000
60.000	−29.400	−138.700	60.000	−28.500	−140.700
70.000	−38.300	174.600	70.000	−37.200	170.500
80.000	−46.500	138.300	80.000	−45.300	132.200
90.000	−54.000	109.100	90.000	−52.700	100.900
100.000	−61.000	84.800	100.000	−59.600	74.900
110.000	−67.310	64.040	110.000	−65.900	52.600
120.000	−73.170	46.260	120.000	−71.750	32.850
130.000	−78.600	31.120	130.000	−77.170	15.840
140.000	−83.760	18.050	140.000	−82.370	1.130
150.000	−88.630	7.770	150.000	−87.400	−11.380

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PIN FUNCTIONS (Pin Numbers Refer to the 14-Pin Package)

NC (Pins 1, 6, 8 and 13): The "no connection" pins should be preferably grounded. These pins are not internally connected.

V_{IN}, V_{OUT} (Pins 2, 9): The input Pin 2 is connected to an 18k resistor tied to the inverting input of an op amp. Pin 2 is protected against static discharge. The device's output, Pin 9, is the output of an op amp which can typically source/sink 3mA/1mA. Although the internal op amps are unity gain stable, driving long coax cables is not recommended.

When testing the device for noise and distortion, the output, Pin 9, should be buffered (Figure 1). *The op amp power supply wire (or trace) should be connected directly to the power source. To eliminate switching transients from filter output, buffer filter output with a third order lowpass (see Figure 5).*

AGND (Pins 3, 5): For dual supply operation these pins should be connected to a ground plane. For single supply operation both pins should be tied to one half supply (Figure 3).

V^+, V^- (Pins 4, 12): Should be bypassed with a 0.1μF capacitor to an adequate analog ground. Low noise, nonswitching power supplies are recommended. *To avoid latchup when the power supplies exhibit high turn-on transients, a 1N5817 Schottky diode should be added from the V^+ and V^- pins to ground (Figure 1, 2 and 3).*

R_{IN} A, OUT C (Pins 7, 14): A very short connection between Pin 7 and Pin 14 is recommended. This connection should be preferably done under the IC package. In a breadboard, use a one inch, or less, shielded coaxial cable: the shield should be grounded. In a PC board, use a one inch trace or less; surround the trace by a ground plane.

50/100 (Pin 10): Ratio Pin. The DC level at this pin determines the ratio of clock frequency to the −3dB frequency of the filter. The ratio is 75:1 when Pin 10 is at V^+, 120:1 when Pin 10 is at GND and 150:1 when Pin 10 is at V^-. This pin should be bypassed with a 0.1μF capacitor to analog ground when it's connected to V^- or V^+ (Figure 1). See Tables 2 through 8 for typical gain and delay responses for the three ratios.

f_{CLK} (Pin 11): For ±5V supplies the logic threshold level is 1.4V. For ±8V and 0V to 5V supplies the logic threshold levels are 2.2V and 3V respectively. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 200ns. The maximum clock frequency for ±5V supplies is 4MHz. For ±7V supplies and above, the maximum clock frequency is 7MHz. Do not allow the clock levels to exceed the power supplies. For single supply operation ≥6V use level shifting at Pin 11 with T^2L levels (see Figure 4).

TYPICAL APPLICATIONS

RECOMMENDED OP AMPS:
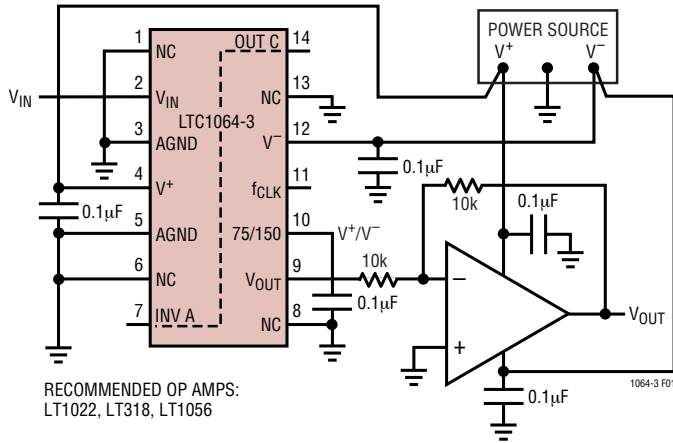LT1022, LT318, LT1056

Figure 1. Buffering the Filter Output. The Buffer Op Amp Should Not Share the LTC1064-3 Power Lines
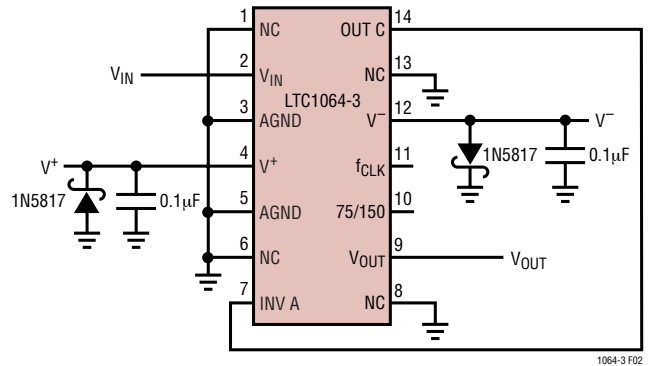

Figure 2. Using Schottky Diodes to Protect the IC from Power Supply Reversal
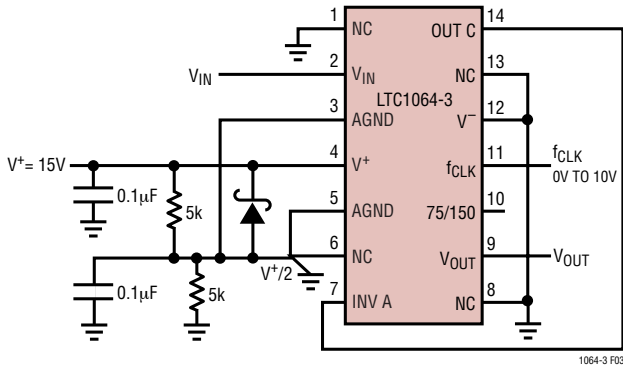

Figure 3. Single Supply Operation. If Fast Power Up or Down Transients are Expected, Use a 1N5817 Schottky Diode Between Pin 4 and Pin 5
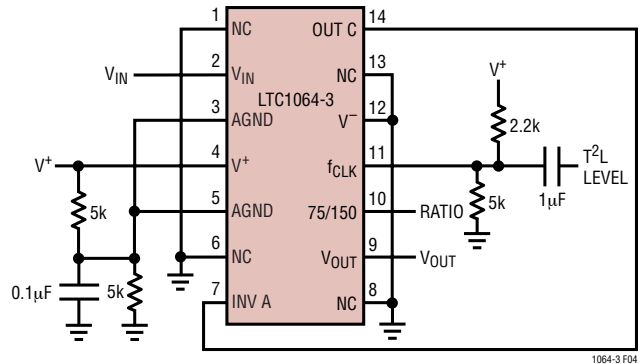

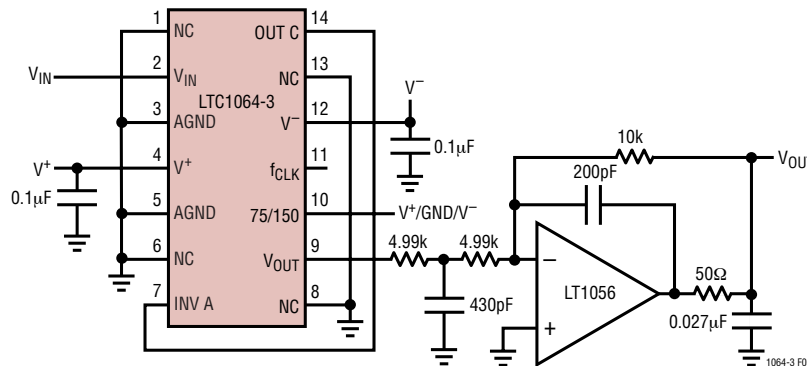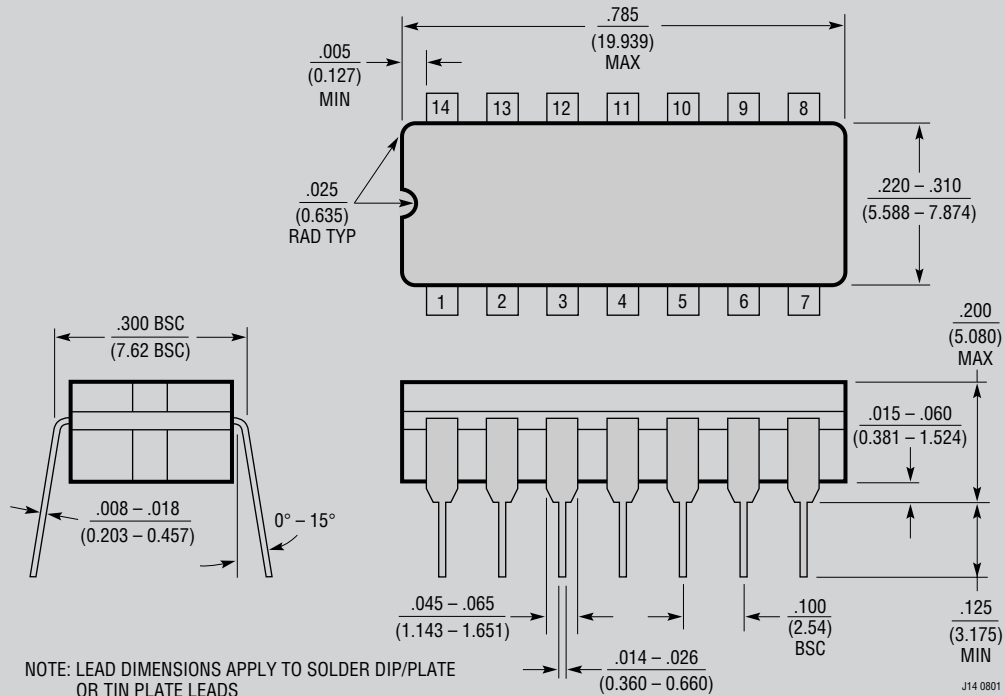**Figure 4. Level Shifting the Input T^{2}L Clock for Single Supply Operation ≥6V**

**Figure 5. Adding an Output Buffer-Filter to Eliminate Any Clock Feedthrough. Passband ±0.1dB to 50kHz, −3dB at 94kHz**

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PACKAGE DESCRIPTION

J Package
14-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)

.785
(19.939)
MAX

.005
(0.127)
MIN

.025
(0.635)
RAD TYP

.220 – .310
(5.588 – 7.874)

.300 BSC
(7.62 BSC)

.008 – .018
(0.203 – 0.457)

0° – 15°

.200
(5.080)
MAX

.015 – .060
(0.381 – 1.524)

.045 – .065
(1.143 – 1.651)

.100
(2.54)
BSC

.014 – .026
(0.360 – 0.660)

.125
(3.175)
MIN

NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE
OR TIN PLATE LEADS

J14 0801

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

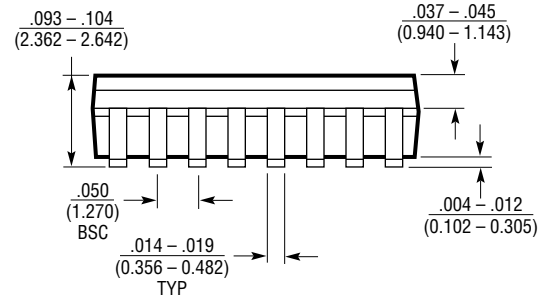**N Package**
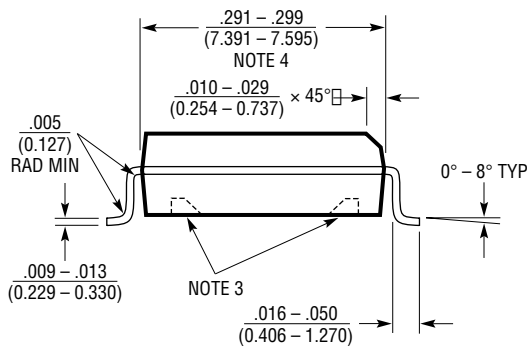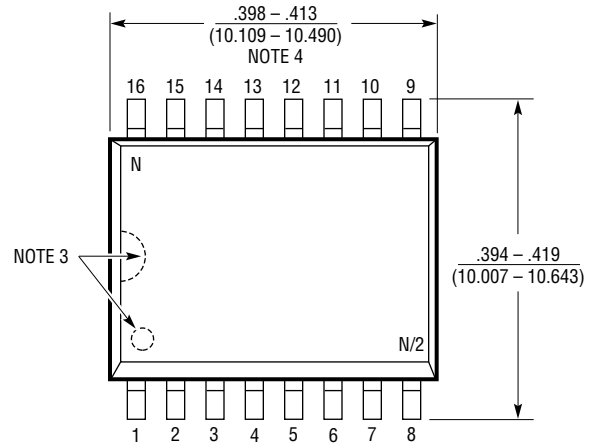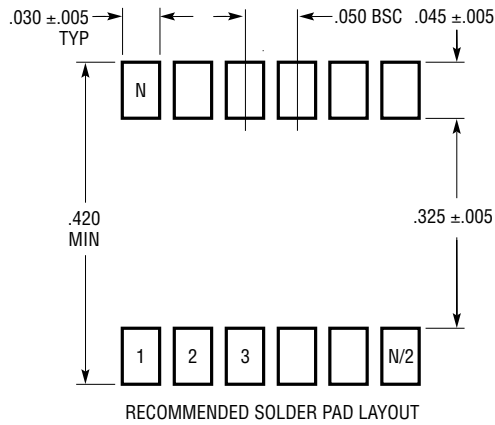**14-Lead PDIP (Narrow 0.300)**
(LTC DWG # 05-08-1510)
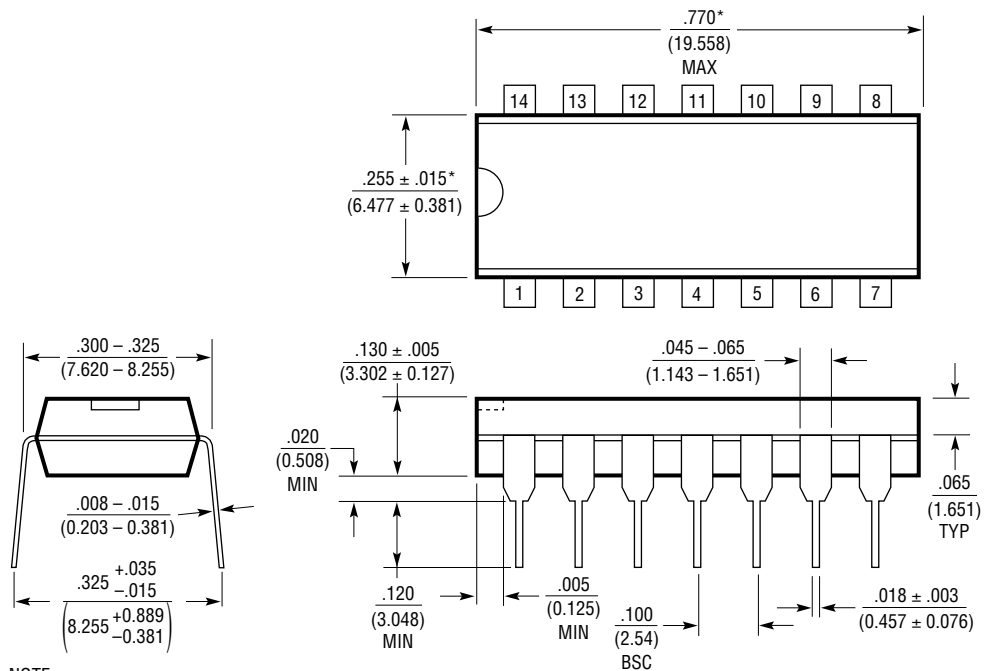
NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

N14 1002

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

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PACKAGE DESCRIPTION

SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)

.030 ±.005
TYP

.050 BSC .045 ±.005

N

.420
MIN

.325 ±.005

1 2 3   N/2

RECOMMENDED SOLDER PAD LAYOUT

.398 – .413
(10.109 – 10.490)
NOTE 4

16 15 14 13 12 11 10 9

N

NOTE 3

.394 – .419
(10.007 – 10.643)

N/2

1 2 3 4 5 6 7 8

.291 – .299
(7.391 – 7.595)
NOTE 4

.010 – .029
(0.254 – 0.737) × 45°

.005
(0.127)
RAD MIN

0° – 8° TYP

.009 – .013
(0.229 – 0.330)

NOTE 3

.016 – .050
(0.406 – 1.270)

.093 – .104
(2.362 – 2.642)

.037 – .045
(0.940 – 1.143)

.050
(1.270)
BSC

.014 – .019
(0.356 – 0.482)
TYP

.004 – .012
(0.102 – 0.305)

S16 (WIDE) 0502

NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
   THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

TYPICAL APPLICATIONS
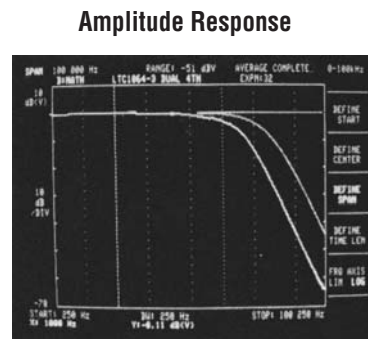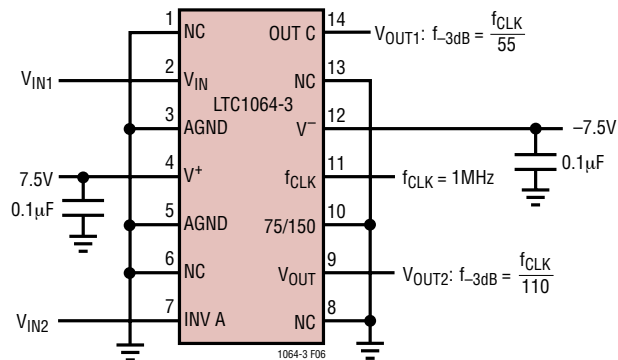

Amplitude Response

Figure 6. Dual 4th Order Bessel Filters. $V_S = \pm7.5V$,
$f_{CLK} = 1MHz$, Pin 10 to GND. $f_{-3dB} = 9kHz$ and $18kHz$

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1069-7	8th Order Linear Phase Lowpass	SO-8 Package
LTC1563	Active RC, 4th Order Bessel Lowpass	Continuous Time, Resistor Programmable Cutoff
LTC1569-6	DC Accurate, 10th Order Lowpass	Linear Phase, Internal Precision Clock, SO-8 Package
LTC1569-7	DC Accurate, 10th Order Lowpass	Linear Phase, Internal Precision Clock, SO-8 Package

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