Linear Phase, 8th Order Lowpass Filter

FEATURES

- Steeper Roll-Off Than 8th Order Bessel Filters
- f_{CUTOFF} up to 100kHz
- Phase Equalized Filter in 14-Pin Package
- Phase and Group Delay Response Fully Tested
- Transient Response Exhibits 5% Overshoot and No Ringing
- Wide Dynamic Range
- 72dB THD or Better Throughout a 50kHz Passband
- No External Components Needed
- Available in 14-Pin DIP and 16-Pin SO Wide Packages

APPLICATIONS

- Data Communication Filters
- Time Delay Networks
- Phase-Matched Filters

DESCRIPTION

The LTC®1064-7 is a clock-tunable monolithic 8th order lowpass filter with linear passband phase and flat group delay. The amplitude response approximates a maximally flat passband while it exhibits steeper roll-off than an equivalent 8th order Bessel filter. For instance, at twice the cutoff frequency the filter attains 34dB attenuation (vs 12dB for Bessel), while at three times the cutoff frequency, the filter attains 68dB attenuation (vs 30dB for Bessel). The cutoff frequency of the LTC1064-7 is tuned via an external TTL or CMOS clock.

The LTC1064-7 features wide dynamic range. With single 5V supply, the S/N + THD is 76dB. Optimum 92dB S/N is obtained with ±7.5V supplies.

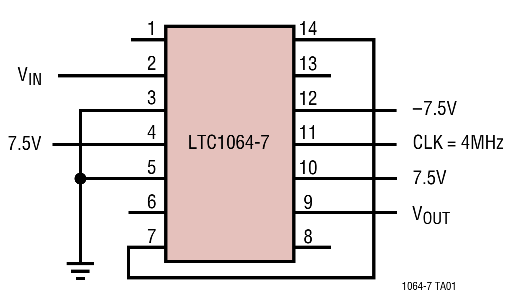
The clock-to-cutoff frequency ratio of the LTC1064-7 can be set to 50:1 (Pin 10 to V^+) or 100:1 (Pin 10 to V^-).

When the filter operates at clock-to-cutoff frequency ratio of 50:1, the input is double-sampled to lower the risk of aliasing.

The LTC1064-7 is pin-compatible with the LTC1064-X series, LTC1164-7 and LTC1264-7.

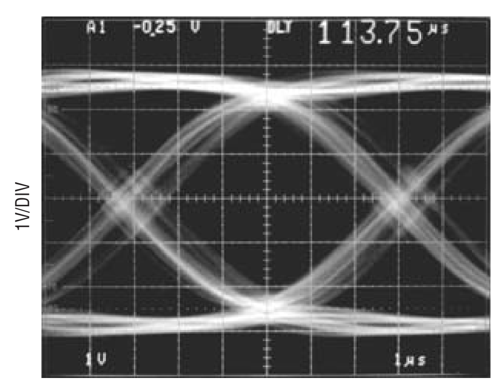
TYPICAL APPLICATION

80kHz Linear Phase Lowpass Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR CLOSE TO THE PACKAGE AND ANY PRINTED CIRCUIT BOARD ASSEMBLY SHOULD MAINTAIN A DISTANCE OF AT LEAST 0.2 INCHES BETWEEN ANY OUTPUT OR INPUT PIN AND THE f_{CLK} LINE.

Eye Diagram



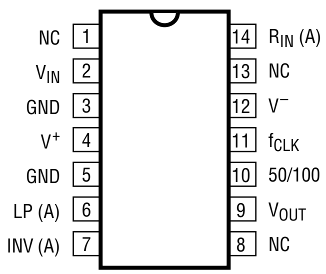
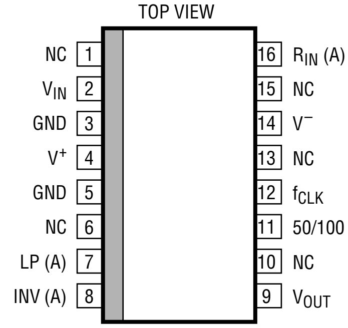
V_S = ±7.5V
f_{CLK} = 4MHz
RATIO = 50:1

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 400mW
Burn-In Voltage 16.5V
Voltage at Any Input ..... $(V^- – 0.3V) \le V_{IN} \le (V^+ + 0.3V)$
Storage Temperature Range .... –65°C to 150°C

Operating Temperature Range
LTC1064-7C .... –40°C to 85°C
LTC1064-7M **OBSOLETE** .... –55°C to 125°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

Package	ORDER PART NUMBER	Package	ORDER PART NUMBER
TOP VIEW  N PACKAGE 14-LEAD PLASTIC DIP T_{JMAX} = 110°C, θ_{JA} = 65°C/W (N)	LTC1064-7CN	TOP VIEW  SW PACKAGE 16-LEAD PLASTIC SO (WIDE) T_{JMAX} = 110°C, θ_{JA} = 85°C/W	LTC1064-7CSW
J PACKAGE 14-LEAD CERAMIC DIP T_{JMAX} = 150°C, θ_{JA} = 65°C/W (J) **OBSOLETE PACKAGE** Consider the N Package as an Alternate Source	LTC1064-7CJ LTC1064-7MJ		

Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.V_S = ±7.5V, R_L = 10k, T_A = 25°C, f_{CUTOFF} = 10kHz or 20kHz, f_{CLK} = 1MHz, TTL or CMOS level (maximum clock rise and fall time ≤ 1µs) and all gain measurements are referenced to passband gain, unless otherwise specified. The filter cutoff frequency is abbreviated as f_{CUTOFF} or f_C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	0.1Hz ≤ f ≤ 0.25 f_{CUTOFF} f_{TEST} = 5kHz, (f_{CLK}/f_C) = 50:1	●	–0.60	0.10	0.65	dB
Gain at 0.5 f_{CUTOFF}	f_{TEST} = 10kHz, (f_{CLK}/f_C) = 50:1	●	–0.90	–0.35	0.15	dB
	f_{TEST} = 5kHz, (f_{CLK}/f_C) = 100:1	●	–1.30	–0.35	1.25	dB
Gain at 0.75 f_{CUTOFF}	f_{TEST} = 15kHz, (f_{CLK}/f_C) = 50:1	●	–2.0	–1.0	–0.35	dB
Gain at f_{CUTOFF}	f_{TEST} = 20kHz, (f_{CLK}/f_C) = 50:1	●	–4.50	–3.4	–2.50	dB
	f_{TEST} = 10kHz, (f_{CLK}/f_C) = 100:1	●	–5.75	–4.5	–3.75	dB
Gain at 2 f_{CUTOFF}	f_{TEST} = 40kHz, (f_{CLK}/f_C) = 50:1	●	–36.5	–34.0	–31.75	dB
	f_{TEST} = 20kHz, (f_{CLK}/f_C) = 100:1	●	–37.0	–34.5	–31.75	dB
Gain with f_{CLK} = 20kHz	f_{TEST} = 200Hz, (f_{CLK}/f_C) = 100:1		–6.5	–4.3	–3.5	dB
Gain with f_{CLK} = 400kHz, V_S = ±2.375V	f_{TEST} = 4kHz, (f_{CLK}/f_C) = 50:1		–0.9	–0.3	0.25	dB
	f_{TEST} = 8kHz, (f_{CLK}/f_C) = 50:1		–4.5	–3.3	–2.00	dB
Phase Factor (*F*) Phase = 180° – *F* (f/f_C) (Note 2)	0.1Hz ≤ f ≤ f_{CUTOFF} (f_{CLK}/f_C) = 50:1			430 ± 2.0		Deg
	(f_{CLK}/f_C) = 100:1			421 ± 2.5		Deg
	(f_{CLK}/f_C) = 50:1	●	422	430	437	Deg
	(f_{CLK}/f_C) = 100:1	●	414	421	429	Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±7.5V, R_L = 10k, f_{CUTOFF} = 10kHz or 20kHz, f_{CLK} = 1MHz, TTL or CMOS level (maximum clock rise and fall time ≤ 1µs) and all gain measurements are referenced to passband gain, unless otherwise specified. The filter cutoff frequency is abbreviated as f_{CUTOFF} or f_C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Phase Nonlinearity (Notes 2, 4)	(f_{CLK}/f_C) = 50:1			±1.0		%
	(f_{CLK}/f_C) = 100:1			±1.0		%
	(f_{CLK}/f_C) = 50:1	●			±2.0	%
	(f_{CLK}/f_C) = 100:1	●			±2.0	%
Group Delay (t_d) $t_d = (F/360)(1/f_C)$ (Note 3)	(f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$			59.7 ± 0.5		µs
	(f_{CLK}/f_C) = 100:1, $f \le f_{CUTOFF}$			117.0 ± 1.0		µs
	(f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$	●	58.6	59.7	60.7	µs
	(f_{CLK}/f_C) = 100:1, $f \le f_{CUTOFF}$	●	115.0	117.0	119.0	µs
Group Delay Deviation (Notes 3, 4)	(f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$			±1.0		%
	(f_{CLK}/f_C) = 100:1, $f \le f_{CUTOFF}$			±1.0		%
	(f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$	●			±2.0	%
	(f_{CLK}/f_C) = 100:1, $f \le f_{CUTOFF}$	●			±2.0	%
Input Frequency Range (Table 9)	(f_{CLK}/f_C) = 50:1			$<f_{CLK}$		kHz
	(f_{CLK}/f_C) = 100:1			$<f_{CLK}/2$		kHz
Maximum f_{CLK}	V_S = 5V (AGND = 2V)			2.0		MHz
	V_S = ±5V			3.5		MHz
	V_S = ±7.5V			5.0		MHz
Clock Feedthrough ($f \ge f_{CLK}$)	50:1			200		$µV_{RMS}$
Wideband Noise ($1Hz \le f \le f_{CLK}$)	V_S = ±2.5V			95 ± 5%		$µV_{RMS}$
	V_S = ±5V			105 ± 5%		$µV_{RMS}$
	V_S = ±7.5V			115 ± 5%		$µV_{RMS}$
Input Impedance			25	40	70	kΩ
Output DC Voltage Swing (Note 5)	V_S = ±2.375V		±1.0	±1.2		V
	V_S = ±5V	●	±2.1	±3.2		V
	V_S = ±7.5V	●	±3.0	±5.0		V
Output DC Offset	50:1, V_S = ±5V			±150	±220	mV
	100:1, V_S = ±5V			±150		mV
Output DC Offset TempCo	50:1, V_S = ±5V			±200		µV/°C
	100:1, V_S = ±5V			±200		µV/°C
Power Supply Current	V_S = ±2.375V, T_A = 25°C			11	22	mA
		●			22	mA
	V_S = ±5V, T_A = 25°C			14	26	mA
		●			28	mA
	V_S = ±7.5V, T_A = 25°C			17	28	mA
		●			32	mA
Power Supply Range			±2.375		±8	V

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Input frequencies, f, are linearly phase shifted through the filter as long as $f \leq f_C$; f_C = cutoff frequency.

Figure 1 curve shows the typical phase response of an LTC1064-7 operating at f_{CLK} = 1MHz, ratio = 50:1, f_C = 20kHz and it closely matches an ideal straight line. The phase shift is described by: phase shift = $180° – F(f/f_C)$; $f \leq f_C$.

F is arbitrarily called the "phase factor" expressed in degrees. The phase factor allows the calculation of the phase at a given frequency.

Example: The phase shift at 14kHz of the LTC1064-7 shown in Figure 1 is:

phase shift = 180° – 430° (14kHz/20kHz) ± nonlinearity = –121° ± 1% or –121° ± 1.20°.

Note 3: Group delay and group delay deviation are calculated from the measured phase factor and phase deviation specifications.

Note 4: Phase deviation and group delay deviation for LTC1064-7MJ is ±4%.

Note 5: The AC swing is typically $11V_{P-P}$, $7V_{P-P}$, $2.8V_{P-P}$, with ±7.5V, ±5V, ±2.5V Supply respectively. For more information refer to the THD + Noise vs Input graphs.

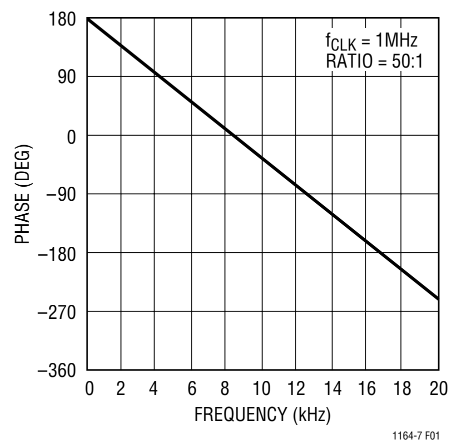
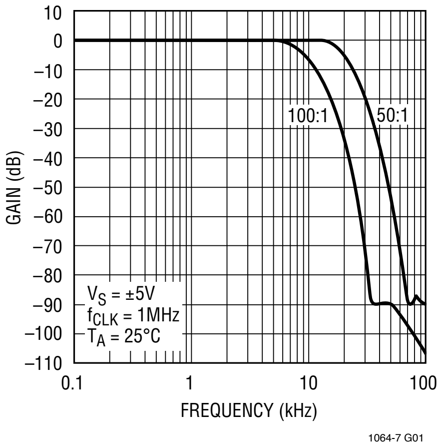


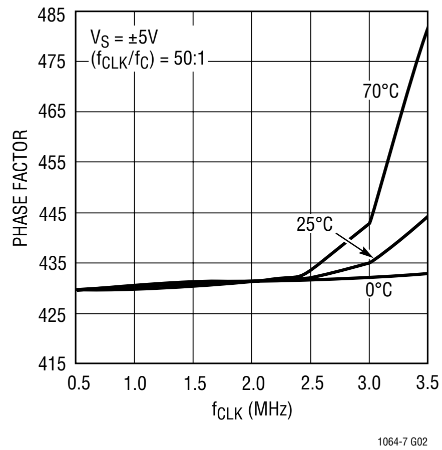
Figure 1. Phase Response in the Passband (Note 2)

TYPICAL PERFORMANCE CHARACTERISTICS

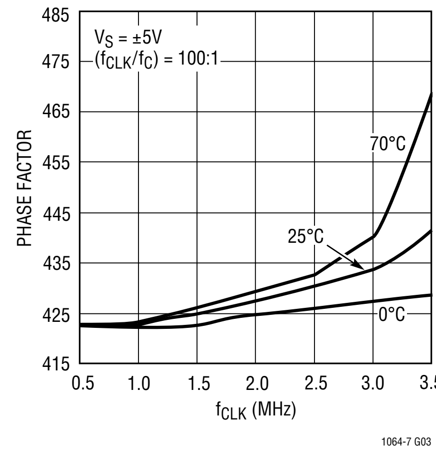
Gain vs Frequency



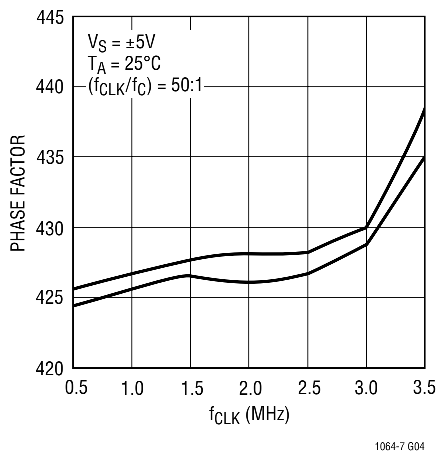
Phase Factor vs f_{CLK} (Typical Unit)



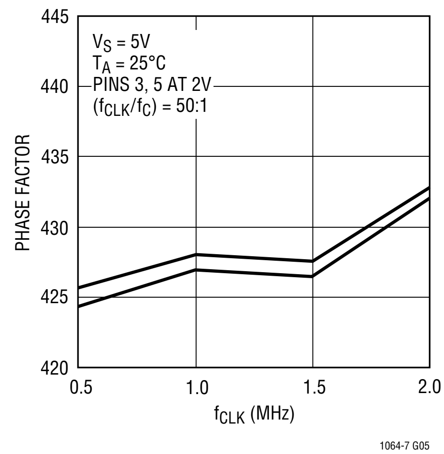
Phase Factor vs f_{CLK} (Typical Unit)



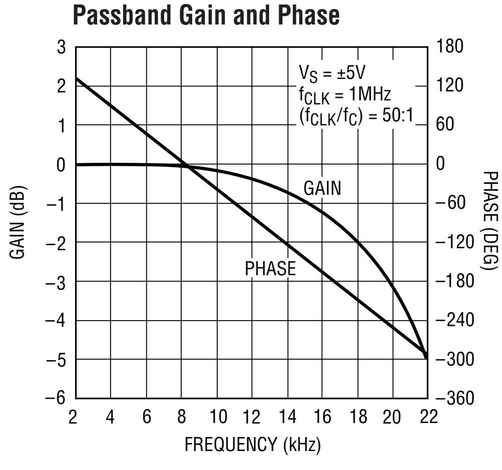
Phase Factor vs f_{CLK} (Min and Max Representative Units)



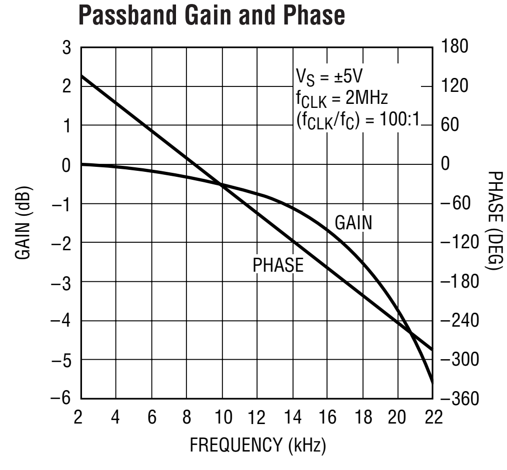
Phase Factor vs f_{CLK} (Min and Max Representative Units)



Passband Gain and Phase

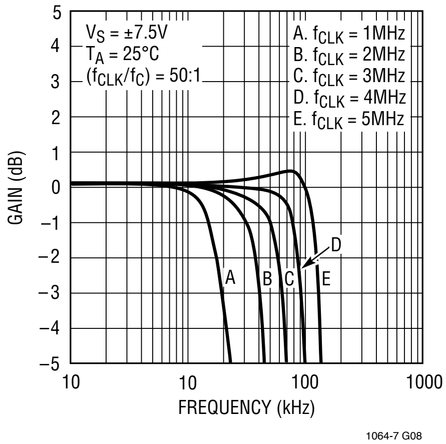


Passband Gain and Phase

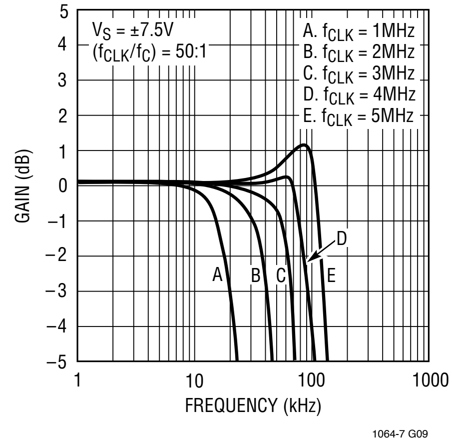


TYPICAL PERFORMANCE CHARACTERISTICS

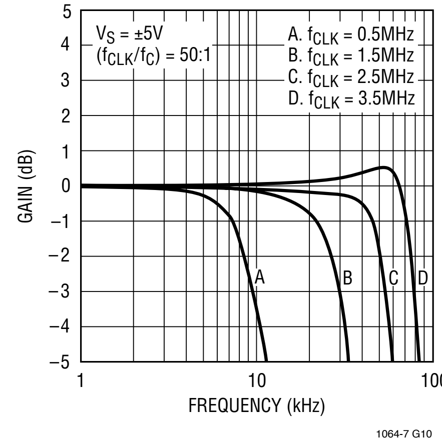
Passband Gain vs Frequency and f_{CLK}



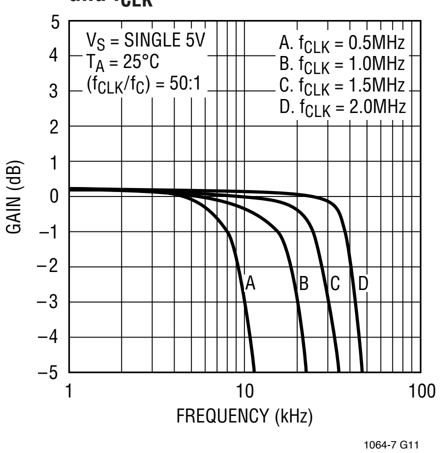
Passband Gain vs Frequency and f_{CLK} at T_A = 85°C



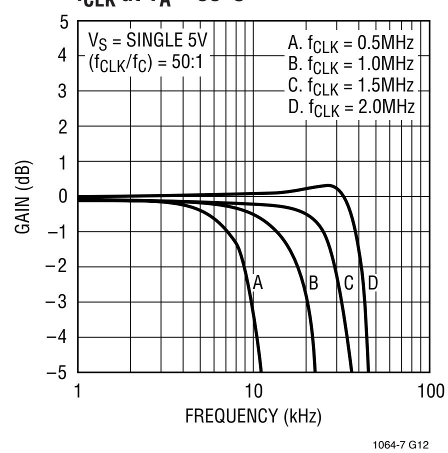
Passband Gain vs Frequency and f_{CLK} at T_A = 85°C



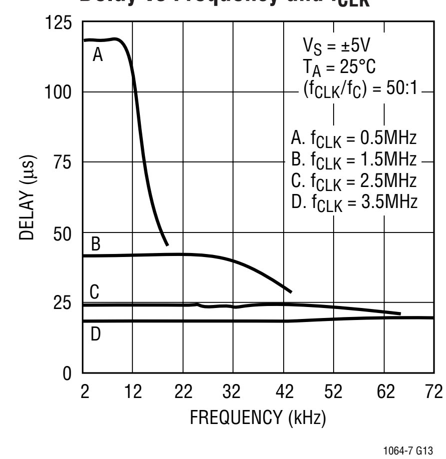
Passband Gain vs Frequency and f_{CLK}



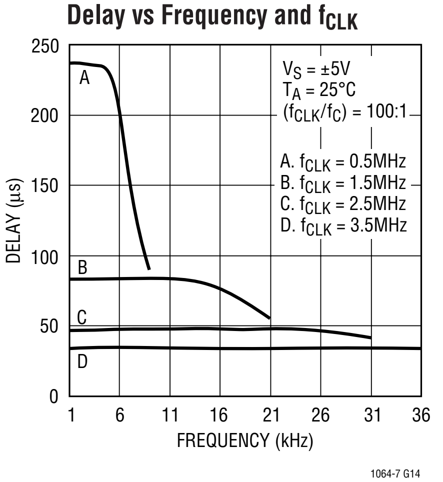
Passband Gain vs Frequency and f_{CLK} at T_A = 85°C



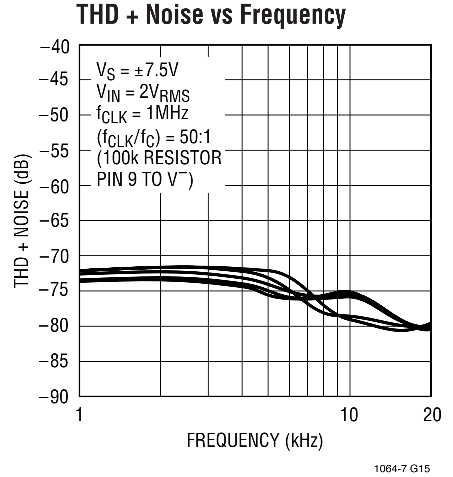
Delay vs Frequency and f_{CLK}



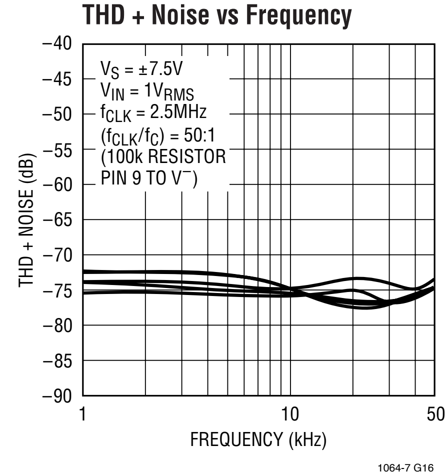
Delay vs Frequency and f_{CLK}



THD + Noise vs Frequency

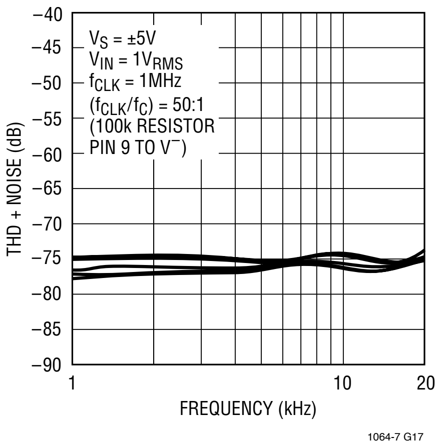


THD + Noise vs Frequency

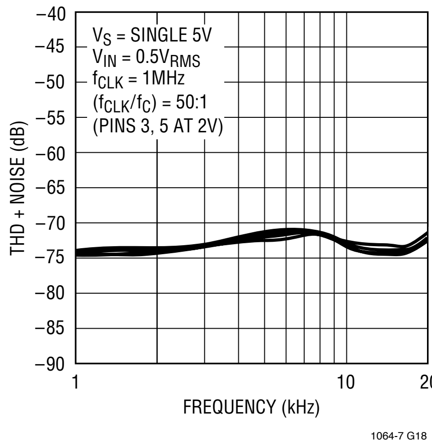


TYPICAL PERFORMANCE CHARACTERISTICS

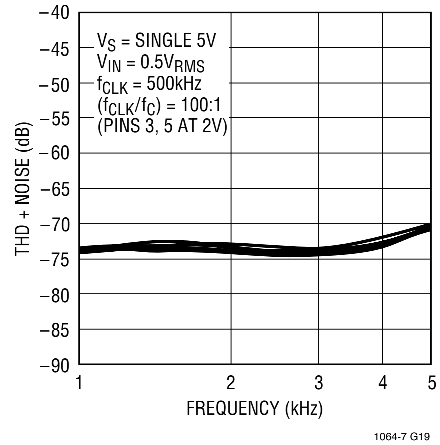
THD + Noise vs Frequency



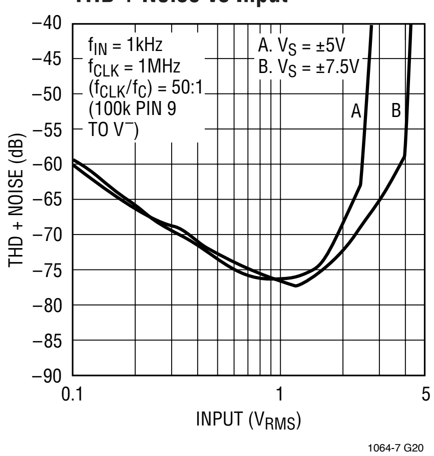
THD + Noise vs Frequency



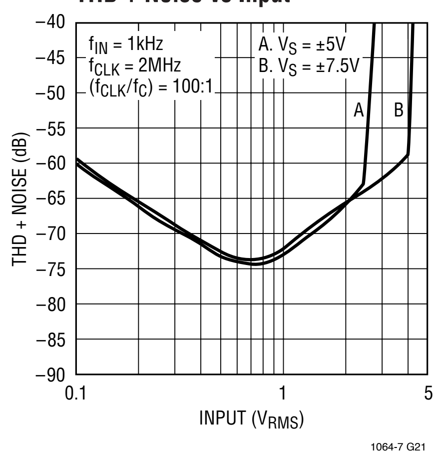
THD + Noise vs Frequency



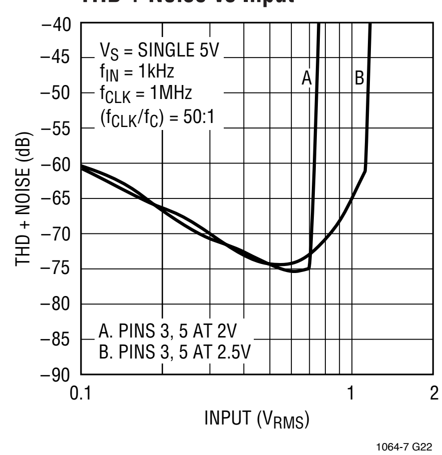
THD + Noise vs Input



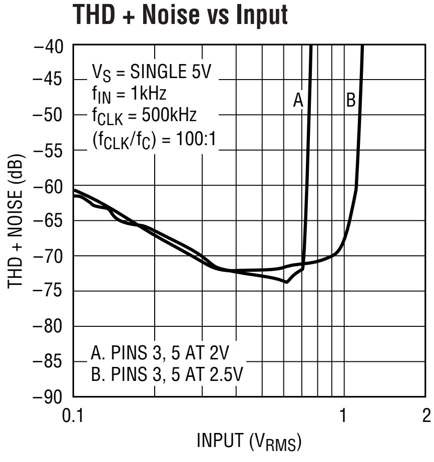
THD + Noise vs Input



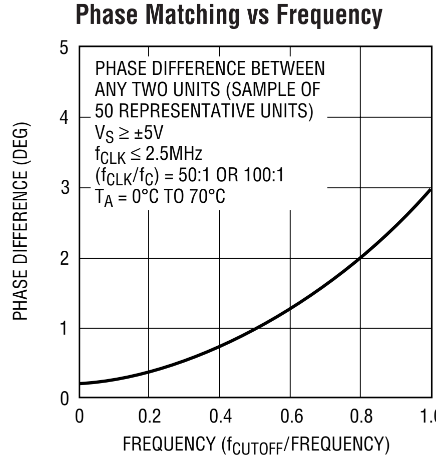
THD + Noise vs Input



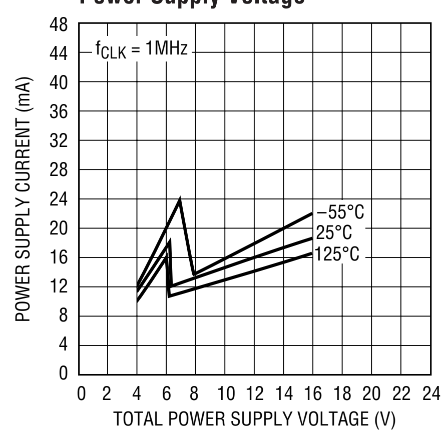
THD + Noise vs Input



Phase Matching vs Frequency



Power Supply Current vs Power Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

Table 1. Passband Gain and Phase
V_S = ±7.5V, (f_{CLK}/f_C) = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.086	180.00
5.000	−0.086	73.54
10.000	−0.334	−33.60
15.000	−1.051	−140.81
20.000	−3.316	−249.30
f_{CLK} = 2MHz (Typical Unit)		
0.000	−0.131	180.00
10.000	−0.131	72.88
20.000	−0.442	−34.71
30.000	−1.108	−141.99
40.000	−3.115	−250.45
f_{CLK} = 3MHz (Typical Unit)		
0.000	−0.156	180.00
15.000	−0.156	72.54
30.000	−0.459	−35.01
45.000	−0.941	−141.95
60.000	−2.508	−250.53
f_{CLK} = 4MHz (Typical Unit)		
0.000	−0.121	180.00
20.000	−0.121	72.12
40.000	−0.292	−35.75
60.000	−0.476	−142.92
80.000	−1.539	−252.63
f_{CLK} = 5MHz (Typical Unit)		
0.000	−0.045	180.00
25.000	−0.045	70.85
50.000	−0.006	−38.25
75.000	0.185	−146.77
100.000	−0.356	−259.27

Table 2. Passband Gain and Phase
V_S = ±7.5V, (f_{CLK}/f_C) = 100:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.203	180.00
2.500	−0.203	74.07
5.000	−0.741	−31.71
7.500	−1.831	−136.47
10.000	−4.451	−240.17
f_{CLK} = 2MHz (Typical Unit)		
0.000	−0.152	180.00
5.000	−0.152	73.79
10.000	−0.575	−32.47
15.000	−1.501	−138.11
20.000	−3.973	−243.84
f_{CLK} = 3MHz (Typical Unit)		
0.000	−0.123	180.00
7.500	−0.123	73.32
15.000	−0.481	−33.64
22.500	−1.312	−140.14
30.000	−3.654	−247.11
f_{CLK} = 4MHz (Typical Unit)		
0.000	−0.116	180.00
10.000	−0.116	72.49
20.000	−0.436	−35.21
30.000	−1.171	−142.33
40.000	−3.353	−250.12
f_{CLK} = 5MHz (Typical Unit)		
0.000	−0.097	180.00
12.500	−0.097	71.00
25.000	−0.351	−38.08
37.500	−0.951	−146.51
50.000	−2.999	−256.13

Table 3. Passband Gain and Phase
V_S = ±5V, (f_{CLK}/f_C) = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	−0.081	180.00
2.500	−0.081	73.71
5.000	−0.345	−33.31
7.500	−1.063	−140.36
10.000	−3.283	−248.52
f_{CLK} = 1MHz (Typical Unit)		
0.000	−0.071	180.00
5.000	−0.071	73.44
10.000	−0.322	−33.83
15.000	−1.036	−141.13
20.000	−3.284	−249.68
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	−0.095	180.00
7.500	−0.095	73.03
15.000	−0.392	−34.53
22.500	−1.075	−141.89
30.000	−3.155	−250.45
f_{CLK} = 2MHz (Typical Unit)		
0.000	−0.127	180.00
10.000	−0.127	72.81
20.000	−0.447	−34.70
30.000	−1.041	−141.77
40.000	−2.856	−250.24
f_{CLK} = 2.5MHz (Typical Unit)		
0.000	−0.126	180.00
12.500	−0.126	72.61
25.000	−0.411	−34.91
37.500	−0.864	−141.88
50.000	−2.397	−250.62
f_{CLK} = 3MHz (Typical Unit)		
0.000	−0.102	180.00
15.000	−0.102	72.23
30.000	−0.292	−35.64
45.000	−0.546	−142.96
60.000	−1.769	−252.73

TYPICAL PERFORMANCE CHARACTERISTICS

Table 3. Passband Gain and Phase
V_S = ±5V, (f_{CLK}/f_C) = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 3.5MHz (Typical Unit)		
0.000	–0.054	180.00
17.500	–0.054	71.07
35.000	–0.108	–38.00
52.500	–0.137	–146.68
70.000	–1.104	–258.97

Table 4. Passband Gain and Phase
V_S = ±5V, (f_{CLK}/f_C) = 100:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	–0.186	180.00
1.250	–0.186	74.10
2.500	–0.726	–31.65
3.750	–1.805	–136.48
5.000	–4.402	–240.33
f_{CLK} = 1MHz (Typical Unit)		
0.000	–0.184	180.00
2.500	–0.184	74.02
5.000	–0.712	–31.80
7.500	–1.785	–136.61
10.000	–4.387	–240.43
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	–0.145	180.00
3.750	–0.145	73.84
7.500	–0.596	–32.32
11.250	–1.556	–137.73
15.000	–4.047	–242.95
f_{CLK} = 2MHz (Typical Unit)		
0.000	–0.116	180.00
5.000	–0.116	73.64
10.000	–0.494	–32.93
15.000	–1.361	–139.03
20.000	–3.761	–245.57
f_{CLK} = 2.5MHz (Typical Unit)		
0.000	–0.101	180.00
6.250	–0.101	73.17
12.500	–0.452	–33.93
18.750	–1.273	–140.58
25.000	–3.611	–247.80
f_{CLK} = 3MHz (Typical Unit)		
0.000	–0.105	180.00
7.500	–0.105	72.36
15.000	–0.445	–35.47
22.500	–1.228	–142.70
30.000	–3.509	–250.58
f_{CLK} = 3.5MHzMHz (Typical Unit)		
0.000	–0.104	180.00
8.750	–0.104	70.81
17.500	–0.437	–38.39
26.250	–1.188	–146.85
35.000	–3.478	–256.10

Table 5. Passband Gain and Phase
V_S = Single 5V, (f_{CLK}/f_C) = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	–0.134	180.00
2.500	–0.134	73.52
5.000	–0.391	–33.67
7.500	–1.109	–140.92
10.000	–3.351	–249.32
f_{CLK} = 1MHz (Typical Unit)		
0.000	–0.148	180.00
5.000	–0.148	73.07
10.000	–0.423	–34.63
15.000	–1.111	–142.25
20.000	–3.241	–251.03
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	–0.157	180.00
7.500	–0.157	72.73
15.000	–0.456	–34.83
22.500	–0.981	–142.08
30.000	–2.687	–251.09
f_{CLK} = 2MHz (Typical Unit)		
0.000	–0.188	180.00
10.000	–0.188	71.37
20.000	–0.304	–37.52
30.000	–0.513	–146.11
40.000	–1.824	–257.46

Table 6. Passband Gain and Phase
V_S = Single 5V, (f_{CLK}/f_C) = 100:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	–0.243	180.00
1.250	–0.243	73.91
2.500	–0.776	–31.98
3.750	–1.861	–136.98
5.000	–4.483	–240.90
f_{CLK} = 1MHz (Typical Unit)		
0.000	–0.208	180.00
2.500	–0.208	73.76
5.000	–0.678	–32.47
7.500	–1.679	–137.87
10.000	–4.221	–242.65
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	–0.115	180.00
3.750	–0.115	73.26
7.500	–0.473	–33.73
11.250	–1.314	–140.40
15.000	–3.715	–247.66
f_{CLK} = 2MHz (Typical Unit)		
0.000	–0.209	180.00
5.000	–0.209	71.18
10.000	–0.499	–37.85
15.000	–1.281	–146.27
20.000	–3.695	–255.38

PIN FUNCTIONS

Power Supply Pins (4, 12)

The V^+ (Pin 4) and the V^- (Pin 12) should be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/µs. When V^+ is applied before V^- and V^- is allowed to go above ground, a signal diode should clamp V^- to prevent latch-up. Figures 2 and 3 show typical connections for dual and single supply operation.

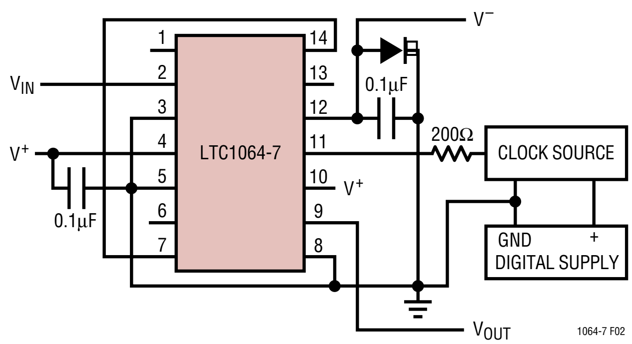


Figure 2. Dual Supply Operation for an f_{CLK}/f_{CUTOFF} = 50:1

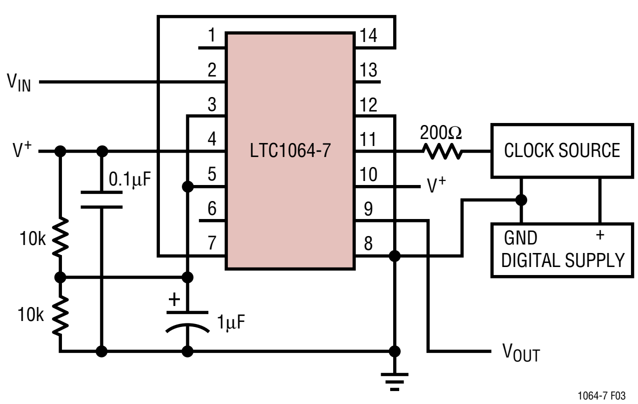


Figure 3. Single Supply Operation for an f_{CLK}/f_{CUTOFF} = 50:1

Clock Input Pin (11)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 7 shows the clock's low and high level threshold values for a dual or single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.1µs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path. A 200Ω resistor between clock source and pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling (Figures 2 and 3).

Table 7. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ −2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Suppl = 5V	≥ 1.45V	≤ 0.5V

Analog Ground Pins (3, 5)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, Pin 3 should be connected to the analog ground plane. For single supply operation pin 3 should be biased at 1/2 supply and should be bypassed to the analog ground plane with at least a 1µF capacitor (Figure 3). For single 5V operation at the highest f_{CLK} of 2MHz, Pin 3 should be biased at 2V. This minimizes passband gain and phase variations.

Ratio Input Pin (10)

The DC level at this pin determines the ratio of the clock frequency to the cutoff frequency of the filter. Pin 10 at V^+ gives a 50:1 ratio and Pin 10 at V^- gives a 100:1 ratio. For single supply operation the ratio is 50:1 when Pin 10 is at V^+ and 100:1 when Pin 10 is at ground. When Pin 10 is not tied to ground, it should be bypassed to analog ground

PIN FUNCTIONS

with a 0.1µF capacitor. If the DC level at Pin 10 is switched mechanically or electrically at slew rates greater than 1V/µs while the device is operating, a 10k resistor should be connected between Pin 10 and the DC source.

Filter Input Pin (2)

The input pin is connected internally through a 40k resistor tied to the inverting input of an op amp.

Filter Output Pins (9, 6)

Pin 9 is the specified output of the filter; it can typically source 3mA and sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion of the filter. When evaluating the device's distortion an output buffer is required. A noninverting buffer, Figure 4, can be used provided that its input common mode range is well within the filter's output swing. Pin 6 is an intermediate filter output providing an unspecified 6th order lowpass filter. Pin 6 should not be loaded.

External Connection Pins (7, 14)

Pins 7 and 14 should be connected together. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane.

NC Pins (1, 5, 8, 13)

Pins 1, 5, 8 and 13 are not connected to any internal circuit point on the device and should preferably be tied to analog ground.

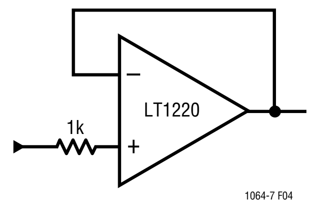


Figure 4. Buffer for Filter Output

APPLICATIONS INFORMATION

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (9). The clock feedthrough is tested with the input pin (2) grounded and it depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown in Table 8.

Table 8. Clock Feedthrough

V_S	50:1	100:1
Single 5V	$90\mu V_{RMS}$	$100\mu V_{RMS}$
±5V	$100\mu V_{RMS}$	$300\mu V_{RMS}$
±7.5V	$120\mu V_{RMS}$	$650\mu V_{RMS}$

Note: The clock feedthrough at single 5V is imbedded in the wideband noise of the filter. Clock waveform is a square wave.

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple R/C lowpass network at the output of the filter pin (9). This R/C will completely eliminate any switching transients.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and it cannot be reduced with post filtering. For instance, the LTC1064-7 wideband noise at ±5V supply is $105\mu V_{RMS}$, $95\mu V_{RMS}$ of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

APPLICATIONS INFORMATION

Speed Limitations

To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown in Table 9.

Table 9. Maximum V_{IN} vs V_S and Clock

POWER SUPPLY	MAXIMUM f_{CLK}	MAXIMUM V_{IN}
±7.5V	5.0MHz	$1.8V_{RMS}$ (f_{IN} > 80kHz)
	4.5MHz	$2.3V_{RMS}$ (f_{IN} > 80kHz)
	4.0MHz	$2.7V_{RMS}$ (f_{IN} > 80kHz)
	≥3.5MHz	$1.4V_{RMS}$ (f_{IN} > 500kHz)
±5V	3.5MHz	$1.6V_{RMS}$ (f_{IN} > 80kHz)
	≥3.0MHz	$0.7V_{RMS}$ (f_{IN} > 400kHz)
Single 5V	2.0MHz	$0.5V_{RMS}$ (f_{IN} > 250kHz)

Table 10. Transient Response of LTC Lowpass Filters

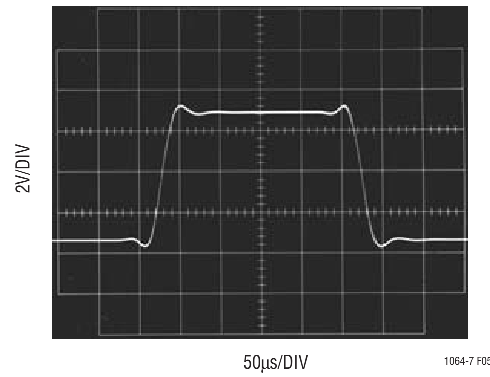
LOWPASS FILTER	DELAY TIME* (SEC)	RISE TIME** (SEC)	SETTLING TIME*** (SEC)	OVER-SHOOT (%)
LTC1064-3 Bessel	$0.50/f_C$	$0.34/f_C$	$0.80/f_C$	0.5
LTC1164-5 Bessel	$0.43/f_C$	$0.34/f_C$	$0.85/f_C$	0
LTC1164-6 Bessel	$0.43/f_C$	$0.34/f_C$	$1.15/f_C$	1
LTC1264-7 Linear Phase	$1.15/f_C$	$0.36/f_C$	$2.05/f_C$	5
LTC1164-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.2/f_C$	5
LTC1064-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.2/f_C$	5
LTC1164-5 Butterworth	$0.80/f_C$	$0.48/f_C$	$2.4/f_C$	11
LTC1164-6 Elliptic	$0.85/f_C$	$0.54/f_C$	$4.3/f_C$	18
LTC1064-4 Elliptic	$0.90/f_C$	$0.54/f_C$	$4.5/f_C$	20
LTC1064-1 Elliptic	$0.85/f_C$	$0.54/f_C$	$6.5/f_C$	20

* To 50% ±5%, ** 10% to 90% ±5%, *** To 1% ±0.5%

Table 11. Aliasing (f_{CLK} = 100kHz)

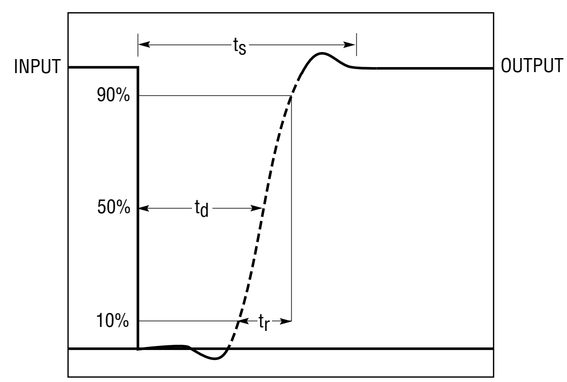
INPUT FREQUENCY ($V_{IN} = 1V_{RMS}$, $f_{IN} = f_{CLK} \pm f_{OUT}$) (kHz)	OUTPUT LEVEL (Relative to Input, 0dB = $1V_{RMS}$) (dB)	OUTPUT FREQUENCY (Aliased Frequency f_{OUT} = ABS [$f_{CLK} \pm f_{IN}$]) (kHz)
50:1, f_{CUTOFF} = 2kHz		
190 (or 210)	−76.1	10.0
195 (or 205)	−51.9	5.0
196 (or 204)	−36.3	4.0
197 (or 203)	−18.4	3.0
198 (or 202)	−3.0	2.0
199.5 (or 200.5)	−0.2	0.5
100:1, f_{CUTOFF} = 1kHz		
97 (or 103)	−74.2	3.0
97.5 (or 102.5)	−53.2	2.5
98 (or 102)	−36.9	2.0
98.5 (or 101.5)	−19.6	1.5
99 (or 101)	−5.2	1.0
99.5 (or 100.5)	−0.7	0.5

Transient Response



V_S = ±7.5V, f_{IN} = 2kHz ± 3V
f_{CLK} = 1MHz, RATIO = 50:1

Figure 5.



RISE TIME (t_r) = $\frac{0.39}{f_{CUTOFF}}$ ±5%

SETTLING TIME (t_s) = $\frac{2.2}{f_{CUTOFF}}$ ±5%
(TO 1% of OUTPUT)

DELAY TIME (t_d) = GROUP DELAY ≈ $\frac{1.2}{f_{CUTOFF}}$
(TO 50% OF OUTPUT)

1064-7 F06

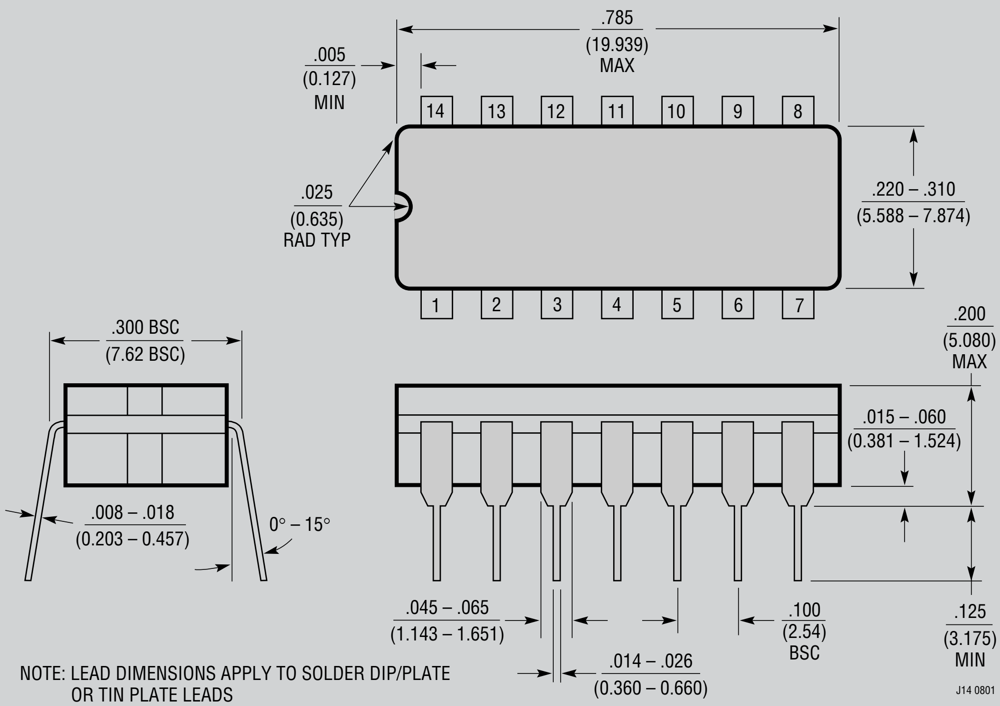
Figure 6.

Aliasing

Aliasing is an inherent phenomenon of sampled data systems and it occurs when input frequencies close to the sampling frequency are applied. For the LTC1064-7 case at 100:1, an input signal whose frequency is in the range of f_{CLK}±3%, will be aliased back into the filter's passband. If, for instance, an LTC1064-7 operating with a 100kHz clock and 1kHz cutoff frequency receives a 98kHz, 10mV input signal, a 2kHz, $143\mu V_{RMS}$ alias signal will appear at its output. When the LTC1064-7 operates with a clock-to-cutoff frequency of 50:1, aliasing occurs at twice the clock frequency. Table 11 shows details.

PACKAGE DESCRIPTION

J Package
14-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

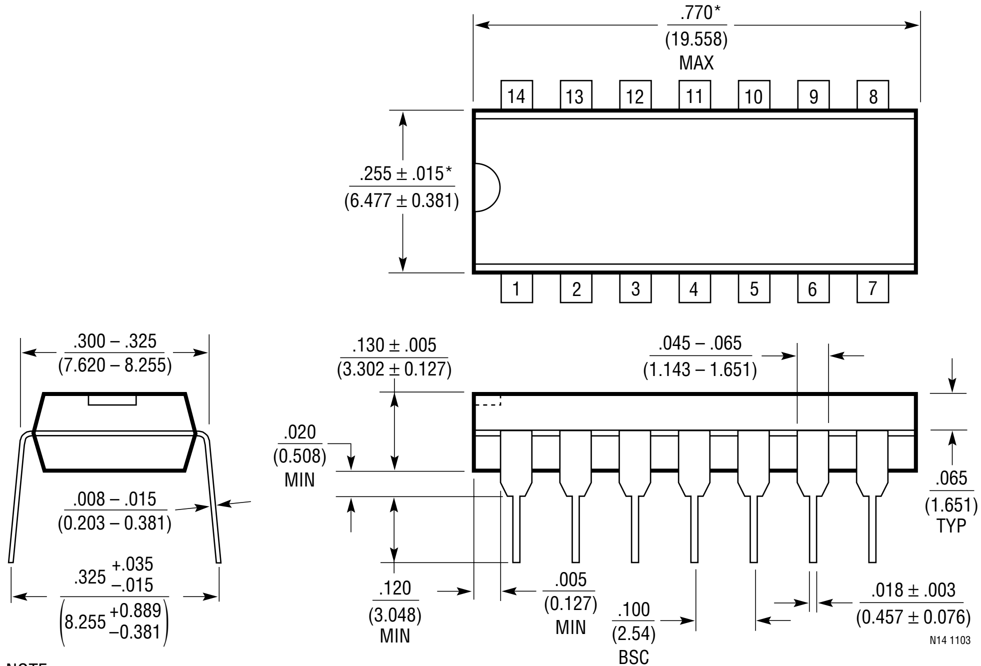


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

N Package
14-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

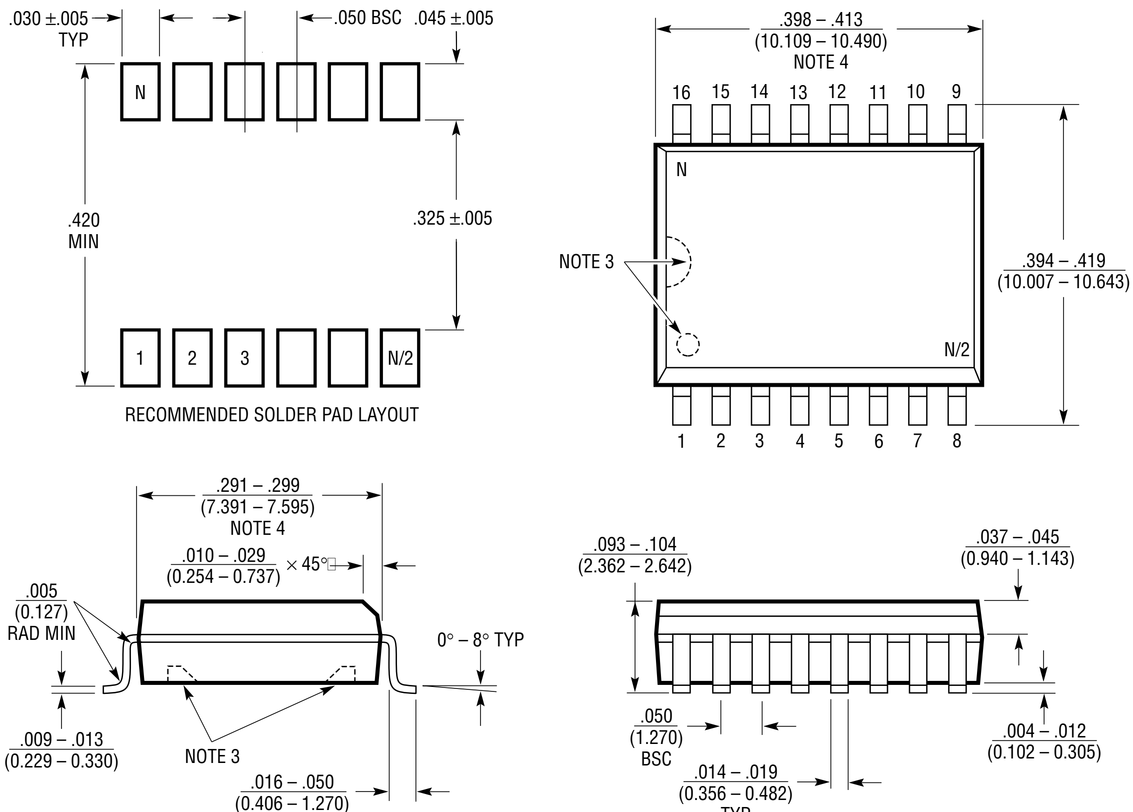


NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)

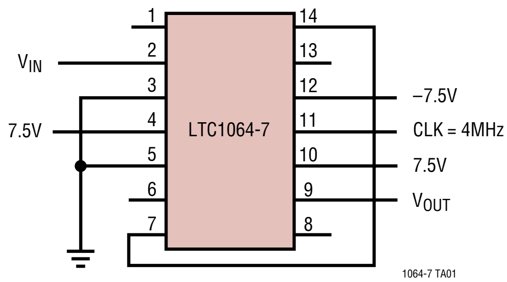


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S16 (WIDE) 0502

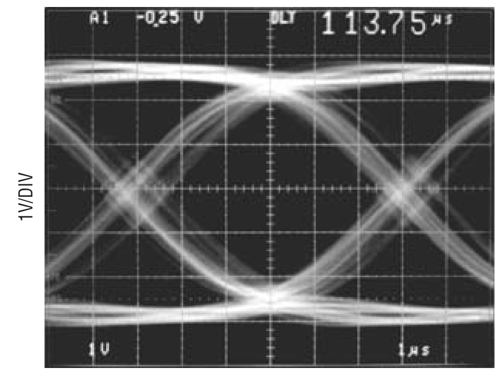
TYPICAL APPLICATION

80kHz Linear Phase Lowpass Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1μF CAPACITOR CLOSE TO THE PACKAGE AND ANY PRINTED CIRCUIT BOARD ASSEMBLY SHOULD MAINTAIN A DISTANCE OF AT LEAST 0.2 INCHES BETWEEN ANY OUTPUT OR INPUT PIN AND THE f_{CLK} LINE.

Eye Diagram



V_S = ±7.5V
f_{CLK} = 4MHz
RATIO = 50:1

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1064	Universal Filter Building Block	Allows for Bandpass (Up to 50kHz) Using External Resistors
LTC1064-1/2/3/4	8th Order Low Pass Filters, F_O Max = 100kHz	Elliptic, Butterworth, Bessel, Cauer
LTC1164	Universal Filter Building Block	Allows for Bandpass (Up to 20kHz) Using External Resistors
LTC1164-5/6/7	8th Order Low Pass Filters, F_O Max = 20kHz	Butterworth, Bessel or Elliptic
LTC1264	Universal Filter Building Block	Allows for Bandpass (Up to 100kHz) Using External Resistors
LTC1264-7	8th Order Low Pass Filter, F_O Max = 200kHz	Flat Group Delay, High Speed Lowpass Filter
LT6600-2.5	Low Noise Differential Amp and 10MHz Lowpass	55μV_{RMS} Noise 100kHz to 10MHz 3V Supply
LT6600-10	Low Noise Differential Amp and 20MHz Lowpass	86μV_{RMS} Noise 100kHz to 20MHz 3V Supply

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