

LTC1555/LTC1556

ABSOLUTE MAXIMUM RATINGS

(Note 1)

| | |
|---|------------------------------|
| V_{IN} , DV_{CC} to GND | -0.3V to 12V |
| V_{CC} to GND | -0.3V to 12V |
| Digital Inputs to GND | -0.3V to 12V |
| LDO, CLK, RST, I/O to GND | -0.3V to ($V_{CC} + 0.3V$) |
| V_{CC} , LDO Short-Circuit Duration | Indefinite |
| Storage Temperature Range | -65°C to 150°C |

Temperature Range

| | |
|---|---------------|
| LTC1555C/LTC1556C | 0°C to 70°C |
| LTC1555I/LTC1556I | -40°C to 85°C |
| Extended Commercial Operating Temperature Range (Note 2) | -40°C to 85°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

PACKAGE/ORDER INFORMATION

| TOP VIEW | ORDER PART NUMBER | TOP VIEW | ORDER PART NUMBER |
|--|--------------------------|---|--------------------------|
| <p>GN PACKAGE 16-LEAD PLASTIC SSOP $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 135^{\circ}C/W$</p> | LTC1555CGN LTC1555IGN | <p>GN PACKAGE 20-LEAD PLASTIC SSOP $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 95^{\circ}C/W$</p> | LTC1556CGN LTC1556IGN |

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 2.7V$ to $10V$, $DV_{CC} = 1.8V$ to $5.5V$, controller digital pins tied to DV_{CC} , SIM digital pins floating, EN, FB pins tied to GND (LTC1556), $C_1 = 0.1\mu F$, $C_{OUT} = 10\mu F$ unless otherwise specified.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------|--|----------------|------|----------|-------------------|
| V_{IN} Operating Voltage | | 2.7 | | 10 | V |
| DV_{CC} Operating Voltage | | 1.8 | | 5.5 | V |
| V_{IN} Operating Current | $2.7V \leq V_{IN} \leq 5V$, $V_{CC} = 5V$, $I_{VCC} = 0$ | | 60 | 100 | μA |
| | $5V < V_{IN} \leq 10V$, $V_{CC} = 5V$, $I_{VCC} = 0$ | | 75 | 135 | μA |
| V_{IN} Shutdown Current | $M_0, M_1 = 0V$, $2.7V \leq V_{IN} \leq 5V$ | | | 1 | μA |
| | $M_0, M_1 = 0V$, $2.7V \leq V_{IN} \leq 5V$ | | | 2 | μA |
| | $M_0, M_1 = 0V$, $5V < V_{IN} \leq 10V$ | | | 25 | μA |
| DV_{CC} Operating Current | $M_0, M_1 = DV_{CC}$, $C_{IN} = 1MHz$ | | 6 | 20 | μA |
| DV_{CC} Shutdown Current | $M_0, M_1 = 0V$ | | | 1 | μA |
| V_{CC} Output Voltage | $0 \leq I_{VCC} \leq 10mA$, $2.7V \leq V_{IN} \leq 10V$ | | | | |
| | $0 \leq I_{VCC} \leq 20mA$, $3V \leq V_{IN} \leq 10V$ | | | | |
| | $M_0, M_1 = DV_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| | $M_0 = DV_{CC}$, $M_1 = 0$ | 2.80 | 3.00 | 3.20 | V |
| V_{CC} Output Ripple | $M_0 = 0$, $M_1 = DV_{CC}$ | $V_{IN} - 0.3$ | | V_{IN} | V |
| | $V_{IN} = 3.6V$, $I_{VCC} = 10mA$, $V_{CC} = 5V$ | | 75 | | mV _{P-P} |

ELECTRICAL CHARACTERISTICS

$V_{IN} = 2.7V$ to $10V$, $DV_{CC} = 1.8V$ to $5.5V$, controller digital pins tied to DV_{CC} , SIM digital pins floating, EN, FB pins tied to GND (LTC1556), $C_1 = 0.1\mu F$, $C_{OUT} = 10\mu F$ unless otherwise specified.

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|--------|--|---------------------|---|--------------------|
| V_{CC} Short-Circuit Current | V_{CC} Shorted to GND | ● | | 12.5 | 40 | mA |
| Auxiliary LDO V_{OUT} (V_{LDO}) | EN = High, $V_{CC} = 5V$, FB = LDO, $I_{LDO} = 5mA$ (LTC1556) | ● | 4.00 | 4.3 | 4.55 | V |
| Auxiliary Switch Resistance | EN = High, $V_{CC} = 5V$, FB = GND (LTC1556) | ● | | 18 | 30 | Ω |
| FB Input Resistance | (LTC1556) | | | 200 | | k Ω |
| Charge Pump f_{OSC} | | ● | 500 | 650 | 800 | kHz |
| Controller Inputs/Outputs, $DV_{CC} = 3V$ | | | | | | |
| Input Current (I_{IH} , I_{IL}) | M0, M1, \overline{SS} , RIN, CIN DDRV, EN | ● ● | -1 -5 | | 1 5 | μA μA |
| High Level Input Current (I_{IH}) | DATA | ● | -20 | | 20 | μA |
| Low Level Input Current (I_{IL}) | DATA | ● | | | 1 | mA |
| High Input Voltage Threshold (V_{IH}) | M0, M1, RIN, CIN, DDRV, EN DATA | ● ● | | | $0.7 \times DV_{CC}$ $DV_{CC} - 0.6$ | V V |
| Low Input Voltage Threshold (V_{IL}) | M0, M1, RIN, CIN, DDRV, EN DATA | ● ● | $0.2 \times DV_{CC}$ 0.4 | | | V V |
| High Level Output Voltage (V_{OH}) | DATA Source Current = $20\mu A$, I/O = V_{CC} | ● | $0.7 \times DV_{CC}$ | | | V |
| Low Level Output Voltage (V_{OL}) | DATA Sink Current = $-200\mu A$, I/O = 0V (Note 3) | ● | | | 0.4 | V |
| DATA Pull-up Resistance | Between DATA and DV_{CC} | ● | 13 | 20 | 28 | k Ω |
| DATA Output Rise/Fall Time | DATA Loaded with 30pF | ● | | 1.3 | 2 | μs |
| SIM Inputs/Outputs, $DV_{CC} = 3V$, $V_{CC} = 3V$ or $5V$ | | | | | | |
| I/O High Input Voltage Threshold (V_{IH}) | $I_{IH(MAX)} = \pm 20\mu A$ | ● | | $0.5 \times V_{CC}$ | $0.7 \times V_{CC}$ | V |
| I/O Low Input Voltage Threshold (V_{IL}) | $I_{IL(MAX)} = 1mA$ | ● | 0.4 | | | V |
| High Level Output Voltage (V_{OH}) | I/O, Source Current = $20\mu A$, DATA or DDRV = DV_{CC} RST, CLK, Source Current = $20\mu A$ | ● ● | $0.8 \times V_{CC}$ $0.9 \times V_{CC}$ | | | V V |
| Low Level Output Voltage (V_{OL}) | I/O, Sink Current = $-1mA$, DATA or DDRV = 0V (Note 3) RST, CLK, Sink Current = $-200\mu A$ | ● ● | | | 0.4 0.4 | V V |
| I/O Pull-Up Resistance | Between I/O and V_{CC} | ● | 6.5 | 10 | 14 | k Ω |
| SIM Timing Parameters, $DV_{CC} = 3V$, $V_{CC} = 5V$ | | | | | | |
| CLK Rise/Fall Time | CLK Loaded with 30pF | ● | | | 18 | ns |
| RST, I/O Rise/Fall Time | RST, I/O Loaded with 30pF | ● | | | 1 | μs |
| CLK Frequency | CLK Loaded with 30pF | ● | | | 5 | MHz |
| V_{CC} Turn-On Time | $\overline{SS} = DV_{CC}$, $C_{OUT} = 10\mu F$, $I_{VCC} = 0$ $\overline{SS} = 0V$, $C_{OUT} = 10\mu F$, $I_{VCC} = 0$ | | | 1 6 | | ms ms |
| V_{CC} Discharge Time to 1V | $I_{VCC} = 0$, $V_{CC} = 5V$, $C_{OUT} = 10\mu F$ | | | 3 | | ms |

The ● denotes specifications which apply over the specified temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

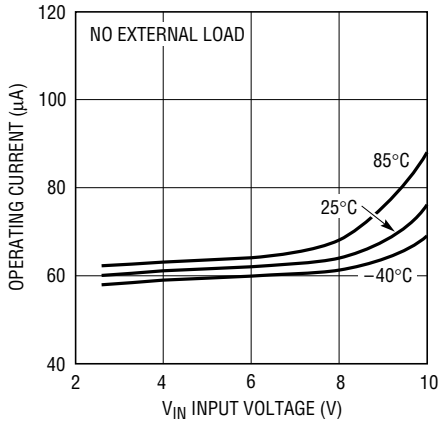
Note 2: C grade device specifications are guaranteed over the $0^{\circ}C$ to $70^{\circ}C$ temperature range. In addition, C grade device specifications are assured

over the $-40^{\circ}C$ to $85^{\circ}C$ temperature range by design or correlation, but are not production tested.

Note 3: The DATA and I/O pull-down drivers must also sink current sourced by the internal pull-up resistors.

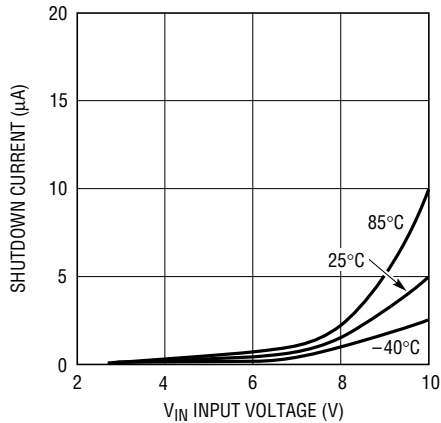
TYPICAL PERFORMANCE CHARACTERISTICS

Operating Current vs Input Voltage



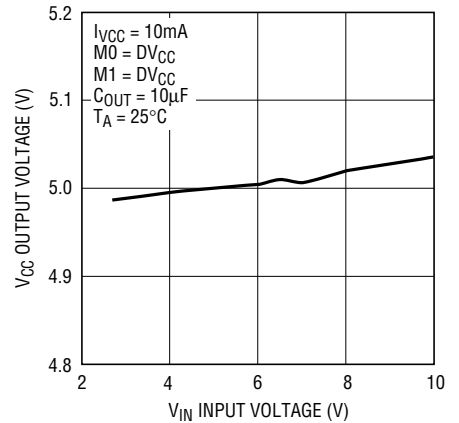
1555/56 G01

Shutdown Current vs Input Voltage



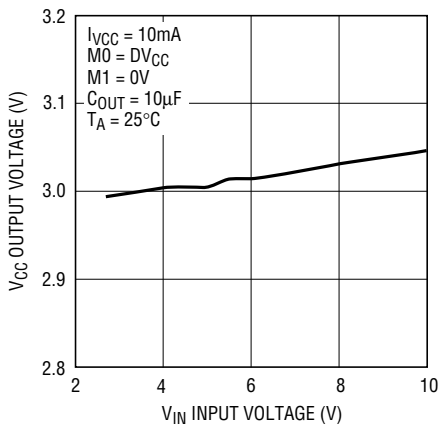
1555/56 G02

V_{CC} Output Voltage vs Input Voltage (5V Mode)



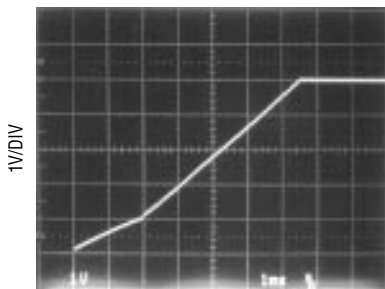
1555/56 G03

V_{CC} Output Voltage vs Input Voltage (3V Mode)



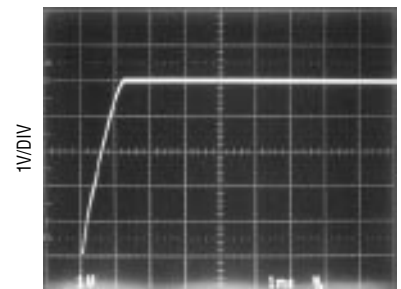
1555/56 G04

V_{CC} Output Voltage Turn-On Time, SS Enabled



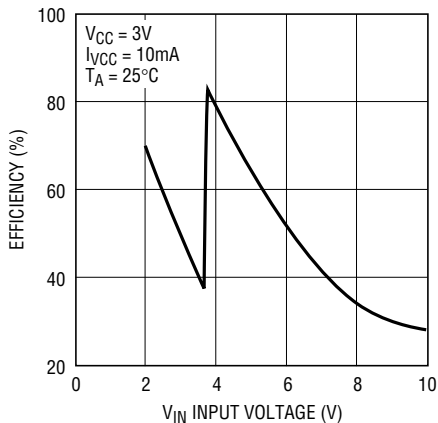
1555/56 G05

V_{CC} Output Voltage Turn-On Time, SS Disabled



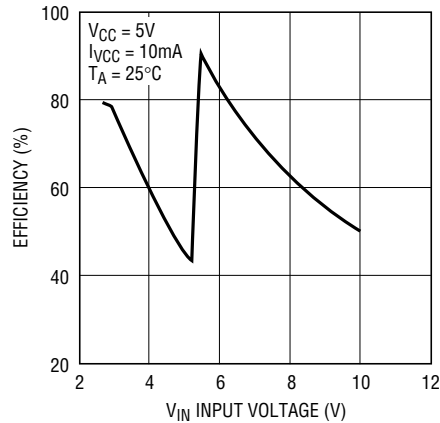
1555/56 G06

3V V_{CC} Efficiency vs Input Voltage



1555/56 G07

5V V_{CC} Efficiency vs Input Voltage



1555/56 G08

PIN FUNCTIONS

LTC1555/LTC1556

CIN (Pin 1): Clock Input Pin from Controller.

RIN (Pin 2): Reset Input Pin from Controller.

DATA (Pin 3): Controller Side Data Input/Output Pin. Can be used for single pin bidirectional data transfer between the controller and the SIM card as long as the controller data pin is open drain. The controller output must be able to sink 1mA max when driving the DATA pin low due to the internal pull-up resistors on the DATA and I/O pins. If the controller data output is not open drain, then the DDRV pin should be used for sending data to the SIM card and the DATA pin used for receiving data from the SIM card (see Figure 1).

DDRV (Pin 4): Optional Data Input Pin for Sending Data to the SIM card. When not needed, the DDRV pin should be left floating or tied to DV_{CC} (an internal 1μA current source will pull the DDRV pin up to DV_{CC} if left floating).

DV_{CC} (Pins 5/7): Supply Voltage for Controller Side Digital I/O Pins. May be between 1.8V and 5.5V (typically 3V).

SS (Pins 6/8): Soft Start Enable Pin. A logic low will enable the charge pump inrush current limiting feature. A logic high will disable the soft start feature and allow V_{CC} to be ramped as quickly as possible upon start-up and coming out of shutdown.

M1 (Pins 7/9): Mode Control Bit 1 (see Truth Table).

M0 (Pins 8/10): Mode Control Bit 0 (see Truth Table).

This table defines the various operating modes that may be obtained via the M0 and M1 mode control pins.

Truth Table

| M0 | M1 | MODE |
|------------------|------------------|-----------------------------------|
| 0V | 0V | Shutdown (V _{CC} = 0V) |
| 0V | DV _{CC} | V _{CC} = V _{IN} |
| DV _{CC} | 0V | V _{CC} = 3V |
| DV _{CC} | DV _{CC} | V _{CC} = 5V |

GND (Pins 9/11, 12): Ground for Both the SIM and the Controller. Should be connected to the SIM GND contact as well as to the V_{IN}/Controller GND. Proper grounding and supply bypassing is required to meet 10kV ESD specifications.

C1⁻ (Pins 10/12): Charge Pump Flying Capacitor Negative Input.

C1⁺ (Pins 11/13): Charge Pump Flying Capacitor Positive Input.

V_{IN} (Pins 12/14): Charge Pump Input Voltage Pin. Input voltage range is 2.7V to 10V. Connect a 10μF low ESR input bypass capacitor close to the V_{IN} pin.

V_{CC} (Pins 13/15): SIM Card V_{CC} Output. This pin should be connected to the SIM V_{CC} contact. The V_{CC} output voltage is determined by the M0 and M1 pins (see Truth Table). V_{CC} is discharged to GND during shutdown (M0, M1 = 0V). A 10μF low ESR output capacitor should connect close to the V_{CC} pin.

I/O (Pins 14/18): SIM Side I/O Pin. The pin is an open drain output with a nominal pull-up resistance of 10k and should be connected to the SIM I/O contact. The SIM card must sink up to 1mA max when driving the I/O pin low due to the internal pull-up resistors on the I/O and DATA pins. The I/O pin is held active low when the part is in shutdown.

RST (Pins 15/19): Level Shifted Reset Output Pin. Should be connected to the SIM RST contact.

CLK (Pins 16/20): Level Shifted Clock Output Pin. Should be connected to the SIM CLK contact. Careful trace routing is recommended due to fast rise and fall edge speeds.

PIN FUNCTIONS

LTC1556 Only

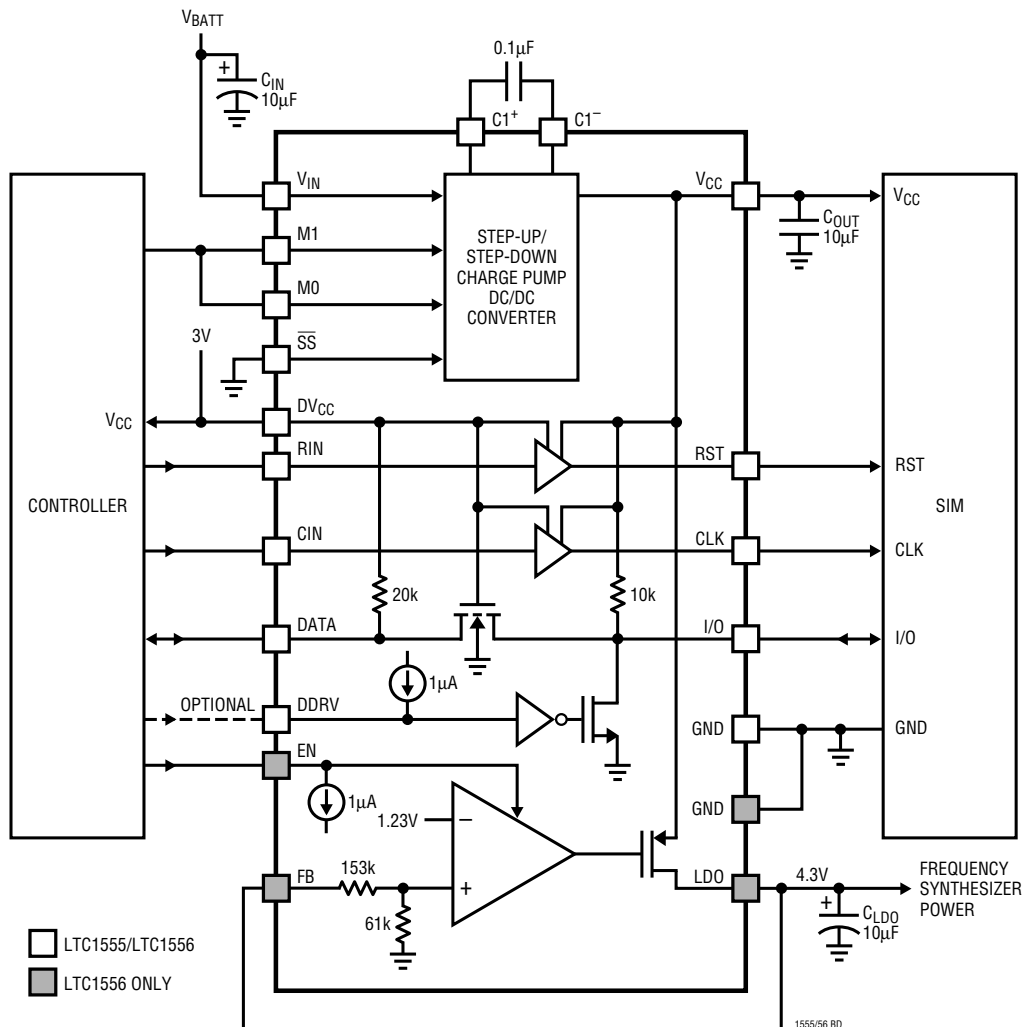
EN (Pin 5): Auxiliary LDO/Power Switch Enable Pin. A logic high on this pin from the controller will enable the auxiliary LDO output. When the LDO is disabled, the LDO output will float or be pulled to ground by the load. If left floating, the EN pin will be pulled down to GND by an internal $1\mu\text{A}$ current source.

FB (Pin 6): Auxiliary LDO Feedback Pin. When FB is connected to the LDO pin (Pin 17), the LDO output is regulated to 4.3V (typ). If the FB pin is left open or tied to

ground, the regulator acts as a $\leq 30\Omega$ switch between V_{CC} and LDO.

LDO (Pin 17): LDO Output Pin. This pin should be tied to the FB pin for 4.3V LDO operation. The 4.3V LDO output is usable only when V_{CC} is 5V (or greater). It is not available when $V_{CC} = 3\text{V}$. The LDO output may also be used as a $\leq 30\Omega$ power switch if the FB pin is grounded or left floating. When used as a regulator, LDO must be bypassed to GND with a $\geq 3.3\mu\text{F}$ capacitor. The LDO output current will subtract from available V_{CC} current.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LTC1555/LTC1556 perform the two primary functions necessary for 3V controllers (e.g., GSM cellular telephone controllers, smart card readers, etc.) to communicate with 5V SIMs or smart cards. They produce a regulated 5V V_{CC} supply for the SIM and provide level translators for communication between the SIM and the controller.

V_{CC} Voltage Regulator

The regulator section of the LTC1555/LTC1556 (refer to the Block Diagram) consists of a step-up/step-down charge pump DC/DC converter. The charge pump can operate over a wide input voltage range (2.7V to 10V) while maintaining a regulated V_{CC} output. The wide V_{IN} range enables the parts to be powered directly from a battery (if desired) rather than from a 3V DC/DC converter output. When V_{IN} is less than the desired V_{CC} the parts operate as switched capacitor voltage doublers. When V_{IN} is greater than V_{CC} the parts operate as gated switch step-down converters. In either case, voltage conversion requires only one small flying capacitor and output capacitor.

The V_{CC} output can be programmed to either 5V or 3V via the M0 and M1 mode pins. This feature is useful in applications where either a 5V or 3V SIM may be used. The charge pump V_{CC} output may also be connected directly to V_{IN} if desired. When the charge pump is put into shutdown (M0, M1 = 0), V_{CC} is pulled to GND via an internal switch to aid in proper system supply sequencing.

The soft start feature limits inrush currents upon start-up or coming out of shutdown mode. When the \overline{SS} pin is tied to GND, the soft start feature is enabled. This limits the effective inrush current out of V_{IN} to approximately 25mA ($C_{OUT} = 10\mu\text{F}$). Inrush current limiting is especially useful when powering the LTC1555/LTC1556 from a 3V DC/DC output since the unlimited inrush current may approach 200mA and cause voltage transients on the 3V supply. However, in cases where fast turn-on time is desired, the soft start feature may be overridden by tying the \overline{SS} pin to DV_{CC} .

Capacitor Selection

For best performance, it is recommended that low ESR ($< 0.5\Omega$) capacitors be used for both C_{IN} and C_{OUT} to reduce noise and ripple. The C_{IN} and C_{OUT} capacitors should be either ceramic or tantalum and should be $10\mu\text{F}$ or greater (ceramic capacitors will produce the smallest output ripple). If the input source impedance is very low ($< 0.5\Omega$), C_{IN} may not be needed. Increasing the size of C_{OUT} to $22\mu\text{F}$ or greater will reduce output voltage ripple—particularly with high V_{IN} voltages (8V or greater). A ceramic capacitor is recommended for the flying capacitor C1 with a value of $0.1\mu\text{F}$ or $0.22\mu\text{F}$.

Output Ripple

Normal LTC1555/LTC1556 operation produces voltage ripple on the V_{CC} pin. Output voltage ripple is required for the parts to regulate. Low frequency ripple exists due to the hysteresis in the sense comparator and propagation delays in the charge pump enable/disable circuits. High frequency ripple is also present mainly from the ESR (equivalent series resistance) in the output capacitor. Typical output ripple ($V_{IN} < 8\text{V}$) under maximum load is 75mV peak-to-peak with a low ESR, $10\mu\text{F}$ output capacitor. For applications requiring V_{IN} to exceed 8V, a $22\mu\text{F}$ or larger C_{OUT} capacitor is recommended to maintain maximum ripple in the 75mV range.

The magnitude of the ripple voltage depends on several factors. High input voltages increase the output ripple since more charge is delivered to C_{OUT} per charging cycle. A large C1 flying capacitor ($> 0.22\mu\text{F}$) also increases ripple in step-up mode for the same reason. Large output current load and/or a small output capacitor ($< 10\mu\text{F}$) results in higher ripple due to higher output voltage dV/dt . High ESR capacitors ($\text{ESR} > 0.5\Omega$) on the output pin cause high frequency voltage spikes on V_{OUT} with every clock cycle.

A $10\mu\text{F}$ ceramic capacitor on the V_{CC} pin should produce acceptable levels of output voltage ripple in nearly all applications. However, there are several ways to further

APPLICATIONS INFORMATION

reduce the ripple. A larger C_{OUT} capacitor (22 μ F or greater) will reduce both the low and high frequency ripple due to the lower C_{OUT} charging and discharging dV/dt and the lower ESR typically found with higher value (larger case size) capacitors. A low ESR ceramic output capacitor will minimize the high frequency ripple, but will not reduce the low frequency ripple unless a high capacitance value is chosen (10 μ F or greater). A reasonable compromise is to use a 10 μ F to 22 μ F tantalum capacitor in parallel with a 1 μ F to 3.3 μ F ceramic capacitor on V_{OUT} to reduce both the low and high frequency ripple. An RC filter may also be used to reduce high frequency voltage spikes (see Figure 1).

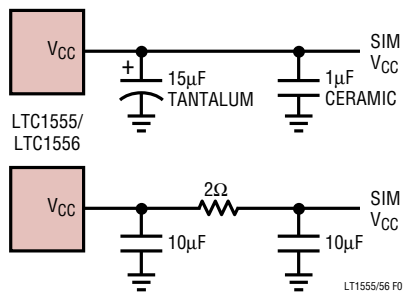


Figure 1. V_{CC} Output Ripple Reduction Techniques

Shutting Down the DV_{CC} Supply

To conserve power, the DV_{CC} supply may be shut down while the V_{IN} supply is still active. When the DV_{CC} supply is brought to 0V, weak internal currents will force the LTC1555/LTC1556 into shutdown mode regardless of the voltages present on the M0 and M1 pins. However, if the M0 and M1 pins are floating or left connected to DV_{CC} as the supply is shut down, the parts may take several

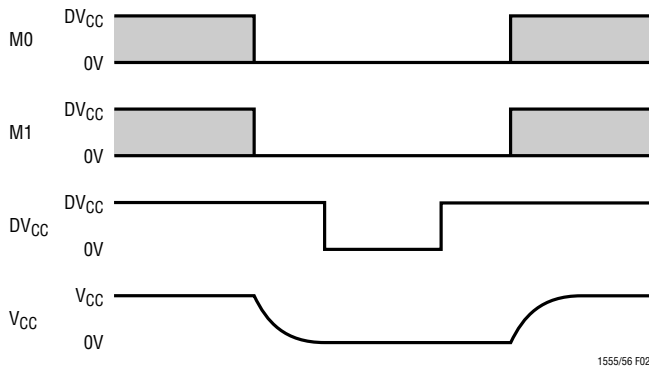


Figure 2. Recommended DV_{CC} Shutdown and Start-Up Timing

hundred milliseconds to completely shut down. To ensure prompt and proper V_{CC} shutdown, always force the M0 and M1 pins to a logic low state before shutting down the DV_{CC} supply (see Figure 2). Similarly, bring the DV_{CC} supply to a valid level before allowing the M0 and M1 pins to go high when coming out of shutdown. This can be achieved with pull-down resistors from M0 and M1 to GND if necessary. (Note: shutting down the DV_{CC} supply with V_{IN} active is not recommended with early date code material. Consult factory for valid date code starting point for shutting down the DV_{CC} supply.)

Level Translators

All SIMs and smart cards contain a clock input, reset input and a bidirectional data input/output. The LTC1555/LTC1556 provide level translators to allow controllers to communicate with the SIM (see Figures 3a and 3b). The CLK and RST inputs to the SIM are level shifted from the controller supply rails (DV_{CC} and GND) to the SIM supply rails (V_{CC} and GND). The data input to the SIM may be provided two different ways. The first method is to use the DATA pin as a bidirectional level translator. This configuration is only allowed if the controller data output pin is open drain (all SIM I/O pins are open drain). Internal pull-up resistors are provided for both the DATA pin and the

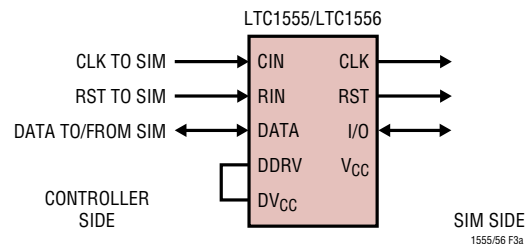


Figure 3a. Level Translator Connections for Bidirectional Controller DATA Pin

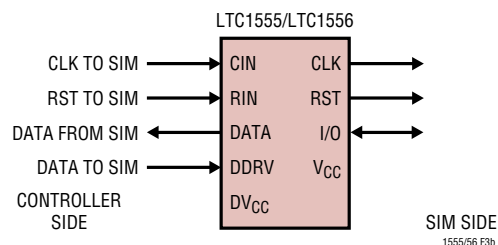


Figure 3b. Level Translator Connections for One-Directional Controller Side DATA Flow

APPLICATIONS INFORMATION

I/O pin on the SIM side. The second method is to use the DDRV pin to send data to the SIM and use the DATA pin to receive data from the SIM. When the DDRV pin is not used, it should either be left floating or tied to DV_{CC} .

Level Translation with $DV_{CC} > V_{CC}$

It is assumed that most applications for these parts will use controller supply voltages (DV_{CC}) less than or equal to V_{CC} . In cases where DV_{CC} is greater than V_{CC} by more than 0.6V or so, the parts' operation will be affected in the following ways: 1) A small DC current (up to 100 μ A) will flow from DV_{CC} to V_{CC} through the DATA pull-up resistor, N-channel pass device and the I/O pull-up resistor (except when the part is in shutdown at which time DV_{CC} is disconnected from V_{CC} by turning off the pass device). If the V_{CC} load current is less than the DV_{CC} current, the V_{CC} output may be pulled out of regulation until sufficient load current pulls V_{CC} back into regulation. 2) When the SIM is sending data back to the controller, a logic high on the I/O pin will result in the DATA pin being pulled up to $[V_{CC} + 1/3(DV_{CC} - V_{CC})]$, not all the way up to DV_{CC} . For example, if DV_{CC} is 5V and V_{CC} is 3V, the DATA pin will only swing from $\approx 0.1V$ to 3.67V when receiving data from the SIM side.

Optional LDO Output

The LTC1556 also contains an internal LDO regulator for providing a low noise boosted supply voltage for low power external circuitry (e.g., frequency synthesizers, etc.) Tying the FB pin to the LDO pin provides a regulated 4.3V at the LDO output (see Figure 4). A 3.3 μ F (minimum) capacitor is

required to ensure output stability. A 10 μ F low ESR capacitor is recommended, however, to minimize LDO output noise. The LDO output may also be used as an auxiliary switch to V_{CC} . If the FB pin is left floating or is tied to GND, the LDO pin will be internally connected to the V_{CC} output through the P-channel pass device. The LDO may be disabled at any time by switching the EN pin from DV_{CC} to GND. The 4.3V LDO output is usable only when V_{CC} is 5V (or greater). It is not available when $V_{CC} = 3V$.

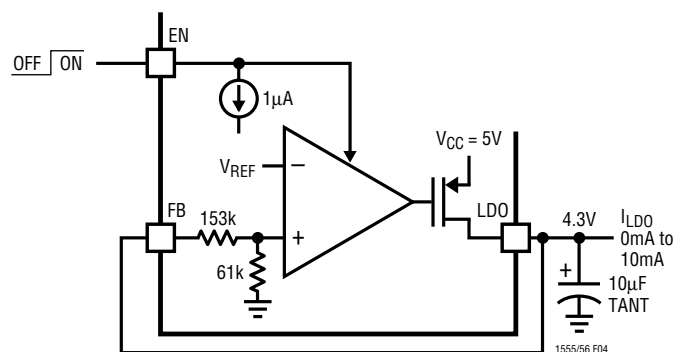


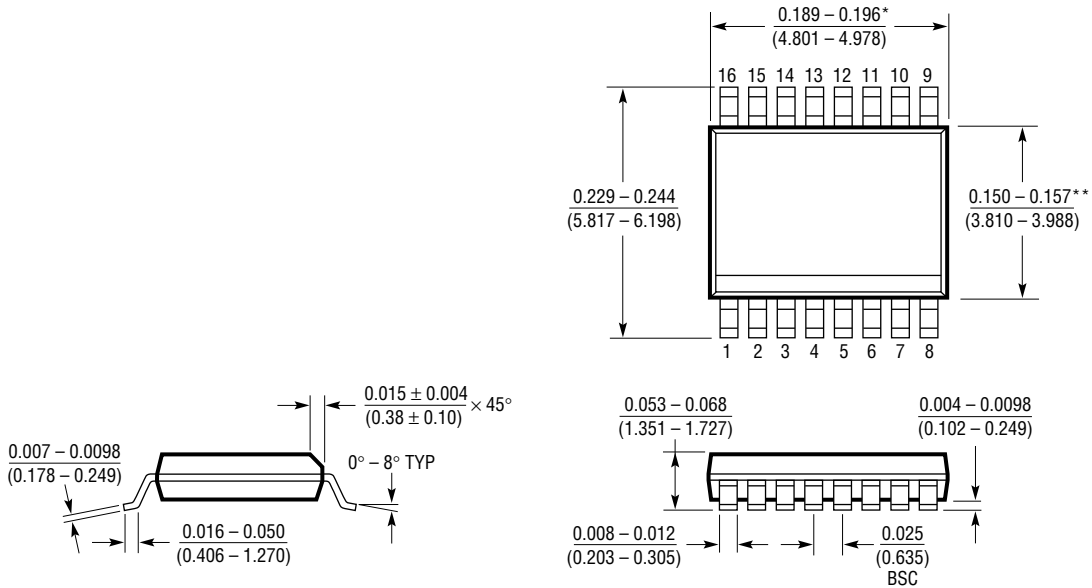
Figure 4. Auxiliary LDO Connections (LTC1556 Only)

10kV ESD Protection

All pins that connect to the SIM (CLK, RST, I/O, V_{CC} , GND) withstand over 10kV of human body model (100pF/1.5k Ω) ESD. In order to ensure proper ESD protection, careful board layout is required. The GND pins should be tied directly to a GND plane. The V_{CC} capacitor should be located very close to the V_{CC} pin and tied immediately to the GND plane.

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
 (LTC DWG # 05-08-1641)

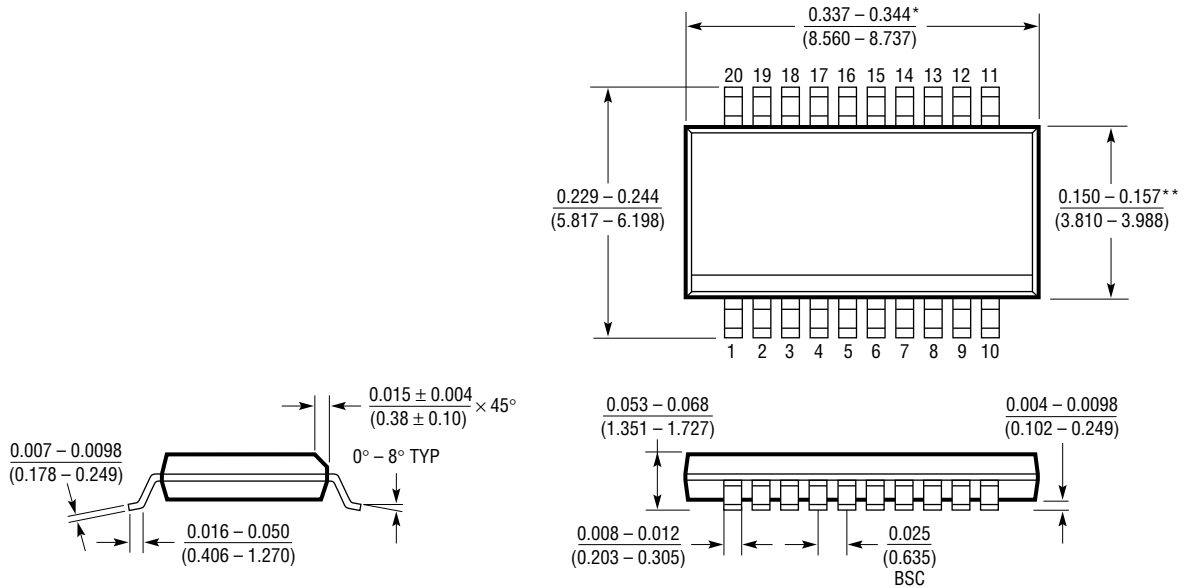


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
 ** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1197

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

GN Package
20-Lead Plastic SSOP (Narrow 0.150)
 (LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006* (0.152mm) PER SIDE
 ** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010* (0.254mm) PER SIDE

GN20 (SSOP) 1197

