16-Bit Byte Wide, Low Glitch Multiplying DAC with 4-Quadrant Resistors

FEATURES

- **True 16-Bit Performance over Industrial Temperature Range**
- **DNL and INL: 1LSB Max**
- **On-Chip 4-Quadrant Resistors Allow Precise 0V to 10V, 0V to –10V or ±10V Outputs**
- **2μs Settling Time to 0.0015% (with LT®1468)**
- **Asynchronous Clear Pin Resets to Zero Scale or Midscale**
- **Glitch Impulse: 1.5nV-s**
- 24-Lead SSOP Package
- Low Power Consumption: 10μW Typ
- Power-On Reset to Zero Scale or Midscale
- 2-Byte Parallel Digital Interface
- Available in 24-Lead SSOP and PDIP Packages

APPLICATIONS

- Process Control and Industrial Automation
- Direct Digital Waveform Generation
- Software-Controlled Gain Adjustment
- Automatic Test Equipment

DESCRIPTION

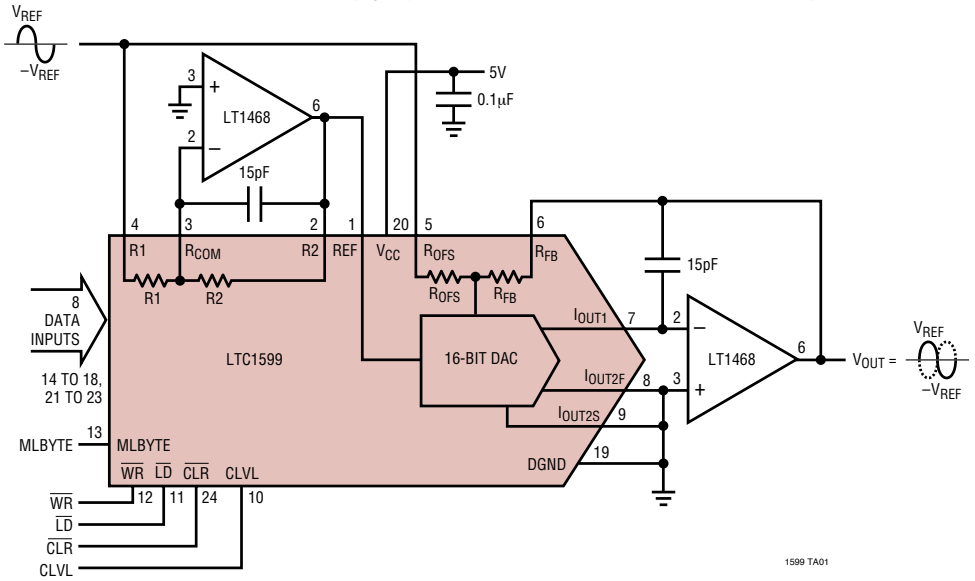
The LTC®1599 is a 2-byte parallel input 16-bit multiplying current output DAC that operates from a single 5V supply. INL and DNL are accurate to 1LSB over the industrial temperature range in both 2- and 4-quadrant multiplying modes. True 16-bit 4-quadrant multiplication is achieved with on-chip 4-quadrant multiplication resistors.

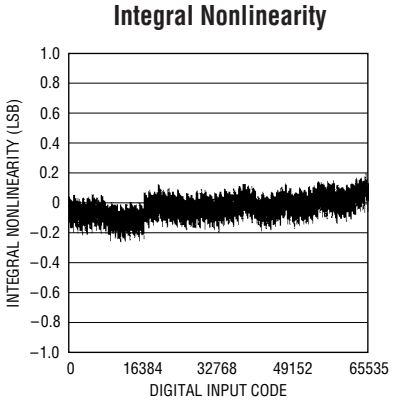
The LTC1599 is available in 24-pin PDIP and SSOP packages and is specified over the commercial and industrial temperature ranges. The device includes an internal deglitcher circuit that reduces the glitch impulse to 1.5nV-s (typ). The asynchronous $\overline{CLR}$ pin resets the LTC1599 to zero scale when the CLVL pin is at a logic low and to midscale when the CLVL pin is at a logic high.

For a full 16-bit wide parallel interface current output DAC, refer to the LTC1597 data sheet. For serial interface 16-bit current output DACs, refer to the LTC1595/LTC1596 data sheet.

TYPICAL APPLICATION

A 16-Bit, 4-Quadrant Multiplying DAC with a Minimum of External Components



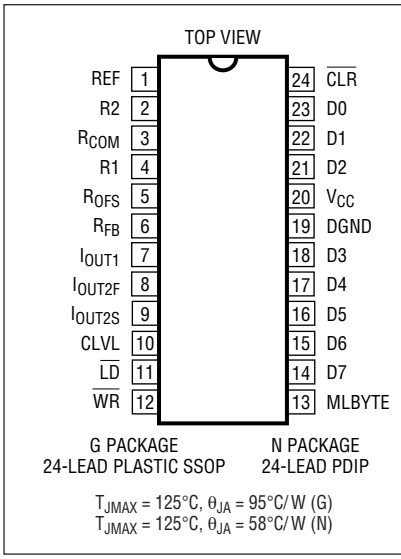


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to DGND ..... –0.3V to 7V
REF, R_{OFS}, R_{FB}, R1, R2 to DGND ..... ±25V
R_{COM} ..... –0.3V to 12V
Digital Inputs to DGND ..... –0.3V to (V_{CC} + 0.3V)
I_{OUT1}, I_{OUT2F}, I_{OUT2S} to DGND .... –0.3V to(V_{CC} + 0.3V)
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
LTC1599C ..... 0°C to 70°C
LTC1599I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
24-LEAD PLASTIC SSOP

N PACKAGE
24-LEAD PDIP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 58°C/W (N)

ORDER PART NUMBER

LTC1599ACG
LTC1599BCG
LTC1599AIG
LTC1599BIG
LTC1599ACN
LTC1599BCN
LTC1599AIN
LTC1599BIN

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V ±10%, V_{REF} = 10V, I_{OUT1} = I_{OUT2F} = I_{OUT2S} = DGND = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1599B MIN	LTC1599B TYP	LTC1599B MAX	LTC1599A MIN	LTC1599A TYP	LTC1599A MAX	UNITS
Accuracy										
	Resolution		●	16			16			Bits
	Monotonicity		●	16			16			Bits
INL	Integral Nonlinearity	T_A = 25°C (Note 2)				±2		±0.25	±1	LSB
		T_{MIN} to T_{MAX}	●			±2		±0.35	±1	LSB
DNL	Differential Nonlinearity	T_A = 25°C				±1		±0.2	±1	LSB
		T_{MIN} to T_{MAX}	●			±1		±0.2	±1	LSB
GE	Gain Error	Unipolar Mode								
		T_A = 25°C (Note 3)				±16		2	±16	LSB
		T_{MIN} to T_{MAX}	●			±24		3	±16	LSB
		Bipolar Mode								
		T_A = 25°C (Note 3)				±16		2	±16	LSB
		T_{MIN} to T_{MAX}	●			±24		3	±16	LSB
	Gain Temperature Coefficient	ΔGain/ΔTemperature (Note 4)	●		1	3		1	3	ppm/°C
	Bipolar Zero Error	T_A = 25°C				±10			±5	LSB
		T_{MIN} to T_{MAX}	●			±16			±8	LSB
I_{LKG}	OUT1 Leakage Current	T_A = 25°C (Note 5)				±5			±5	nA
		T_{MIN} to T_{MAX}	●			±15			±15	nA
PSRR	Power Supply Rejection	V_{CC} = 5V ±10%	●		±1	±2		±1	±2	LSB/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V ±10%, V_{REF} = 10V, I_{OUT1} = I_{OUT2F} = I_{OUT2S} = DGND = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
R_{REF}	DAC Input Resistance (Unipolar)	(Note 6)	●	4.5	6	10	kΩ
R1, R2	R1, R2 Resistance (Bipolar)	(Notes 6, 13)	●	9	14	20	kΩ
R_{OFS}, R_{FB}	Feedback and Offset Resistances	(Note 6)	●	9	13.5	20	kΩ
AC Performance (Note 4)							
	Output Current Settling Time	(Notes 7, 8)			1		µs
	Midscale Glitch Impulse	(Note 12)			1.5		nV-s
	Digital-to-Analog Glitch Impulse	(Note 9)			1		nV-s
	Multiplying Feedthrough Error	V_{REF} = ±10V, 10kHz Sine Wave			1		mV_{P-P}
THD	Total Harmonic Distortion	(Note 10)			108		dB
	Output Noise Voltage Density	(Note 11)			10		$nV/\sqrt{Hz}$
Analog Outputs (Note 4)							
C_{OUT}	Output Capacitance (Note 4)	DAC Register Loaded to All 1s: C_{OUT1} DAC Register Loaded to All 0s: C_{OUT1}	● ●		115 70	130 80	pF pF
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current		●		0.001	±1	µA
C_{IN}	Digital Input Capacitance	(Note 4) V_{IN} = 0V	●			8	pF
Timing Characteristics							
t_{DS}	Data to $\overline{WR}$ Setup Time		●	80	20		ns
t_{DH}	Data to $\overline{WR}$ Hold Time		●	0	–12		ns
t_{WR}	$\overline{WR}$ Pulse Width		●	80	25		ns
t_{BWS}	MLBYTE to $\overline{WR}$ Setup Time		●	0	–12		ns
t_{BWH}	MLBYTE to $\overline{WR}$ Hold Time		●	0	–12		ns
t_{LD}	$\overline{LD}$ Pulse Width		●	150	55		ns
t_{CLR}	Clear Pulse Width		●	150	50		ns
t_{LWD}	$\overline{WR}$ to $\overline{LD}$ Delay Time		●	0			ns
Power Supply							
V_{CC}	Supply Voltage		●	4.5	5	5.5	V
I_{CC}	Supply Current	Digital Inputs = 0V or V_{CC}	●			10	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: ±1LSB = ±0.0015% of full scale = ±15.3ppm of full scale.

Note 3: Using internal feedback resistor.

Note 4: Guaranteed by design, not subject to test.

Note 5: $I_{(OUT1)}$ with DAC register loaded to all 0s.

Note 6: Typical temperature coefficient is 100ppm/°C.

Note 7: I_{OUT1} load = 100Ω in parallel with 13pF.

Note 8: To 0.0015% for a full-scale change, measured from the falling edge of $\overline{LD}$.

Note 9: V_{REF} = 0V. DAC register contents changed from all 0s to all 1s or all 1s to all 0s. $\overline{LD}$ high, $\overline{WR}$ and MLBYTE pulsed.

Note 10: V_{REF} = $6V_{RMS}$ at 1kHz. DAC register loaded with all 1s. R_L = 600Ω. Unipolar mode op amp = LT1468.

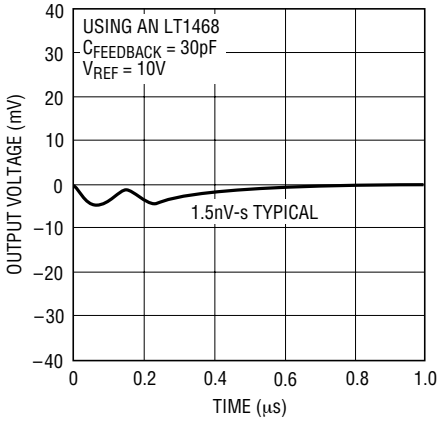
Note 11: Calculation from $e_n = \sqrt{4kTRB}$ where: k = Boltzmann constant (J/°K), R = resistance (Ω), T = temperature (°K), B = bandwidth (Hz).

Note 12: Midscale transition code 0111 1111 1111 1111 to 1000 0000 0000 0000.

Note 13: R1 and R2 are measured between R1 and R_{COM}, R2 and R_{COM}.

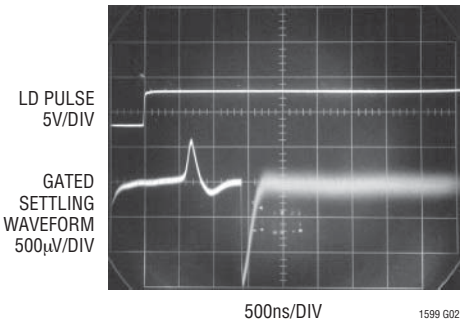
TYPICAL PERFORMANCE CHARACTERISTICS

Midscale Glitch Impulse



1599 G01

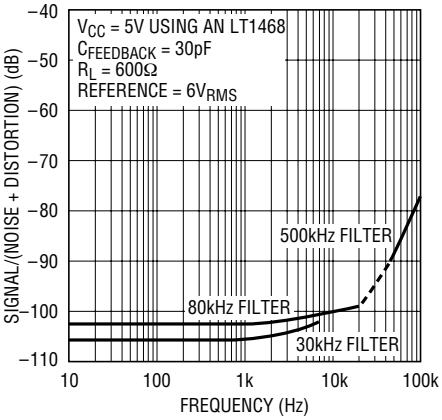
Full-Scale Settling Waveform



1599 G02

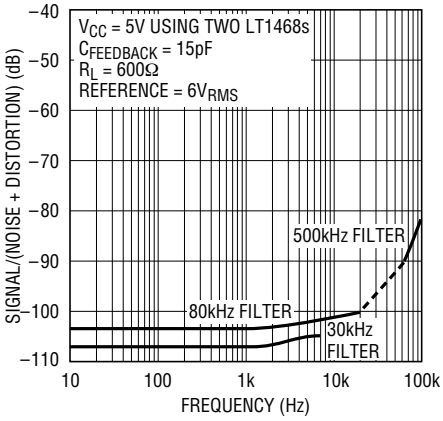
USING LT1468 OP AMP
$C_{FEEDBACK}$ = 20pF
0V to 10V STEP

Unipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency



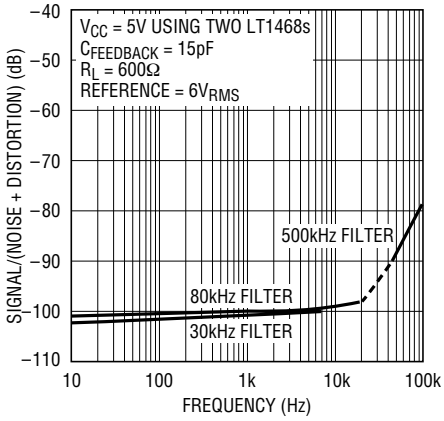
1599 G03

Bipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency, Code = All Zeros



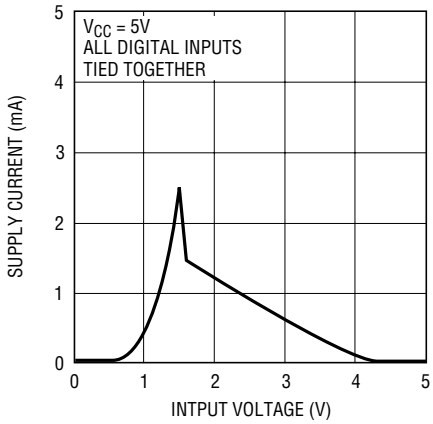
1599 G04

Bipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency, Code = All Ones



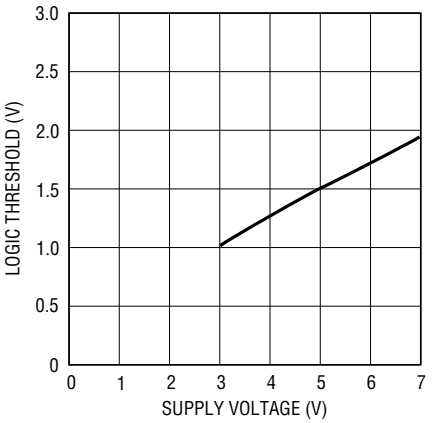
1599 G05

Supply Current vs Input Voltage



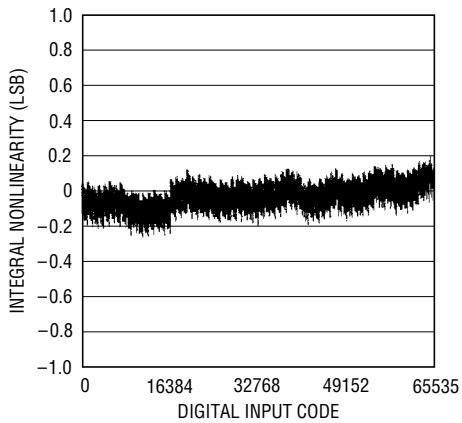
1599 G06

Logic Threshold vs Supply Voltage



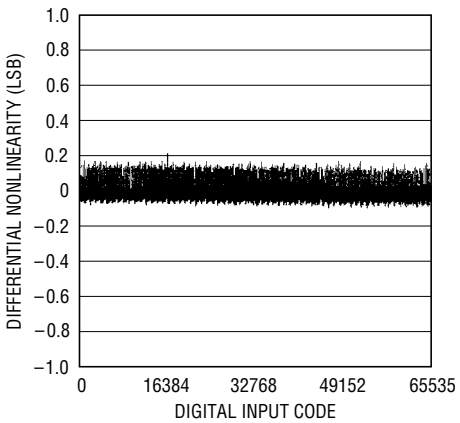
1599 G07

Integral Nonlinearity (INL)



1599 G08

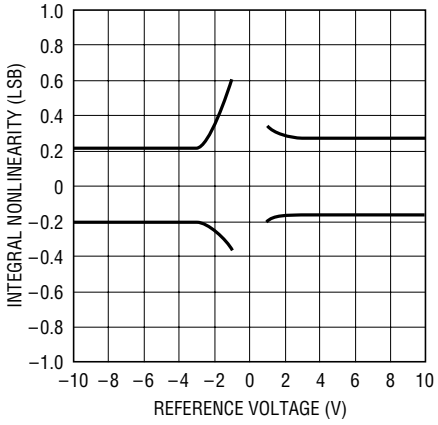
Differential Nonlinearity (DNL)



1598 G09

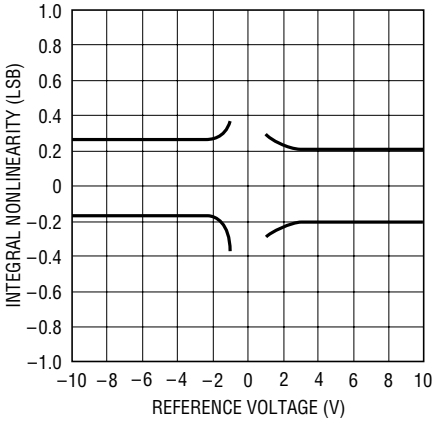
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity vs Reference Voltage in Unipolar Mode



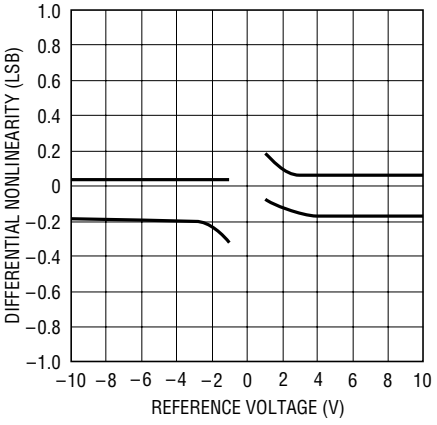
1599 G10

Integral Nonlinearity vs Reference Voltage in Bipolar Mode



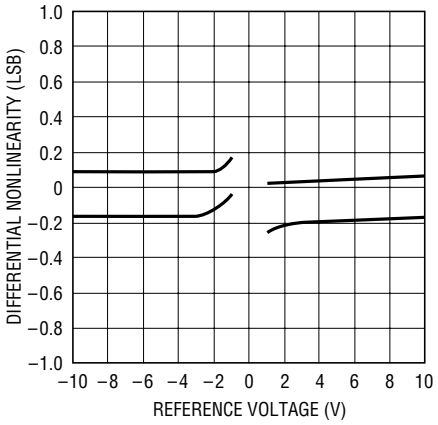
1599 G11

Differential Nonlinearity vs Reference Voltage in Unipolar Mode



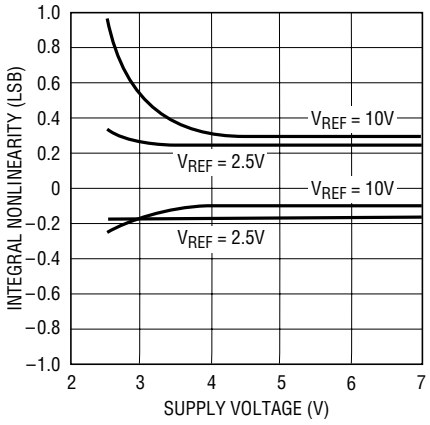
1599 G12

Differential Nonlinearity vs Reference Voltage in Bipolar Mode



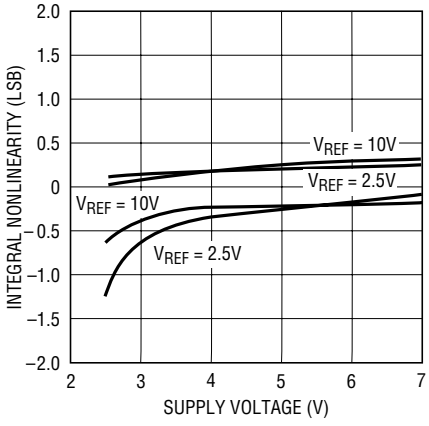
1599 G13

Integral Nonlinearity vs Suppy Voltage in Unipolar Mode



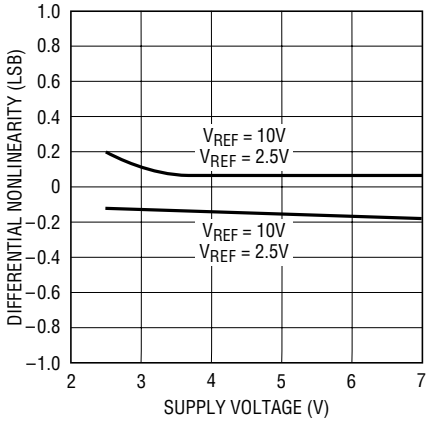
1599 G14

Integral Nonlinearity vs Suppy Voltage in Bipolar Mode



1599 G15

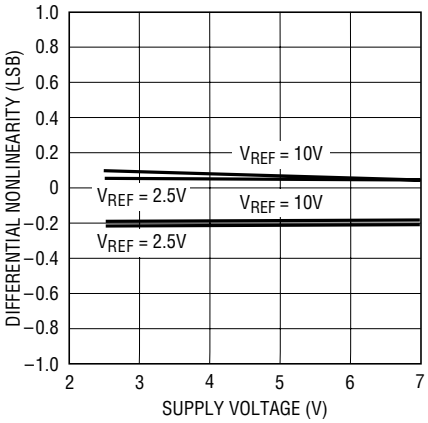
Differential Nonlinearity vs Suppy Voltage in Unipolar Mode



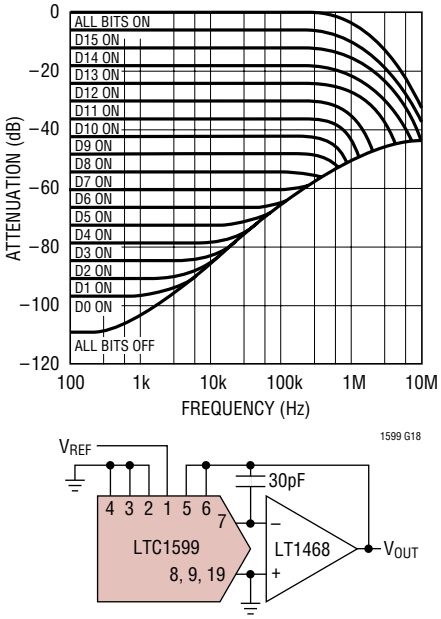
1599 G16

TYPICAL PERFORMANCE CHARACTERISTICS

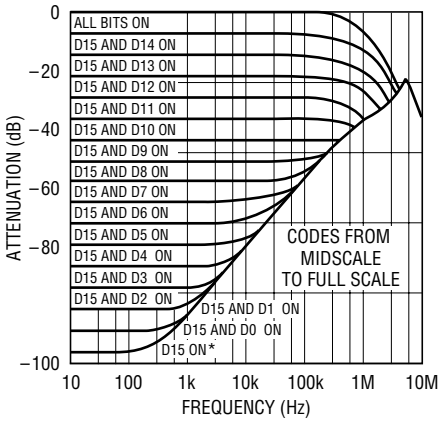
Differential Nonlinearity vs Supply Voltage in Bipolar Mode



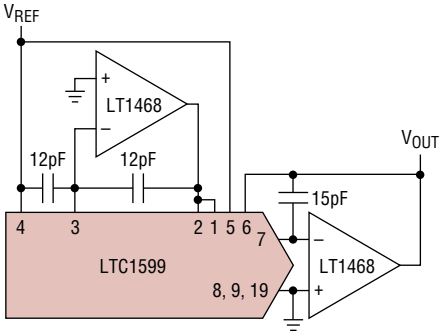
Unipolar Multiplying Mode Frequency Response vs Digital Code



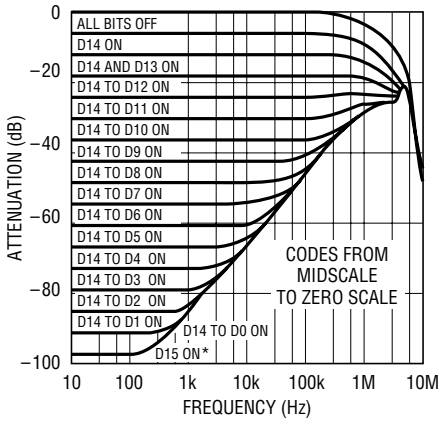
Bipolar Multiplying Mode Frequency Response vs Digital Code



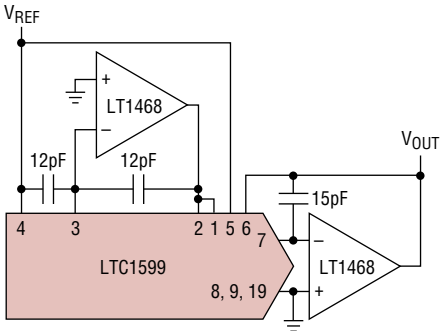
*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO –96dB TYPICAL (–78dB MAX, A GRADE)



Bipolar Multiplying Mode Frequency Response vs Digital Code



*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO –96dB TYPICAL (–78dB MAX, A GRADE)



PIN FUNCTIONS

REF (Pin 1): Reference Input. Typically ±10V, accepts up to ±25V. In 2-quadrant mode, this pin is the reference input. In 4-quadrant mode, this pin is driven by external inverting reference amplifier.

R2 (Pin 2): 4-Quadrant Resistor R2. Typically ±10V, accepts up to ±25V. In 2-quadrant operation, connect this pin to ground. In 4-quadrant mode tie to the REF pin and to the output of an external amplifier. See Figures 1 and 3.

R_{COM} (Pin 3): Center Tap Point of the Two 4-Quadrant Resistors R1 and R2. Normally tied to the inverting input of an external amplifier in 4-quadrant operation, otherwise connect this pin to ground. See Figures 1 and 3. The absolute maximum voltage range on this pin is –0.3V to 12V.

R1 (Pin 4): 4-Quadrant Resistor R1. Typically ±10V, accepts up to ±25V. In 2-quadrant operation connect this pin to ground. In 4-quadrant mode tie to R_{OFS} (Pin 5). See Figures 1 and 3.

R_{OFS} (Pin 5): Bipolar Offset Resistor. Typically swings ±10V, accepts up to ±25V. In 2-quadrant operation, tie to R_{FB}. In 4-quadrant operation tie to R1.

R_{FB} (Pin 6): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp. Typically swings ±10V. Swings ±V_{REF}.

I_{OUT1} (Pin 7): DAC Current Output. Tie to the inverting input of the current to voltage converter op amp.

I_{OUT2F} (Pin 8): Force Complement Current Output. Normally tied to ground.

I_{OUT2S} (Pin 9): Sense Complement Current Output. Normally tied to ground.

CLVL (Pin 10): Clear Level. CLVL = 0, selects reset to zero code. CLVL = 1, selects reset to midscale code. Normally hardwired to a logic high or a logic low.

$\overline{LD}$ (Pin 11): DAC Digital Input Load Control Input. When $\overline{LD}$ is taken to a logic low, data is loaded from the input register into the DAC register, updating the DAC output.

$\overline{WR}$ (Pin 12): DAC Digital Write Control Input. When $\overline{WR}$ is taken to a logic low, data is loaded from the 8 digital input pins into the 16-bit wide input register. The MLBYTE pin determines whether the MSB or LSB byte is loaded.

MLBYTE (Pin 13): MSB or LSB Byte Select. When MLBYTE is taken to a logic low and $\overline{WR}$ is taken to a logic low, data is loaded from the 8 digital input pins into the first 8 bits of the 16-bit wide input register. When MLBYTE is taken to a logic high and $\overline{WR}$ is taken to a logic low, data is loaded from the 8 digital input pins into the 8 MSB bits of the input register.

D7 to D3 (Pins 14 to 18): Digital Input Data Bits.

DGND (Pin 19): Digital Ground. Tie to ground.

V_{CC} (Pin 20): The Positive Supply Input. 4.5V ≤ V_{CC} ≤ 5.5V. Requires a bypass capacitor to ground.

D2 to D0 (Pins 21 to 23): Digital Input Data Bits.

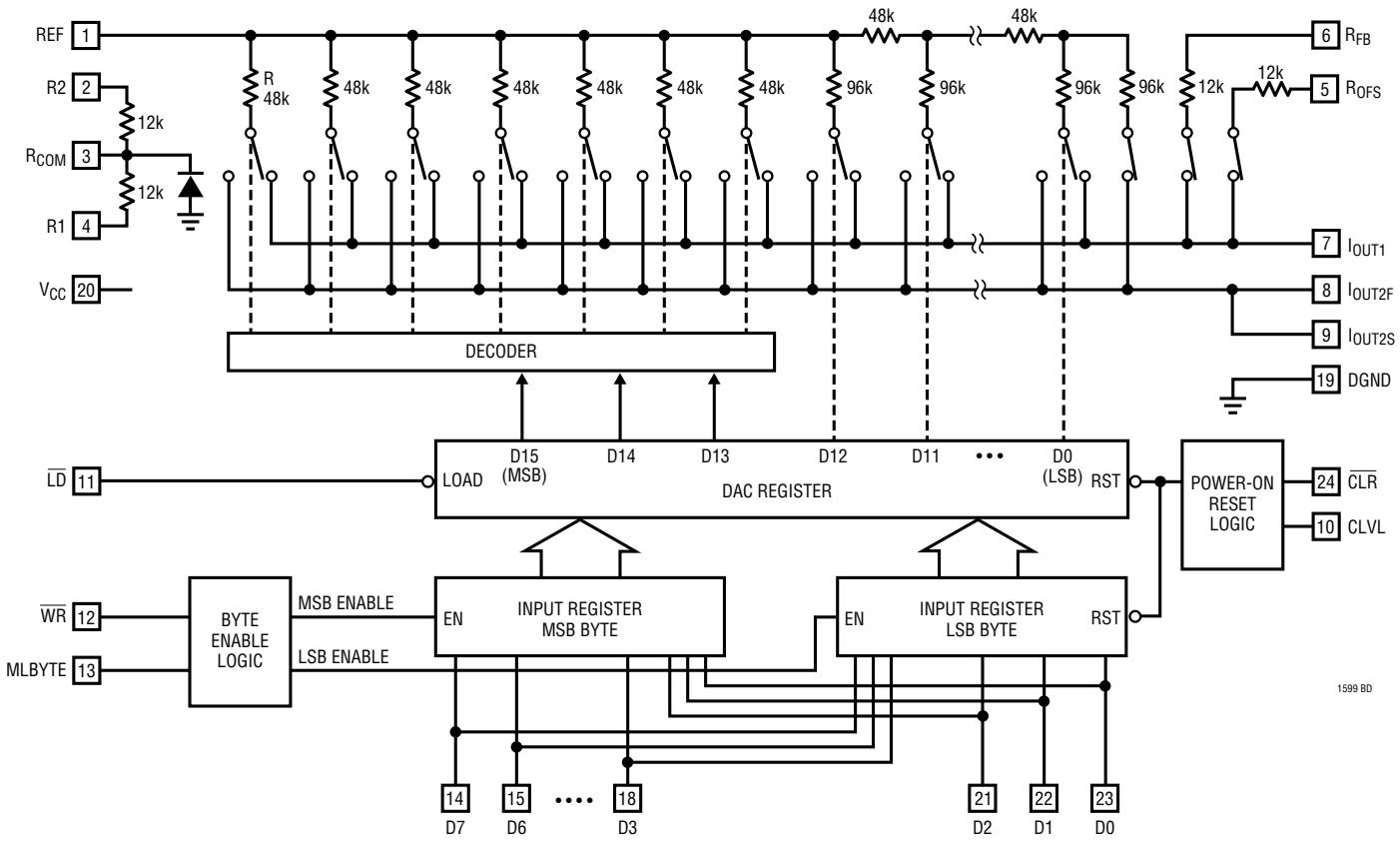
$\overline{CLR}$ (Pin 24): Digital Clear Control Function for the DAC. When $\overline{CLR}$ and CLVL are taken to a logic low, the DAC output and all internal registers are set to zero code. When $\overline{CLR}$ is taken to a logic low and CLVL is taken to a logic high, the DAC output and all internal registers are set to midscale code.

TRUTH TABLE

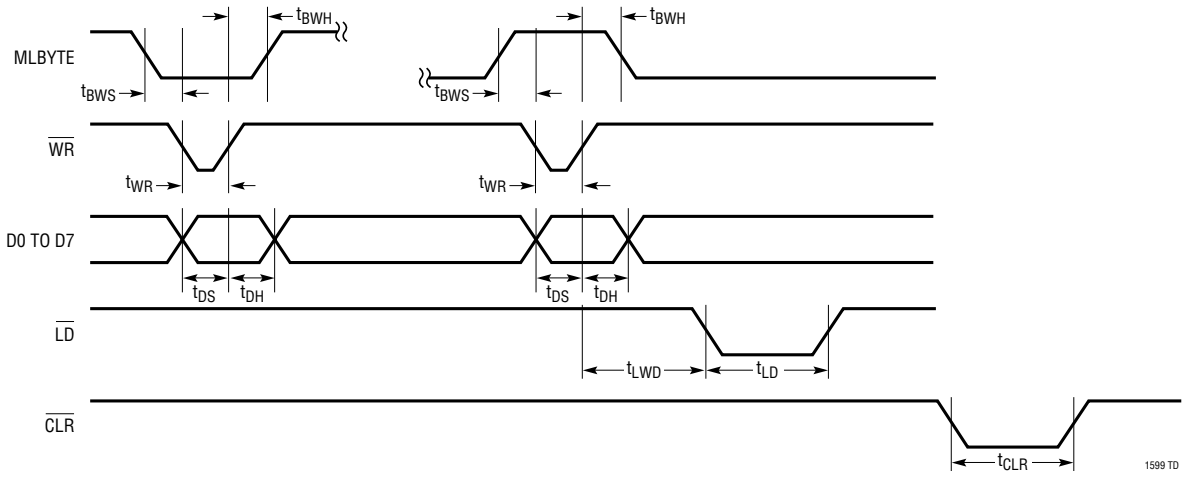
Table 1

CONTROL INPUTS				
$\overline{CLR}$	$\overline{WR}$	MLBYTE	$\overline{LD}$	REGISTER OPERATION
0	X	X	X	Reset Input and DAC Registers to Zero Scale When CLVL = 0 and Midscale When CLVL = 1
1	⎍	0	1	Load the LSB Byte of the Input Register with All 8 Data Bits
1	⎍	1	1	Load the MSB Byte of the Input Register with All 8 Data Bits
1	1	X	⎍	Load the DAC Register with the Contents of the Input Register
1	1	X	1	No Register Operation
1	⎍	X	⎍	Flow-Through Mode. The DAC Register and the Selected Input Register Are Transparent. The Unselected Input Register Retains Its Previous Data Byte. Note Only One Byte Is Transparent at a Time, the Selected Byte Being Determined By the Logic Value of MLBYTE Prior to $\overline{WR}$ Being Pulsed Low.

BLOCK DIAGRAM



TIMING DIAGRAM



APPLICATIONS INFORMATION

Description

The LTC1599 is a 16-bit multiplying, current output DAC with a 2-byte (8-bit wide) digital interface. The device operates from a single 5V supply and provides both unipolar 0V to –10V or 0V to 10V and bipolar ±10V output ranges from a 10V or –10V reference input. It has three additional precision resistors on chip for bipolar operation. Refer to the Block Diagram regarding the following description.

The 16-bit DAC consists of a precision R-2R ladder for the 13LSBs. The 3MSBs are decoded into seven segments of resistor value R (48k typ). Each of these segments and the R-2R ladder carries an equally weighted current of one eighth of full scale. The feedback resistor R_{FB} and 4-quadrant resistor R_{OFS} have a value of R/4. 4-quadrant resistors R1 and R2 have a magnitude of R/4. R1 and R2 together with an external op amp (see Figure 4) inverts the reference input voltage and applies it to the 16-bit DAC input REF, in 4-quadrant operation. The REF pin presents a constant input impedance of R/8 in unipolar mode and R/12 in bipolar mode. The output impedance of the current output pin I_{OUT1} varies with DAC input code. The I_{OUT1} capacitance due to the NMOS current steering switches also varies with input code from 70pF to 115pF. I_{OUT2F} and I_{OUT2S} are normally tied to the system analog ground. An added feature of the LTC1599 is a proprietary deglitcher that reduces glitch impulse to 1.5nV-s over the DAC output voltage range.

Digital Section

The LTC1599 has a byte wide (8-bit), digital input data bus. The device is double-buffered with two 16-bit registers. The double-buffered feature permits the update of several DACs simultaneously. The input register is loaded directly from an 8-bit (or higher) microprocessor bus in a two step sequence. The MLBYTE pin selects whether the 8 input data bits are loaded into the LSB or the MSB byte of the input register. When MLBYTE is brought to a logic low level and $\overline{WR}$ is given a logic low going pulse, the 8 data bits are loaded into the LSB byte of the input register. Conversely, when MLBYTE is brought to a logic high level and $\overline{WR}$ is given a logic low going pulse, the 8 data bits are loaded into the MSB byte of the input register. If $\overline{WR}$ is brought to a logic low level, the existing level of MLBYTE determines which byte is loaded into the input register. If the logic level of MLBYTE is changed while $\overline{WR}$ remains low, no change will occur. This is because $\overline{WR}$ is an edge triggered signal and once it goes low it locks out any further changes in MLBYTE. $\overline{WR}$ must be brought high and then low again to accept the new MLBYTE condition. The second register (DAC register) is updated with the data from the input register when the $\overline{LD}$ pin is brought to a logic low level. Updating the DAC register updates the DAC output with the new data. The deglitcher is activated on the falling edge of the $\overline{LD}$ pin. The asynchronous clear pin resets the LTC1599 to zero scale when the CLVL pin is at a logic low level and to midscale when the CLVL pin is at a logic high level. $\overline{CLR}$ resets both the input and DAC registers. The device also has a power-on reset. Table 1 shows the truth table for the device.

Unipolar Mode
(2-Quadrant Multiplying, V_{OUT} = 0V to $-V_{REF}$)

The LTC1599 can be used with a single op amp to provide 2-quadrant multiplying operation as shown in Figure 1. With a fixed –10V reference, the circuit shown gives a precision unipolar 0V to 10V output swing.

Bipolar Mode
(4-Quadrant Multiplying, $V_{OUT} = -V_{REF}$ to V_{REF})

The LTC1599 contains on chip all the 4-quadrant resistors necessary for bipolar operation. 4-quadrant multiplying operation can be achieved with a minimum of external components, a capacitor and a dual op amp, as shown in Figure 3. With a fixed 10V reference, the circuit shown gives a precision bipolar –10V to 10V output swing.

Op Amp Selection

Because of the extremely high accuracy of the 16-bit LTC1599, careful thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Tables 2 and 3 contain equations for evaluating the effects of op amp parameters on the LTC1599's accuracy when

APPLICATIONS INFORMATION

configured in unipolar or bipolar modes of operation (Figures 1 and 3). These are the changes the op amp can cause to the INL, DNL, unipolar offset, unipolar gain error, bipolar zero and bipolar gain error. Table 4 contains a partial list of LTC precision op amps recommended for use with the LTC1599. The two sets of easy-to-use design equations simplify the selection of op amps to meet the system's specified error budget. Select the amplifier from Table 4 and insert the specified op amp parameters in either Table 2 or Table 3. Add up all the errors for each category to determine the effect the op amp has on the accuracy of the LTC1599. Arithmetic summation gives an (unlikely) worst-case effect. RMS summation produces a more realistic effect.

Op amp offset will contribute mostly to output offset and gain error and has minimal effect on INL and DNL. For the LTC1599, a 500μV op amp offset will cause about 0.55LSB INL degradation and 0.15LSB DNL degradation with a 10V full-scale range (20V range in bipolar). For the LTC1599 configured in the unipolar mode, the same 500μV op amp offset will cause a 3.3LSB zero-scale error and a 3.45LSB gain error with a 10V full-scale range.

While not directly addressed by the simple equations in Tables 2 and 3, temperature effects can be handled just as easily for unipolar and bipolar applications. First, consult an op amp's data sheet to find the worst-case V_{OS} and I_B over temperature. Then, plug these numbers in the V_{OS} and I_B equations from Table 2 or Table 3 and calculate the temperature induced effects.

For applications where fast settling time is important, Application Note 74, entitled "*Component and Measurement Advances Ensure 16-Bit DAC Settling Time*," offers a thorough discussion of 16-bit DAC settling time and op amp selection.

Table 2. Easy-to-Use Equations Determine Op Amp Effects on DAC Accuracy in Unipolar Applications

OP AMP	INL (LSB)	DNL (LSB)	UNIPOLAR OFFSET (LSB)	UNIPOLAR GAIN ERROR (LSB)
V_{OS} (mV)	$V_{OS} \bullet 1.2 \bullet (10V/V_{REF})$	$V_{OS} \bullet 0.3 \bullet (10V/V_{REF})$	$V_{OS} \bullet 6.6 \bullet (10V/V_{REF})$	$V_{OS} \bullet 6.9 \bullet (10V/V_{REF})$
I_B (nA)	$I_B \bullet 0.00055 \bullet (10V/V_{REF})$	$I_B \bullet 0.00015 \bullet (10V/V_{REF})$	$I_B \bullet 0.065 \bullet (10V/V_{REF})$	0
A_{VOL} (V/V)	$10k/A_{VOL}$	$3k/A_{VOL}$	0	$131k/A_{VOL}$

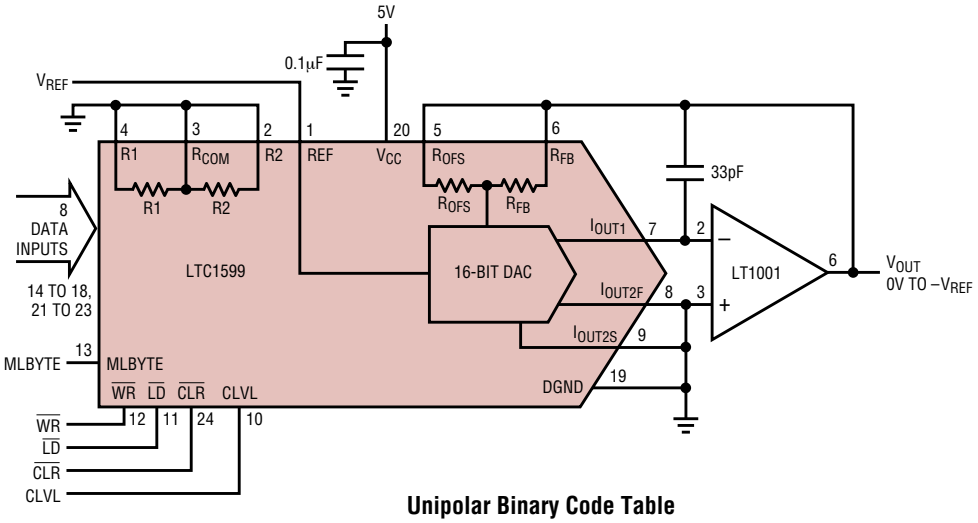
Table 3. Easy-to-Use Equations Determine Op Amp Effects on DAC Accuracy in Bipolar Applications

OP AMP	INL (LSB)	DNL (LSB)	BIPOLAR ZERO ERROR (LSB)	BIPOLAR GAIN ERROR (LSB)
V_{OS1} (mV)	$V_{OS1} \bullet 1.2 \bullet (10V/V_{REF})$	$V_{OS1} \bullet 0.3 \bullet (10V/V_{REF})$	$V_{OS1} \bullet 9.9 \bullet (10V/V_{REF})$	$V_{OS1} \bullet 6.9 \bullet (10V/V_{REF})$
I_{B1} (nA)	$I_{B1} \bullet 0.00055 \bullet (10V/V_{REF})$	$I_{B1} \bullet 0.00015 \bullet (10V/V_{REF})$	$I_{B1} \bullet 0.065 \bullet (10V/V_{REF})$	0
A_{VOL1}	$10k/A_{VOL}$	$3k/A_{VOL1}$	0	$196k/A_{VOL1}$
V_{OS2} (mV)	0	0	$V_{OS2} \bullet 6.7 \bullet (10V/V_{REF})$	$V_{OS2} \bullet 13.2 \bullet (10V/V_{REF})$
I_{B2} (nA)	0	0	$I_{B2} \bullet 0.065 \bullet (10V/V_{REF})$	$I_{B2} \bullet 0.13 \bullet (10V/V_{REF})$
A_{VOL2}	0	0	$65k/A_{VOL2}$	$131k/A_{VOL2}$

Table 4. Partial List of LTC Precision Amplifiers Recommended for Use with the LTC1599, with Relevant Specifications

	Amplifier Specifications								
AMPLIFIER	V_{OS} μV	I_B nA	A_{OL} V/mV	VOLTAGE NOISE nV/√Hz	CURRENT NOISE pA/√Hz	SLEW RATE V/μs	GAIN BANDWIDTH PRODUCT MHz	$t_{SETTLING}$ with LTC1599 μs	POWER DISSIPATION mW
LT1001	25	2	800	10	0.12	0.25	0.8	120	46
LT1097	50	0.35	1000	14	0.008	0.2	0.7	120	11
LT1112 (Dual)	60	0.25	1500	14	0.008	0.16	0.75	115	10.5/Op Amp
LT1124 (Dual)	70	20	4000	2.7	0.3	4.5	12.5	19	69/Op Amp
LT1468	75	10	5000	5	0.6	22	90	2.5	117

APPLICATIONS INFORMATION

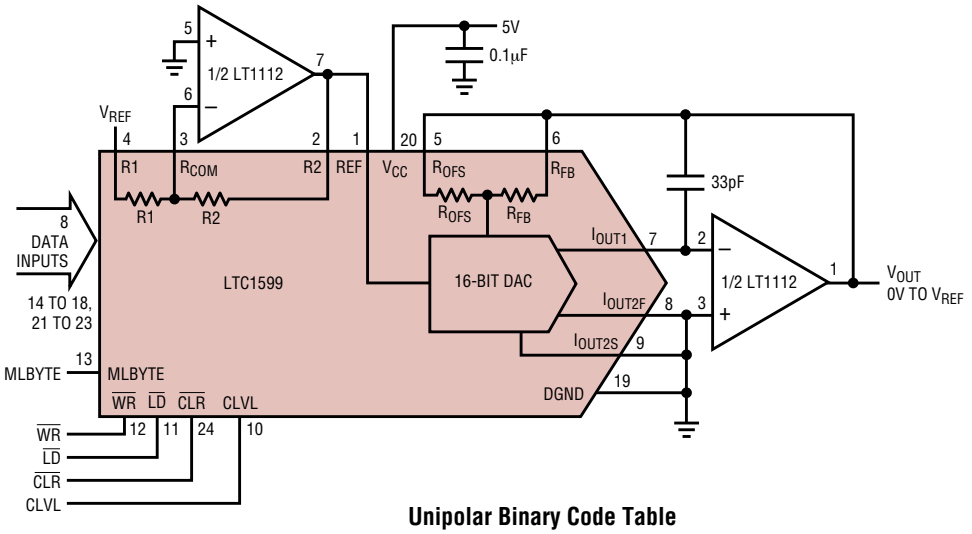


Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB			LSB	
1111	1111	1111	1111	$-V_{REF}$ (65,535/65,536)
1000	0000	0000	0000	$-V_{REF}$ (32,768/65,536) = $-V_{REF}/2$
0000	0000	0000	0001	$-V_{REF}$ (1/65,536)
0000	0000	0000	0000	0V

1599 F01

Figure 1. Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to $-V_{REF}$



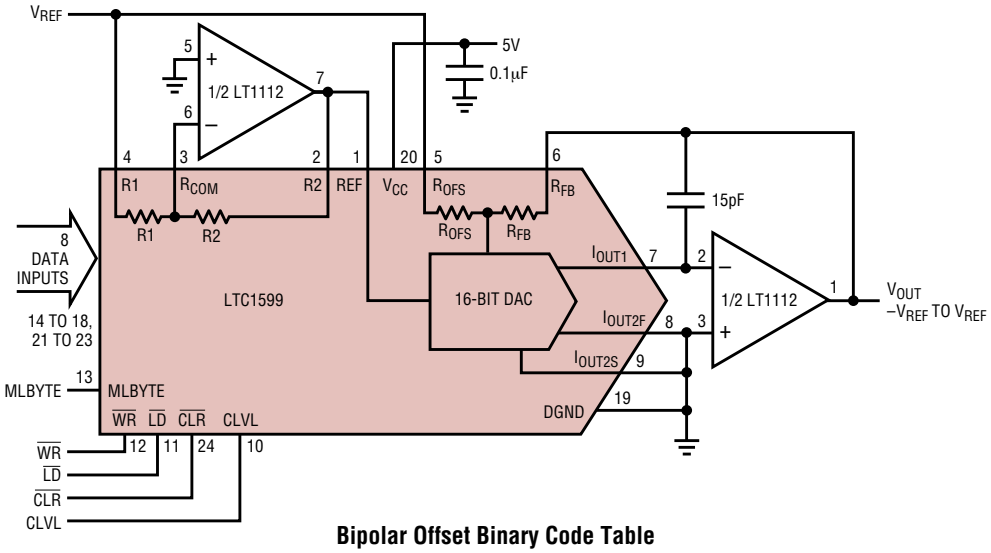
Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB			LSB	
1111	1111	1111	1111	V_{REF} (65,535/65,536)
1000	0000	0000	0000	V_{REF} (32,768/65,536) = $V_{REF}/2$
0000	0000	0000	0001	V_{REF} (1/65,536)
0000	0000	0000	0000	0V

1599 F02

Figure 2. Noninverting Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to V_{REF}

APPLICATIONS INFORMATION



Bipolar Offset Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB			LSB	
1111	1111	1111	1111	V_{REF} (32,767/32,768)
1000	0000	0000	0001	V_{REF} (1/32,768)
1000	0000	0000	0000	0V
0111	1111	1111	1111	$-V_{REF}$ (1/32,768)
0000	0000	0000	0000	$-V_{REF}$

1599 F03

Figure 3. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}

Precision Voltage Reference Considerations

Much in the same way selecting an operational amplifier for use with the LTC1599 is critical to the performance of the system, selecting a precision voltage reference also requires due diligence. As shown in the section describing the basic operation of the LTC1599, the output voltage of the DAC circuit is directly affected by the voltage reference; thus, any voltage reference error will appear as a DAC output voltage error.

There are three primary error sources to consider when selecting a precision voltage reference for 16-bit applications: output voltage initial tolerance, output voltage temperature coefficient and output voltage noise.

Initial reference output voltage tolerance, if uncorrected, generates a full-scale error term. Choosing a reference with low output voltage initial tolerance, like the LT1236 (±0.05%), minimizes the gain error caused by the reference; however, a calibration sequence that corrects for system zero- and full-scale error is always recommended.

A reference's output voltage temperature coefficient affects not only the full-scale error, but can also affect the circuit's INL and DNL performance. If a reference is chosen with a loose output voltage temperature coefficient, then the DAC output voltage along its transfer characteristic will be very dependent on ambient conditions. Minimizing the error due to reference temperature coefficient can be achieved by choosing a precision reference with a low output voltage temperature coefficient and/or tightly controlling the ambient temperature of the circuit to minimize temperature gradients.

As precision DAC applications move to 16-bit and higher performance, reference output voltage noise may contribute a dominant share of the system's noise floor. This in turn can degrade system dynamic range and signal-to-noise ratio. Care should be exercised in selecting a voltage reference with as low an output noise voltage as practical for the system resolution desired. Precision voltage references, like the LT1236, produce low output noise in the 0.1Hz to 10Hz region, well below the 16-bit LSB level in 5V

APPLICATIONS INFORMATION

or 10V full-scale systems. However, as the circuit bandwidths increase, filtering the output of the reference may be required to minimize output noise.

Table 5. Partial List of LTC Precision References Recommended for Use with the LTC1599, with Relevant Specifications

REFERENCE	INITIAL TOLERANCE	TEMPERATURE DRIFT	0.1Hz to 10Hz NOISE
LT1019A-5, LT1019A-10	±0.05%	5ppm	$12\mu V_{P-P}$
LT1236A-5, LT1236A-10	±0.05%	5ppm	$3\mu V_{P-P}$
LT1460A-5, LT1460A-10	±0.075%	10ppm	$20\mu V_{P-P}$

Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding should be used. I_{OUT2F} and I_{OUT2S} must be tied to the star ground with as low a resistance as possible. When it is not possible to locate star ground close to I_{OUT2F} and I_{OUT2S}, separate traces should be used to route these pins to star ground. This minimizes the voltage drop from these pins to ground caused by the code dependent current flowing to ground. When the resistance of these circuit board traces becomes greater than 1Ω, the circuit in Figure 4 eliminates voltage drop errors caused by high resistance traces. This preserves the excellent accuracy (1LSB INL and DNL) of the LTC1599.

A 16-Bit, 4mA to 20mA Current Loop Controller for Industrial Applications

Modern process control systems must often deal with legacy 4mA to 20mA analog current loops as a means of interfacing with actuators and valves located at a distance. The circuit in Figure 5 provides an output to a current loop controlled by an LTC1599, a 16-bit current output DAC. A dual rail-to-rail op amp (U1, LT1366) controls a P-channel power FET (Q2) to produce a current mirror with a precise 8:1 ratio as defined by a resistor array. The input current to this mirror circuit is produced by a grounded base cascode stage using a high gain transistor (Q1). The use of a bipolar transistor in this location results in an error term associated with U1B and Q1's base current (–0.2% for the device shown). For control applications however, absolute accuracy of the output to an actuator is usually not required. If a higher degree of absolute accuracy is required, Q1 can be replaced with an N-channel JFET; however, this requires a single amplifier at U1B with the ability to drive the gate below ground. An enhancement mode N-channel FET can be used in place of Q1 but MOSFET leakage current must be considered and gate overdrive must be avoided.

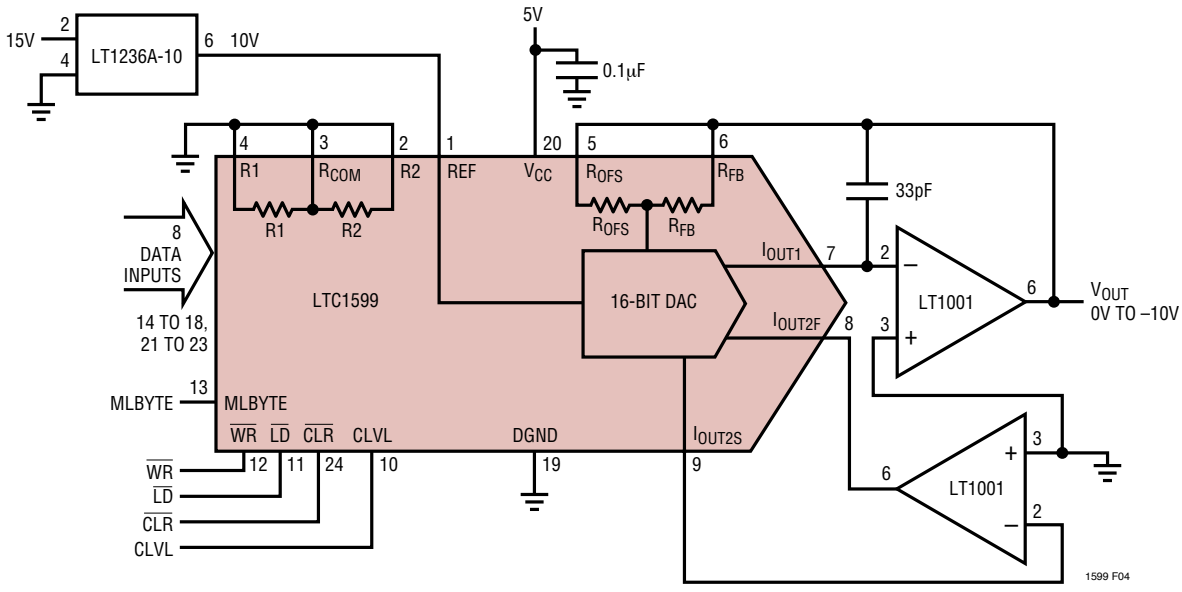


Figure 4. Driving I_{OUT2F} and I_{OUT2S} with a Force/Sense Amplifier

APPLICATIONS INFORMATION

The output current of the DAC is converted to a voltage via U3 (LT1112), producing 0V to –2.5V at Pin 1 of U3. The resulting current in Q1 is determined by two elements of resistor array, R_{N1} (3mA max). The emitter of Q1 is maintained at 0V by the action of U1B.

In applications that do not require 16-bit resolution and accuracy, the LTC1599 can be replaced by the 14-bit parallel LTC1591. Furthermore, the resistor array can be substituted with discrete resistors, and Q2 could be replaced by a high gain bipolar PNP; for example, an FZT600 from Zetex.

No trim is provided a shown, as it is expected that software control is preferable. The output range of 4mA to 20mA is defined by software, as the full output range is nominally 0mA to 24mA.

U1 is a rail-to-rail amplifier that can operate on suppy voltages up to 36V. This defines the maximum voltage on the loop power. If higher loop voltages are required, a separate low power amplifier at U1A, powered by a zener regulated supply and referenced to loop power, would allow voltages up to the breakdown voltages of Q1 and Q2.

In the example shown, the use of a dual op amp requires a zener clamp to protect the gate of the MOS power transistor. If a separate shunt-regulated supply is provided for the amplifier replacing U1A, the gate clamp (Z1) is not required.

As shown, this topology uses the LTC1599's internal divider (R1 and R2) to reduce the reference from 5V to 2.5V. If a 2.5V reference is used, it can be connected directly to REF (Pin 1). Alternatively, if the op amp is powered such that it has –10V output capability, the divider and amplifier prior to the REF input are not required and R_{OFS} can be used for other purposes such as offset trim. The two R_{N1} resistors at the emitter of Q1 must be changed in this case.

Note that the output of the current transmitter shows a network that is intended to provide a first line of defense against ESD and prevent oscillation (1000pF and 10Ω) that could otherwise occur in the power MOSFET if lead inductance were more than a few inches. C1 should be as close as possible to Q2. Using MOSFETs that have higher threshold voltages may require changing Z1 in order to allow full current output.

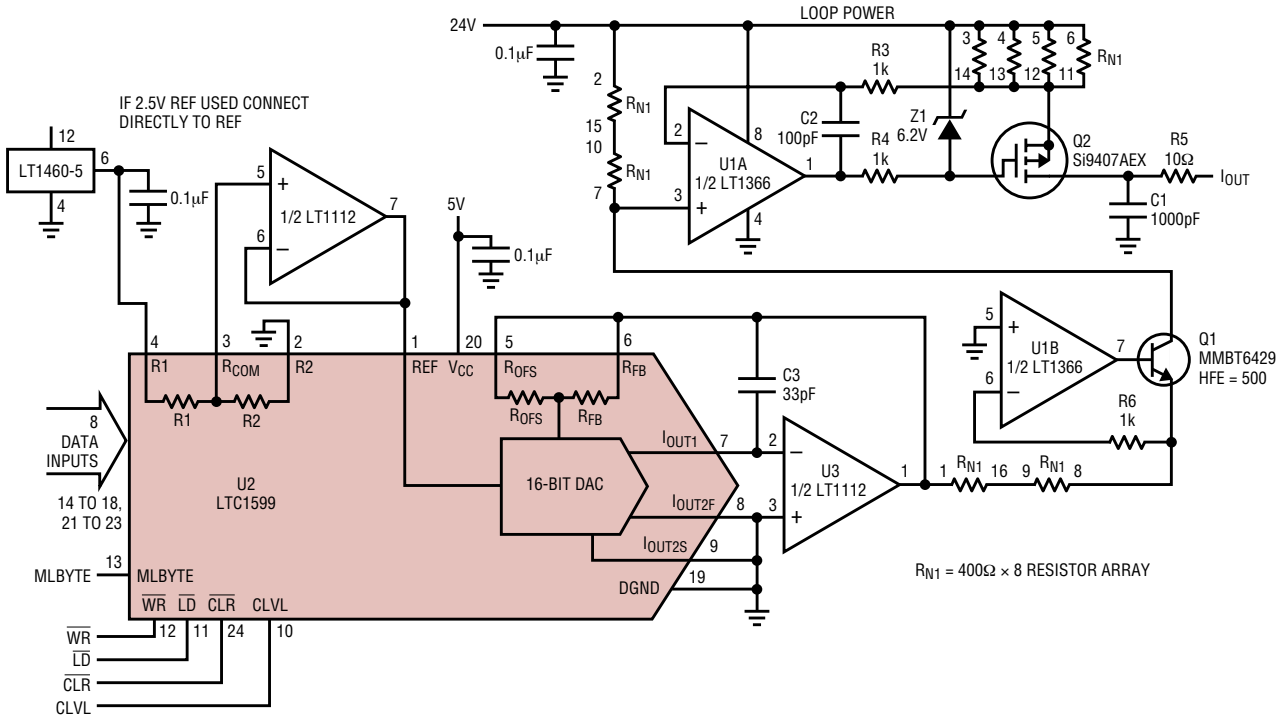


Figure 5. 16-Bit Current Loop Controller for Industrial Applications

APPLICATIONS INFORMATION

A 16-Bit General Purpose Analog Output Circuit

Industrial applications often use analog signals of 0V to 5V, 0V to 10V, ±5V or ±10V. The topology in Figure 6 uses an LTC1599 to produce a universal analog output, capable of operation over all these ranges, with only software configuration. High precision analog switches are used to provide uncompromising stability in all ranges and matched resistors internal to the LTC1599 are used, as well as a configuration that minimizes the effects of channel resistance in the switches. Note that in all cases the analog switches have minimal current flowing through them. The use of unbuffered analog switches in series with the feedback/divider resistors would result in an error because of temperature coefficient mismatch between the internal DAC resistors and the switch channel resistances, as well as the channel resistance variation over the signal range. Quad analog switch U3 (DG212B) allows configuration of feedback terms and selection of the reference voltage. Switch C allows the buffered reference voltage to be injected into the summing node via Pin 5 (R_{OFS}) for bipolar outputs. When active, switch D places R_{OFS} in parallel with R_{FB}, producing an output at full scale voltage equal to the voltage at the REF pin of the LTC1599.

The other switches in U3 (A and B) are used to select the 10V reference produced by the LT1019, or 5V produced by the R3 and R4 divider.

An inexpensive precision divider can be implemented using an 8-element resistor array, paralleling four resistors for R3 and four resistors for R4. Symmetry in the interconnection of these resistors will ensure compensation for temperature gradient across the resistor array. An alternative to a resistor divider is the LTC1043 switched capacitor building block. It can be configured as a high precision divide-by-2. Please consult the LTC1043 data sheet for more information.

The NOR gate (U4) ensures that switches C and D are not enabled simultaneously. This eliminates contention between the reference buffer and the output amplifier.

This topology can be modified to accept a high current buffer following the LT1112, if higher output current levels are required or difficult loads need be driven. Adjustment of C_{FB}'s value may be required for the buffer amplifier chosen.

Note that the analog switches must handle the full output swing in this configuration, but there is a variety of suitable switches on the market including the LTC201. The DG212B as shown is a newer generation part with lower leakage, providing a performance advantage.

The DG333A, a quad single-pole, double-throw switch, could be used for a 2-channel version similar to this circuit. Alternatively, a single channel can be created with the additional switches used as switched capacitor divide-by-2, as shown on the LTC1043 data sheet. In choosing analog switches, keep in mind the logic levels and the signal levels required.

Table 1. Configuration Settings for the Various Output Ranges

V_{OUT} MODE	REFSEL	BIPOLAR/$\overline{\text{UNIPOLAR}}$	GAIN
0V to 5V	1	0	0
0V to 10V	1	0	1
–5V to 5V	1	1	1
–10V to 10V	0	1	1

APPLICATIONS INFORMATION

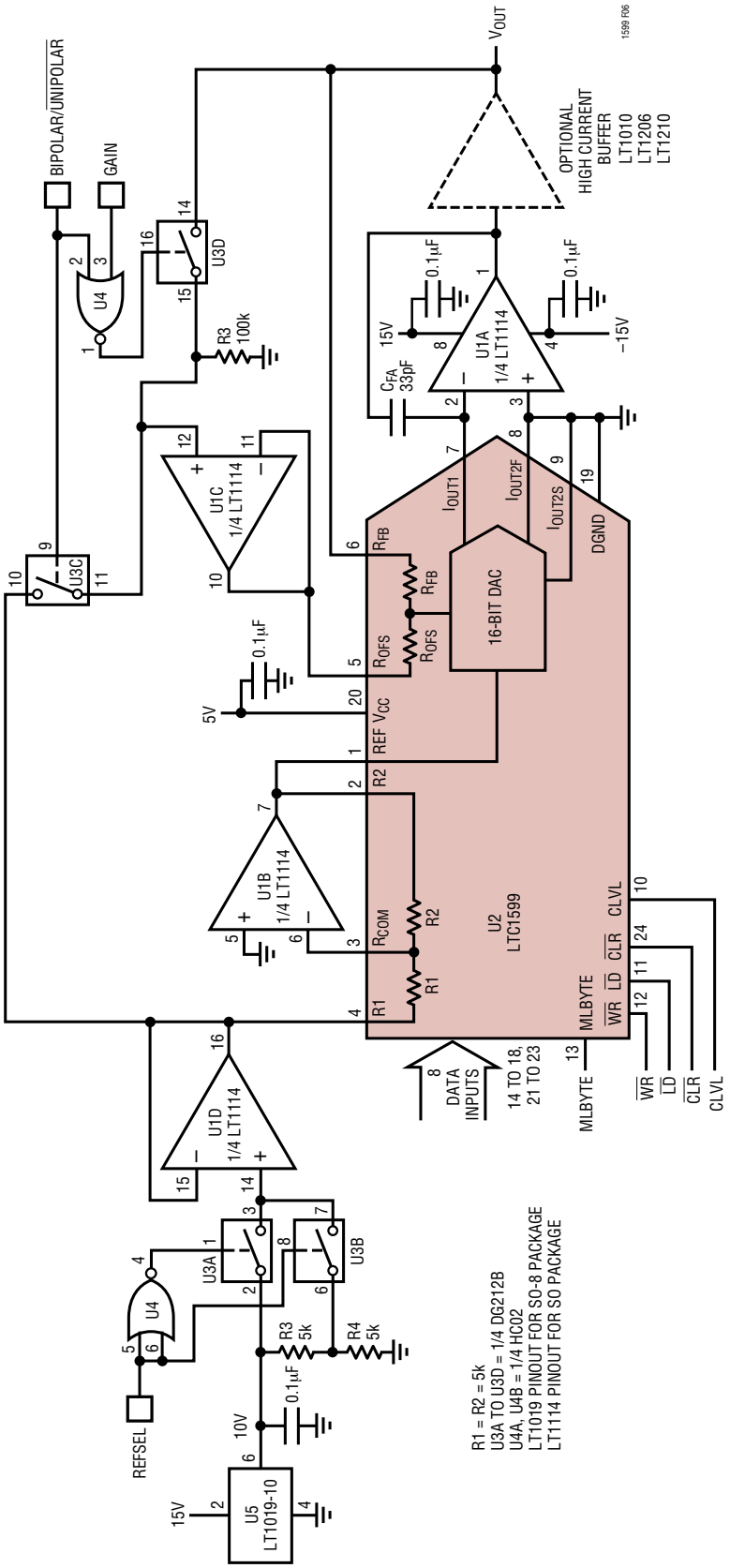


Figure 6. 16-Bit General Purpose Analog Output Circuit

APPLICATIONS INFORMATION

Interfacing to the 68HC11

The circuit in Figure 7 is an example of using the 68HC11 to control the LTC1599. Data is sent to the DAC using two 8-bit parallel transfers from the controller's Port B. The $\overline{WR}$ signal is generated by manipulating the logic output on Port A's bit 3, the MLBYTE command is sent to the DAC using Port A's bit 4, and the $\overline{LD}$ command comes from the $\overline{SS}$ output on Port D's bit 5.

The sample listing 68HC11 assembly code in Listing A is designed to emulate the Timing Diagram found earlier in this data sheet. After variable declaration, the main portion of the program retrieves the least significant byte from memory, forces MLBYTE and $\overline{WR}$ to a logic low, and then writes the low byte data to Port B. It then sets $\overline{WR}$ and

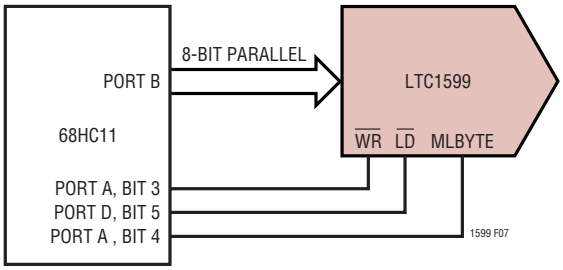


Figure 7. Using the 68HC11 to Control the LTC1599

MLBYTE high. Next, the most significant byte is copied from memory and $\overline{WR}$ is again asserted low. The high byte is written to Port B and $\overline{WR}$ is returned high. The transfer of the 16 bits is completed by cycling the $\overline{LD}$ input low and then high using the $\overline{SS}$ output on Port D.

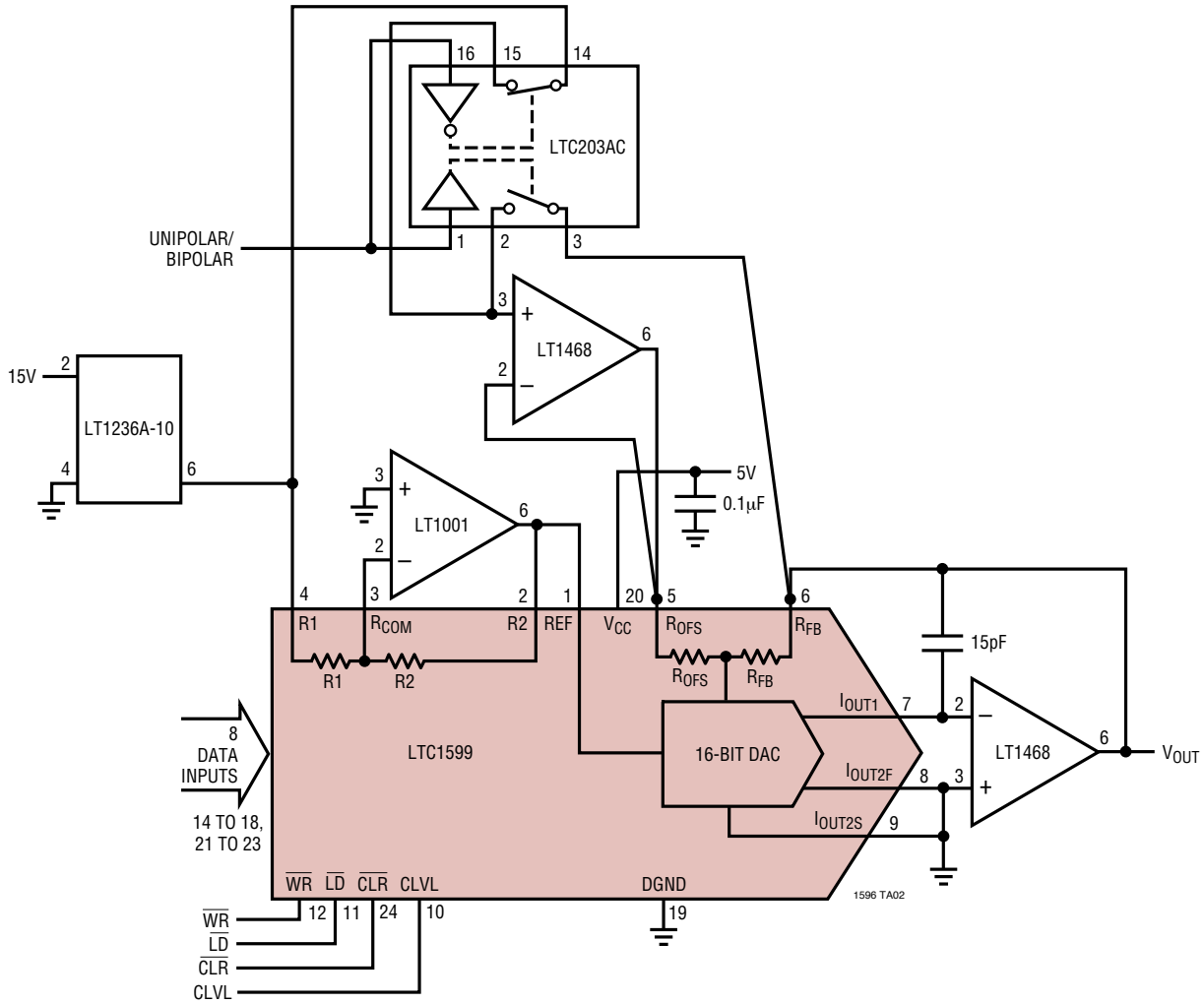
```
*****************************************************************
*                                                               *
* This example program uses 8-bit parallel port B, port A and port D  *
* to transfer 16-bit parallel data to the LTC1599 16-bit current output  *
* DAC. Port B at $1004 is used for two eight bit transfers. Port A,  *
* bit 3 is used for the LTC1599's WR command and bit 4 is used for the  *
* MLBYTE command. Port D' SS output is used for the LTC1599's LD  *
* command                                                       *
*                                                               *
*****************************************************************
*
*****************************************
* 68HC11 register definitions           *
*****************************************
*
* PIOC    EQU     $1002     Parallel I/O control register
*                           "STAF,STAI,CWOM,HNDS, OIN, PLS, EGA,INVB"
PORTA   EQU     $1000     Port A data register
*                           "Bit7,Bit6,Bit5,Bit4,Bit3,Bit2,Bit1,Bit0"
PORTB   EQU     $1004     Port B data register
*                           "Bit7,Bit6,Bit5,Bit4,Bit3,Bit2,Bit1,Bit0"
PORTD   EQU     $1008     Port D data register
*                           " -  , -  , SS* ,CSK ;MOSI,MISO,TxD ,RxD "
DDRD    EQU     $1009     Port D data direction register
SPCR    EQU     $1028     SPI control register
MBYTE   EQU     $00       This memory location holds the LTC1599's bits 15 - 08
LBYTE   EQU     $01       This memory location holds the LTC1599's bits 07 - 00
*
*****************************************
* Start OUTDATA Routine                 *
*****************************************
*
        ORG     $C000     Program start location
INIT1   LDAA    #$2F      -,-,1,0;1,1,1,1
*                         -, -, SS*-Hi, SCK-Lo, MOSI-Hi, MISO-Hi, X, X
        STAA    PORTD     Keeps SS* a logic high when DDRD, Bit5 is set
        LDAA    #$38      -,-,1,1;1,0,0,0
        STAA    DDRD      SS* , SCK, MOSI are configured as Outputs
*                         MISO, TxD, RxD  are configured as Inputs
* DDRD's Bit5 is a 1 so that port D's SS* pin is a general output
```

APPLICATIONS INFORMATION

```
GETDATA PSHX
        PSHY
        PSHA
        LDY     #$1000    Setup index
*
*****************************************
* Retrieve DAC data from memory and     *
* send it to the LTC1599                *
*****************************************
*
        LDAA    LBYTE                   Retrieve the least significant byte from memory
        BCLR    PORTA,Y %00010000       This sets PORTA, Bit4 output to a logic
*                                       low, forcing MLBYTE input to a logic low
        BCLR    PORTA,Y %00001000       This forces a low on the LTC1599's WR pin
        STAA    PORTB                   Transfer the least significant byte to the DAC
        BSET    PORTA,Y %00001000       This forces a high on the LTC1599's WR pin
        BSET    PORTA,Y %00010000       This sets PORTA, Bit4 output to a logic
*                                       high, forcing MLBYTE to a logic high
        LDAA    MBYTE                   Retrieve the most significant byte from memory
        BCLR    PORTA,Y %00001000       This forces a low on the LTC1599's WR pin
        STAA    PORTB                   Transfer the most significant byte to the DAC
        BSET    PORTA,Y %00001000       This forces a high on the LTC1599's WR pin
*
*****************************************
* The next two instructions exercise    *
* the LD input, latching the data       *
* that was just loaded                  *
*****************************************
*
        BCLR    PORTD,Y %00100000       LD goes low
        BSET    PORTD,Y %00100000       and returns high
*
*****************************************
* Data transfer routine completed       *
*****************************************
*
        PULA            Restore the A register
        PULY            Restore the Y register
        PULX            Restore the X register
        RTS
```

TYPICAL APPLICATION

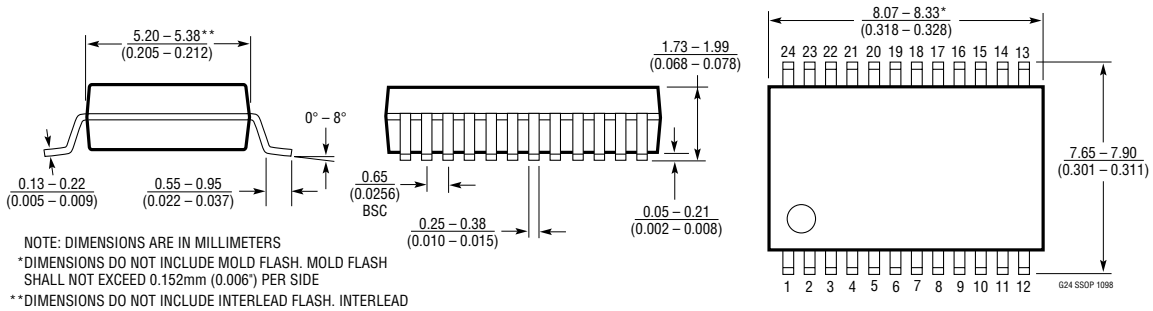
16-Bit V_{OUT} DAC Programmable Unipolar/Bipolar Configuration



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

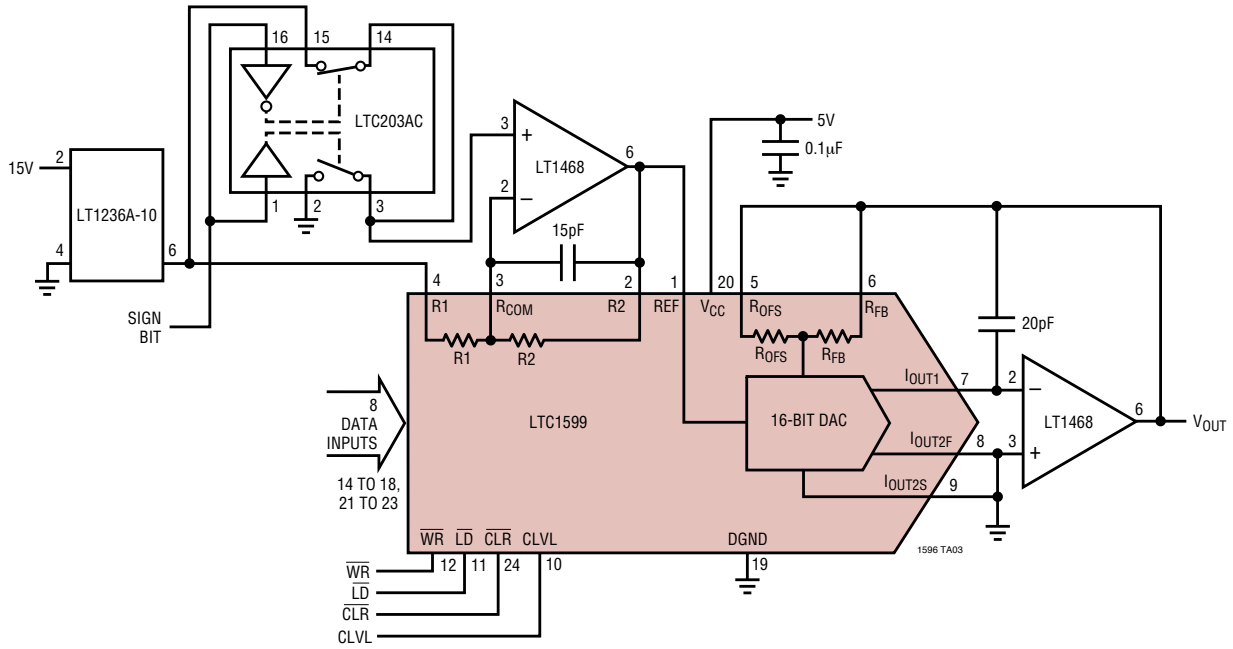
G Package
24-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



NOTE: DIMENSIONS ARE IN MILLIMETERS
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

TYPICAL APPLICATION

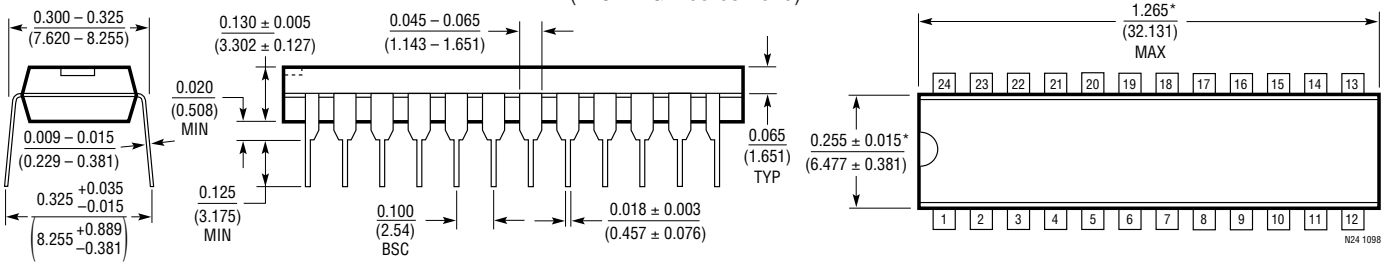
17-Bit Sign Magnitude DAC with Bipolar Zero Error of 140μV (0.92LSB at 17 Bits) at 25°C



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
24-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1236	Precision Reference	0.05% Initial Accuracy, 5ppm Temperature Drift
LT1468	16-Bit Accurate Op Amp	90MHz Gain Bandwidth, 22V/μs Slew Rate
LTC1591/LTC1597	Parallel 14/16-Bit Current Output DACs	On-Chip 4-Quadrant Resistors
LTC1595/LTC1596	Serial 16-Bit Current Output DACs	Low Glitch, ±1LSB Maximum INL, DNL
LTC1650	16-Bit Voltage Output DAC	Low Power, Deglitched, 4-Quadrant Multiplying V_{OUT} DAC, ±4.5V Output Swing
LTC1657	16-Bit Parallel Voltage Output DAC	Low Power, 16-Bit Monotonic Over Temperature, Multiplying Capability
LTC1658	14-Bit Rail-to-Rail Micropower DAC	Low Power Multiplying V_{OUT} DAC in MSOP. Output Swings from GND to REF.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com

1599f LT/TP 1199 4K • PRINTED IN USA