SMBus VID Voltage Programmers

FEATURES

- **Fully Compliant with Intel 5-Bit Mobile (LTC1699-80) and Desktop VRM8.4 (LTC1699-81) and VRM9.0 (LTC1699-82) VID Specifications**
- **Precision ±0.35% Programmable Resistor Divider for Use with 0.8V Referenced DC/DC Converters**
- Two Different Divider Settings Can Be Stored Using a 2-Wire SMBus Serial Interface (Rev 1.1)
- Built-In Safeguards Minimize Misprogramming Due to Bus Conflicts
- Three Open-Drain Pins (CPU_ON, IO_ON, CLK_ON) and a Global Control Pin (VRON)to Shutdown or Soft-Start 3 DC/DC Converters Simultaneously
- PGOOD Pin and 50µs PGOOD Timer
- Available in MSOP-8 and SSOP-16 Package

APPLICATIONS

- Intel Desktop Pentium® III Power Supply
- Intel Mobile Pentium® Power Supply with Intel SpeedStep™ Technology
- Desktop AMD Athlon™ Power Supply
- Software Programmable Remote Power Supply
- Power Supplies with Voltage Margining

DESCRIPTION

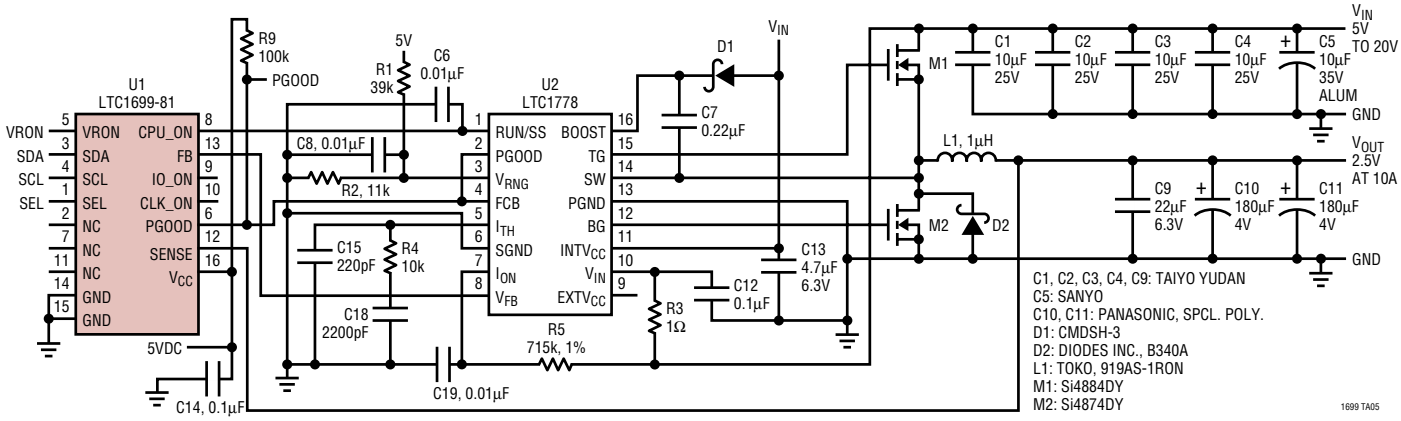
The LTC®1699-80, LTC1699-81 and LTC1699-82 are precision (±0.35% max), digitally programmed resistor dividers that comply with Intel 5-bit mobile (LTC1699-80), desktop VRM8.4 (LTC1699-81) and VRM9.0 (LTC1699-82) VID specifications. Each IC can switch the output of a DC/DC converter between two set voltages. A digital input pin, SEL, selects one of two divider settings stored into registers via a 2-wire SMBus interface.

The SMBus interface uses Write Word protocol to setup the registers and to turn the DC/DC converters on or off. Read Word protocol is used to verify register contents and to return the On/Off status of the converters. The LTC1699-80, LTC1699-81 and LTC1699-82 incorporate safeguards against errors due to bus conflicts.

Three open-drain N-channel outputs (CPU_ON, IO_ON and CLK_ON) are provided to turn DC/DC converter supplies on or off via their RUN/SS inputs. A global control pin, VRON is used to turn the converters on or off simultaneously. An internal timer pulls the PGOOD pin low for 50µs if the divider setting changes or the converters are turned on via the SMBus and the VRON pin.

TYPICAL APPLICATION

SMBus Controlled High Efficiency DC/DC Converter



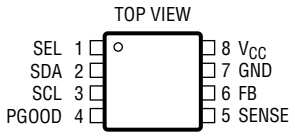
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 7V
All Pins ..... –0.3V to 7V
Operating Temperature
Range (Note 2) ..... $-40°C \le T_A \le 85°C$
Junction Temperature ..... 125°C

Storage Temperature ..... $-65°C \le T_A \le 150°C$
Lead Temperature (Soldering, 10 sec) ..... 300°C

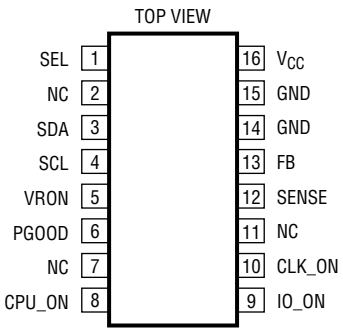
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LTC1699EMS8-80 LTC1699EMS8-81 LTC1699EMS8-82
MS8 PART MARKING
LTPV LTPW LTTB



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1699EGN-80 LTC1699EGN-81 LTC1699EGN-82
GN PART MARKING
169980 169981 169982

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 2.7V ≤ V_{CC} ≤ 5.5V (Notes 3, 4) unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Operating Supply Voltage Range			2.7		5.5	V
I_{CC}	Supply Current	CPU_ON, IO_ON, CLK_ON, PGOOD Pins Are Open	●			350	µA
$R_{FB-SENSE}$	Resistance between SENSE and FB	LTC1699-80, LTC1699-82	●	7	10	13	kΩ
		LTC1699-81	●	14	20	26	kΩ
DE	Divider Error	All Divider Settings	●	–0.35		0.35	%
V_{IH}	SCL, SDA Input High Voltage		●	2.1			V
V_{IL}	SCL, SDA Input Low Voltage		●			0.8	V
V_{IH}	SEL, VRON Input High Voltage				1.3	2.0	V
V_{IL}	SEL, VRON Input Low Voltage		●	0.8	1.3		V
V_{HYST}	SEL, VRON Hysteresis				±50		mV
V_{OL}	SDA, CPU_ON, IO_ON, CLK_ON Output Low Voltage	I = 3mA	●			0.4	V
I_{IN}	SCL, SDA, SEL, VRON Input Current	SDA Not Acknowledging, $0 \le V_{PIN} \le 5.5V$, V_{PIN} = 5.5V for VRON only	●			±10	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 2.7V ≤ V_{CC} ≤ 5.5V (Notes 3, 4) unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SK1}	SDA, PGOOD, CPU_ON, IO_ON, CLK_ON Sink Current at V_{CC} = 2.7V	0 ≤ V_{PIN} ≤ 2.7V	●	5	19	60	mA
I_{SK2}	SDA, PGOOD, CPU_ON, IO_ON, CLK_ON Sink Current at V_{CC} = 5.5V	0 ≤ V_{PIN} ≤ 5.5V	●	35	65	150	mA
I_{LKG}	PGOOD, CPU_ON, IO_ON, CLK_ON Leakage Current	0 ≤ V_{PIN} ≤ 5.5V	●			±2	µA
I_{PU}	VRON Pull-Up Current	V_{PIN} = 0	●	–1	–2.5	–7	µA
Timing (Note 5)							
f_{SMB}	SMBus Operating Frequency		●	10		100	KHz
t_{BUF}	Bus Free Time Between Stop/Start		●	4.7			µs
$t_{HD:STA}$	Hold Time After (Repeated) Start		●	4.0			µs
$t_{SU:STA}$	Repeated Start Setup Time		●	4.7			µs
$t_{SU:STO}$	Stop Condition Setup Time		●	4.0			µs
$t_{HD:DAT}$	Data Hold Time		●	300			ns
$t_{SU:DAT}$	Data Setup Time		●	250			ns
t_{LOW}	Clock Low Period		●	4.7			µs
t_{HIGH}	Clock High Period		●	4.0			µs
t_f	SCL, SDA Fall Time	0.9V_{CC} to 0.65V	●			300	ns
t_r	SCL, SDA Rise Time	0.65V to 2.25V	●			1000	ns
t_{SSH}	SEL to SENSE High (Note 6)	Toggle SEL to Switch from Min V_{OUT} to Max V_{OUT}, VFB = 0.8V			500		ns
t_{SSL}	SEL to SENSE Low (Note 6)	Toggle SEL to Switch from Max V_{OUT} to Min V_{OUT}, VFB = 0.8V			500		ns
t_{SPL}	SEL Toggling to PGOOD Low	Toggle SEL to Select New Code C_L = 100pF, 10kΩ Pull-Up, S2 in Figure 1	●		160	500	ns
t_{PH}	Stop Bit to CPU_ON, IO_ON or CLK_ON High (Note 7)	C_L = 100pF, 10kΩ Pull-Up, S2 in Figure 1	●			2	µs
t_{PL}	Stop Bit to CPU_ON, IO_ON or CLK_ON Low (Note 7)	C_L = 0.1µF, 10kΩ Pull-Up, S1 in Figure 1	●		20	50	µs
t_{PPL}	Stop Bit to PGOOD Low (Note 6)	C_L = 100pF, 10kΩ Pull-Up, S2 in Figure 1	●			250	ns
t_{VH}	VRON High to CPU_ON, IO_ON or CLK_ON High	C_L = 100pF, 10kΩ Pull-Up, S2 in Figure 1	●			2	µs
t_{VL}	VRON Low to CPU_ON, IO_ON, CLK_ON Low	C_L = 0.1µF, 10kΩ Pull-Up, S1 in Figure 1	●			50	µs
t_{VPL}	VRON Low to PGOOD Low	C_L = 100pF, 10kΩ Pull-Up, S2 in Figure 1	●		130	500	ns
t_{PGL}	PGOOD Low Duration	C_L = 100pF, 10kΩ Pull-Up, S2 in Figure 1	●	30	50	70	µs

Note1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1699-80E, LTC1699-81E and LTC1699-82E are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 4: All typical numbers are given for V_{CC} = 5V and T_A = 25°C.

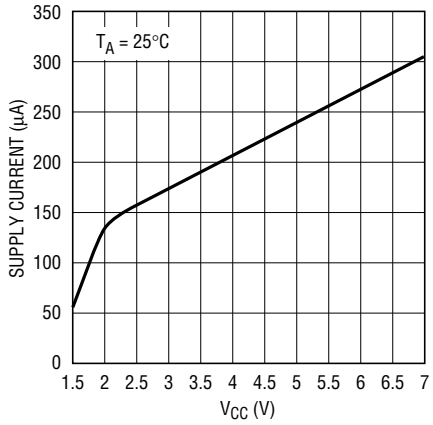
Note 5: These parameters are guaranteed by design and are not tested in production. SMBus timing is referenced to V_{IL} and V_{IH} levels.

Note 6: Dominated by the switching regulator. The delay due to the LTC1699-80, LTC1699-81 or LTC1699-82 is typically 500ns.

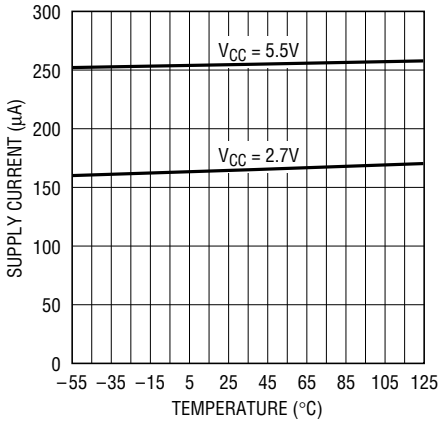
Note 7: Measured from the rising edge of SDA during Data High acknowledgement.

TYPICAL PERFORMANCE CHARACTERISTICS

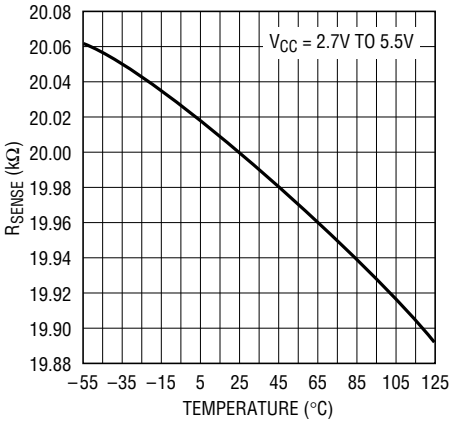
Supply Current vs Supply Voltage



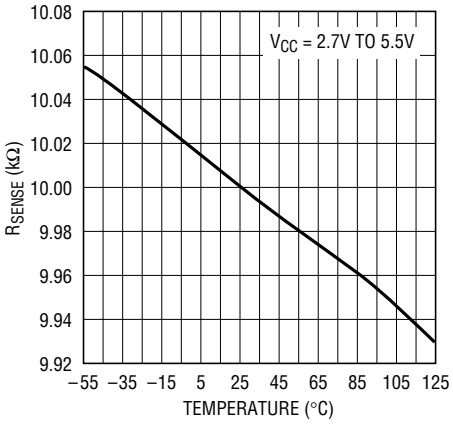
Supply Current vs Temperature



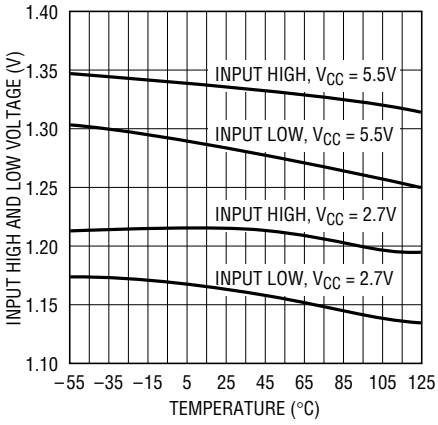
Resistance Between SENSE and FB Pins vs Temperature (LTC1699-81)



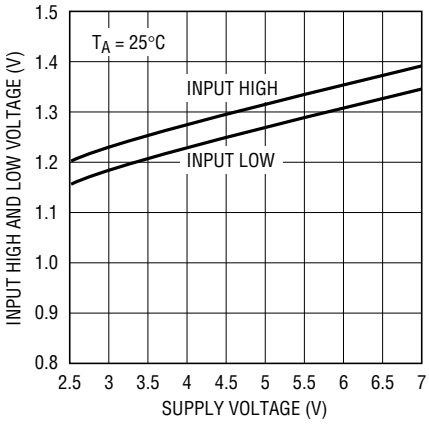
Resistance Between SENSE and FB Pins vs Temperature (LTC1699-80, LTC1699-82)



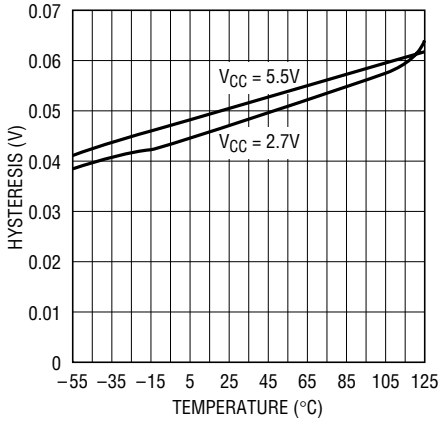
SCL, SDA, SEL and VRON Input High and Low Voltage vs Temperature



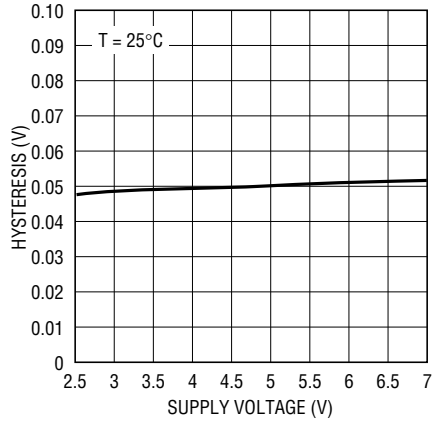
SCL, SDA, SEL and VRON Input High and Low Voltage vs Supply Voltage



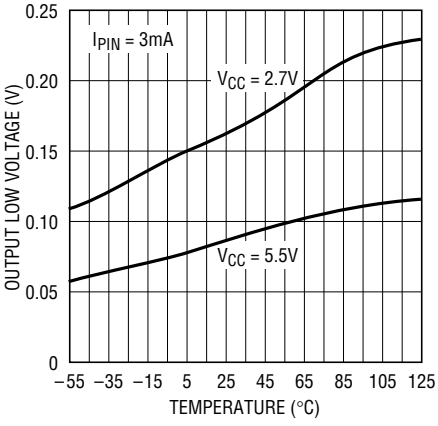
SCL, SDA, SEL and VRON Hysteresis vs Temperature



SCL, SDA, SEL and VRON Hysteresis vs Supply Voltage

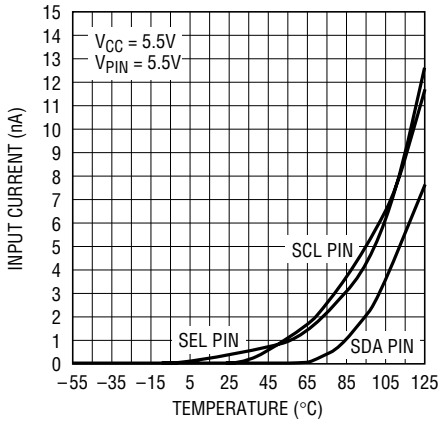


SDA, CPU_ON, IO_ON, CLK_ON Output Low Voltage vs Temperature

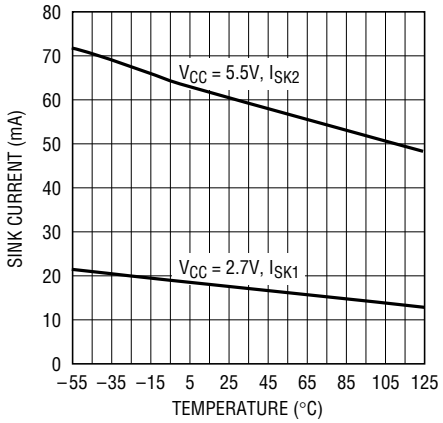


TYPICAL PERFORMANCE CHARACTERISTICS

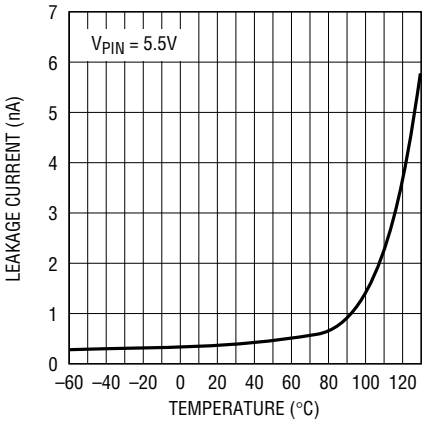
SCL, SDA and SEL Input Current vs Temperature



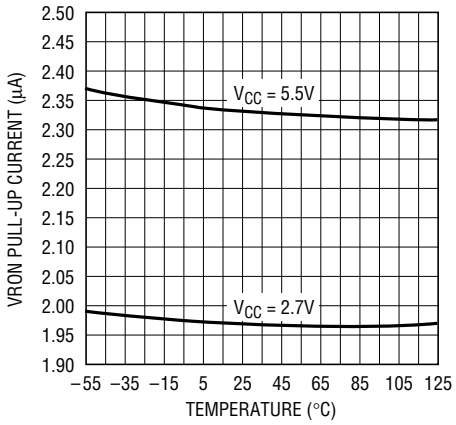
SDA, PGOOD, CPU_ON, IO_ON, CLK_ON Sink Current vs Temperature



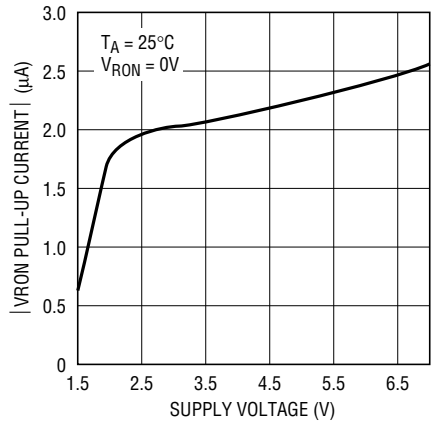
PGOOD, CPU_ON, IO_ON, CLK_ON Leakage Current vs Temperature



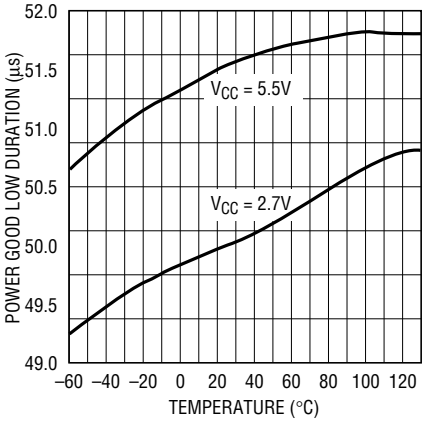
VRON Pull-Up Current vs Temperature



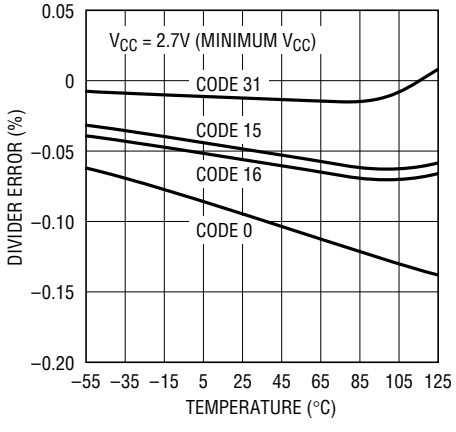
VRON Pull-Up Current vs Supply Voltage



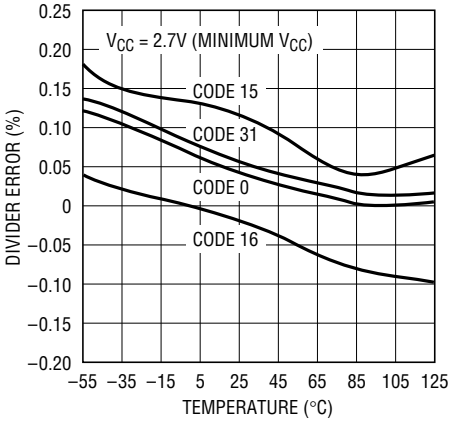
Power Good Low Duration vs Temperature



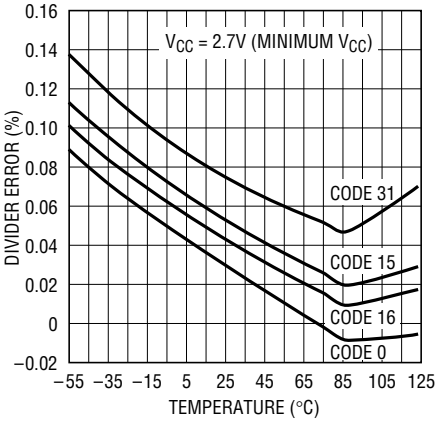
LTC1699-80 Divider Error vs Temperature



LTC1699-81 Divider Error vs Temperature



LTC1699-82 Divider Error vs Temperature



PIN FUNCTIONS

Note: Pin numbers apply to 16-lead SSOP packages.

SEL (Pin 1): Register Select Input. A TTL compatible logic input pin that is used to select 1 of 2 resistor divider settings. SEL selects the setting in Register 0 if pulled low and the setting in Register 1 if pulled high.

NC (Pin 2): Not connected.

SDA (Pin 3): SMBus Data Input/Output. SDA is a high impedance input when address, command or data bits are shifted in. It is an open drain, N-channel output when acknowledging or sending data back to the microprocessor during read-back. It requires a pull-up resistor or current source to V_{CC}.

SCL (Pin 4): SMBus Clock Input. Data at the SDA pin is latched into the LTC1699 at the rising edge of the clock and is shifted out of the SDA pin at the falling edge of the clock. SCL is a high impedance input pin. It is driven by the open collector output of a microprocessor and requires a pull-up resistor or current source to V_{CC}.

VRON (Pin 5): Global Control Input. This TTL compatible input pin is pulled up internally by a 2.5μA current source. Pulling VRON low forces the open drain output pins (CPU_ON, IO_ON, CLK_ON and PGOOD) to pull to ground. If the LTC1699-80, LTC1699-81 or LTC1699-82 is programmed to turn on DC/DC converters, pulling VRON high three-states the CPU_ON, IO_ON and CLK_ON pins and allows the DC/DC converters to soft-start.

PGOOD (Pin 6): Power Good Output. This open drain output is pulled low for 50μs each time the LTC1699-80, LTC1699-81 or LTC1699-82 turns on the DC/DC converters or SEL is toggled to select a new code. PGOOD may be connected to the FCB input of an LTC DC/DC converter to force the converter into continuous mode operation. This reduces the time needed for the converter output to settle to a lower output voltage under light load conditions if the SEL pin is toggled.

NC (Pin 7): Not connected.

CPU_ON (Pin 8): CPU DC/DC Converter Control. Open drain output, usually connected to the RUN/SS pin of a DC/DC converter that generates the CPU core supply. It pulls low to shut down the converter or becomes a high impedance state to allow the converter to soft-start.

IO_ON (Pin 9): I/O DC/DC Converter Control. Open drain output, normally connected to the RUN/SS pin of the DC/DC converter that generates the I/O supply. It pulls low to shut down the converter or becomes a high impedance state to allow the converter to soft-start.

CLK_ON (Pin 10): Clock DC/DC Converter Control. Open drain output, optionally connected to the RUN/SS pin of the DC/DC converter that generates the supply for the clock buffer. It pulls low to shut down the converter or becomes a high impedance state to allow the converter to soft-start.

NC (Pin 11): Not connected.

SENSE (Pin 12): Sense Input. Upper terminal of the resistor divider that is connected directly to the output voltage being regulated.

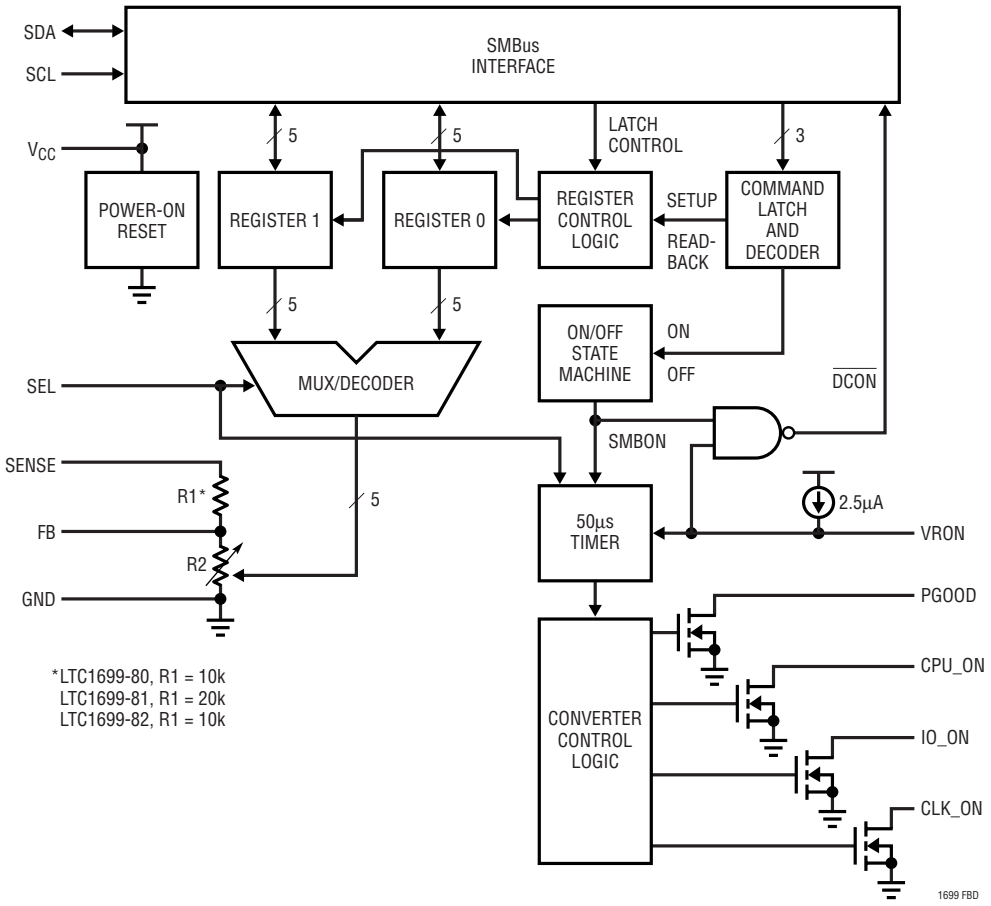
FB (Pin 13): Feedback Input. Center tap of the divider that is connected to the feedback pin of an LTC 0.8V referenced DC/DC converter.

GND (Pin 14): Ground. Connect to regulator signal ground.

GND (Pin 15): Divider Ground. Short to Pin 14.

V_{CC} (Pin 16): Positive Supply. $2.7V \leq V_{CC} \leq 5.5V$. Bypass this pin to ground with a 0.1μF ceramic capacitor.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUIT

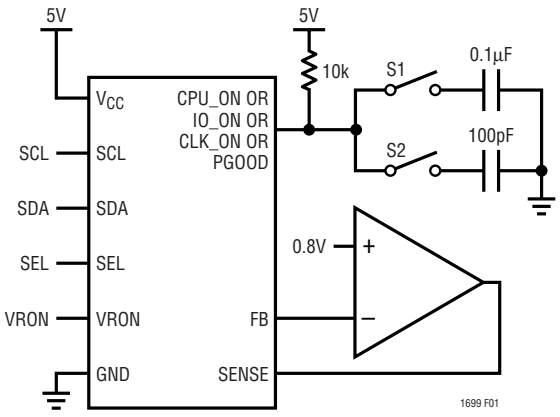
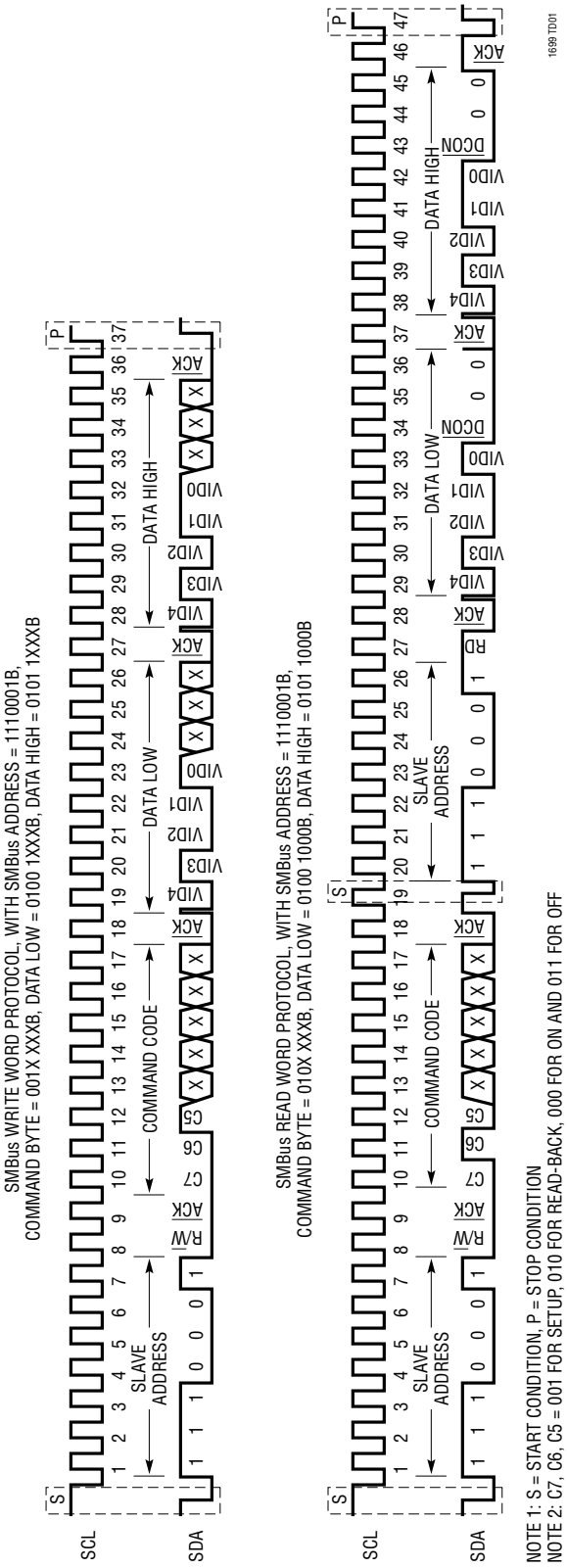


Figure 1. Load for Timing Tests

TIMING DIAGRAMS

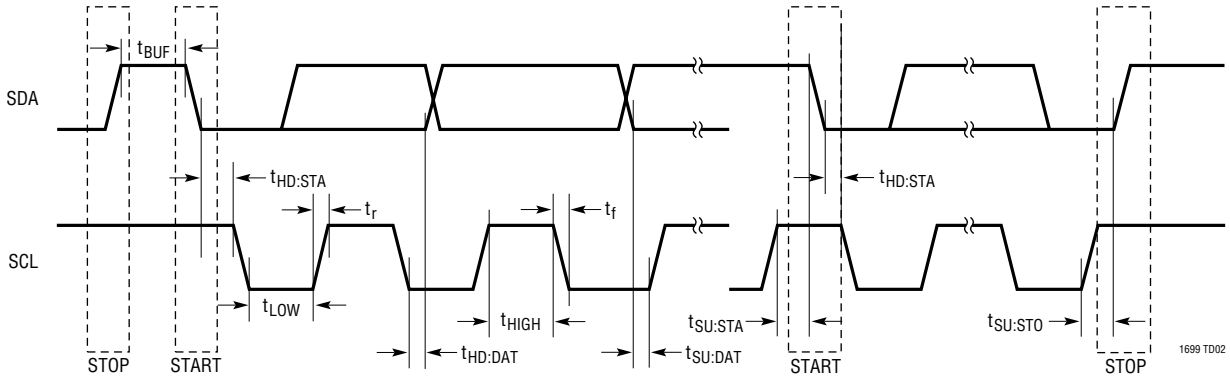
Operating Sequences



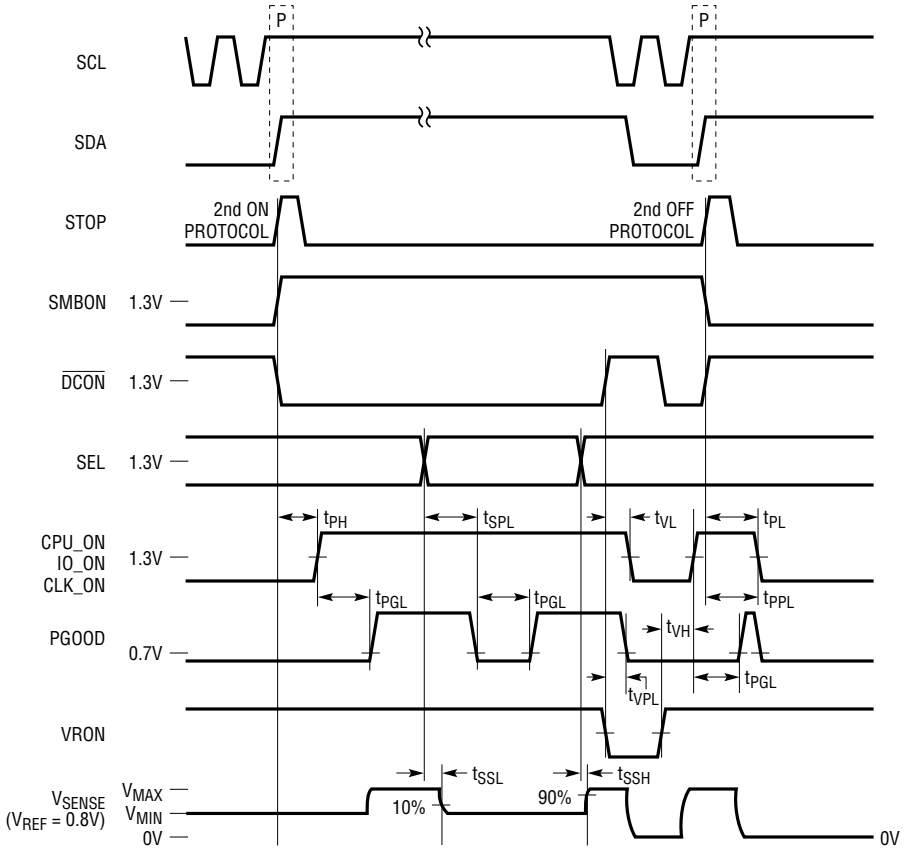
NOTE 1: S = START CONDITION, P = STOP CONDITION
NOTE 2: C7, C6, C5 = 001 FOR SETUP, 010 FOR READ-BACK, 000 FOR ON AND 011 FOR OFF

TIMING DIAGRAMS

Timing for SMBus Interface



CLK_ON, IO_ON, CLK_ON, PGOOD TIMING



NOTE: TIMING RELATIVE TO THE STOP BIT (P) IS MEASURED FROM THE RISING EDGE OF SDA
SEE TABLE 1 FOR V_{MIN} AND V_{MAX} SENSE VOLTAGES

1699 TD03

APPLICATIONS INFORMATION

In general, adjustable DC/DC Converters regulate the output voltage by dividing it down with a resistor divider and comparing the result against a precision reference voltage (V_{REF}). As shown in the Block Diagram, the LTC1699-80, LTC1699-81 and LTC1699-82 are variable resistor dividers, which are programmed through a 2-wire SMBus interface. They are specifically designed to simplify the implementation of a voltage regulator module (VRM) in both portable and desktop computers.

Two 5-bit divider settings can be programmed into Register 0 and Register 1 using the SMBus interface. The microprocessor selects one of these settings using the TTL compatible SEL pin to control a 10:5 multiplexer (MUX). The precision ±0.35% divider is intended to set the

Table 1. DC/DC Converter Output Voltage for V_{REF} = 0.8V

VID4	VID3	VID2	VID1	VID0	LTC1699-80	LTC1699-81	LTC1699-82
0	0	0	0	0	2.000V	2.05V	1.850V
0	0	0	0	1	1.950V	2.00V	1.825V
0	0	0	1	0	1.900V	1.95V	1.800V
0	0	0	1	1	1.850V	1.90V	1.775V
0	0	1	0	0	1.800V	1.85V	1.750V
0	0	1	0	1	1.750V	1.80V	1.725V
0	0	1	1	0	1.700V	1.75V	1.700V
0	0	1	1	1	1.650V	1.70V	1.675V
0	1	0	0	0	1.600V	1.65V	1.650V
0	1	0	0	1	1.550V	1.60V	1.625V
0	1	0	1	0	1.500V	1.55V	1.600V
0	1	0	1	1	1.450V	1.50V	1.575V
0	1	1	0	0	1.400V	1.45V	1.550V
0	1	1	0	1	1.350V	1.40V	1.525V
0	1	1	1	0	1.300V	1.35V	1.500V
0	1	1	1	1	1.250V	1.30V	1.475V
1	0	0	0	0	1.275V	3.50V	1.450V
1	0	0	0	1	1.250V	3.40V	1.425V
1	0	0	1	0	1.225V	3.30V	1.400V
1	0	0	1	1	1.200V	3.20V	1.375V
1	0	1	0	0	1.175V	3.10V	1.350V
1	0	1	0	1	1.150V	3.00V	1.325V
1	0	1	1	0	1.125V	2.90V	1.300V
1	0	1	1	1	1.100V	2.80V	1.275V
1	1	0	0	0	1.075V	2.70V	1.250V
1	1	0	0	1	1.050V	2.60V	1.225V
1	1	0	1	0	1.025V	2.50V	1.200V
1	1	0	1	1	1.000V	2.40V	1.175V
1	1	1	0	0	0.975V	2.30V	1.150V
1	1	1	0	1	0.950V	2.20V	1.125V
1	1	1	1	0	0.925V	2.10V	1.100V
1	1	1	1	1	0.900V	2.00V	1.075V

APPLICATIONS INFORMATION

output voltage of a DC/DC converter that generates the CPU core supply voltage. Its programmable ratios (see Table 1) are designed for 0.8V-referenced converters such as the LTC1628, LTC1702, LTC1735 and LTC1778 and comply with the Intel 5-bit desktop (VRM8.4 for LTC1699-81 and VRM9.0 for LTC1699-82) and 5-bit mobile VID codes. On power-up, the outputs of both registers are internally set to 11111B.

The LTC1699-80, LTC1699-81 and LTC1699-82 provide three pins, CPU_ON, IO_ON, and CLK_ON to (optionally) control three DC/DC converters that generate the CPU, I/O and clock buffer V_{CC} voltages in a VRM. These open drain, N-channel output pins usually connect to the RUN/SS pins of the converters and pull low to shut down the converters or become a high impedance state to allow the converters to soft-start.

The PGOOD pin is driven from an internal timer that pulls PGOOD low for 50µs typical whenever the resistor divider setting is changed or the converters are allowed to soft-start. Over the entire temperature and supply voltage range, the timer low period is 70µs max which meets the 100µs max converter output settling time specified by Intel. The PGOOD pin, if tied to the FCB pin of an LTC DC/DC converter, reduces the time needed for the converter output to decrease to a lower voltage under light load conditions by forcing the converter into continuous mode for 50µs.

The TTL compatible VRON input pin and the output of the internal on/off state machine (SMBON) control the state of the CPU_ON, IO_ON, CLK_ON and PGOOD pins. SMBON is accessed using SMBus protocols and must be programmed to a high state before the converters can turn on. The SMBus protocols (see Figure 2) incorporate safeguards against errors caused by bus conflicts.

Resistor Divider

The resistor divider is designed specifically for DC/DC converters, such as the LTC1628, LTC1702, LTC1735, LTC1778 and LTC1929 with a reference voltage of 0.8V. It consists of a fixed resistor, R_{FB1} connected between the SENSE and FB pins and a variable resistor, R_{FB2}, connected between the FB and GND pins. The SENSE and FB pins are tied to the output and feedback nodes of the DC/DC converter respectively. The output of the DC/DC converter is given by:

$$V_{OUT} = V_{REF} \bullet (R_{FB2}+R_{FB1})/R_{FB2}$$

where V_{REF} is the internal reference voltage of the converter. Each resistor has a tolerance of ±30% but the ratio, $(R_{FB2}+R_{FB1})/R_{FB2}$, is specified to within ±0.35% over temperature. The error budget for the DC/DC converter output voltage must include the ±0.35% ratio tolerance and the tolerance in V_{REF}.

The value of R_{FB1} is fixed and R_{FB2} is changed to vary the divider setting. The value of R_{FB2} for any divider setting can be calculated from the above equation, assuming that R_{FB1} = 10kΩ for the LTC1699-80 and LTC1699-82 and 20kΩ for the LTC1699-81. Table 1 shows the output voltage of a DC/DC converter (V_{REF} = 0.8V) for all 32 settings of the resistor divider. The divider setting is determined by the outputs (VID0-VID4) of the register selected by the SEL pin.

SMBus Interface

The SMBus interface uses two wires: SDA and SCL. Data to the LTC1699-80, LTC1699-81 or LTC1699-82, is latched at the rising edge of the SCL clock input and shifted out at the falling edge. The V_{IL} and V_{IH} logic threshold voltages of the SDA and SCL pins are 0.8V and 2.1V respectively and comply with Rev 1.1 version of the Intel System Management Bus Specifications.

The Write Word and Read Word protocols (Figure 2) share three common features. First, the 7-bit slave address for both protocols is internally hardwired to 1110 001B = E2H. A single R/$\overline{W}$ bit follows the slave address. This bit is low for data transfer from the microprocessor to the LTC1699-80, LTC1699-81 or LTC1699-82 and high for transfers in the opposite direction.

Second, the LTC1699-80, LTC1699-81 and LTC1699-82 decode only the three most significant bits of the 8-bit command code. Table 2 shows the four valid combinations. All other combinations are ignored.

Third, the Data Low and Data High bytes correspond to Registers 0 and 1 respectively. In Write Word protocol with C7 = C6 = 0, C5 = 1, the five most significant bits (VID0-VID4) of these bytes specify a resistor divider setting.

APPLICATIONS INFORMATION

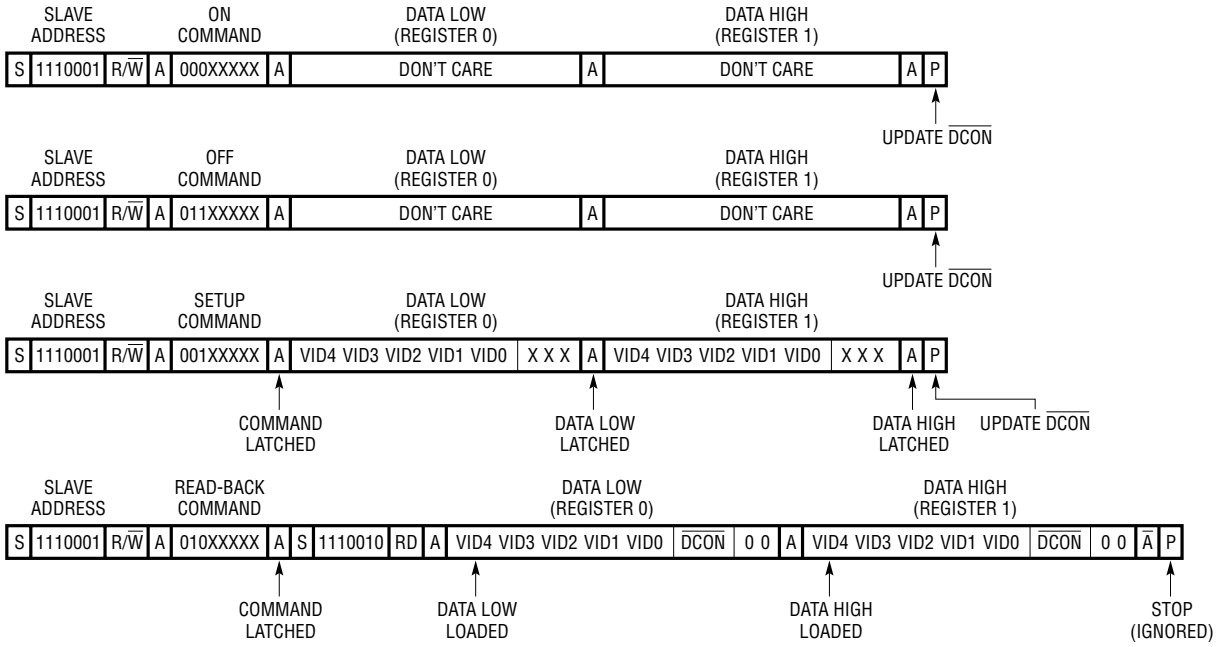


Figure 2. Write Word and Read Word Protocols

Table 2. LTC1699-80, LTC1699-81 and LTC1699-82 Command Bits

C7	C6	C5	COMMAND	PROTOCOL
0	0	0	On	Write Word
0	1	1	Off	Write Word
0	0	1	Setup	Write Word
0	1	0	Read-Back	Read Word

Write Word Protocol

Each Write Word protocol (Figure 2) begins with a start bit (S) and ends with a stop bit (P). As shown in the Timing Diagram the start and stop bits are defined as high to low and low to high transitions respectively, while SCL is high. In between the start and stop bits, the microprocessor transmits four bytes to the LTC1699-80, LTC1699-81 or LTC1699-82. These are the address byte, an 8-bit command code and two data bytes. The LTC1699-80, LTC1699-81 and LTC1699-82 sample each bit at the rising edges of the SCL clock.

When the microprocessor issues a start bit, all the slave devices on the bus, including the LTC1699-80, LTC1699-81 or LTC1699-82 clock in the address byte, which consists of a 7-bit slave address and the R/$\overline{W}$ bit (set to 0). If the slave address from the microprocessor does not match the internal hardwired address, the LTC1699-80, LTC1699-81 or LTC1699-82 returns to an idle state and waits for the next start bit. If the slave address matches, the LTC1699-80, LTC1699-81 or LTC1699-82 acknowledges by pulling the SDA line low for one clock cycle after the address byte. After detecting the acknowledgement bit (A), the microprocessor transmits the second byte or command code. The command code identifies the type of Write Word protocol as Setup, On or Off (Table 2). The Setup protocol is used to load two resistor divider settings into Register 0 and 1. The On and Off protocols turn the converters on or off in conjunction with the VRON pin.

Once all 8 bits of the command code are clocked in, the LTC1699-80, LTC1699-81 or LTC1699-82 issues a second acknowledgement bit to the microprocessor. After detecting the acknowledgement bit, the microprocessor transmits two data bytes. Each data byte is acknowledged in turn for all three Write Word protocols but is only latched into Register 0 or 1 in Setup protocol. This prevents previously loaded settings from accidentally being changed. The first or Data Low byte is loaded into Register 0. The second or Data High byte is loaded into

APPLICATIONS INFORMATION

Register 1. After issuing the final acknowledgement bit, the SMBus interface returns to an idle state and waits for the next start bit.

Read Word Protocol

The Read Word protocol starts off like Write Word protocol but after the command code acknowledgment, the microprocessor issues a second start bit (called a repeated start). This is followed by the slave address but with the R/$\overline{W}$ bit set high to indicate that data direction is now from the LTC1699-80, LTC1699-81 or LTC1699-82 to the microprocessor. The LTC1699-80, LTC1699-81 or LTC1699-82 then acknowledges the slave address and clocks the contents of Register 0 (Data Low byte) to the microprocessor. The Data Low byte is acknowledged by the microprocessor. On detecting the acknowledgment bit, the LTC1699-80, LTC1699-81 or LTC1699-82 clocks out the contents of Register 1 (Data High byte). As defined in the SMBus specifications, the microprocessor does not acknowledge the last data byte. The LTC1699-80, LTC1699-81 or LTC1699-82 enters an idle state to wait for the next start bit after clocking out the Data High byte. The five most significant bits (VID0-VID4) of the Data Low and High bytes are the resistor divider settings previously loaded using the Setup protocol. The next bit below the VID0-VID4 bits is the status of the $\overline{DCON}$ signal. If this bit is low (high), the DC/DC converters are switched on (off). The two unused, least significant bits of the Data Low and Data High bytes are clocked out as zeros which removes the need to mask out these bits in software.

Safeguards

The LTC1699-80, LTC1699-81 and LTC1699-82 provide safeguards against incorrect divider codes and the unintentional turn-on or turn-off of the DC/DC converters. Incorrect codes due to bus conflicts during Setup protocols can cause damage to circuits powered by the DC/DC converters. The safeguards built into the LTC1699-80, LTC1699-81 and LTC1699-82 include Read-Back, repeated On and Off protocols, ignoring On protocols if the registers have not been setup, locking out registers while the DC/DC converters are operating and latching in VID codes only in Setup protocols.

After power-up, the microprocessor must set up the registers before the LTC1699-80, LTC1699-81 and LTC1699-82 recognizes On protocols. This requirement ensures that the correct DC/DC converter output is programmed before the converters are turned on. After setup, Read-Back allows the contents of Registers 0 and 1 to be verified in case the VID codes were corrupted by noise or bus conflicts.

In order to turn on the DC/DC converter, two On protocols must be sent to slave address E2H without any other (E2H) protocols in between. Protocols to other slave addresses are still allowed and are ignored. Similarly, two Off protocols must be sent to slave address E2H to turn the converters off. The On and Off protocols are monitored by an internal state machine. The output of the state machine, SMBON, is high after two On commands and low after two Off commands. Repeated On and Off protocols reduce the chances of bus conflicts and noise turning the converter on or off accidentally. In both On and Off protocols, the LTC1699-80, LTC1699-81 and LTC1699-82, do not latch in the Data Low and Data High bytes. This protects the settings that have already been loaded into the registers and verified by read-back.

Once the converters are turned on (both SMBON and VRON are high) the contents of Registers 0 and 1 are protected and can only be altered with Setup protocols if VRON is pulled low or two Off protocols are sent to the LTC1699-80, LTC1699-81 or LTC1699-82 (to force SMBON low).

DC/DC Converter Control

The LTC1699-80, LTC1699-81 and LTC1699-82 provide six pins for DC/DC converter control: SEL, VRON, CPU_ON, IO_ON, CLK_ON and PGOOD. These pins (except SEL) and the output of the internal on/off state machine (SMBON) determine if the DC/DC converters are operating or in shutdown.

The SEL and VRON pins are TTL compatible, high impedance inputs with a logic threshold of 1.3V over the entire 2.7V to 5.5V supply range. They are compatible with 3.3V logic and have ±50mV of hysterisis for noise rejection. When pulled high or low, the SEL pin selects Register 1 and 0 respectively as the active divider setting. The VRON

APPLICATIONS INFORMATION

pin is used to shut down the converters without the need for lengthy SMBus Off protocols and can also be used to turn on up to three DC/DC converters simultaneously. The VRON pin has an internal 2.5uA current source pull-up.

The CPU_ON, IO_ON and CLK_ON pins are N-channel, open drain outputs. These outputs can be connected to the RUN/SS pin of LTC DC/DC converters that generate the V_{CC} supplies of the CPU, I/O circuits and the clock buffer. The RUN/SS pin shuts down the converter if pulled low and also serves as a connection for the soft-start capacitor. The CPU_ON, IO_ON and CLK_ON pins are open drain outputs and do not interfere with soft-start when switched into a high impedance state. To keep the I/O and clock buffer V_{CC} supplies alive at all times, disconnect the IO_ON and CLK_ON pins from the corresponding RUN/SS pins. The N-channel FETs at the CPU_ON, IO_ON and CLK_ON pins typically discharge a 0.1µF (0.01µF) soft-start capacitor from 3V to 0.35V in 21µs (2.3µs) with V_{CC} = 2.7V.

The PGOOD or "Power Good" pin is also an open drain, N-channel output. The PGOOD pin pulls low if the DC/DC converters are shutdown. If the converters are turned on, an internal timer keeps PGOOD low for 50µs (typical) which allows time for the converters to enter regulation. Toggling the SEL pin while the converters are turned on also causes the PGOOD pin to pull low for 50µs. The PGOOD pin may be used to force continuous operation in an LTC DC/DC converter. If the SEL pin is toggled to select a lower output voltage, it may take an unacceptably long time for the output of the DC/DC converter to decrease to the new voltage under light load conditions. To reduce this time needed, the PGOOD pin can be connected to the FCB (force continuous bar) pin of the converter. When the SEL pin is toggled to select a new code, FCB pin is forced low for 50µs. This forces the DC/DC converter out of Burst Mode™ operation and into continuous mode.

The VRON pin and SMBON, the output of the internal on/off state machine, control the state of the CPU_ON, IO_ON, CLK_ON and PGOOD pins. The $\overline{DCON}$ signal is a logical NAND function of the logical states of VRON and SMBON and is the status bit that is returned during Read-back. Table 3 shows the state of the CPU_ON, IO_ON, and CLK_ON pins for various combinations of VRON and SMBON.

Table 3. DC/DC Converter Control Pins

VRON	SMBON	$\overline{DCON}$	PGOOD	CPU_ON, IO_ON, CLK_ON
0	X (Note 3)	1	0	0
1	0	1	0	0
1	↑	↓	0 for 50µs (Note 1)	Z (Note 2)
↑	1	↓	0 for 50µs (Note 1)	Z (Note 2)

Note 1: Also triggered by SEL pin toggling.

Note 2: Z = High Impedance

Note 3: X = Don't care

If the $\overline{DCON}$ control bit goes high, the N-channel transistor at the CPU_ON, IO_ON, CLK_ON and PGOOD pins turn on, pulling these pins to ground. Any connected RUN/SS pins are pulled to ground, shutting down the converters.

If the $\overline{DCON}$ control bit goes low, the N-channel transistor at the CPU_ON, CLK_ON, IO_ON and PGOOD pins turn off and become high impedance outputs. This allows the soft-start capacitor at each RUN/SS pin to charge up and the DC/DC converters wake up gradually with a soft-start cycle. The PGOOD pin also pulls low for typically 50µs to indicate that the converter outputs are temporarily out of regulation. An internal timer determines the duration of the low pulse. The timer is triggered by SEL toggling or $\overline{DCON}$ going low.

Power-Up Reset

On power-up, the internal POR circuit generates a low reset pulse, which stays low until V_{CC} rises above approximately 2.2V. The reset pulse forces the SMBus interface into an idle state in which it listens for a start bit. At the same time the outputs of both Register 0 and Register 1 are set to 11111B. The $\overline{DCON}$ bit is pulled high so that the CPU_ON, IO_ON, CLK_ON and PGOOD pins are pulled low to shut down the DC/DC converters.

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APPLICATIONS INFORMATION

Operating Sequence

A typical control sequence for the LTC1699-80, LTC1699-81 and LTC1699-82 is as follows:

- On power up, the $\overline{DCON}$ bit is preset to a high state by the power-on reset (POR) circuit. The CPU_ON, IO_ON and CLK_ON pins are pulled low to shut down the DC/DC converters. PGOOD pulls low to indicate that the converters are not in regulation.
- Pull VRON low as a precaution. Take SEL high or low to select the divider setting; e.g., one that suits the existing power source (battery or wall-pack).
- Use the Setup protocol to load the appropriate divider settings in Registers 0 and 1 and enable the on/off state machine.
- Use the Read-Back protocol to verify the contents of Registers 0 and 1.
- Repeat the setup and read-back if the codes are incorrect (due to bus conflicts).
- Send two On protocols in succession to clear the $\overline{DCON}$ bit.
- Use the Read-Back protocol to verify that the $\overline{DCON}$ is low. A high state will indicate that an On command code was corrupted by bus conflicts.
- Pull VRON high. Since $\overline{DCON}$ = 0, the CPU_ON, IO_ON and CLK_ON pins enter a high impedance state, allowing the DC/DC converters to soft-start. PGOOD stays low for 50µs.
- To shut down the supply, send two Off protocols to set the $\overline{DCON}$ bit high or pull VRON low if immediate shutdown is required.

The VRON signal in the 8-pin MSOP versions of the LTC1699-80, LTC1699-81 and LTC1699-82 are pulled high internally by a 2.5µA current source. For these versions, the converters are turned on or off only through the SMBus interface.

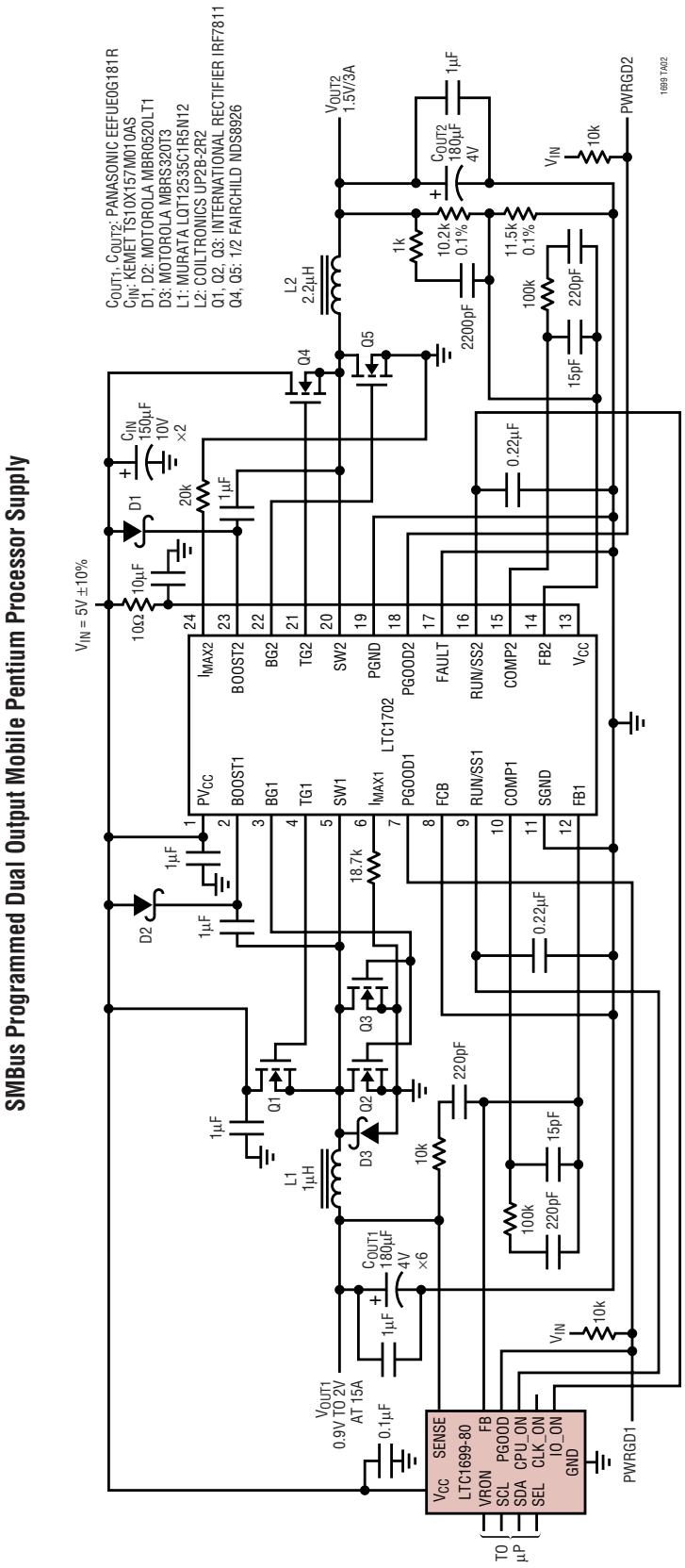
Overvoltage Protection Faults

Toggling the SEL pin, i.e. changing the ladder setting "on the fly" can trigger some converters with over-voltage fault protection (OVP) into a fault state if the new setting calls for a lower output voltage. For some converters such as the LTC1702, cycling the power supply is the only way to clear the fault and restore normal operation.

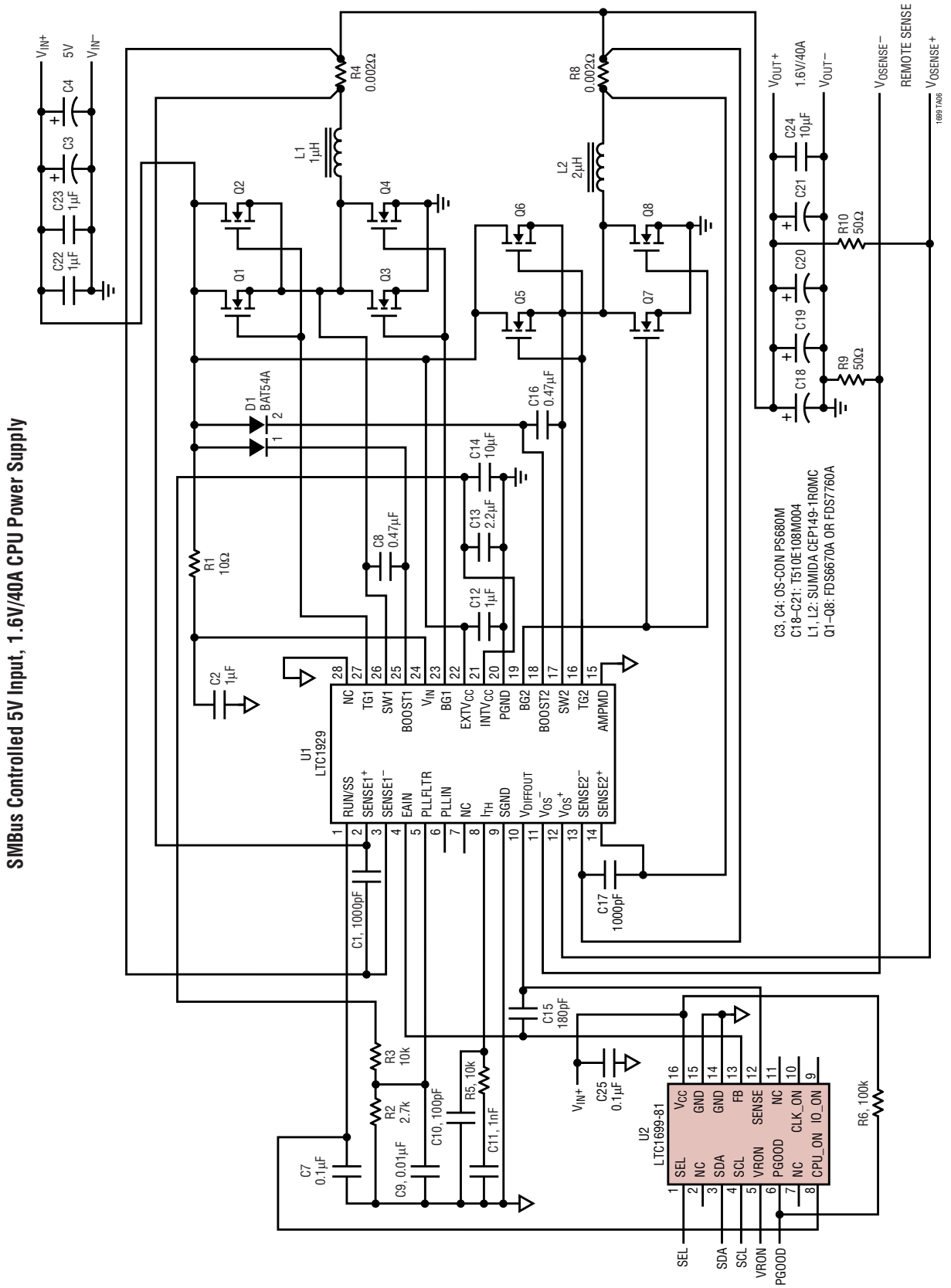
For the LTC1702, an OVP fault is triggered if the difference between the programmed and prevailing output voltages is greater than 15%, and persists for more than 25µs. To prevent the OVP fault from disabling the LTC1702, tie the FAULT pin of the LTC1702 low. Tying FAULT low does not disable the OVP circuit but blocks its effects.

TYPICAL APPLICATIONS

SMBus Programmed Dual Output Mobile Pentium Processor Supply

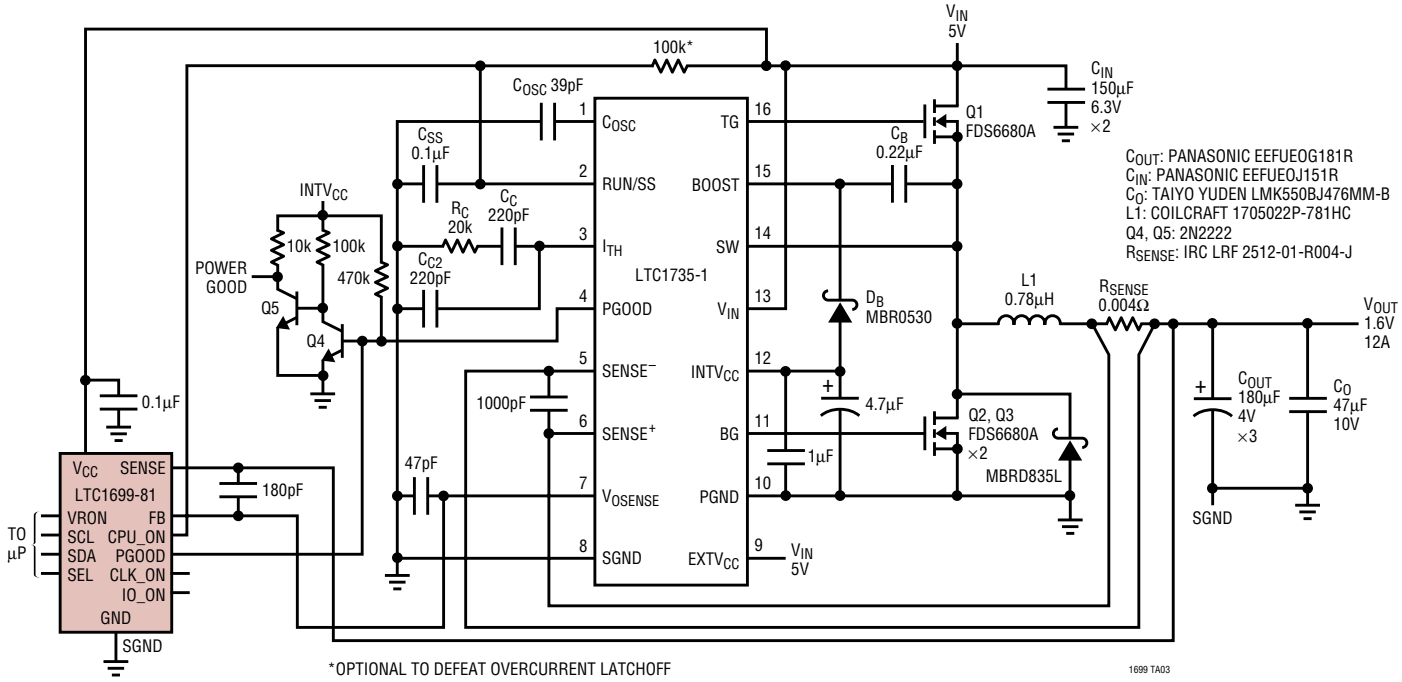


TYPICAL APPLICATIONS



TYPICAL APPLICATIONS

SMBus Programmed CPU Core Voltage Regulator for 2-Step Applications (V_{IN} = 5V) with Burst Mode Operation Disabled



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

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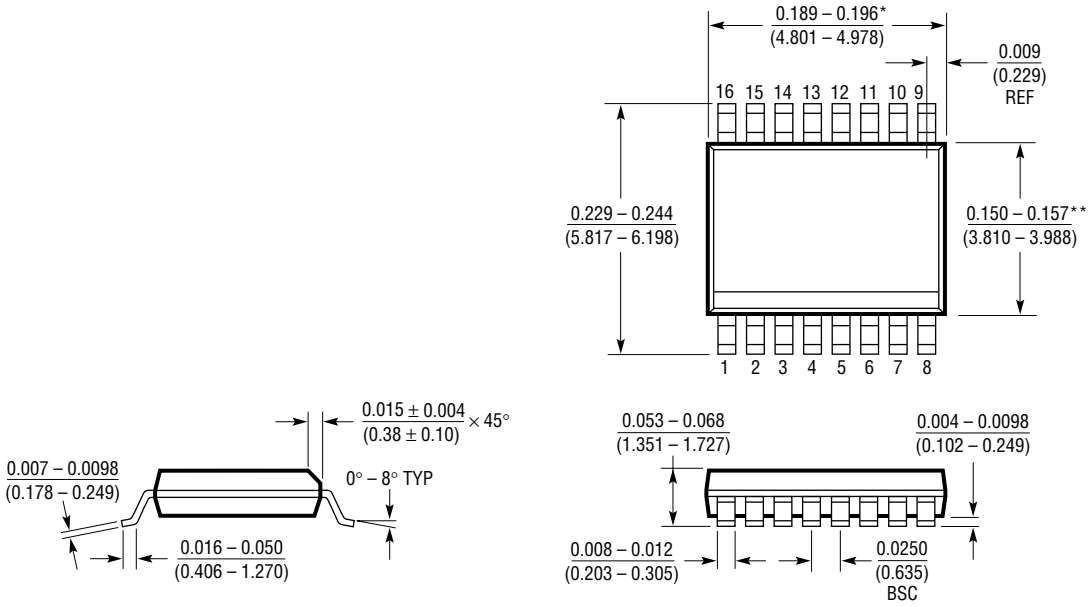
(LTC DWG # 05-08-1641)

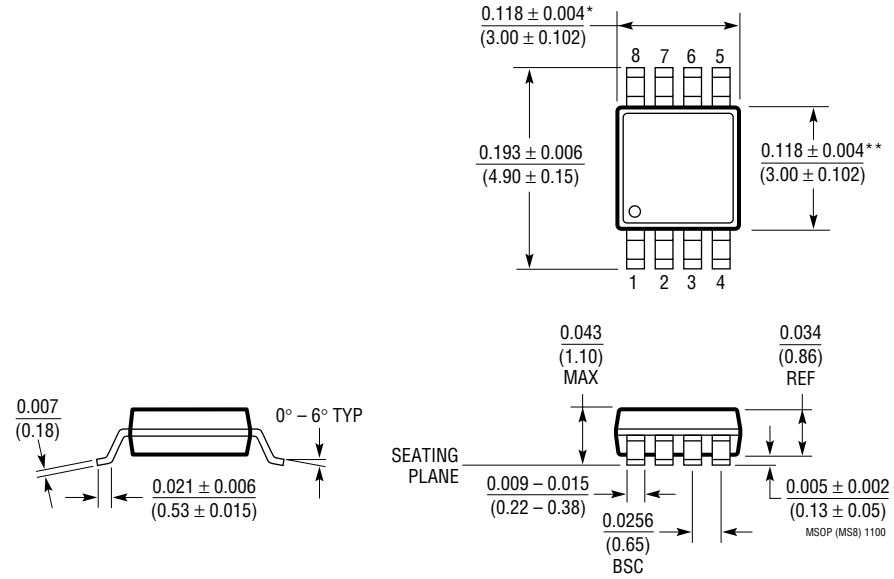


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)

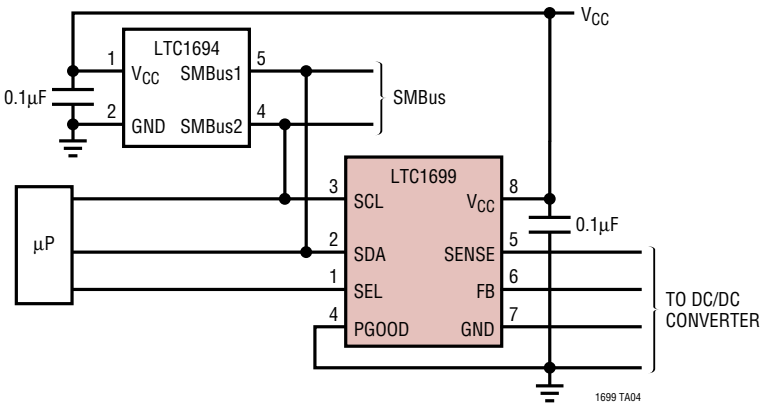


* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

TYPICAL APPLICATION

Enhanced Data Transmission Speed



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628/ LTC1628-PG	High Efficiency, 2-phase, Synchronous Step Down Switching Regulators	Dual Controller, 0.8V Reference, Wide Input Voltage Range
LTC1694/ LTC1694-1	SMBus/I^2C Accelerators in SOT-23	Improves SMBus/I^2C Data Integrity
LTC1702	Dual 1 MHz Synchronous 5V to 2.xV/1.xV Switching Regulator Controller	Low Input Voltages, High Efficiency
LTC1735/ LTC1735-1	High Efficiency Synchronous Step Down Switching Regulators	0.8V Reference, Wide Input Voltage Range, Synchronizable/ Programmable Fixed Frequency
LTC1878	Monolithic Synchronous Step Down Switching Regulator	0.8V Reference, Internal Synchronous Switch, $2.65V \le V_{IN} \le 6V$
LTC1706-19	VID Voltage Programmer	Parallel Interface, Designed for 1.19V Referenced Switching Regulators
LTC1706-81	5-Bit Desktop VID Programmer	Parallel Interface, 0.8V Reference Intel Desktop VID Codes (VRM8.4)
LTC1706-82	VID Programmer for Intel VRM9.0	Parallel Interface, 0.8V Reference Intel Desktop VID codes (VRM9.0)
LTC1778	Wide Operating Range, No R_{SENSE}™ Step-Down Controller	2% to 90% Duty Cycle at 200kHz, $t_{ON(MIN)} \le 100ns$, Stable with Ceramic C_{OUT}
LTC1929/ LTC1929-PG	2-Phase High Efficiency Synchronous Step-Down Switching Regulators	2-Phase Single Output Controller, Wide V_{IN} Range: 4V to 36V Operation

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