LTC2051/LTC2052

Dual/Quad Zero-Drift Operational Amplifiers

FEATURES

- **Maximum Offset Voltage of 3μV**
- **Maximum Offset Voltage Drift of 30nV/°C**
- **Small Footprint, Low Profile MS8/GN16 Packages**
- **Single Supply Operation: 2.7V to ±5.5V**
- Noise: 1.5μV_{P-P} (0.01Hz to 10Hz Typ)
- Voltage Gain: 140dB (Typ)
- PSRR: 130dB (Typ)
- CMRR: 130dB (Typ)
- Supply Current: 0.75mA (Typ) per Amplifier
- Extended Common Mode Input Range
- Output Swings Rail-to-Rail
- Operating Temperature Range –40°C to 125°C
- Available in 3mm × 3mm × 0.8mm DFN Package

APPLICATIONS

- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition
- DC Accurate RC Active Filters
- Low Side Current Sense

DESCRIPTION

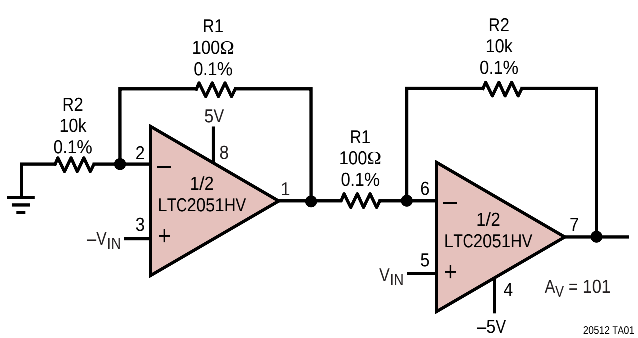
The LTC®2051/LTC2052 are dual/quad zero-drift operational amplifiers available in the MS8 and SO-8/GN16 and S14 packages. For space limited applications, the LTC2051 is available in a 3mm × 3mm × 0.8mm dual fine pitch leadless package (DFN). They operate from a single 2.7V supply and support ±5V applications. The current consumption is 750μA per op amp.

The LTC2051/LTC2052, despite their miniature size, feature uncompromising DC performance. The typical input offset voltage and offset drift are 0.5μV and 10nV/°C. The almost zero DC offset and drift are supported with a power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) of more than 130dB.

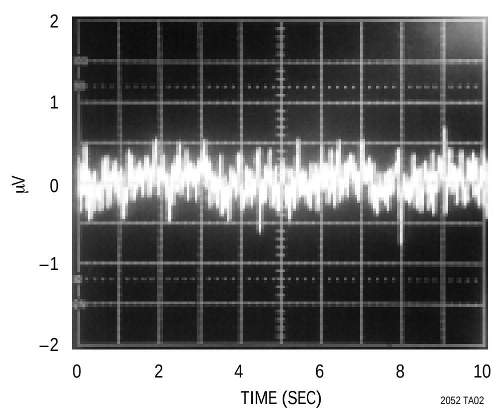
The input common mode voltage ranges from the negative supply up to typically 1V from the positive supply. The LTC2051/LTC2052 also have an enhanced output stage capable of driving loads as low as 2kΩ to both supply rails. The open-loop gain is typically 140dB. The LTC2051/LTC2052 also feature a 1.5μV_{P-P} DC to 10Hz noise and a 3MHz gain-bandwidth product.

TYPICAL APPLICATION

High Performance Low Cost Instrumentation Amplifier



Input Referred Noise 0.1Hz to 10Hz

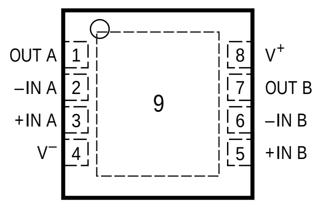


ABSOLUTE MAXIMUM RATINGS (Note 1)

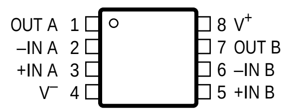
Total Supply Voltage (V^+ to V^-)
LTC2051/LTC2052 .... 7V
LTC2051HV/LTC2052HV 12V
Input Voltage (Note 5) .... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short-Circuit Duration .... Indefinite

Operating Temperature Range .... –40°C to 125°C
Specified Temperature Range (Note 3) –40°C to 125°C
Storage Temperature Range .... –65°C to 150°C
DD Package .... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) .... 300°C

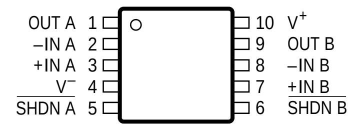
PACKAGE/ORDER INFORMATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 160°C/W
EXPOSED PAD (PIN 9) IS CONNECTED TO V^- (PIN 4)

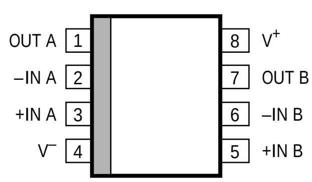


MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 250°C/W



MS10 PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 250°C/W

ORDER PART NUMBER*	DD PART MARKING	ORDER PART NUMBER	MS8 PART MARKING	ORDER PART NUMBER	MS10 PART MARKING
LTC2051CDD	LAAN	LTC2051CMS8	LTMN	LTC2051CMS10	LTMQ
LTC2051IDD		LTC2051IMS8	LTMP	LTC2051IMS10	LTMR
LTC2051HVCDD	LAEL	LTC2051HVCMS8	LTPJ	LTC2051HVCMS10	LTRB
LTC2051HVIDD		LTC2051HVIMS8	LTPK	LTC2051HVIMS10	LTRC
		LTC2051HMS8	LTVF		
		LTC2051HVHMS8	LTVH		



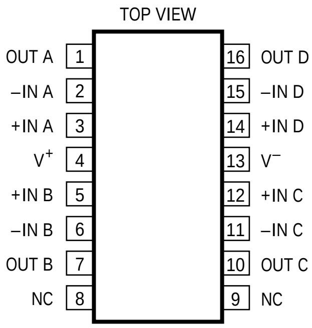
S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 190°C/W

ORDER PART NUMBER	S8 PART MARKING
LTC2051CS8	2051
LTC2051IS8	2051I
LTC2051HVCS8	2051HV
LTC2051HVIS8	051HVI
LTC2051HS8	2051H
LTC2051HVHS8	051HVH

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

PACKAGE/ORDER INFORMATION

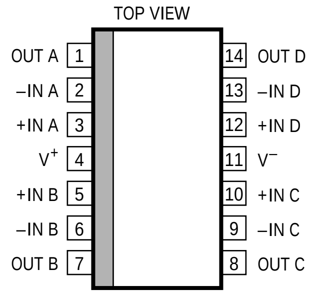


GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC2052CGN
LTC2052IGN
LTC2052HVCGN
LTC2052HVIGN
LTC2052HGN
LTC2052HVHGN

GN PART MARKING
2052
2052I
2052HV
052HVI
2052H
052HVH



S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC2052CS
LTC2052IS
LTC2052HVCS
LTC2052HVIS
LTC2052HS
LTC2052HVHS

AVAILABLE OPTIONS

PART NUMBER	AMPS/PACKAGE	SPECIFIED TEMP RANGE	SPECIFIED VOLTAGE	PACKAGE
LTC2051CDD	2	0°C to 70°C	3V, 5V	DD
LTC2051CS8	2	0°C to 70°C	3V, 5V	SO-8
LTC2051CMS8	2	0°C to 70°C	3V, 5V	8-Lead MSOP
LTC2051CMS10	2	0°C to 70°C	3V, 5V	10-Lead MSOP
LTC2051HVCDD	2	0°C to 70°C	3V, 5V, ±5V	DD
LTC2051HVCS8	2	0°C to 70°C	3V, 5V, ±5V	SO-8
LTC2051HVCMS8	2	0°C to 70°C	3V, 5V, ±5V	8-Lead MSOP
LTC2051HVCMS10	2	0°C to 70°C	3V, 5V, ±5V	10-Lead MSOP
LTC2051IDD	2	–40°C to 85°C	3V, 5V	DD
LTC2051IS8	2	–40°C to 85°C	3V, 5V	SO-8
LTC2051IMS8	2	–40°C to 85°C	3V, 5V	8-Lead MSOP
LTC2051IMS10	2	–40°C to 85°C	3V, 5V	10-Lead MSOP
LTC2051HVIDD	2	–40°C to 85°C	3V, 5V, ±5V	DD
LTC2051HVIS8	2	–40°C to 85°C	3V, 5V, ±5V	SO-8
LTC2051HVIMS8	2	–40°C to 85°C	3V, 5V, ±5V	8-Lead MSOP
LTC2051HVIMS10	2	–40°C to 85°C	3V, 5V, ±5V	10-Lead MSOP
LTC2051HS8	2	–40°C to 125°C	3V, 5V	SO-8
LTC2051HMS8	2	–40°C to 125°C	3V, 5V	8-Lead MSOP
LTC2051HVHS8	2	–40°C to 125°C	3V, 5V, ±5V	SO-8
LTC2051HVHMS8	2	–40°C to 125°C	3V, 5V, ±5V	8-Lead MSOP
LTC2052CS	4	0°C to 70°C	3V, 5V	14-Lead SO
LTC2052CGN	4	0°C to 70°C	3V, 5V	16-Lead SSOP
LTC2052HVCS	4	0°C to 70°C	3V, 5V, ±5V	14-Lead SO
LTC2052HVCGN	4	0°C to 70°C	3V, 5V, ±5V	16-Lead SSOP

AVAILABLE OPTIONS

PART NUMBER	AMPS/PACKAGE	SPECIFIED TEMP RANGE	SPECIFIED VOLTAGE	PACKAGE
LTC2052IS	4	–40°C to 85°C	3V, 5V	14-Lead SO
LTC2052IGN	4	–40°C to 85°C	3V, 5V	16-Lead SSOP
LTC2052HVIS	4	–40°C to 85°C	3V, 5V, ±5V	14-Lead SO
LTC2052HVIGN	4	–40°C to 85°C	3V, 5V, ±5V	16-Lead SSOP
LTC2052HS	4	–40°C to 125°C	3V, 5V	14-Lead SO
LTC2052HGN	4	–40°C to 125°C	3V, 5V	16-Lead SSOP
LTC2052HVHS	4	–40°C to 125°C	3V, 5V, ±5V	14-Lead SO
LTC2052HVHGN	4	–40°C to 125°C	3V, 5V, ±5V	16-Lead SSOP

ELECTRICAL CHARACTERISTICS

(LTC2051/LTC2052, LTC2051HV/LTC2052HV) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, 5V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		LTC2051C/LTC2052C LTC2051I/LTC2052I MIN	TYP	MAX	LTC2051H/LTC2052H MIN	TYP	MAX	UNITS
Input Offset Voltage	(Note 2)			±0.5	±3		±0.5	±3	µV
Average Input Offset Drift	(Note 2)	●		0.01	±0.03		0.01	±0.05	µV/°C
Long-Term Offset Drift				50			50		nV/√mo
Input Bias Current (Note 4)	V_S = 3V			±8	±50		±8	±50	pA
	V_S = 3V	●			±100			±3000	pA
	V_S = 5V			±25	±75		±25	±75	pA
	V_S = 5V	●			±150			±3000	pA
Input Offset Current (Note 4)	V_S = 3V				±100			±100	pA
	V_S = 3V	●			±150			±700	pA
	V_S = 5V				±150			±150	pA
	V_S = 5V	●			±200			±700	pA
Input Noise Voltage	R_S = 100Ω, DC to 10Hz			1.5			1.5		μV_{P-P}
Common Mode Rejection Ratio	V_{CM} = GND to V^+ – 1.3,		115	130		115	130		dB
	V_S = 3V	●	110	130		110	130		dB
	V_{CM} = GND to V^+ – 1.3,		120	130		120	130		dB
	V_S = 5V	●	115	130		115	130		dB
Power Supply Rejection Ratio			120	130		120	130		dB
		●	115	130		115	130		dB
Large-Signal Voltage Gain	R_L = 10k, V_S = 3V		120	140		120	140		dB
		●	115	140		115	140		dB
	R_L = 10k, V_S = 5V		125	140		125	140		dB
		●	120	140		120	140		dB
Output Voltage Swing High	R_L = 2k to GND	●	V^+ – 0.15	V^+ – 0.06		V^+ – 0.15	V^+ – 0.06		V
	R_L = 10k to GND	●	V^+ – 0.05	V^+ – 0.02		V^+ – 0.05	V^+ – 0.02		V
Output Voltage Swing Low	R_L = 2k to GND	●		2	15		2	15	mV
	R_L = 10k to GND	●		2	15		2	15	mV
Slew Rate				2			2		V/µs
Gain Bandwidth Product				3			3		MHz
Supply Current (Per Amplifier)	No Load, V_S = 3V, V_{SHDN} = V_{IH}	●		0.75	1.0		0.75	1.1	mA
	No Load, V_S = 5V, V_{SHDN} = V_{IH}	●		0.85	1.2		0.85	1.3	mA
Supply Current, Shutdown	V_{SHDN} = V_{IL}, V_S = 3V	●		2	5		2	5	µA
	V_{SHDN} = V_{IL}, V_S = 5V	●		4	10		4	10	µA

ELECTRICAL CHARACTERISTICS

(LTC2051/LTC2052, LTC2051HV/LTC2052HV) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, 5V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		LTC2051C/LTC2052C LTC2051I/LTC2052I MIN	TYP	MAX	LTC2051H/LTC2052H MIN	TYP	MAX	UNITS
Shutdown Pin Input Low Voltage (V_{IL})		●			V^- + 0.5			V^- + 0.5	V
Shutdown Pin Input High Voltage (V_{IH})		●	V^+ – 0.5			V^+ – 0.5			V
Shutdown Pin Input Current	V_{SHDN} = V_{IL}, V_S = 3V	●		–1	–3		–1	–3	μA
	V_{SHDN} = V_{IL}, V_S = 5V	●		–2	–5		–2	–5	μA
Internal Sampling Frequency				7.5			7.5		kHz

(LTC2051HV/LTC2052HV) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		LTC2051C/LTC2052C LTC2051I/LTC2052I MIN	TYP	MAX	LTC2051H/LTC2052H MIN	TYP	MAX	UNITS
Input Offset Voltage	(Note 2)			±1	±3		±1	±3	μV
Average Input Offset Drift	(Note 2)	●		0.01	±0.03		0.01	±0.05	μV/°C
Long-Term Offset Drift				50			50		$nV/\sqrt{mo}$
Input Bias Current (Note 4)				±90	±150		±90	±150	pA
		●			±300			±3000	pA
Input Offset Current (Note 4)					±300			±300	pA
		●			±500			±700	pA
Input Noise Voltage	R_S = 100Ω, DC to 10Hz			1.5			1.5		$μV_{P-P}$
Common Mode Rejection Ratio	V_{CM} = V^- to V^+ – 1.3		125	130		125	130		dB
		●	120	130		120	130		dB
Power Supply Rejection Ratio			120	130		120	130		dB
		●	115	130		115	130		dB
Large-Signal Voltage Gain	R_L = 10k		125	140		125	140		dB
		●	120	140		120	140		dB
Maximum Output Voltage Swing	R_L = 2k to GND	●	±4.75	±4.92		±4.50	±4.92		V
	R_L = 10k to GND	●	±4.90	±4.98		±4.85	±4.98		V
Slew Rate				2			2		V/μs
Gain Bandwidth Product				3			3		MHz
Supply Current (Per Amplifier)	No Load, V_{SHDN} = V_{IH}	●		1	1.5		1	1.5	mA
Supply Current, Shutdown	V_{SHDN} = V_{IL}	●		15	30		15	30	μA
Shutdown Pin Input Low Voltage (V_{IL})		●			V^- + 0.5			V^- + 0.5	V
Shutdown Pin Input High Voltage (V_{IH})		●	V^+ – 0.5			V^+ – 0.5			V
Shutdown Pin Input Current	V_{SHDN} = V_{IL}	●		–7	–15		–7	–15	μA
Internal Sampling Frequency				7.5			7.5		kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: These parameters are guaranteed by design. Thermocouple effects preclude measurements of these voltage levels during automated testing.

Note 3: All versions of the LTC2051/LTC2052 are designed, characterized and expected to meet the extended temperature limits of –40°C and 125°C. The LTC2051C/LTC2052C/LTC2051HVC/LTC2052HVC are guaranteed to meet the temperature limits of 0°C and 70°C. The LTC2051I/LTC2052I/LTC2051HVI/LTC2052HVI are guaranteed to meet temperature limits of –40°C and 85°C. The LTC2051H/LTC2051HVH and LTC2052H/LTC2052HVH are guaranteed to meet the temperature limits of –40°C and 125°C.

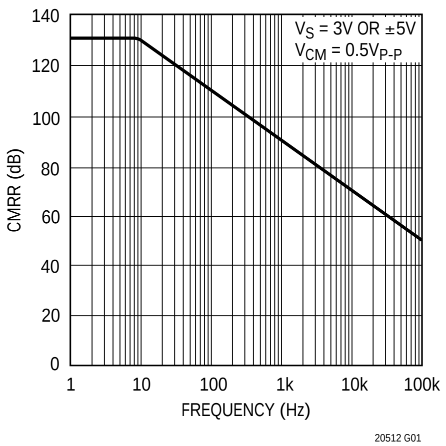
Note 4: The bias current measurement accuracy depends on the proximity of the negative supply bypass capacitors to the device under test. Because of this, only the bias current of channel B (LTC2051) and channels A and B (LTC2052) are 100% tested to the data sheet specifications. The bias currents of the remaining channels are 100% tested to relaxed limits, however, their values are guaranteed by design to meet the data sheet limits.

Note 5: This parameter is guaranteed to meet specified performance through design and characterization. It has not been tested.

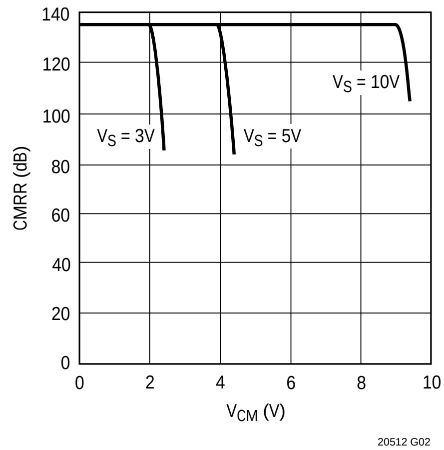
Note 6: The θ_{JA} specified for the DD package is with minimal PCB heat spreading metal. Using expanded metal area on all layers of a board reduces this value.

TYPICAL PERFORMANCE CHARACTERISTICS

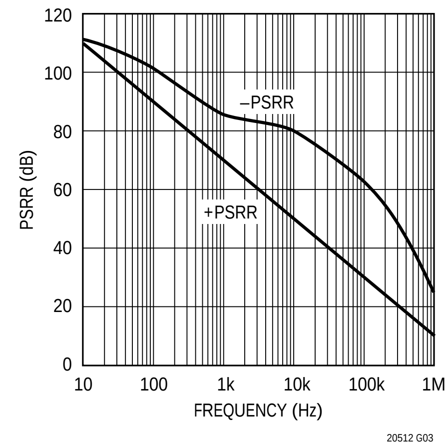
Common Mode Rejection Ratio vs Frequency



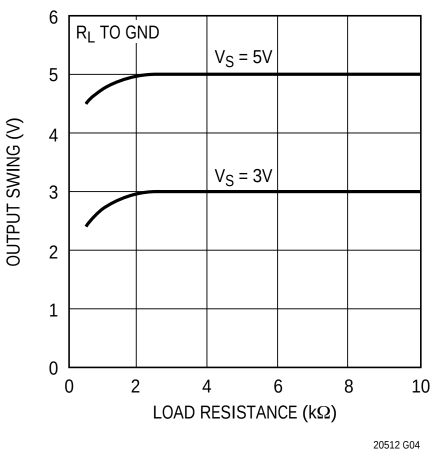
DC CMRR vs Common Mode Input Range



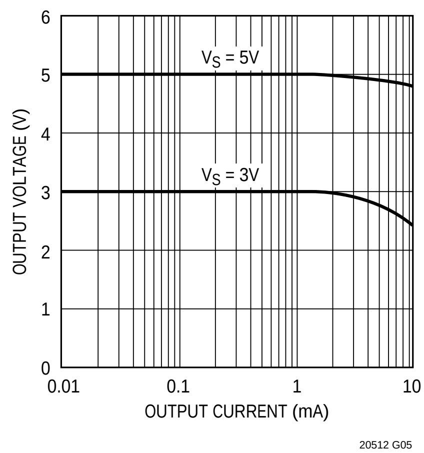
PSRR vs Frequency



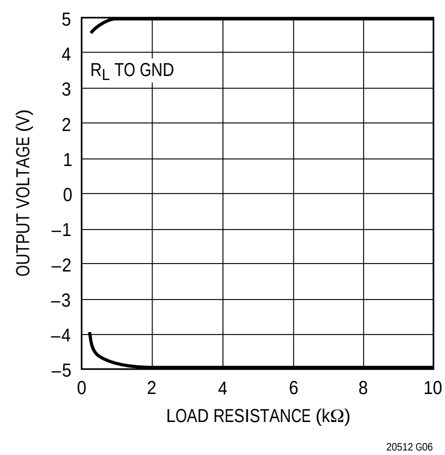
Output Voltage Swing vs Load Resistance



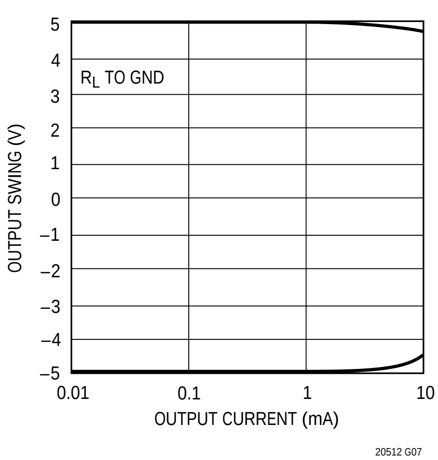
Output Swing vs Output Current



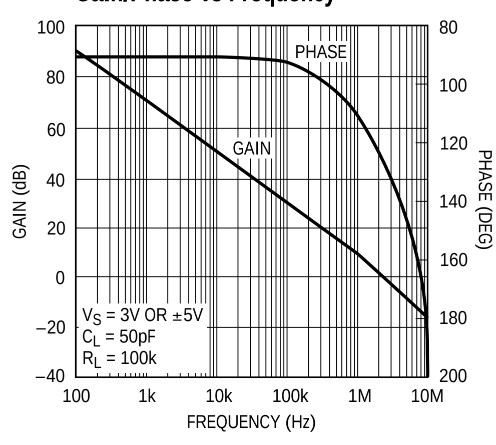
Output Swing vs Load Resistance ±5V



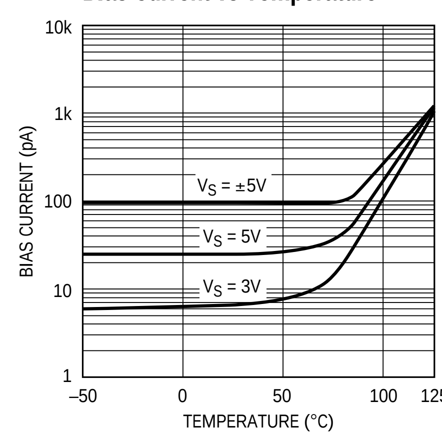
Output Swing vs Output Current, ±5V Supply



Gain/Phase vs Frequency

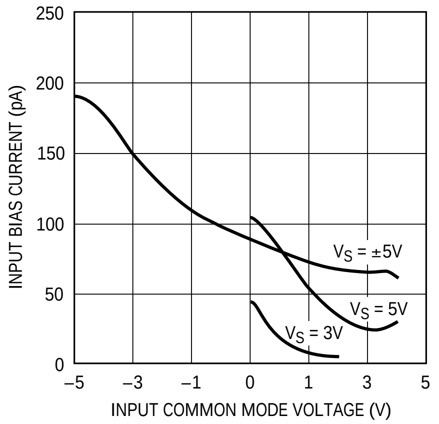


Bias Current vs Temperature

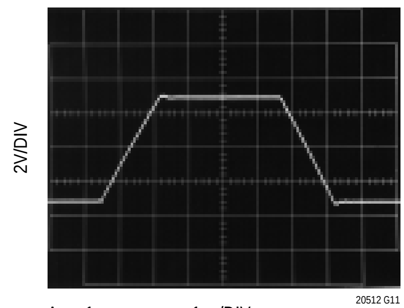


TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Input Common Mode Voltage

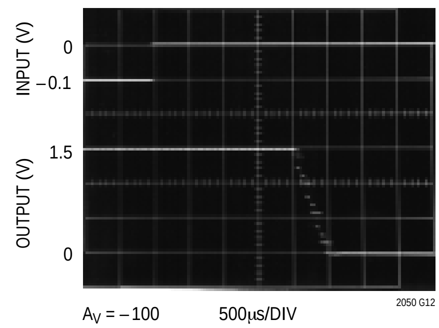


Transient Response



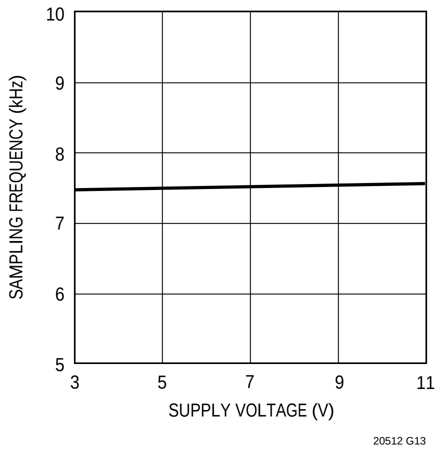
A_V = 1 1µs/DIV
R_L = 10k
C_L = 100pF
V_S = ±5V

Input Overload Recovery

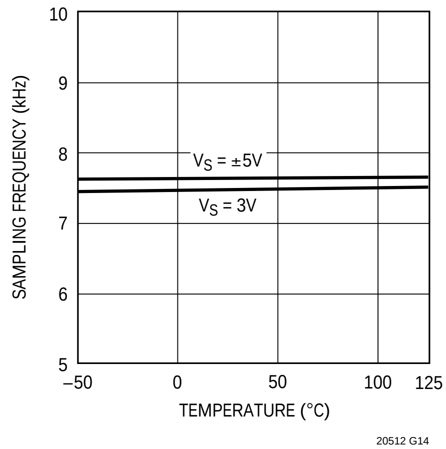


A_V = –100 500µs/DIV
R_L = 100k
C_L = 10pF
V_S = 3V

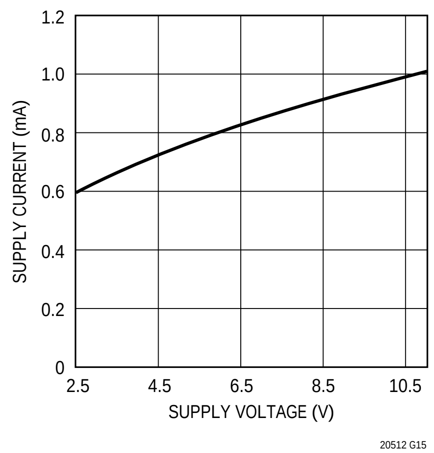
Sampling Frequency vs Supply Voltage



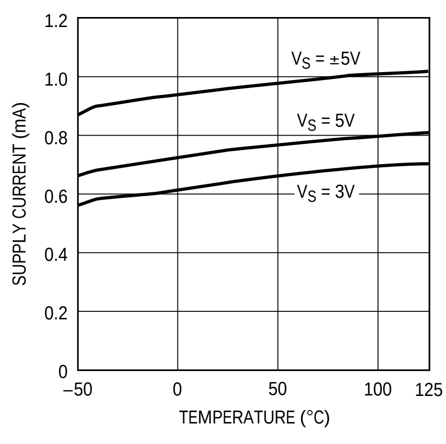
Sampling Frequency vs Temperature



Supply Current (Per Amplifier) vs Supply Voltage



Supply Current (Per Amplifier) vs Temperature



APPLICATIONS INFORMATION

Shutdown

The LTC2051 includes a shutdown pin in the 10-lead MSOP. When this active low pin is high or allowed to float, the device operates normally. When the shutdown pin is pulled low, the device enters shutdown mode; supply current drops to 3μA, all clocking stops and the output assumes a high impedance state.

Clock Feedthrough, Input Bias Current

The LTC2051/LTC2052 use autozeroing circuitry to achieve an almost zero DC offset over temperature, common mode voltage and power supply voltage. The frequency of the clock used for autozeroing is typically 7.5kHz. The term clock feedthrough is broadly used to indicate visibility of this clock frequency in the op amp output spectrum. There are typically two types of clock feedthrough in autozeroed op amps like the LTC2051/LTC2052.

The first form of clock feedthough is caused by the settling of the internal sampling capacitor and is input referred; that is, it is multiplied by the closed-loop gain of the op amp. This form of clock feedthrough is independent of the magnitude of the input source resistance or the magnitude of the gain setting resistors. The LTC2051/LTC2052 have a residue clock feedthrough of less than $1\mu V_{RMS}$ input referred at 7.5kHz.

The second form of clock feedthrough is caused by the small amount of charge injection occurring during the sampling and holding of the op amps input offset voltage. The current spikes are multiplied by the impedance seen at the input terminals of the op amp, appearing at the output multiplied by the closed-loop gain of the op amp. To reduce this form of clock feedthrough, use smaller valued gain setting resistors and minimize the source resistance at the input. If the resistance seen at the inputs is less than 10k, this form of clock feedthrough is less than $1\mu V_{RMS}$ input referred at 7.5kHz, or less than the amount of residue clock feedthrough from the first form previously described.

Placing a capacitor across the feedback resistor reduces either form of clock feedthrough by limiting the bandwidth of the closed-loop gain.

Input bias current is defined as the DC current into the input pins of the op amp. The same current spikes that cause the second form of clock feedthrough previously described, when averaged, dominate the DC input bias current of the op amp below 70°C.

At temperatures above 70°C, the leakage of the ESD protection diodes on the inputs increase the input bias currents of both inputs in the positive direction, while the current caused by the charge injection stays relatively constant. At elevated temperatures (above 85°C) the leakage current begins to dominate and both the negative and positive pin's input bias currents are in the positive direction (into the pins).

Input Pins, ESD Sensitivity

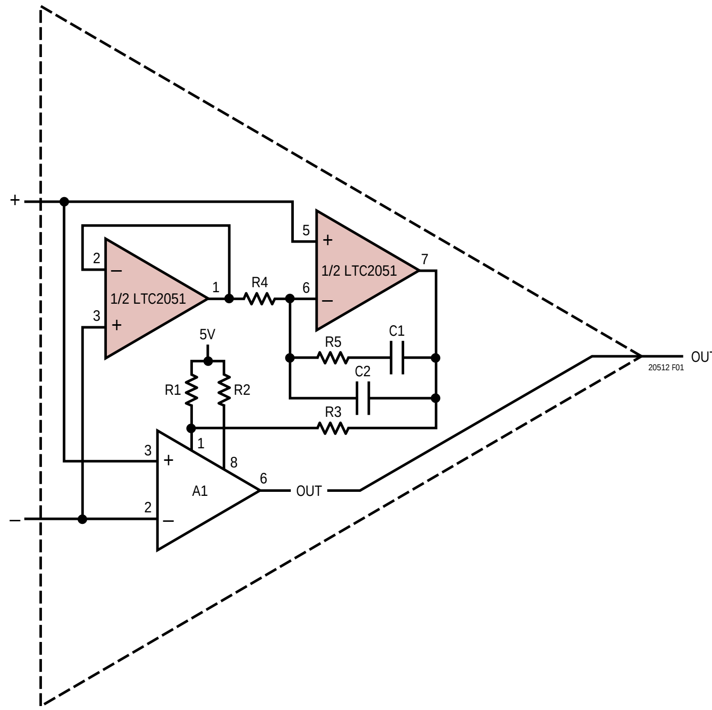
ESD voltages above 700V on the input pins of the op amp will cause the input bias currents to increase (more DC current into the pins). At these voltages, it is possible to damage the device to a point where the input bias current exceeds the maximums specified in this data sheet.

TYPICAL APPLICATION

The dual chopper op amp buffers the inputs of A1 and corrects its offset voltage and offset voltage drift. With the RC values shown, the power-up warm-up time is typically 20 seconds. The step response of the composite amplifier does not present settling tails. The LT®1677 should be used when extremely low noise, V_{OS} and V_{OS} drift are needed and the input source resistance is low. (For instance a 350Ω strain gauge bridge.) The LT1012 or equivalent should be used when low bias current (100pA) is also required in conjunction with DC to 10Hz low noise, low V_{OS} and V_{OS} drift. The measured typical input offset voltages are less than 1μV.

TYPICAL APPLICATION

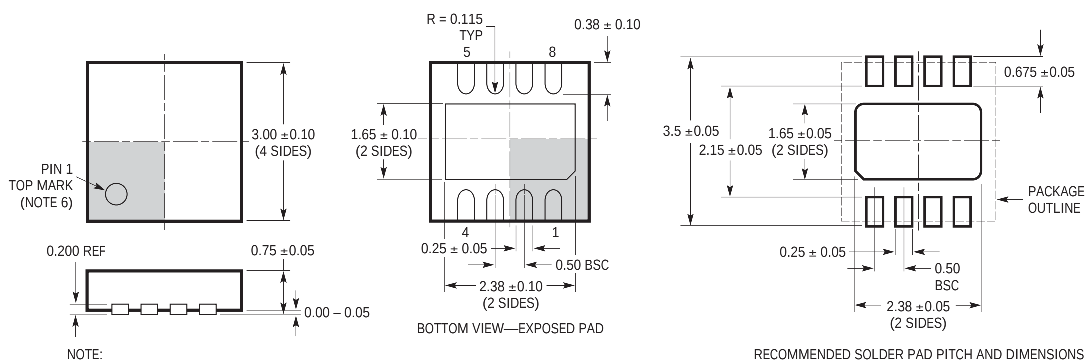
Obtaining Ultralow V_{OS} Drift and Low Noise



A1	R1	R2	R3	R4	R5	C1	C2	$\bar{e}_{IN}$ (DC – 1Hz)	$\bar{e}_{IN}$ (DC – 10Hz)
LT1677	2.49k	3.01k	340k	10k	100k	0.01µF	0.001µF	0.15µV$_{P-P}$	0.2µV$_{P-P}$
LT1012	750Ω	57Ω	250k	10k	100k	0.01µF	0.001µF	0.3µV$_{P-P}$	0.4µV$_{P-P}$

PACKAGE DESCRIPTION

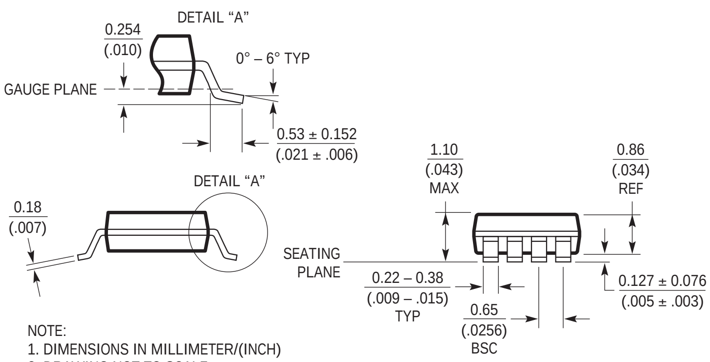
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)

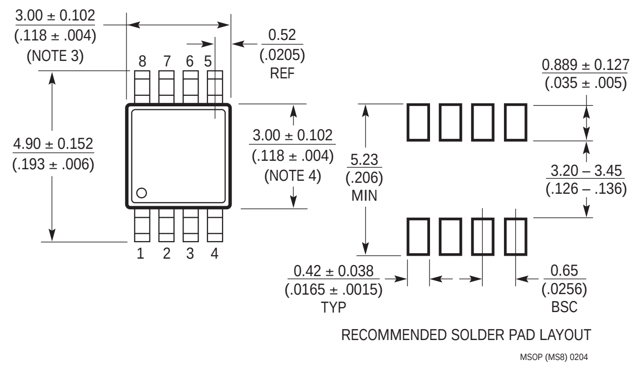


NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

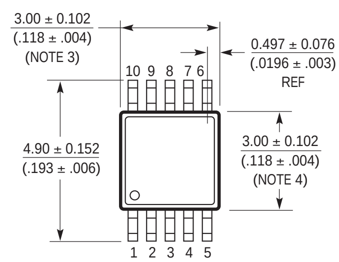
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)

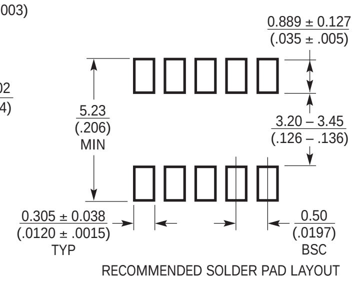


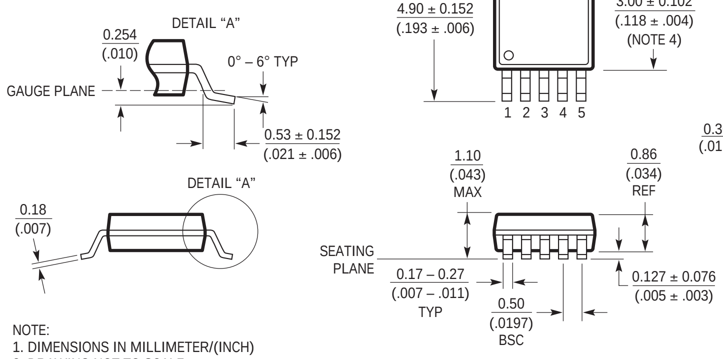


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



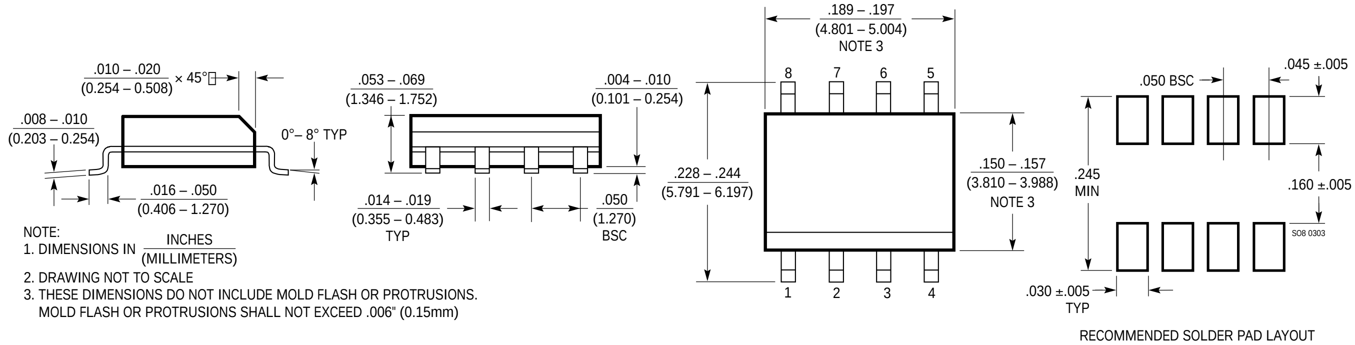




NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

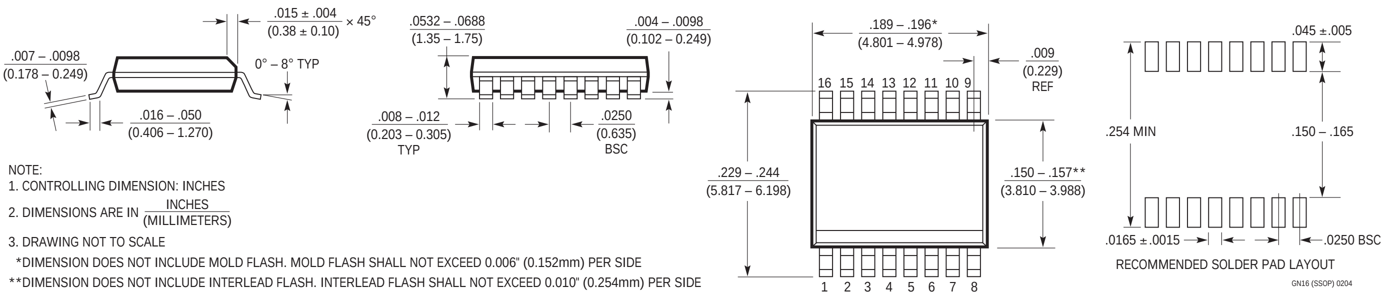
PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



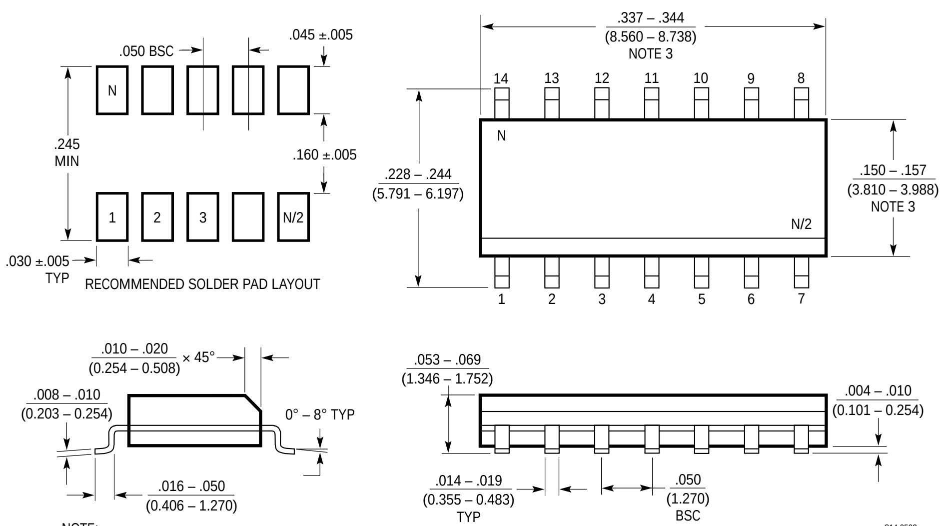
NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN INCHES / (MILLIMETERS)
3. DRAWING NOT TO SCALE
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

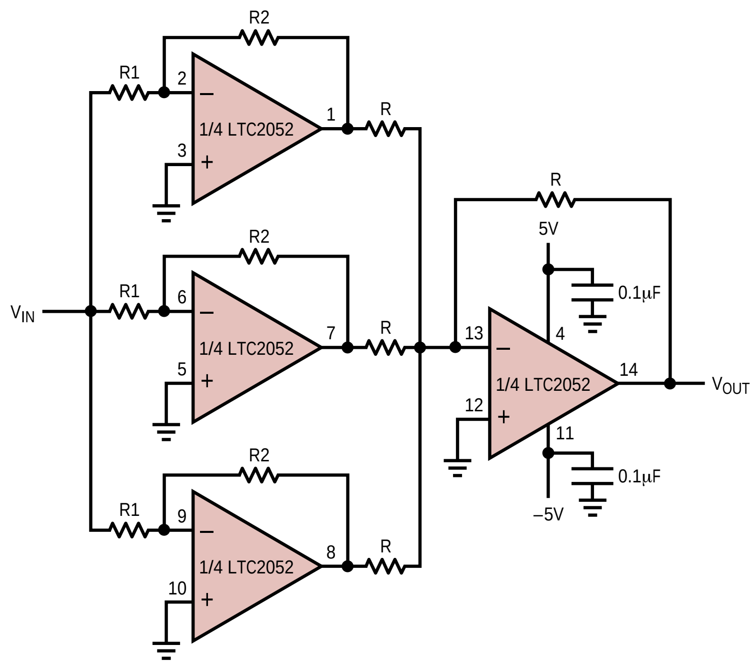
S Package
14-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

TYPICAL APPLICATION

Paralleling Amplifiers to Improve Noise



$$\frac{V_{OUT}}{V_{IN}} = 3\,\frac{R2}{R1}\text{; INPUT DC – 10Hz NOISE} \cong 0.8\mu V_{P\text{-}P} = \frac{\text{NOISE OF EACH PARALLEL OP AMP}}{\sqrt{3}}$$

20512 F02

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1051/LTC1053	Precision Zero-Drift Op Amp	Dual/Quad
LTC1151	±15V Zero-Drift Op Amp	Dual High Voltage Operation ±18V
LTC1152	Rail-to-Rail Input and Output Zero-Drift Op Amp	Single Zero-Drift Op Amp with Rail-to-Rail Input and Output and Shutdown
LTC2050	Zero-Drift Op Amp in SOT-23	Single Supply Operation 2.7V to ±5V, Shutdown
LTC2053	Zero-Drift Precision Instrumentation Amp	MS8, 116dB CMRR, Two External Resistors Set Gain
LTC6800	Rail-to-Rail Input and Output Instrumentation Amp	Low Cost, MS8, Two External Resistors Set Gain

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