LTC3330

Energy Harvesting DC/DC with Battery Backup

FEATURES

- **Dual Input, Single Output DC/DC's with Input Prioritizer**
  - **Energy Harvesting Input: 3.0V to 18V Buck DC/DC**
  - **Primary Cell Input: 1.8V to 5.5V Buck-Boost DC/DC**
- **Zero Battery I_Q When Powering Load from Harvested Energy**
- **Ultralow Quiescent Current: 900nA at No-Load**
- **Low Noise LDO Post Regulator**
- Integrated Supercapacitor Balancer
- Up to 50mA of Output Current
- Programmable DC/DC and LDO Output Voltages, Buck UVLO, and Buck-Boost Peak Input Current
- Integrated Low Loss Full-Wave Bridge Rectifier
- Input Protective Shunt–Up to 25mA at $V_{IN} \geq 20V$
- 5mm × 5mm QFN-32 Package

APPLICATIONS

- Energy Harvesting
- Solar Powered Systems with Primary Cell Backup
- Wireless HVAC Sensors and Security Devices
- Mobile Asset Tracking

DESCRIPTION

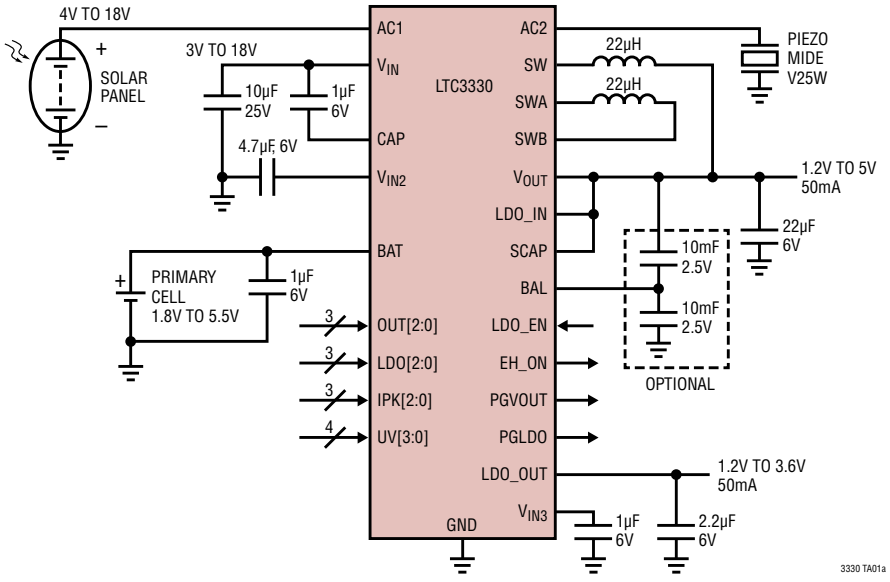
The LTC®3330 integrates a high voltage energy harvesting power supply plus a DC/DC converter powered by a primary cell battery to create a single output supply for alternative energy applications. The energy harvesting power supply, consisting of an integrated full-wave bridge rectifier and a high voltage buck converter, harvests energy from piezoelectric, solar, or magnetic sources. The primary cell input powers a buck-boost converter capable of operation down to 1.8V at its input. Either DC/DC converter can deliver energy to a single output. The buck operates when harvested energy is available, reducing the quiescent current draw on the battery to essentially zero. The buck-boost takes over when harvested energy goes away.

A low noise LDO post regulator and a supercapacitor balancer are also integrated, accommodating a wide range of output storage configurations.

Voltage and current settings for both inputs and outputs are programmable via pin-strapped logic inputs.

The LTC3330 is available in a 5mm × 5mm QFN-32 package.

TYPICAL APPLICATION



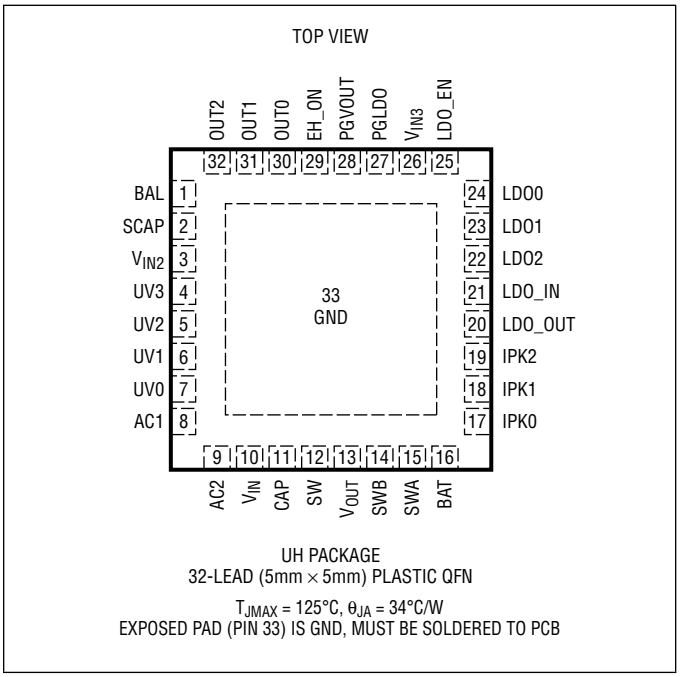
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}
Low Impedance Source .....–0.3 to 18V*
Current-Fed, I_{SW} = 0A.....25mA
AC1, AC2.....0 to V_{IN}
BAT, V_{OUT}, V_{IN3}, LDO_IN, SCAP, PGVOUT, PGLDO, EH_ON.....–0.3 to 6V
V_{IN2}.....–0.3V to [Lesser of (V_{IN} + 0.3V) or 6V]
CAP..... [Higher of –0.3V or (V_{IN} – 6V)] to V_{IN}
LDO_OUT, LDO[2:0], LDO_EN..–0.3V to LDO_IN + 0.3V
BAL.....–0.3V to SCAP + 0.3V
OUT[2:0]..... –0.3V to [Lesser of (V_{IN3} + 0.3V) or 6V]
IPK[2:0] ..... –0.3V to [Lesser of (V_{IN3} + 0.3V) or 6V]
UV[3:0] ..... –0.3V to [Lesser of (V_{IN2} + 0.3V) or 6V]
I_{AC1}, I_{AC2}.....±50mA
I_{SW}, I_{SWA}, I_{SWB}, I_{VOUT}.....350mA
I_{LDO_OUT}.....50mA
Operating Junction Temperature Range
(Notes 2, 3).....–40°C to 125°C
Storage Temperature Range .....–65°C to 125°C

*V_{IN} has an internal 20V clamp

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 33) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3330EUH#PBF	LTC3330EUH#TRPBF	3330	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LTC3330IUH#PBF	LTC3330IUH#TRPBF	3330	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 5V, BAT = 3.6V, SCAP = 0V, LDO_IN = 0V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Buck Input Voltage Range		●	3.0		18	V
V_{BAT}	Buck-Boost Input Voltage Range		●	1.8		5.5	V
I_{VIN}	V_{IN} Quiescent Current						
	V_{IN} Input in UVLO	V_{IN} = 2.5V, BAT = 0V			450	700	nA
	Buck Enabled, Sleeping	V_{IN} = 4V, BAT = 0V			1150	1800	nA
	Buck Enabled, Sleeping	V_{IN} = 18V, BAT = 0V			1650	2500	nA
	Buck Enabled, Not Sleeping	V_{IN} = 5V, BAT = 0V, I_{SW1} = 0A (Note 4)			150	250	µA
I_{BAT}	BAT Quiescent Current						
	BAT Input with V_{IN} Active	BAT = 1.8V, V_{IN} = 5V				10	nA
	Buck-Boost Enabled, Sleeping	BAT = 5V, V_{IN} = 0V			900	1500	nA
	Buck-Boost Enabled, Not Sleeping	BAT = 5V, V_{IN} = 0V, I_{SWA} = I_{SWB} = 0A (Note 4)			200	330	µA
V_{LDO_IN}	LDO_IN Input Range		●	1.8V		5.5V	
I_{LDO_IN}	LDO_IN Quiescent Current	LDO_IN = 5.0V, I_{LDO_OUT} = 0A			400	600	nA
I_{LDO_OUT}	LDO_OUT Leakage Current	LDO_IN = 5.0V, LDO_OUT = 5.0V			125		nA
LDO_OUT	Regulated LDO Output Voltage	Error as a Percentage of Target	●	–2.0		2.0	%
	LDO Line Regulation (1.8V to 5.5V)	LDO_OUT = 1.2V, 10mA Load			2		mV/V
	LDO Load Regulation (10µA to 10mA)	LDO_IN = 5.0V, LDO_OUT = 3.3V			2		mV/mA
	LDO Dropout Voltage	LDO_OUT = 3.3V, 10mA LOAD			90		mV
	LDO Current Limit	LDO_IN = 5.0V		50			mA
I_{VOUT}	V_{OUT} Leakage Current	V_{OUT} = 5.0V			125		nA
I_{SCAP}	Supercapacitor Balancer Quiescent Current	SCAP = 5.0V			165	250	nA
I_{SOURCE}	Supercapacitor Balancer Source Current	SCAP = 5.0V, BAL = 2.4V		10			mA
I_{SINK}	Supercapacitor Balancer Sink Current	SCAP = 5.0V, BAL = 2.6V		10			mA
V_{BAL}	Supercapacitor Balance Point	Percentage of SCAP Voltage	●	49	50	51	%
V_{INUVLO}	V_{IN} Undervoltage Lockout Thresholds (Rising or Falling)	3V Level	●	2.85	3.00	3.15	V
		4V Level	●	3.80	4.00	4.20	V
		5V Level	●	4.75	5.00	5.25	V
		6V Level	●	5.70	6.00	6.30	V
		7V Level	●	6.65	7.00	7.35	V
		8V Level	●	7.60	8.00	8.40	V
		9V Level	●	8.55	9.00	9.45	V
		10V Level	●	9.50	10.0	10.5	V
		11V Level	●	10.4	11.0	11.6	V
		12V Level	●	11.4	12.0	12.6	V
		13V Level	●	12.3	13.0	13.7	V
		14V Level	●	13.3	14.0	14.7	V
		15V Level	●	14.2	15.0	15.8	V
		16V Level	●	15.2	16.0	16.8	V
		17V Level	●	16.1	17.0	17.9	V
		18V Level	●	17.1	18.0	18.9	V
V_{SHUNT}	V_{IN} Shunt Regulator Voltage	I_{VIN} = 1mA		19.0	20.0	21.0	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SHUNT}	Maximum Protective Shunt Current			25			mA
	Internal Bridge Rectifier Loss ($\|V_{AC1} - V_{AC2}\| - V_{IN}$)	I_{BRIDGE} = 10µA I_{BRIDGE} = 50mA		700 1400	800 1500	900 1600	mV mV
	Internal Bridge Rectifier Reverse Leakage Current	$V_{REVERSE}$ = 18V				20	nA
	Internal Bridge Rectifier Reverse Breakdown Voltage	$I_{REVERSE}$ = 1µA		V_{SHUNT}	30		V
V_{OUT}	Regulated Buck/Buck-Boost Output Voltage	1.8V Output Selected Sleep Threshold Wakeup Threshold	 ● ●	 TBD	 1.806 1.794	 TBD 	 V V
		2.5V Output Selected Sleep Threshold Wakeup Threshold	 ● ●	 TBD	 2.508 2.492	 TBD 	 V V
		2.8V Output Selected Sleep Threshold Wakeup Threshold	 ● ●	 TBD	 2.809 2.791	 TBD 	 V V
		3.0V Output Selected Sleep Threshold Wakeup Threshold	 ● ●	 TBD	 3.010 2.990	 TBD 	 V V
		3.3V Output Selected Sleep Threshold Wakeup Threshold	 ● ●	 TBD	 3.311 3.289	 TBD 	 V V
		3.6V Output Selected Sleep Threshold Wakeup Threshold	 ● ●	 TBD	 3.612 3.588	 TBD 	 V V
		4.5V Output Selected Sleep Threshold Wakeup Threshold	 ● ●	 TBD	 4.515 4.485	 TBD 	 V V
		5.0V Output Selected Sleep Threshold Wakeup Threshold	 ● ●	 TBD	 5.017 4.983	 TBD 	 V V
I_{PEAK_BUCK}	Buck Peak Switch Current			200	250	350	mA
I_{BUCK}	Available Buck Output Current		●	100			mA
I_{IPEAK_BB}	Buck-Boost Peak Switch Current	250mA Target Selected			250	350	mA
		150mA Target Selected			150	TBD	mA
		100mA Target Selected			100	TBD	mA
		50mA Target Selected			50	TBD	mA
		25mA Target Selected			25	TBD	mA
		15mA Target Selected			15	TBD	mA
		10mA Target Selected			10	TBD	mA
		5mA Target Selected			5	TBD	mA
I_{BB}	Available Buck-Boost Current	I_{IPEAK_BB} = 250mA, BAT = 1.8V, V_{OUT} = 3.3V	●	50			mA
R_{P_BUCK}	Buck PMOS Switch On-Resistance				1.1		Ω
R_{N_BUCK}	Buck NMOS Switch On-Resistance				1.3		Ω
R_{P_BB}	Buck-Boost PMOS Switch On-Resistance	Input and Output Switches			0.5		Ω
R_{N_BB}	Buck-Boost NMOS Switch On-Resistance	Input and Output Switches			0.5		Ω
R_{P_LDO}	LDO PMOS Switch On-Resistance	LDO_IN = 2.5V, I_{LDO_OUT} = 50mA			7		Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 5V, BAT = 3.6V, SCAP = 0V, LDO_IN = 0V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{LEAK(P)}$	PMOS Switch Leakage	Buck/Buck-Boost Regulators		–20		20	nA
$I_{LEAK(N)}$	NMOS Switch Leakage	Buck/Buck-Boost Regulators		–20		20	nA
	Maximum Buck Duty Cycle	Buck/Buck-Boost Regulators	●	100			%
	PGVOUT Threshold	As a Percentage of V_{OUT} Target	●	90	92.5	95	%
	PGLDO Threshold	As a Percentage of LDO_OUT Target	●	90	92.5	95	%
V_{IH}	Digital Input High Voltage	Pins LDO_EN, OUT[2:0], LDO[2:0], IPK[2:0], UV[3:0]	●	1.2			V
V_{IL}	Digital Input Low Voltage	Pins LDO_EN, OUT[2:0], LDO[2:0], IPK[2:0], UV[3:0]	●			0.4	V
I_{IH}	Digital Input High Current	Pins LDO_EN, OUT[2:0], LDO[2:0], IPK[2:0], UV[3:0]			0	10	nA
I_{IL}	Digital Input Low Current	Pins LDO_EN, OUT[2:0], LDO[2:0], IPK[2:0], UV[3:0]			0	10	nA
V_{OH}	PGVOUT, PGLDO, EH_ON Output High Voltage	V_{IN3} = 5V, 10µA Out of Pin	●	4.6			V
V_{OL}	PGVOUT, PGLDO, EH_ON Output Low Voltage	V_{IN3} = 5V, 10µA into Pin	●			0.4	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

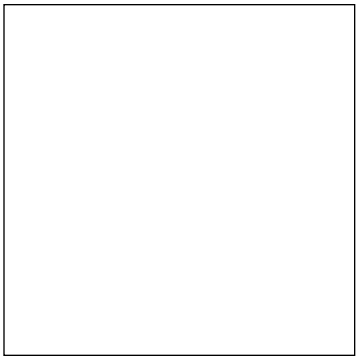
Note 2: The LTC3330E is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3330E is guaranteed to meet specifications from 0°C to 85°C. The LTC3330I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient T_A and power dissipation PD according to the following formula: $T_J = T_A + (P_D \bullet \theta_{JA})$.

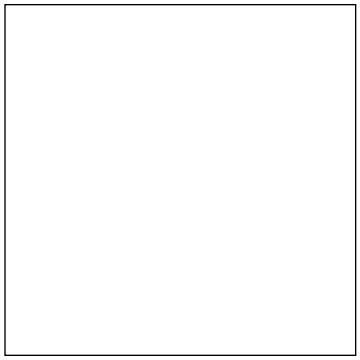
Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

TYPICAL PERFORMANCE CHARACTERISTICS

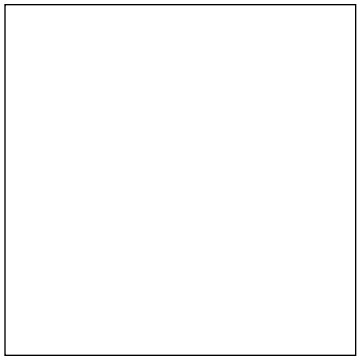
I_{VIN} in UVLO vs V_{IN}



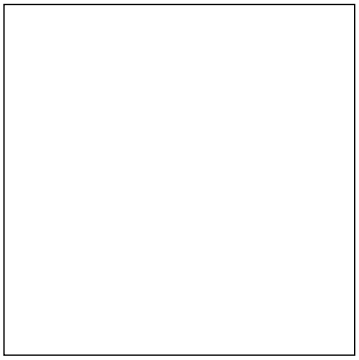
I_{VIN} in Sleep vs V_{IN}



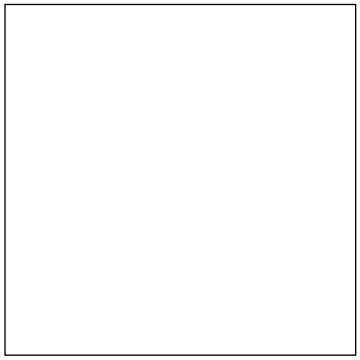
I_{BAT} in Sleep vs BAT



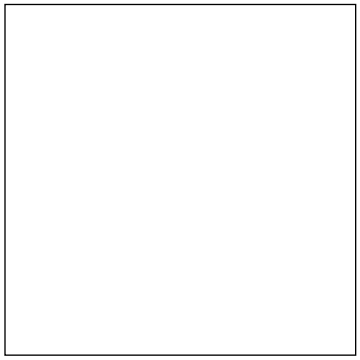
UVLO Rising vs Temperature



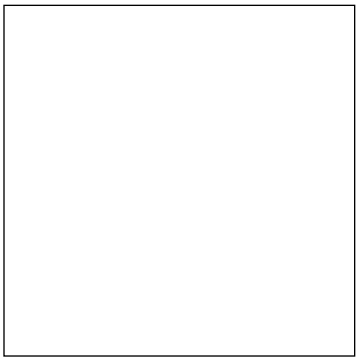
UVLO Falling vs Temperature



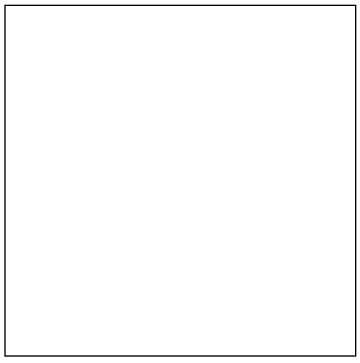
V_{SHUNT} vs Temperature



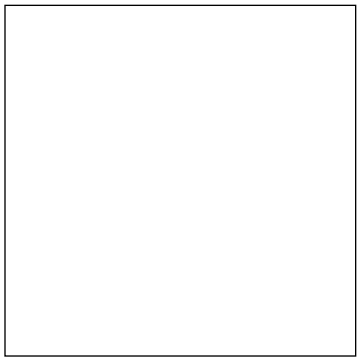
Total Bridge Rectifier Drop vs Bridge Current



Bridge Leakage vs Temperature

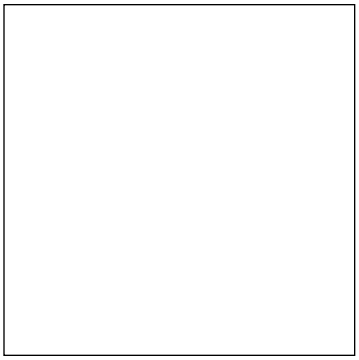


Bridge Frequency Response

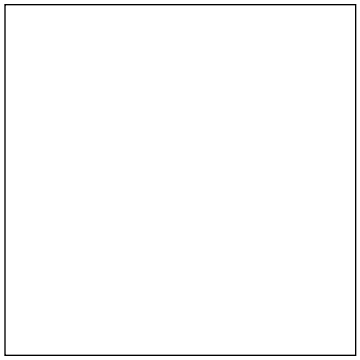


TYPICAL PERFORMANCE CHARACTERISTICS

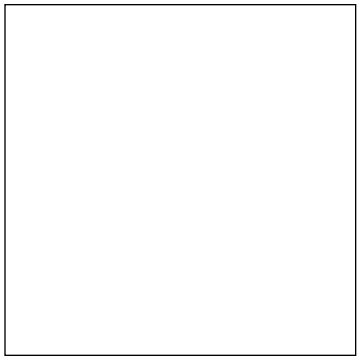
V_{OUT} vs Temperature (1.8V, 2.5V, 2.8V, 3.0V)



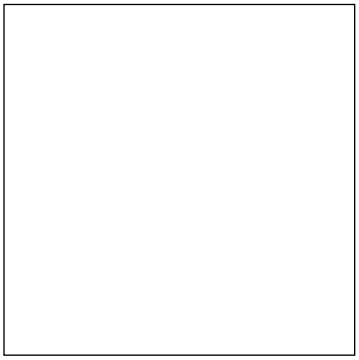
V_{OUT} vs Temperature (3.3V, 3.6V, 4.5V, 5.0V)



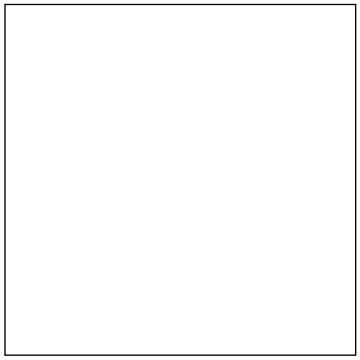
I_{VOUT} vs Temperature



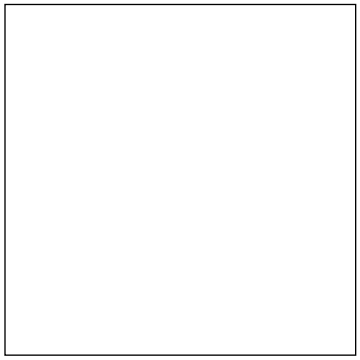
V_{OUT} Load Regulation Buck/Buck-Boost



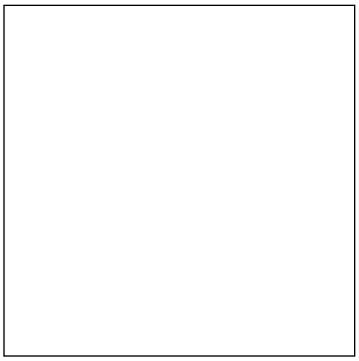
V_{OUT} Line Regulation Buck/Buck-Boost



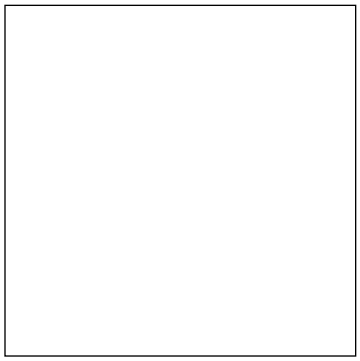
$I_{PEAK-BUCK}$ vs Temperature



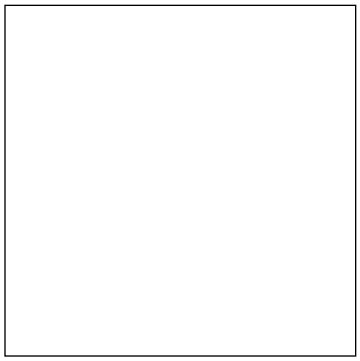
$R_{DS(ON)}$ of Buck PMOS/NMOS vs Temperature



I_{PEAK_BB} vs Temperature (250mA, 150mA, 100mA, 50mA)

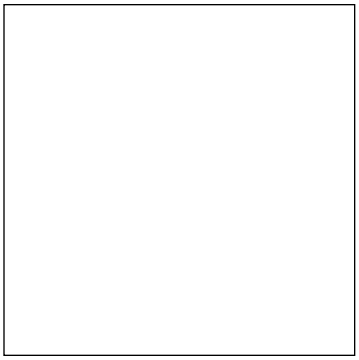


I_{PEAK_BB} vs Temperature (25mA, 15mA, 10mA, 5mA)

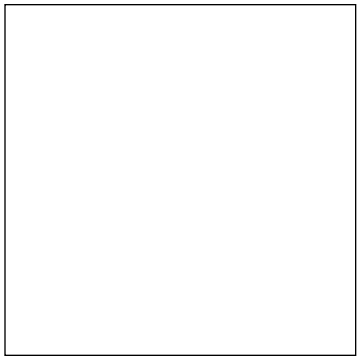


TYPICAL PERFORMANCE CHARACTERISTICS

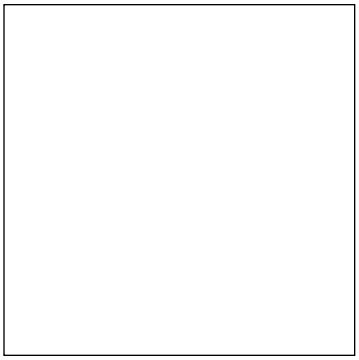
$R_{DS(ON)}$ of Buck-Boost PMOS/ NMOS vs Temperature



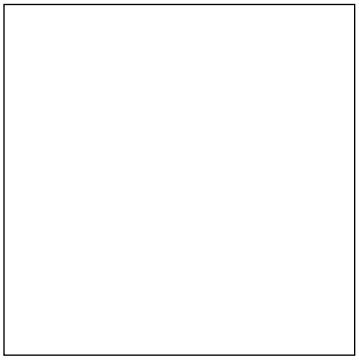
Buck Switching Waveforms



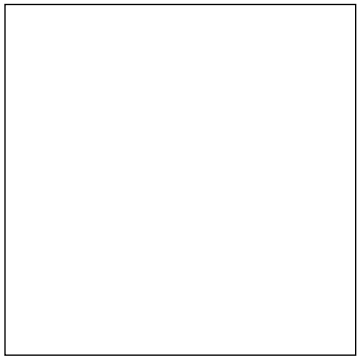
Buck-Boost Switching Waveforms



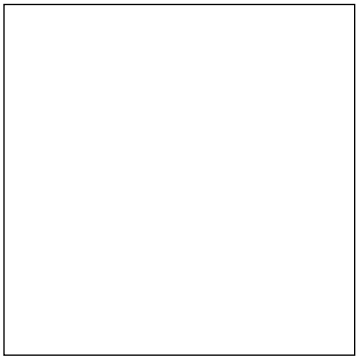
Buck Efficiency vs I_{LOAD}



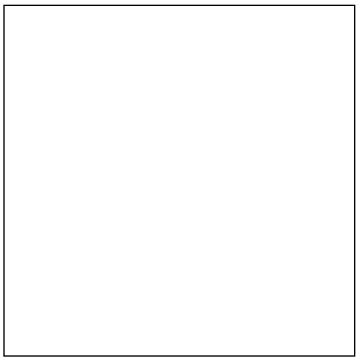
Buck-Boost Efficiency vs I_{LOAD}



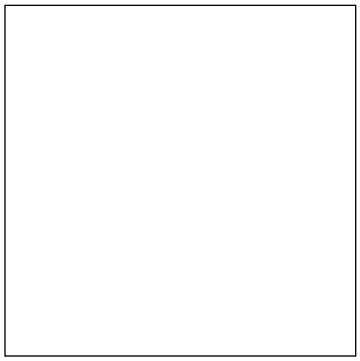
Prioritizer Buck-Boost to Buck Transition



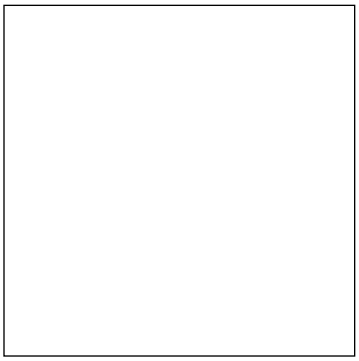
Prioritizer Buck to Buck-Boost Transition



I_{SCAP} vs SCAP

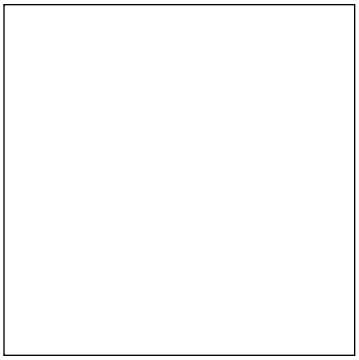


Supercapacitor Balancer Source/ Sink Current

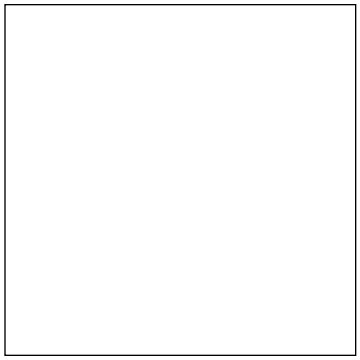


TYPICAL PERFORMANCE CHARACTERISTICS

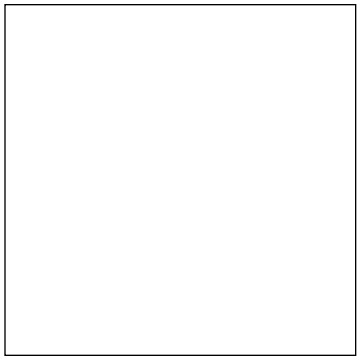
I_{LDO_IN} vs LDO_IN



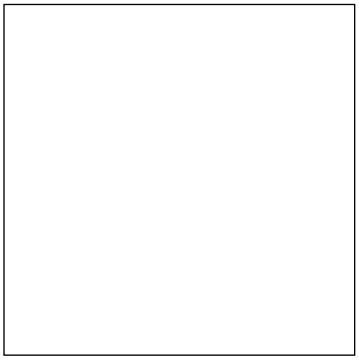
LDO_OUT vs Temperature



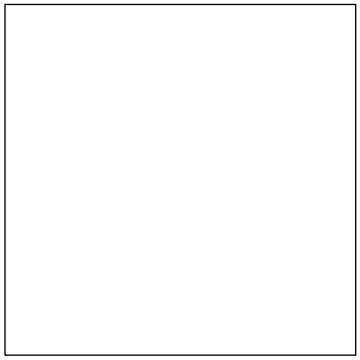
LDO Load Step



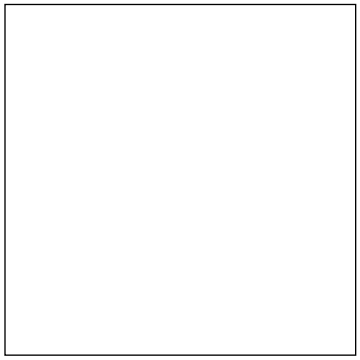
LDO Load Regulation



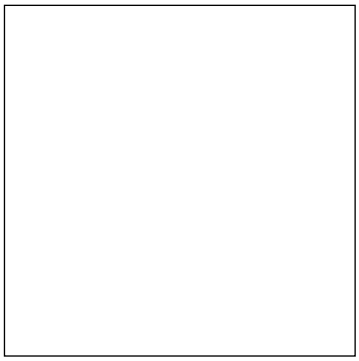
LDO Line Regulation



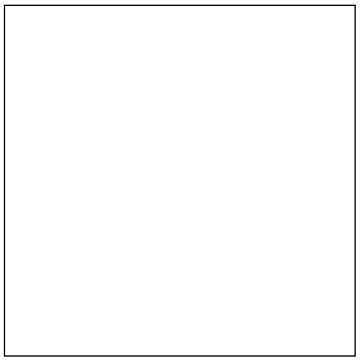
LDO Current Limit



$R_{DS(ON)}$ of LDO PMOS



LDO Start-Up



PIN FUNCTIONS

BAL (Pin 1): Supercapacitor Balance Point. The common node of a stack of two supercapacitors is connected to BAL. A source/sink balancing current of up to 10mA is available. Tie BAL along with SCAP to GND to disable the balancer and its associated quiescent current.

SCAP (Pin 2): Supply and Sense Point for Supercapacitor Balancer. Tie the top of a 2-capacitor stack to SCAP and the middle of the stack to BAL to activate balancing. Tie SCAP along with BAL to GND to disable the balancer and its associated quiescent current.

V_{IN2} (Pin 3): Internal Low Voltage Rail to Serve as Gate Drive for Buck NMOS Switch. Connect a 4.7µF (or larger) capacitor from V_{IN2} to GND. This pin is not intended for use as an external system rail.

UV3, UV2, UV1, UV0 (Pins 4, 5, 6, 7): UVLO Select Bits for the Buck Switching Regulator. Tie high to V_{IN2} or low to GND to select the desired UVLO rising and falling thresholds (see Table 4). Do not float.

AC1 (Pin 8): Input Connection for Piezoelectric Element or Other AC Source (used in conjunction with AC2 for differential AC inputs).

AC2 (Pin 9): Input Connection for Piezoelectric Element or Other AC Source (used in conjunction with AC1 for differential AC inputs).

V_{IN} (Pin 10): Rectified Input Voltage. A capacitor on this pin serves as an energy reservoir and input supply for the buck regulator. The V_{IN} voltage is internally clamped to a maximum of 20V (typical).

CAP (Pin 11): Internal Rail Referenced to V_{IN} to Serve as Gate Drive for Buck PMOS Switch. Connect a 1µF (or larger) capacitor between CAP and V_{IN}. This pin is not intended for use as an external system rail.

SW (Pin 12): Switch Node for the Buck Switching Regulator. Connect a 22µH or greater external inductor between this node and V_{OUT}.

V_{OUT} (Pin 13): Regulated Output Voltage Derived from the Buck or Buck-Boost Switching Regulator.

SWB (Pin 14): Switch Node for the Buck-Boost Switching Regulator. Connect an external inductor between this node and SWA of value per Table 3.

SWA (Pin 15): Switch Node for the Buck-Boost Switching Regulator. Connect an external inductor between this node and SWB of value per Table 3.

BAT (Pin 16): Input for Battery. BAT serves as the input to the buck-boost switching regulator.

IPK0, IPK1, IPK2 (Pins 17, 18, 19): IPEAK Select Bits for the Buck-Boost Switching Regulator. Tie high to V_{IN3} or low to GND to select the desired IPEAK (see Table 3). Do not float.

LDO_OUT (Pin 20): Regulated LDO Output. This output can be used as a quiet supply. One mode is provided to run the LDO as a current limited switch to alternately power up and power down circuitry without low power modes.

LDO_IN (Pin 21): Input Voltage for the LDO regulator.

LDO2, LDO1, LDO0 (Pins 22, 23, 24): LDO Voltage Select Bits. Tie high to LDO_IN or low to GND to select the desired LDO_OUT voltage (see Table 2). Do not float.

LDO_EN (Pin 25): LDO Enable Input. Active high input with logic levels referenced to LDO_IN. Do not float.

V_{IN3} (Pin 26): Internal Low Voltage Rail Used by the Prioritizer. Connect a 1µF (or larger) capacitor from V_{IN3} to GND. This pin is not intended for use as an external system rail.

PGLDO (Pin 27): Power Good Output for LDO_OUT. Logic level output referenced to an internal maximum rail (see Operation). PGLDO transitioning high indicates 92.5% (typical) regulation has been reached on LDO_OUT. PGLDO remains high until LDO_OUT falls to 90.0% (typical) of the programmed regulation point.

PGVOUT (Pin 28): Power Good Output for V_{OUT}. Logic level output referenced to an internal maximum rail (see Operation). PGVOUT transitioning high indicates regulation has been reached on V_{OUT} (V_{OUT} = Sleep Rising). PGVOUT remains high until V_{OUT} falls to 92.5% (typical) of the programmed regulation point.

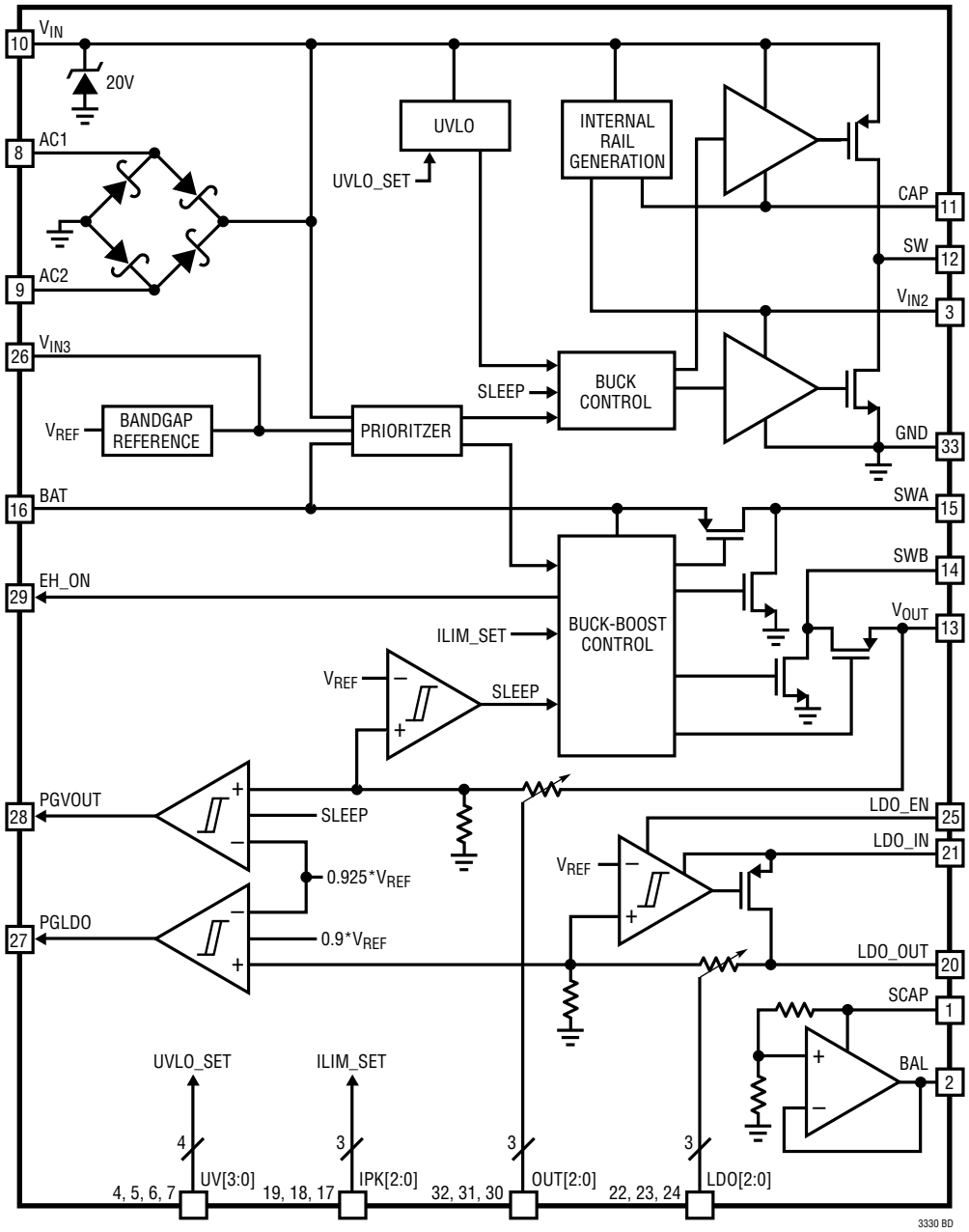
BAT_ON (Pin 29): Switcher Status. Logic level output referenced to V_{IN3}. EH_ON is high when the buck switching regulator is in use. It is pulled low when buck-boost switching regulator is in use.

PIN FUNCTIONS

OUT0, OUT1, OUT2 (Pins 30, 31, 32): V_{OUT} Voltage Select Bits. Tie high to V_{IN3} or low to GND to select the desired V_{OUT} (see Table 1). Do not float.

GND (Exposed Pad Pin 11): Ground. The exposed pad must be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3330.

BLOCK DIAGRAM



OPERATION

Modes of Operation

The following four tables detail all programmable settings on the LTC3330.

Table 1. Output Voltage Selection

OUT2	OUT1	OUT2	V_{OUT}
0	0	0	1.8V
0	0	1	2.5V
0	1	0	2.8V
0	1	1	3.0V
1	0	0	3.3V
1	0	1	3.6V
1	1	0	4.5V
1	1	1	5.0V

Table 2. LDO Voltage Selection

LDO2	LDO1	LDO0	LDO_OUT
0	0	0	1.2V
0	0	1	1.5V
0	1	0	1.8V
0	1	1	2.0V
1	0	0	2.5V
1	0	1	3.0V
1	1	0	3.3V
1	1	1	= LDO_IN

Table 3. I_{LIM} Selection

IPK_2	IPK_1	IPK_0	I_{LIM}	L_{MIN}
0	0	0	5mA	1100µH
0	0	1	10mA	560µH
0	1	0	15mA	360µH
0	1	1	25mA	220µH
1	0	0	50mA	110µH
1	0	1	100mA	56µH
1	1	0	150mA	36µH
1	1	1	250mA	22µH

Table 4. V_{IN} UVLO Threshold Selection

UV3	UV2	UV1	UV0	UVLO RISING	UVLO FALLING
0	0	0	0	4V	3V
0	0	0	1	5V	4V
0	0	1	0	6V	5V
0	0	1	1	7V	6V
0	1	0	0	8V	7V
0	1	0	1	8V	5V
0	1	1	0	10V	9V
0	1	1	1	10V	5V
1	0	0	0	12V	11V
1	0	0	1	12V	5V
1	0	1	0	14V	13V
1	0	1	1	14V	5V
1	1	0	0	16V	15V
1	1	0	1	16V	5V
1	1	1	0	18V	17V
1	1	1	1	18V	5V

OPERATION

OVERVIEW

The LTC3330 combines a buck switching regulator and a buck-boost switching regulator to produce an energy harvesting solution with battery backup. The converters are controlled by a prioritizer that selects which converter to use based on the availability of a battery and/or harvestable energy. If harvested energy is available the buck regulator is active and the buck-boost is OFF. With an optional LDO and supercapacitor balancer and an array of different configurations the LTC3330 suits many applications.

BUCK CONVERTER

The synchronous buck converter is an ultralow quiescent current power supply tailored to energy harvesting applications. It is designed to interface directly to a piezoelectric or alternative A/C power source, rectify the input voltage, and store harvested energy on an external capacitor while maintaining a regulated output voltage. It can also bleed off any excess input power via an internal shunt regulator.

INTERNAL BRIDGE RECTIFIER

An internal full-wave bridge rectifier accessible via the differential AC1 and AC2 inputs rectifies AC sources such as those from a piezoelectric element. The rectified output is stored on a capacitor at the V_{IN} pin and can be used as an energy reservoir for the buck converter. The bridge rectifier has a total drop of about 800mV with typical piezo-generated currents (~10µA), but is capable of carrying up to 50mA. Either side of the bridge can be operated independently as single-ended AC or DC inputs.

UNDERVOLTAGE LOCKOUT

When the voltage on V_{IN} rises above the UVLO rising threshold the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor. When the input capacitor voltage is depleted below the UVLO falling threshold the buck converter is disabled. These thresholds can be set according to Table 4 which offers UVLO rising thresholds from 4V to 18V with large or small hysteresis windows (see Table 4). Extremely low quiescent current (450nA typical) in UVLO allows energy to accumulate on the input capacitor in situations where energy must be harvested from low power sources.

INTERNAL RAIL GENERATION

Two internal rails, CAP and V_{IN2}, are generated from V_{IN} and are used to drive the high side PMOS and low side NMOS of the buck converter, respectively. Additionally the V_{IN2} rail serves as logic high for the UVLO threshold select bits UV[3:0]. The V_{IN2} rail is regulated at 4.8V above GND while the CAP rail is regulated at 4.8V below V_{IN}. These are not intended to be used as external rails. Bypass capacitors are connected to the CAP and V_{IN2} pins to serve as energy reservoirs for driving the buck switches. When V_{IN} is below 4.8V, V_{IN2} is equal to V_{IN} and CAP is held at GND. Figure 1 shows the ideal V_{IN}, V_{IN2} and CAP relationship.

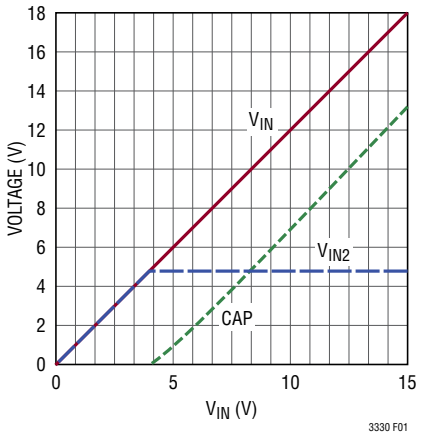


Figure 1. Ideal V_{IN}, V_{IN2} and CAP Relationship

BUCK OPERATION

The buck regulator uses a hysteretic voltage algorithm to control the output through internal feedback from the V_{OUT} sense pin. The buck converter charges an output capacitor through an inductor to a value slightly higher than the regulation point. It does this by ramping the inductor current up to 260mA through an internal PMOS switch and then ramping it down to 0mA through an internal NMOS switch. This efficiently delivers energy to the output capacitor. The ramp rate is determined by V_{IN},

OPERATION

V_{OUT}, and the inductor value. When the buck brings the output voltage into regulation the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During this operating mode load current is provided by the output capacitor. When the output voltage falls below the regulation point the buck regulator wakes up and the cycle repeats. This hysteretic method of providing a regulated output reduces losses associated with FET switching and maintains an output at light loads. The buck delivers a minimum of 100mA of average load current when it is switching. V_{OUT} can be set from 1.8V to 5V via OUT[2:0] (see Table 1).

When the sleep comparator signals that the output has reached the sleep threshold the buck converter may be in the middle of a cycle with current still flowing through the inductor. Normally both synchronous switches would turn off and the current in the inductor would freewheel to zero through the NMOS body diode, but the NMOS switch is kept on to prevent the conduction loss that would occur in the diode if the NMOS were off. If the PMOS is on when the sleep comparator trips the NMOS will turn on immediately in order to ramp down the current. If the NMOS is on it will be kept on until the current reaches zero.

Though the quiescent current when the buck is switching is much greater than the sleep quiescent current, it is still a small percentage of the average inductor current which results in high efficiency over most load conditions. The buck operates only when sufficient energy has been accumulated in the input capacitor and the length of time the converter needs to transfer energy to the output is much less than the time it takes to accumulate energy. Thus, the buck operating quiescent current is averaged over a long period of time so that the total average quiescent current is low. This feature accommodates sources that harvest small amounts of ambient energy.

BUCK-BOOST CONVERTER

The buck-boost uses the same hysteretic voltage algorithm as the buck to control the output, V_{OUT}, with the same sleep comparator. The buck-boost has three modes of operation: buck, buck-boost, and boost. An internal mode comparator determines the mode of operation based on BAT and V_{OUT}. Figure 2 shows the four internal switches of the buck-boost converter. In each mode the inductor current is ramped up to IPEAK. This IPEAK value is programmable via IPK[2:0] and ranges from 5mA to 250mA (see Table 3).

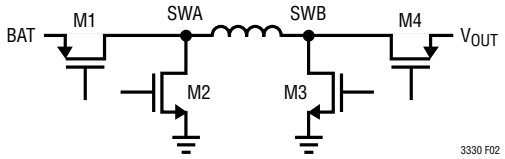


Figure 2: Buck-Boost Power Switches

In BUCK mode M4 is always on and M3 is always off. The inductor current is ramped up through M1 to IPEAK and down to 0mA through M2. In boost mode M1 is always on and M2 is always off. The inductor current is ramped up to IPEAK when M3 is on and is ramped to 0mA when M4 is on as V_{OUT} is greater than BAT in boost mode. Buck-boost mode is very similar to boost mode in that M1 is always on and M2 is always off. If BAT is less than V_{OUT} the inductor current is ramped up to IPEAK through M3. When M4 turns on the current in the inductor will start to ramp down. However, because BAT is close to V_{OUT} and M1 and M4 have finite on-resistance the current ramp will exhibit a slow exponential decay, lowering the average current delivered to V_{OUT}. For this reason the lower current threshold is set to IPEAK/2 in buck-boost mode to maintain high average current to the load. If BAT is greater than V_{OUT} in buck-boost mode the inductor current still ramps up to IPEAK and down to IPEAK/2. It can still ramp down If BAT is greater than V_{OUT} because the final value of the current in the inductor is $(V_{IN} – V_{OUT})/(R_{ON1} + R_{ON4})$. If BAT is exactly IPEAK/2•$(R_{ON1} + R_{ON4})$ above V_{OUT} the inductor current will not reach the IPEAK/2 threshold and switches M1 and M4 will stay on all the time. For higher BAT voltages the mode comparator will switch the converter to buck mode. M1 and M4 will remain on for BAT voltages up to V_{OUT} + IPEAK•$(R_{ON1} + R_{ON4})$. At

OPERATION

this point the current in the inductor is equal to IPEAK and the IPEAK comparator will trip turning off M1 and turning on M2 causing the inductor current to ramp down to IZERO, completing the transition from buck-boost mode to buck mode.

V_{OUT} Power Good

A power good comparator is provided for the V_{OUT} output. It transitions high the first time the LTC3330 goes to sleep, indicating that V_{OUT} has reached regulation. It transitions low when V_{OUT} falls to 92.5% (typical) of its value at regulation. The PGVOUT output is referenced to an internal rail that is generated to be the highest of V_{IN2}, BAT, and V_{OUT} less a Schottky diode drop.

Prioritizer

The input prioritizer on the LTC3330 decides whether to use the energy harvesting input or the battery input to power V_{OUT}. If a battery is powering the buck-boost converter and harvested energy causes a UVLO rising transition on V_{IN}, the prioritizer will shut off the buck-boost and turn on the buck, orchestrating a smooth transition that maintains regulation of V_{OUT}. When harvestable energy disappears, the prioritizer will first poll the battery voltage. If the battery voltage is above 1.8V the prioritizer will switch back to the buck-boost while maintaining regulation. If the battery voltage is below 1.8V the buck-boost is not enabled and V_{OUT} cannot be supported until harvestable energy is again available. If either BAT or V_{IN} is grounded, the prioritizer allows the other input to run if its input is high enough for operation.

When the prioritizer selects the V_{IN} input the current on the BAT input drops to zero. However, if the voltage on BAT is higher than V_{IN2}, 150nA (typical) will appear as quiescent current on BAT due to internal level shifting. This only affects a small range of battery voltages and UVLO settings.

A digital output, EH_ON, is low when the prioritizer has selected the BAT input and is high when the prioritizer has selected the V_{IN} input. The EH_ON output is referenced to V_{IN3}.

Low Drop Out Regulator

An integrated low drop out regulator (LDO) is available with its own input, LDO_IN. It will regulate LDO_OUT to seven different output voltages based on the LDO[2:0] pins. An eighth mode is provided to turn the LDO into a current-limited switch in which the PMOS is always on. LDO_EN enables the LDO when high and when low eliminates all quiescent current on LDO_IN. The LDO is designed to provide 50mA over a range of LDO_IN and LDO_OUT combinations. A current limit set above 50mA is available to dial back the current if the output is grounded or the load demands more than 50mA. The LDO also features a 1ms soft-start for smooth output start-up.

A power good signal on the PGLDO pin indicates when the voltage at LDO_OUT rises above 92.5% (typical) of its final value, or after tripped, when the LDO_OUT falls below 90.0% of that value. The PGLDO output is referenced to an internal rail that is generated to be the highest of V_{IN2}, BAT, and V_{OUT} less a Schottky diode drop.

Supercapacitor

An integrated supercapacitor balancer with 165nA of quiescent current is available to balance a stack of two supercapacitors. Typically the input, SCAP, will tie to V_{OUT} to allow for increased energy storage at V_{OUT} with supercapacitors. The BAL pin is tied to the middle of the stack and can source and sink 10mA to regulate the BAL pin's voltage to half that of the SCAP pin's voltage. To disable the balancer and its associated quiescent current the SCAP and BAL pins can be tied to ground.

TYPICAL APPLICATIONS

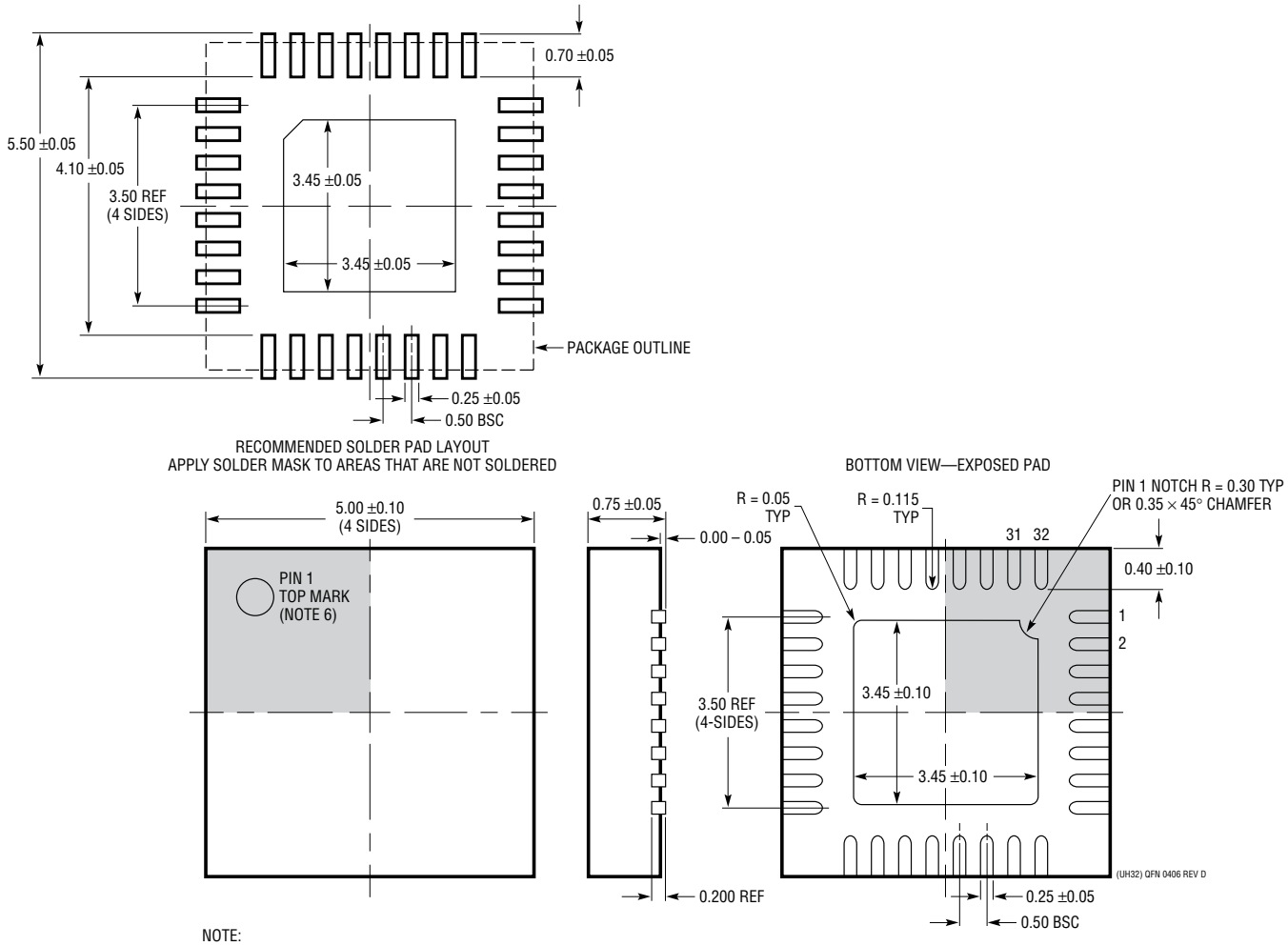
TYPICAL APPLICATIONS

TYPICAL APPLICATIONS

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

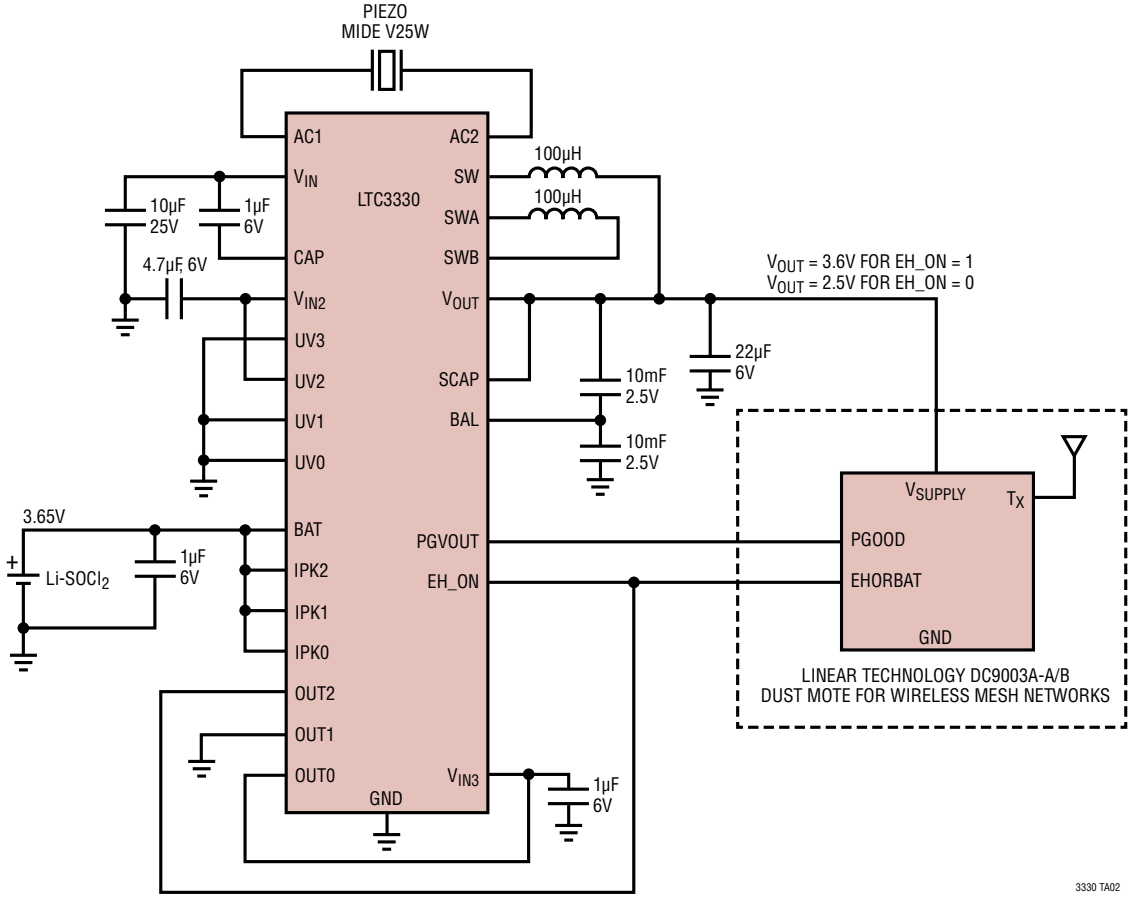
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

UPS System for Wireless Mesh Networks with Output Supercapacitor Energy Storage



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1389	Nanopower Precision Shunt Voltage Reference	800nA Operating Current, 1.25V/2.5V/4.096V
LTC1540	Nanopower Comparator with Reference	0.3µA I_Q, Drives 0.01µF, Adjustable Hysteresis, 2V to 11V Input Range
LT3009	3µA I_Q, 20mA Low Dropout Linear Regulator	Low 3µA I_Q, 1.6V to 20V Range, 20mA Output Current
LTC3108	Ultralow Voltage Step-Up Converter and Power Manager	Operates from 20mV inputs, LDO, Reserve Output, Power Good
LTC3109	Auto-Polarity, Ultralow Voltage Step-Up Converter and Power Manager	Operates from 30mV Inputs, Auto-Polarity Architecture, LDO, Energy Storage Capability, Power Good
LTC3388-1/ LTC3388-3	20V High Efficiency Nanopower Step-Down Regulator	860nA I_Q in Sleep, 2.7V to 20V Input, V_{OUT}: 1.2V to 5.0V, Enable and Standby Pins
LTC3588-1	Piezoelectric Energy Harvesting Power Supply	<1µA I_Q in Regulation, 2.7V to 20V Input Range, Integrated Bridge Rectifier
LTC3588-2	Piezoelectric Energy Harvesting Power Supply	<1µA I_Q in Regulation, UVLO Rising = 16V, UVLO Falling = 14V, V_{OUT} = 3.45V, 4.1V, 4.5V, 5.0V
LTC4070	Li-Ion/Polymer Shunt Battery Charger System	450nA I_Q, 1% Float Voltage Accuracy, 50mA Shunt Current 4.0V/4.1V/4.2V
LTC4071	Li-Ion/Polymer Shunt Battery Charger System with Low Battery Disconnect	550nA I_Q, 1% Float Voltage Accuracy, 50mA Shunt Current 4.0V/4.1V/4.2V, 2.7V or 3.2V Battery Disconnect Levels

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