Synchronous 1A Buck-Boost and 600mA Buck Converters

FEATURES

- **Dual High Efficiency DC/DC Converters:**
  Buck-Boost (V_{OUT}: 2.2V to 5.25V, I_{OUT} = 1A at V_{OUT} = 3.3V, $V_{IN} \geq$ 3V)
  Buck (V_{OUT}: 0.8V to V_{IN}, I_{OUT} = 600mA)
- **2.2V to 5.5V Input Voltage Range**
- **Pin-Selectable Burst Mode® Operation**
- **Uncommitted Gain Block for LDO Controller, Battery Good Indication or Sequencing**
- Programmable 100kHz to 2MHz Switching Frequency
- 55µA Total Quiescent Current for Both Converters in Burst Mode Operation
- Thermal and Overcurrent Protection
- <1µA Quiescent Current in Shutdown
- 24-Lead 4mm × 4mm QFN Package

APPLICATIONS

- Portable Media Players
- Digital Cameras
- Handheld PCs, PDAs
- GPS Receivers

DESCRIPTION

The LTC®3520 combines 1A buck-boost and 600mA synchronous buck DC/DC converters in a tiny 4mm × 4mm package. A programmable switching frequency allows the efficiency to be optimized while minimizing the solution footprint. Both converters feature soft-start and current limit protection. The uncommitted gain block can be configured as an LDO or utilized as a battery-good comparator.

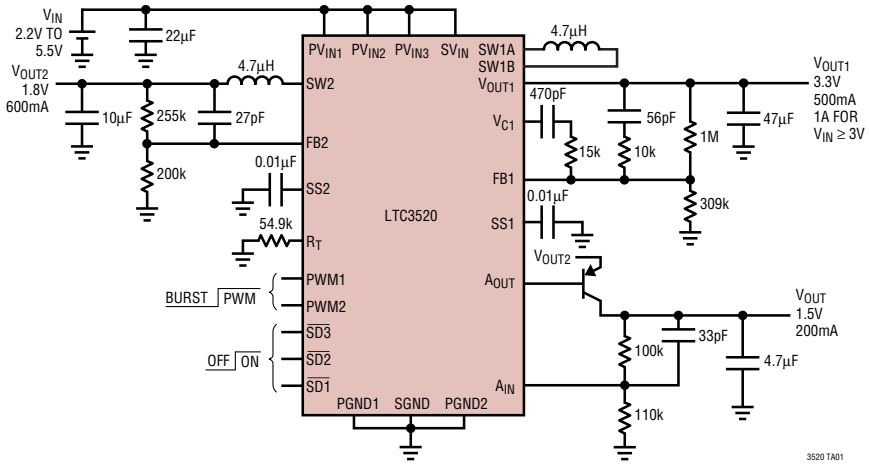
The buck converter is current mode controlled with internal synchronous rectification to improve efficiency. Pin-selectable Burst Mode operation can be enabled to improve light load efficiency, or the buck converter can be operated in low noise PWM mode for sensitive applications.

The buck-boost converter provides continuous conduction operation to maximize efficiency and minimize noise. At light loads, use of Burst Mode operation will improve efficiency.

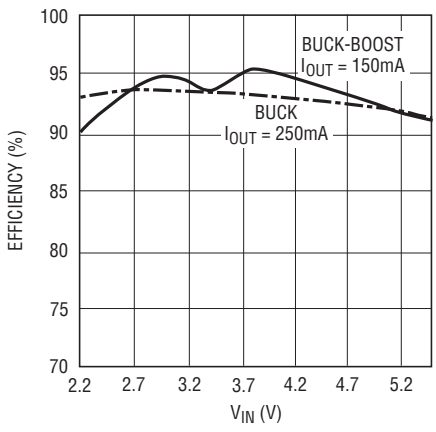
The LTC3520 provides a <1µA shutdown mode and overtemperature shutdown on both converters. The LTC3520 is available in a low profile (0.75mm) 24-lead 4mm × 4mm QFN package.

TYPICAL APPLICATION

3.3V at 500mA, 1.8V at 600mA and 1.5V at 200mA Converter



Efficiency vs V_{IN}

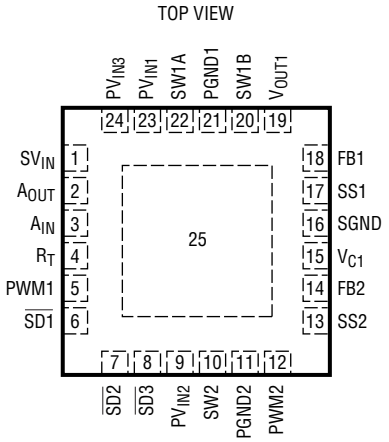


ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN1}, PV_{IN2}, PV_{IN3}, SV_{IN} Voltage ..... –0.3V to 6V
SW1A, SW1B, SW2 Voltage
DC ..... –0.3V to 6V
Pulsed <100ns ..... –1V to 7V
Voltage, All Other Pins ..... –0.3V to 6V
Operating Temperature Range (Note 2) ... –40°C to 85°C
Maximum Junction Temperature (Note 5) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3520EUF#PBF	LTC3520EUF#TRPBF	3520	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, S_{VIN} = P_{VIN1} = P_{VIN2} = P_{VIN3} = 3.6V, V_{OUT1} = 3.3V, R_T = 54.9k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage		●	2.2		5.5	V
Quiescent Current in Shutdown	$V_{\overline{SD1}}$ = $V_{\overline{SD2}}$ = $V_{\overline{SD3}}$ = 0V	●		0.01	1	µA
Undervoltage Lockout	SV_{IN} Rising			2	2.2	V
Burst Mode Quiescent Current, Both Converters	V_{FB1} = V_{FB2} = 0.88V, $V_{\overline{SD3}}$ = 0V			55		µA
Oscillator Frequency	R_T = 54.9k	●	0.8	1	1.2	MHz
Buck Converter						
PMOS Switch Resistance				0.32		Ω
NMOS Switch Resistance				0.18		Ω
NMOS Switch Leakage	V_{SW2} = 5V, S_{VIN} = P_{VIN1} = P_{VIN2} = P_{VIN3} = 5V			0.1	5	µA
PMOS Switch Leakage	V_{SW2} = 0V, S_{VIN} = P_{VIN1} = P_{VIN2} = P_{VIN3} = 5V			0.1	10	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, S_{VIN} = P_{VIN1} = P_{VIN2} = P_{VIN3} = 3.6V, V_{OUT1} = 3.3V, R_T = 54.9k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Voltage (FB2 Pin)	(Note 4)	●	0.771	0.790	0.809	V
Feedback Input Current (FB2 Pin)				1	50	nA
PMOS Current Limit	(Note 3)	●	0.8	1.25		A
Maximum Duty Cycle	V_{FB2} = 0.72V	●	100			%
Minimum Duty Cycle	V_{FB2} = 0.88V	●			0	%
Soft-Start Charging Current				6		µA
$\overline{SD2}$ Input High Voltage			1.4			V
$\overline{SD2}$ Input Low Voltage					0.4	V
$\overline{SD2}$ Input Current				0.01	1	µA
Buck-Boost Converter						
Output Voltage		●	2.2		5.25	V
PMOS Switch Resistance				0.20		Ω
NMOS Switch Resistance				0.15		Ω
NMOS Switch Leakage	V_{SW1A} = V_{SW1B} = 5V, S_{VIN} = P_{VIN1} = P_{VIN2} = P_{VIN3} = 5V			0.1	5	µA
PMOS Switch Leakage	V_{SW1A} = V_{SW1B} = 0V, S_{VIN} = P_{VIN1} = P_{VIN2} = P_{VIN3} = 5V			0.1	10	µA
Feedback Voltage (FB1 Pin)		●	0.766	0.782	0.798	V
Feedback Input Current (FB1 Pin)				1	50	nA
Forward Current Limit	(Note 3)	●	1.4	2		A
Reverse Current Limit	(Note 3)			560		mA
Burst Mode Operation Current Limit	(Note 3)			325		mA
Error Amplifier Gain				80		dB
Error Amplifier Sink Current				500		µA
Error Amplifier Source Current				14		µA
Maximum Duty Cycle	Boost (% Switch C is On) Buck (% Switch A is On)	●	70 100	80		% %
Minimum Duty Cycle		●			0	%
Soft-Start Charging Current				6		µA
$\overline{SD1}$, PWM1 Input High Voltage			1.4			V
$\overline{SD1}$, PWM1 Input Low Voltage					0.4	V
$\overline{SD1}$, PWM1 Input Current				0.01	1	µA
Gain Block						
Quiescent Current	V_{AIN} = 0.88V, $V_{\overline{SD1}}$ = $V_{\overline{SD2}}$ = 0V			45		µA
A_{IN} Pin Threshold Voltage		●	0.770	0.786	0.802	V
A_{IN} Pin Input Bias Current				1	50	nA
A_{OUT} Sink Current	V_{AIN} = 0.72V, V_{AOUT} = 1.8V			17		mA
A_{OUT} Source Current	V_{AIN} = 0.88V, V_{AOUT} = 1.8V			18		µA
A_{OUT} Pin Voltage	V_{AIN} = 0.72V, I_{AOUT} = 1mA			25	150	mV
Open Loop Gain				80		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3.6V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, R_T = 54.9k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay	A_{OUT} Falling			11		µs
$\overline{SD3}$ Input High Voltage			1.4			V
$\overline{SD3}$ Input Low Voltage					0.4	V
$\overline{SD3}$ Input Current				0.01	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3520 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Current measurements are performed when the LTC3520 is not switching. The current limit values in operation will be somewhat higher due to the propagation delay of the comparators.

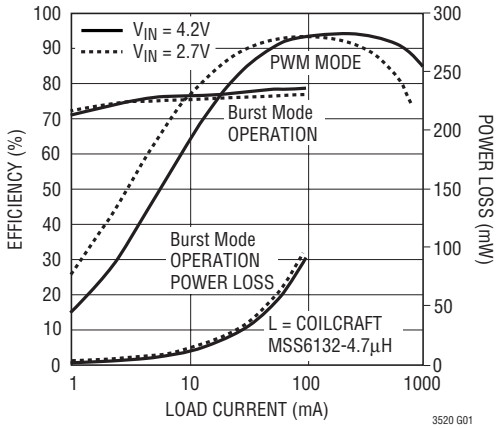
Note 4: The LTC3520 is tested in a proprietary non-switching test mode that internally connects the FB2 pin to the output of the buck converter error amplifier.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

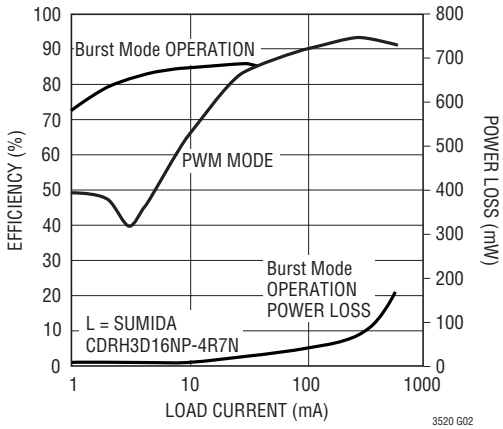
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, unless otherwise specified)

Buck-Boost Efficiency
Lithium-Ion to 3.3V

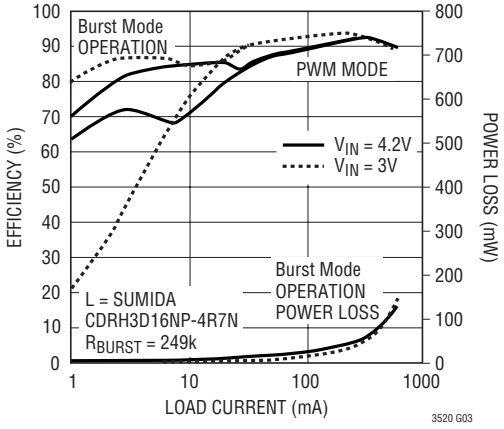


Buck Efficiency
Lithium-Ion to 2.7V

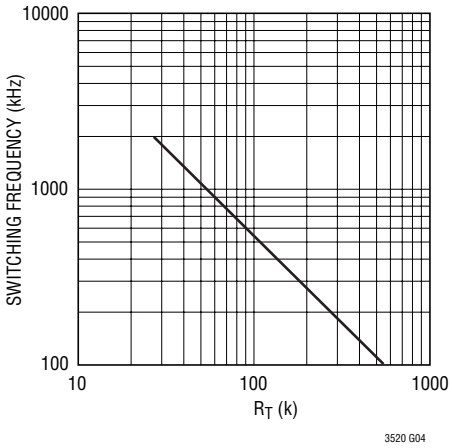


TYPICAL PERFORMANCE CHARACTERISTICS

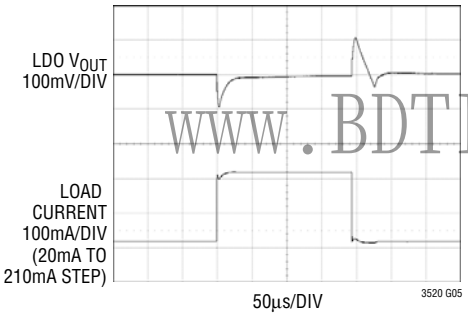
Buck Efficiency
Lithium-Ion to 1.8V



Switching Frequency vs R_T

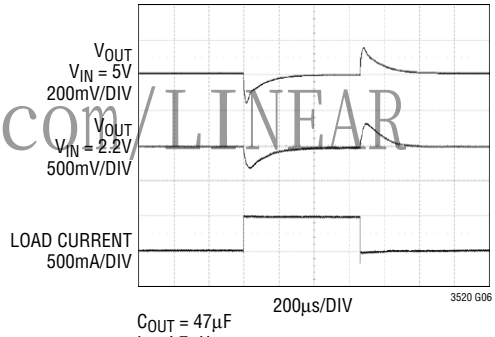


LDO Load
Transient Response



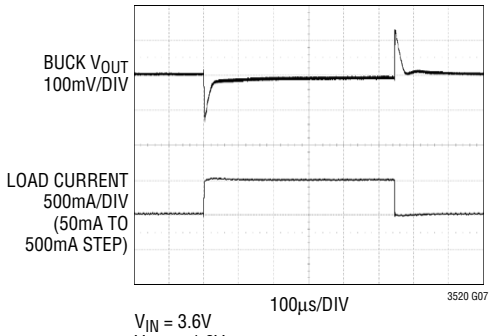
V_{IN} = 3.6V C_{OUT} = 4.7µF
V_{OUT} = 1.5V LDO INPUT VOLTAGE = 1.8V

Buck-Boost Load
Transient Response



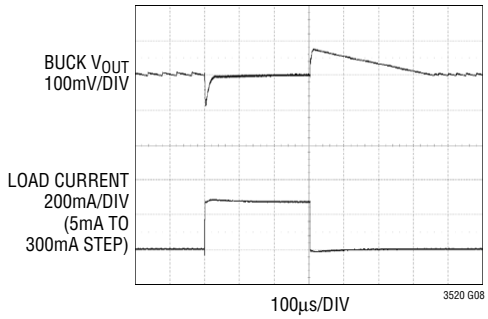
C_{OUT} = 47µF
L = 4.7µH
V_{IN} = 3.3V

Buck Load Transient
Response (PWM Mode)



V_{IN} = 3.6V
V_{OUT} = 1.8V
C_{OUT} = 10µF

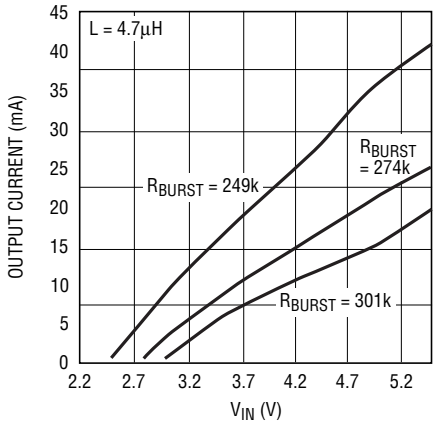
Buck Load Transient
Response (Burst Mode Operation)



V_{IN} = 3.6V C_{OUT} = 22µF
V_{OUT} = 1.8V R_{BURST} = 249k

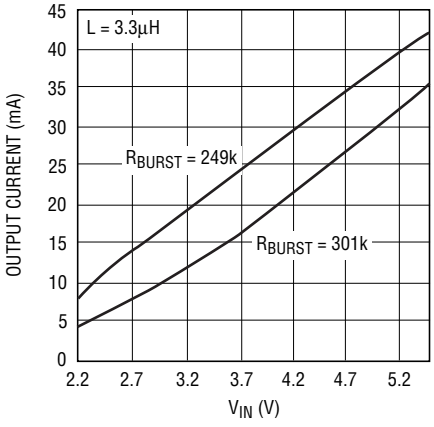
TYPICAL PERFORMANCE CHARACTERISTICS

Buck Burst Mode Threshold
V_{OUT} = 1.8V



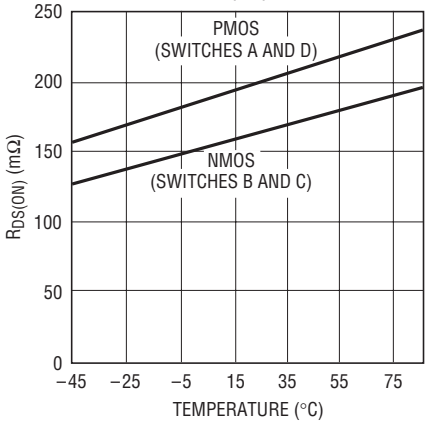
3520 G09

Buck Burst Mode Threshold
V_{OUT} = 1.2V



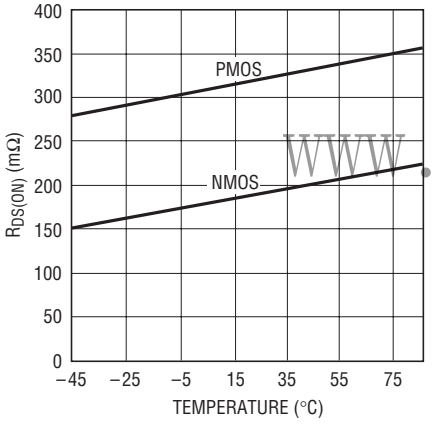
3520 G09b

Buck-Boost $R_{DS(ON)}$



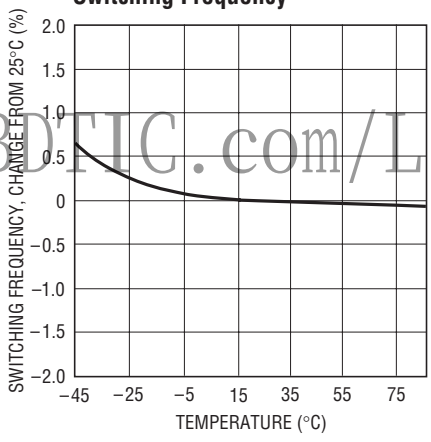
3520 G10

Buck $R_{DS(ON)}$



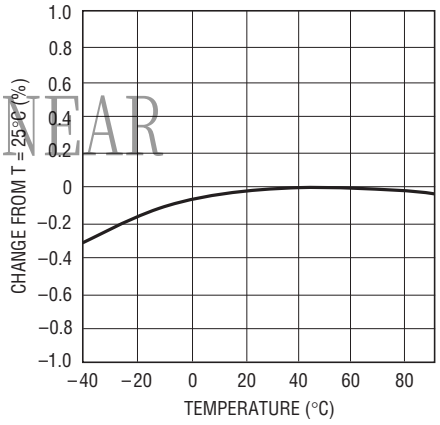
3520 G11

Switching Frequency



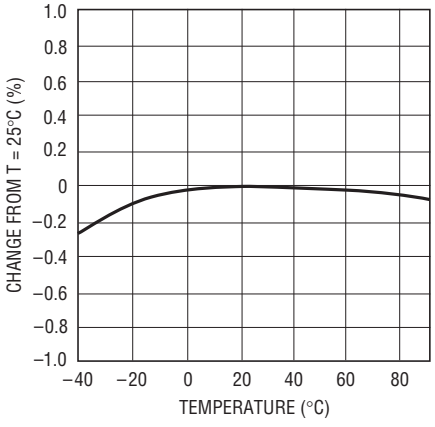
3520 G12

Buck-Boost Feedback Voltage



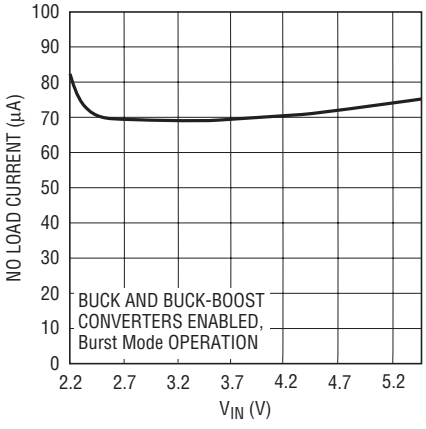
3520 G13

Buck Feedback Voltage



3520 G14

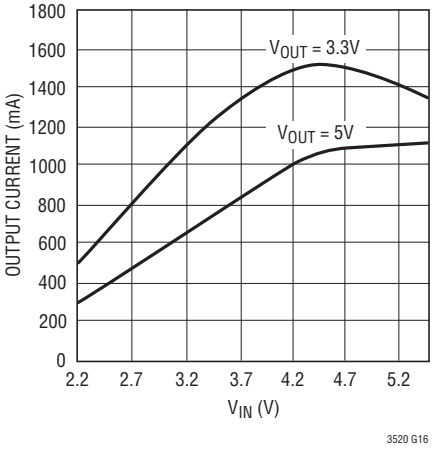
No Load Input Current



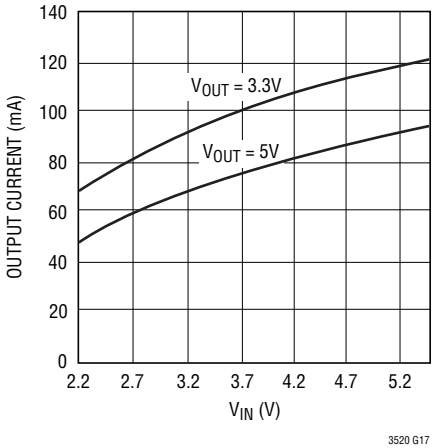
3520 G15

TYPICAL PERFORMANCE CHARACTERISTICS

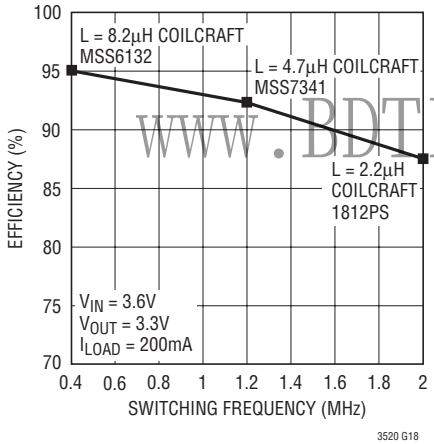
Buck-Boost Maximum Output Current, PWM Mode



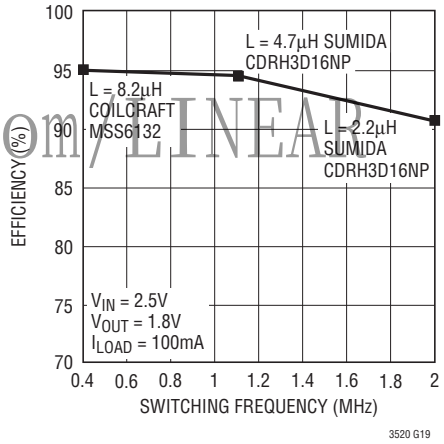
Buck-Boost Maximum Output Current, Burst Mode Operation



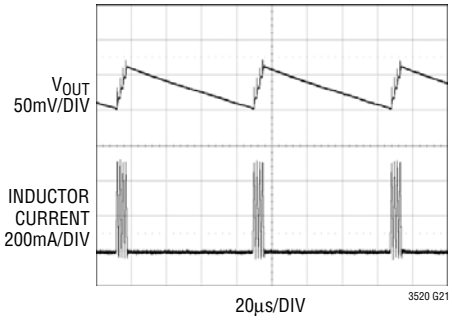
Buck-Boost PWM Mode Efficiency vs Frequency



Buck Efficiency vs Frequency

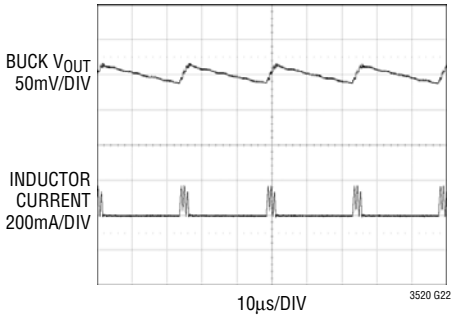


Buck-Boost Burst Mode Operation



C_{OUT} = 22µF I_{LOAD} = 25mA
L = 4.7µH V_{IN} = 3.6V

Buck Burst Mode Operation



V_{IN} = 3.6V R_{BURST} = 249k
V_{OUT} = 1.8V C_{OUT} = 10µF
I_{LOAD} = 10mA

PIN FUNCTIONS

SV_{IN} (Pin 1): Small Signal Power Supply Connection. This pin is used to power the internal circuitry of the LTC3520. This pin should be bypassed using a 0.1µF or larger ceramic capacitor placed as close as possible to the pin with a short return path to ground. **Pins PV_{IN1}, PV_{IN2}, PV_{IN3}, and SV_{IN} must be connected together in the application circuit.**

A_{OUT} (Pin 2): Uncommitted Amplifier Output. This pin should be connected to the base of an external PNP transistor for use as an LDO regulator. If used as a battery-good indicator or for supply sequencing, this pin is the comparator output.

A_{IN} (Pin 3): Non-Inverting Input to the Uncommitted Amplifier. In LDO applications, this pin is connected to the LDO feedback voltage.

R_T (Pin 4): Programs the Frequency of the Internal Oscillator. This pin must be tied to ground via an external resistor. The value of the resistor controls the oscillator frequency. For details on choosing the value of this resistor see the Applications Information section of this datasheet.

PWM1 (Pin 5): Logic Input Used to Choose Between Burst and PWM Mode for the Buck-Boost Converter. This pin cannot be left floating.

PWM1 = Low: The buck-boost converter will operate in variable frequency mode to improve efficiency at light loads. In this mode, the LTC3520 can only supply a reduced load current (typically 50mA).

PWM1 = High: The buck-boost converter will remain in low noise, fixed frequency PWM mode at all load currents.

$\overline{SD1}$ (Pin 6): Buck-Boost Active-Low Shutdown Pin. Forcing this pin above 1.4V enables the buck-boost converter. Forcing this pin below 0.4V disables the buck-boost converter. This pin cannot be left floating.

$\overline{SD2}$ (Pin 7): Buck Active-Low Shutdown Pin. Forcing this pin above 1.4V enables the buck converter. Forcing this pin below 0.4V disables the buck converter. This pin cannot be left floating.

$\overline{SD3}$ (Pin 8): Uncommitted Amplifier Active-Low Shutdown Pin. Forcing this pin above 1.4V enables the uncommitted amplifier. Forcing this pin below 0.4V disables the uncommitted amplifier. This pin cannot be left floating.

PV_{IN2} (Pin 9): High Current Power Supply Connection Used to Supply the Buck Converter PMOS Power Device. This pin should be bypassed by a 22µF or larger ceramic capacitor. The bypass capacitor should be placed as close to the pin as possible and should have a short return path to ground. **Pins PV_{IN1}, PV_{IN2}, PV_{IN3}, and SV_{IN} must be connected together in the application circuit.**

SW2 (Pin 10): Buck Converter Switch Node. This pin must be connected to one side of the buck inductor.

PGND2 (Pin 11): High Current Ground Connection for the Buck Converter N-Channel MOSFET Power Device. The PCB trace connecting this pin to ground should be made as short and wide as possible.

PWM2 (Pin 12): Burst/PWM Mode Control Pin for the Buck Converter. This pin can be used in the following ways:

PWM2 forced high: With PWM2 forced high, the buck converter will be forced into low noise fixed frequency operation. The buck converter will remain in this mode unless the load current is low enough that the minimum on-time is reached at which point the converter will begin pulse-skipping to maintain regulation.

PWM2 connected to ground via resistor: PWM2 can be connected to ground through a resistor to control the load current at which Burst Mode operation is entered and exited. Larger resistor values will cause the buck converter to enter Burst Mode operation at lower load currents and will result in lower output voltage ripple in Burst Mode operation. Smaller resistor values will cause Burst Mode operation to be entered at higher load currents and the Burst Mode ripple will be larger.

PWM2 forced low: With PWM2 forced to ground, the buck converter will operate in Burst Mode operation for all but the highest load currents. Generally, this mode of operation is utilized to force the buck converter into Burst Mode operation when it is known that the load current will be relatively low (under 75mA) or in applications that are not sensitive to output voltage ripple.

PIN FUNCTIONS

SS2 (Pin 13): Buck Converter Soft-Start Pin. This pin must be connected to a soft-start capacitor. The value of the capacitor determines the duration of the soft-start period. For information on choosing the value of this capacitor, see the Applications Information section of this datasheet.

FB2 (Pin 14): Feedback Voltage for the Buck Converter. This pin is derived from a resistor divider on the buck output voltage. The buck output voltage is given by the following equation where R1 is a resistor between FB2 and ground and R2 is a resistor between FB2 and the buck output voltage:

$$V_{OUT} = 0.790V\left(1+\frac{R2}{R1}\right)$$

V_{C1} (Pin 15): Buck-Boost Error Amplifier Output. A frequency compensation network is connected to FB1 to compensate the loop. During Burst Mode operation, V_{C1} is driven internally by a clamp circuit.

SGND (Pin 16): Small Signal Ground. This pin is used as a ground reference for the internal circuitry of the LTC3520.

SS1 (Pin 17): Buck-Boost Converter Soft-Start Pin. This pin must be connected to a soft-start capacitor. The value of the capacitor determines the duration of the soft-start period. For information on choosing the value of this capacitor, see the Applications Information section of this datasheet.

FB1 (Pin 18): Feedback Voltage for the Buck-Boost Converter. This pin is derived from a resistor divider on the buck-boost output voltage. The buck-boost output voltage is given by the following equation where R1 is a resistor between FB1 and ground and R2 is a resistor between FB1 and the buck-boost output voltage:

$$V_{OUT} = 0.782V\left(1+\frac{R2}{R1}\right)$$

V_{OUT1} (Pin 19): Buck-Boost Output Voltage Node. This pin should be connected to a low ESR buck-boost output capacitor. The capacitor should be placed as close to the IC as possible and should have a short return path to ground.

SW1B (Pin 20): Buck-Boost Switch Node. This pin must be connected to one side of the buck-boost inductor.

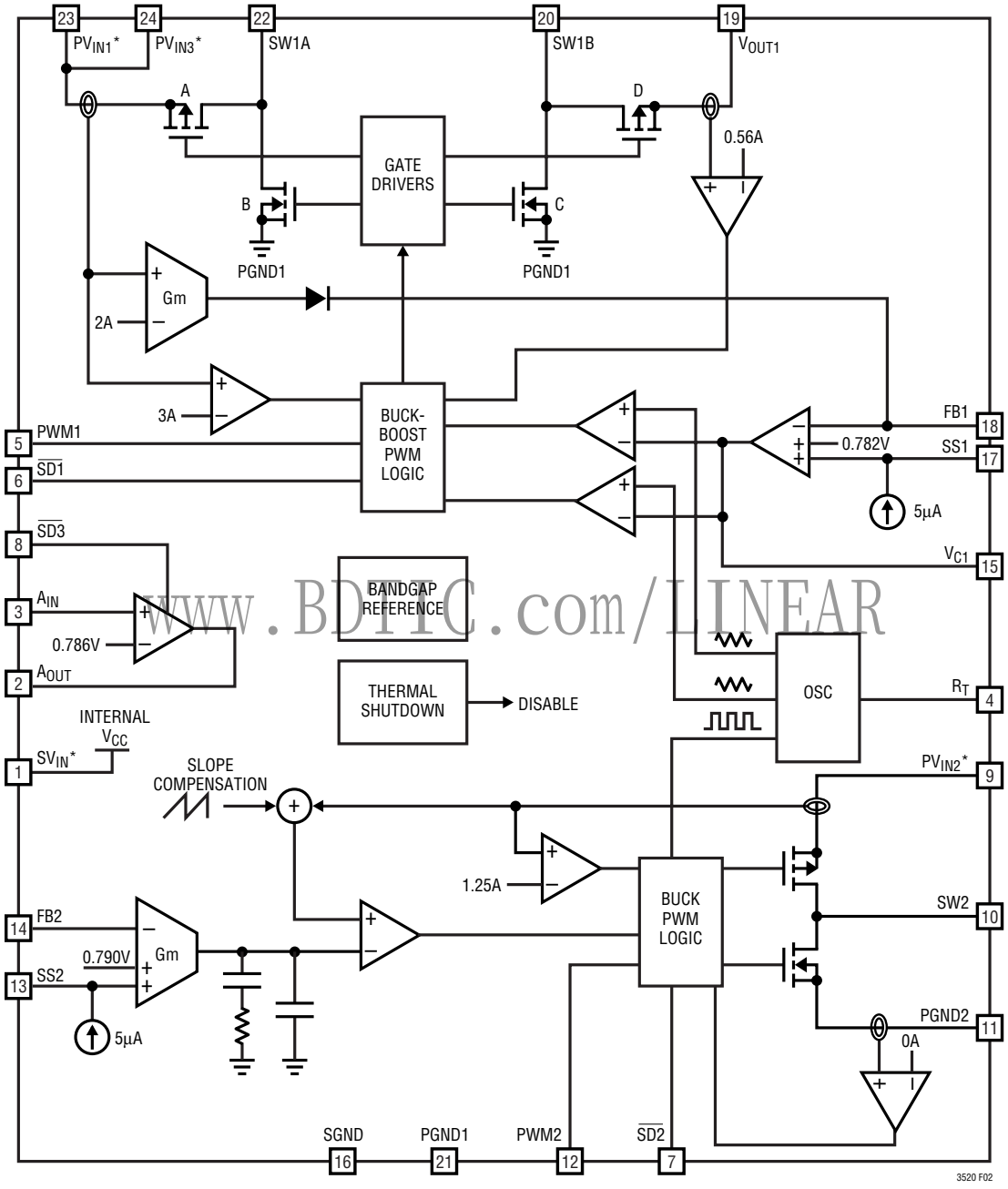
PGND1 (Pin 21): High Current Ground Connection for the Buck-Boost NMOS Power Devices. The PCB trace connecting this pin to ground should be made as short and wide as possible.

SW1A (Pin 22): Buck-Boost Switch Node. This pin must be connected to one side of the buck-boost inductor.

PV_{IN1} (Pin 23), PV_{IN3} (Pin 24): High Current Power Supply Connections Used to Power the Buck-Boost Converter Power Switch A. These pins should be connected together and bypassed by a 22µF or larger ceramic capacitor. The bypass capacitor should be placed as close to the pin as possible and should have a short return path to ground. **Pins PV_{IN1}, PV_{IN2}, PV_{IN3}, and SV_{IN} must be connected together in the application circuit.**

Exposed Pad (Pin 25): Ground. The Exposed Pad must be electrically connected to ground and soldered to the PCB. **Pins PGND1, PGND2, SGND, and the Exposed Pad must be connected together in the application circuit.**

BLOCK DIAGRAM



*PINS SV_{IN}, PV_{IN1}, PV_{IN2} AND PV_{IN3} MUST BE CONNECTED TOGETHER IN THE APPLICATION.

OPERATION

The LTC3520 combines a synchronous buck DC/DC converter and a four-switch buck-boost DC/DC converter in a single 4mm x 4mm QFN package. The buck-boost converter utilizes a proprietary switching algorithm which allows its output voltage to be regulated above, below, or equal to the input voltage. The buck converter provides a high efficiency lower voltage output and supports 100% duty cycle operation to extend battery life. In Burst Mode operation, the total quiescent current for both converters is reduced to 55µA (typical). Both converters operate synchronously from a common internal oscillator whose frequency is programmed via an external resistor. In addition, the LTC3520 contains an uncommitted gain block which can be configured as a comparator for low battery detection or as a power-good indicator. Alternatively, the gain block can be utilized in conjunction with an external PNP to create an LDO, thereby allowing the LTC3520 to generate a third low noise output voltage.

BUCK CONVERTER OPERATION

PWM Mode Operation

When the PWM2 pin is held high, the LTC3520 buck converter uses a constant-frequency, current mode control architecture. Both the main (P-channel MOSFET) and synchronous rectifier (N-channel MOSFET) switches are internal. At the start of each oscillator cycle, the P-channel switch is turned on and remains on until the current waveform with superimposed slope compensation ramp exceeds the error amplifier output. At this point, the synchronous rectifier is turned on and remains on until the inductor current falls to zero or a new switching cycle is initiated. As a result, the buck converter operates with discontinuous inductor current at light loads which improves efficiency. At extremely light loads, the minimum on-time of the main switch will be reached and the buck converter will begin turning off for multiple cycles in order to maintain regulation.

Burst Mode Operation

Burst Mode operation is enabled by either connecting PWM2 to ground through a resistor, R_{BURST}, or by shorting PWM2 to ground. The buck converter will automatically transition between PWM mode at high load current and Burst Mode operation at light currents. Typical curves for the Burst Mode entry threshold are provided in the Typical Performance Characteristics section of this datasheet. Under dropout and near dropout conditions, Burst Mode operation will not be entered.

The value of R_{BURST} controls the load current at which Burst Mode operation will be entered. Larger resistor values will cause Burst Mode operation to be entered at lighter load currents. However, if the value of R_{BURST} is too large, then the buck converter will not enter Burst Mode operation at any current, especially when operating with V_{IN} close to the buck output voltage. Conversely, if R_{BURST} is too small, the ripple in Burst Mode operation may become objectionable, especially at high input voltages. For most applications, choosing R_{BURST} = 301k represents a reasonable compromise.

The output voltage ripple in Burst Mode operation is dependent upon the value of R_{BURST}, the input voltage, the output voltage, the inductor value and the output capacitor. The Burst Mode operation output voltage ripple can be reduced by increasing the size of the output capacitor, increasing the value of the inductor or increasing the value of R_{BURST}.

Low Dropout Operation

As the input voltage decreases to a value approaching the output regulation voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage will force the power P-channel MOSFET switch to remain on for more than one cycle until 100% duty cycle operation is reached and the power switch remains on continuously. In this dropout state, the output voltage will be determined by the input voltage less the resistive voltage drop across the main switch and series resistance of the inductor.

Slope Compensation

Current mode control requires the use of slope compensation to prevent subharmonic oscillations in the inductor current waveform at high duty cycle operation. This is accomplished internally on the LTC3520 through the addition of a compensating ramp to the current sense signal. In some current mode ICs, current limiting is performed by clamping the error amplifier voltage to a fixed maximum.

OPERATION

This leads to a reduced output current capability at large step-down ratios. In contrast, the LTC3520 performs current limiting prior to the addition of the slope compensation ramp and therefore achieves a peak inductor current limit that is independent of duty cycle.

Soft-Start

The buck converter incorporates a voltage mode soft-start circuit which is adjustable via the value of an external soft-start capacitor, C_{SS}. The typical soft-start duration is given by the following equation:

$$t_{SS}(ms) = 0.15C_{SS}(nF)$$

The buck converter remains in regulation during soft-start and will therefore respond to output load transients which occur during this time. In addition, the output voltage rise-time has minimal dependency on the size of the output capacitor or load current.

Error Amplifier and Compensation

The LT3520 buck converter utilizes an internal transconductance error amplifier. Compensation of the feedback loop is performed internally to reduce the size of the application circuit and simplify the design process. The compensation network has been designed to allow use of a wide range of output capacitors while simultaneously ensuring a rapid response to load transients.

BUCK-BOOST CONVERTER OPERATION

PWM Mode Operation

When the PWM pin is held high, the LTC3520 buck-boost converter operates in a constant-frequency PWM mode using voltage mode control. A proprietary switching algorithm allows the converter to switch between buck, buck-boost, and boost modes without discontinuity in inductor current or loop characteristics. The switch topology for the buck-boost converter is shown in Figure 1.

When the input voltage is significantly greater than the output voltage, the buck-boost converter operates in buck mode. Switch D turns on continuously and switch C remains off. Switches A and B are pulse width modulated to produce the required duty cycle to support the output regulation voltage. As the input voltage decreases, switch A remains on for a larger portion of the switching cycle. When the duty cycle reaches approximately 85%, the switch pair AC begins turning on for a small fraction of the switching period. As the input voltage decreases further, the AC switch pair remains on for longer durations and the duration of the BD phase decreases proportionally. As the input voltage drops below the output voltage, the AC phase will eventually increase to the point that there is no longer any BD phase. At this point, switch A remains on continuously while switch pair CD is pulse width modulated to obtain the desired output voltage. In this case, the converter is operating solely in boost mode.

This switching algorithm provides a seamless transition between operating modes and eliminates discontinuities in average inductor current, inductor current ripple, and loop transfer function throughout all three operational modes. These advantages result in increased efficiency and stability in comparison to the traditional four-switch buck-boost converter.

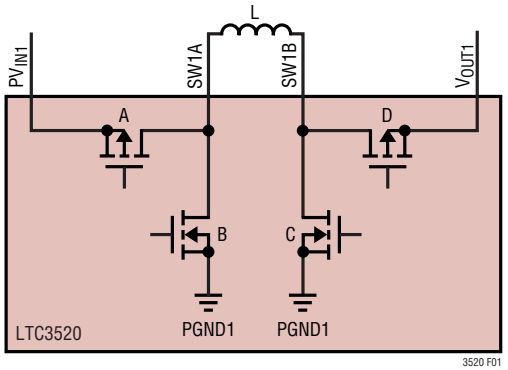


Figure 1. Buck-Boost Switch Topology

OPERATION

Error Amplifier

The error amplifier operates in voltage mode. Appropriate loop compensation components must be utilized around the amplifier (between the FB1 and V_{C1} pins) in order to ensure stable operation. For improved bandwidth, an additional RC feedforward network can be placed across the upper feedback divider resistor.

Current Limit Operation

The buck-boost converter has two current limit circuits. The primary current limit is an average current limit circuit which injects an amount of current into the feedback node which is proportional to the extent that the switch A current exceeds the current limit value. Due to the high gain of this loop, the injected current forces the error amplifier output to decrease until the average current through switch A decreases approximately to the current limit value. The average current limit utilizes the error amplifier in an active state and thereby provides a smooth recovery with little overshoot once the current limit fault condition is removed. Since the current limit is based on the average current through switch A, the peak inductor current in current limit will have a dependency on the duty cycle (i.e., on the input and output voltages in the overcurrent condition).

The speed of the average current limit circuit is limited by the dynamics of the error amplifier. On a hard output short, it would be possible for the inductor current to increase substantially beyond current limit before the average current limit circuit would react. For this reason, there is a second current limit circuit which turns off switch A if the current ever exceeds approximately 150% of the average current limit value. This provides additional protection in the case of an instantaneous hard output short.

Reverse Current Limit

The reverse current comparator on switch D monitors the inductor current entering the V_{OUT1} pin. If this current exceeds 560mA (typical) switch D is turned off for the remainder of the switching cycle.

Burst Mode Operation

With the PWM1 pin held low, the buck-boost converter operates utilizing a variable frequency switching algorithm designed to improve efficiency at light loads and reduce the standby current at zero load. In Burst Mode operation, the inductor is charged with fixed peak amplitude current pulses. These current pulses are repeated as often as necessary to maintain the output regulation voltage. The typical output current which can be supplied in Burst Mode operation is dependent upon the input and output voltage as given by the following formula:

$$I_{OUT(MAX),BURST} = \frac{0.13 \bullet V_{IN}}{V_{IN} + V_{OUT}} A$$

In Burst Mode operation, the error amplifier is not used but is instead placed in a low current standby mode to reduce supply current and improve light load efficiency.

Soft-Start

The buck-boost converter incorporates a voltage mode soft-start circuit which is adjustable via the value of an external soft-start capacitor, C_{SS}. The typical soft-start duration is given by the following equation:

$$t_{SS}(ms) = 0.15C_{SS}(nF)$$

The converter remains in regulation during soft-start and will therefore respond to output load transients that occur during this time. In addition, the output voltage rise time has minimal dependency on the size of the output capacitor or load. During soft-start, the buck-boost converter is forced into PWM operation regardless of the state of the PWM1 pin.

Transition From Burst to PWM Operation

In Burst Mode operation, the compensation network is not used and the V_{C1} pin is disconnected from the error amplifier. During long periods of Burst Mode operation, leakage currents in the external components or on the PCB could cause the compensation capacitor to charge or discharge resulting in a large output transient when returning to the fixed frequency mode of operation. To prevent this from happening, the LTC3520 employs an active clamp circuit that holds the voltage on the V_{C1} pin to the optimal level during Burst Mode operation. This minimizes any output transient when returning to fixed frequency operation.

OPERATION

COMMON FUNCTIONS

Oscillator

The buck-boost and buck converters operate from a common internal oscillator. The switching frequency for both converters is set by the value of an external resistor, R_T, located between the R_T pin and ground according to the following equation:

$$f(kHz) = \frac{54{,}000}{R_T(k\Omega)}$$

Gain Block

The LTC3520 contains a gain block (pins A_{IN} and A_{OUT}) that can be used as a low battery indicator or power-good comparator for either the buck or buck-boost output voltage. Typical circuits for these applications are shown in Figure 2. A small-valued capacitor can be added from A_{OUT} to GND to provide filtering and prevent glitching during slow transitions through the threshold region. The gain block is not disabled by the undervoltage lockout. This allows the uncommitted amplifier to be utilized as a low battery indicator down to a supply voltage of 1.6V typically.

The A_{OUT} pin is not an open-drain output. Rather, it is a push-pull output that can both sink and source current. The uncommitted amplifier is internally powered by the higher of either the SV_{IN} or V_{OUT1} voltages. This restricts the maximum voltage on the A_{OUT} pin to either the input supply voltage or the buck-boost output voltage, whichever is larger.

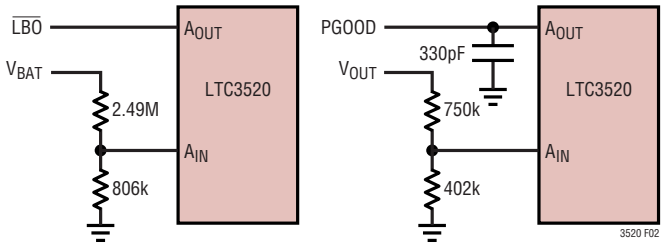


Figure 2. Gain Block Used as a Comparator

Alternatively, the gain block can be utilized as an LDO with the addition of an external PNP as shown in Figure 3. The LDO is convenient for applications requiring a third output (possibly a low current 2.5V or a quiet 3V supply). An external PMOS can be used in place of the PNP, but a much larger output capacitor is required to ensure stability at light load. The gain block has an independent shutdown pin ($\overline{SD3}$) and should be disabled when not in use to reduce quiescent current.

Thermal Shutdown

If the die temperature exceeds 150°C both converters will be disabled. All power devices will be turned off and all switch nodes will be high impedance. The soft-start circuits for both converters are reset during thermal shutdown to provide a smooth recovery once the overtemperature condition is eliminated. Both converters will restart (if enabled) when the die temperature drops to approximately 140°C.

Undervoltage Lockout

If the supply voltage decreases below 2V (typical) then both converters will be disabled and all power devices will be turned off. The soft-start circuits for both converters are reset during undervoltage lockout to provide a smooth restart once the input voltage rises above the undervoltage lockout threshold.

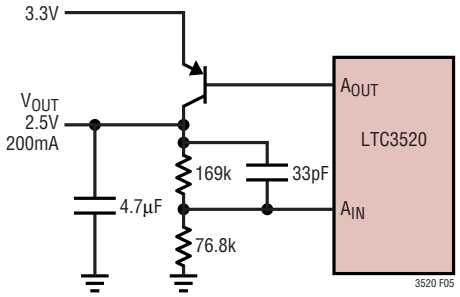


Figure 3. Gain Block Configured as an LDO

APPLICATIONS INFORMATION

The basic LTC3520 application circuit is shown as the Typical Application on the front page of this datasheet. The external component selection is determined by the desired output voltages, output currents, and ripple voltage requirements of each particular application. However, basic guidelines and considerations for the design process are provided in this section.

Operating Frequency Selection

The operating frequency choice is a tradeoff between efficiency and application area. Higher operating frequencies allow the use of smaller inductors and smaller input and output capacitors, thereby reducing application area. However, higher operating frequencies also increase switching losses and therefore decrease efficiency. Typical efficiency versus switching frequency curves for both converters are given in the Typical Performance Characteristics section of this datasheet.

Buck Inductor Selection

The choice of buck inductor value influences both the efficiency and the magnitude of the output voltage ripple. Larger inductance values will reduce inductor current ripple and will therefore lead to lower output voltage ripple. For a fixed DC resistance, a larger value inductor will yield higher efficiency by lowering the peak current and reducing core losses. However, a larger inductor within the same family will generally have a greater series resistance, thereby offsetting this efficiency advantage.

Given a desired peak to peak current ripple, ΔI_L, the required inductor can be calculated via the following expression, where f represents the switching frequency in MHz:

$$L = \frac{1}{f\Delta I_L} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)\mu H$$

A reasonable choice for ripple current is ΔI_L = 240mA which represents 40% of the maximum 600mA load current. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current in order to prevent core saturation and loss of efficiency during operation. To optimize efficiency, an inductor with low series resistance should be utilized.

In particularly space restricted applications it may be advantageous to use a much smaller value inductor at the expense of larger ripple current. In such cases, the converter will operate in discontinuous conduction for a wider range of output loads and efficiency will be reduced. In addition, there is a minimum inductor value required to maintain stability of the current loop (given the fixed internal slope compensation). Specifically, if the buck converter is going to be utilized at duty cycles over 40%, the inductance value must be at least L_{MIN} as given by the following equation:

$$L_{MIN} = 1.4 \bullet V_{OUT}\,\mu H$$

Table 1 depicts the minimum required inductance for several common output voltages.

Table 1. Buck Minimum Inductance

OUTPUT VOLTAGE	MINIMUM INDUCTANCE
0.8V	1.1µH
1.2V	1.7µH
2V	2.8µH
2.7V	3.8µH
3.3V	4.5µH

Buck Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck output in order to minimize voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. In addition to controlling the ripple magnitude, the value of the output capacitor also sets the loop crossover frequency and therefore can impact loop stability. There is both a minimum and maximum capacitance value required to ensure stability of the loop. If the output capacitance is too small, the loop crossover frequency will increase to the point where switching delay and the high frequency parasitic poles of the error amplifier will degrade the phase margin. In addition, the wider bandwidth produced by a small output capacitor will make the loop more susceptible to switching noise. At the other extreme, if the output capacitor is too large, the crossover frequency can decrease too far below the compensation zero and also lead to degraded phase margin. Table 2 provides a guideline for the range of allowable values of low ESR

APPLICATIONS INFORMATION

output capacitors. Larger value output capacitors can be accommodated provided they have sufficient ESR to stabilize the loop or by adding a feedforward capacitor in parallel with the upper feedback resistor.

Table 2. Buck Output Capacitor Range

V_{OUT}	C_{MIN}	C_{MAX}
0.8V	30µF	100µF
1.2V	15µF	50µF
1.8V	10µF	30µF
2.7V	7µF	22µF
3.3V	6µF	20µF

Buck Input Capacitor Selection

The PV_{IN2} pin provides current to the buck converter PMOS power switch. It is recommended that a low ESR ceramic capacitor with a value of at least 22µF be used to bypass this pin. The capacitor should be placed as close to the pin as possible and have a short return to ground.

Buck Output Voltage Programming

The buck converter output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.790V\left(1+\frac{R2}{R1}\right)$$

The external divider is connected to the output as shown in Figure 4. A reasonable compromise between noise immunity and quiescent current is provided by choosing R2 = 249k. The required value for R1 can then be solved via the formula above. It is recommended that a 27pF feedforward capacitor be placed in parallel with R2 in order to improve the transient response and reduce Burst Mode ripple.

Buck-Boost Output Voltage Programming

The buck-boost output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.782V\left(1+\frac{R2}{R1}\right)$$

The external divider is connected to the output as shown in Figure 5. In addition to setting the output voltage, the value of R2 plays an integral role in compensation of the buck-boost control loop. For more details, see the Closing the Buck-Boost Feedback Loop section of this datasheet.

Buck-Boost Inductor Selection

To achieve high efficiency, a low ESR inductor should be utilized for the buck-boost converter. The inductor must have a saturation rating greater than the worst case average inductor current plus half the ripple current. The peak-to-peak inductor current ripple will be larger in buck and boost mode than in the buck-boost region. The peak-to-peak inductor current ripple for each mode can be calculated from the following formulas, where f is the frequency in MHz and L is the inductance in µH:

$$\Delta I_{L,P-P,BUCK} = \frac{1}{fL}\frac{V_{OUT}(V_{IN}-V_{OUT})}{V_{IN}}$$

$$\Delta I_{L,P-P,BOOST} = \frac{1}{fL}\frac{V_{IN}(V_{OUT}-V_{IN})}{V_{OUT}}$$

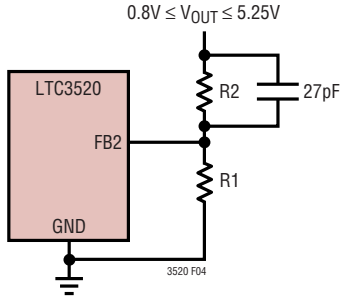


Figure 4. Setting the Buck Output Voltage

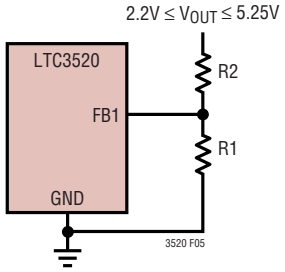


Figure 5. Setting the Buck-Boost Output Voltage

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In addition to affecting output current ripple, the size of the inductor can also affect the stability of the feedback loop. In boost mode, the converter transfer function has a right half plane zero at a frequency that is inversely proportional to the value of the inductor. As a result, a large inductor can move this zero to a frequency that is low enough to degrade the phase margin of the feedback loop. It is recommended that the inductor value be chosen less than 10µH if the buck-boost converter is to be used in the boost region.

Buck-Boost Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck-boost converter output in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. The capacitor should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor ESR and ESL, the peak-to-peak output voltage ripple can be calculated by the following formulas, where f is the frequency in MHz, C_{OUT} is the capacitance in µF, L is the inductance in µH, and I_{LOAD} is the output current in amps.

$$\Delta V_{P-P,BOOST} = \frac{I_{LOAD}(V_{OUT} - V_{IN})}{C_{OUT}\ V_{OUT} f}$$

$$\Delta V_{P-P,BUCK} = \frac{1}{8LC_{OUT}f^2}\frac{(V_{IN} - V_{OUT})\,V_{OUT}}{V_{IN}}$$

Since the output current is discontinuous in boost mode, the ripple in this mode will generally be much larger than the magnitude of the ripple in buck mode. In addition to controlling the ripple magnitude, the value of the output capacitor also affects the location of the resonant frequency in the open loop converter transfer function. If the output capacitor is too small, the bandwidth of the converter will extend high enough to degrade the phase margin. To prevent this from happening, it is recommended that a minimum value of 22µF be used for the buck-boost output capacitor.

Buck-Boost Input Capacitor Selection

The supply current to the buck-boost converter is provided by the PV_{IN1} and PV_{IN3} pins. It is recommended that a low ESR ceramic capacitor with a value of at least 22µF be located as close to this pin as possible.

Inductor Style and Core Material

Different inductor core materials and styles have an impact on the size and price of an inductor at any given peak current rating. Toroid or shielded pot cores in ferrite or permalloy materials are small and reduce emissions, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. However, the inductor must also have low ESR to provide acceptable efficiency and must be able to carry the highest current required by the application without saturating. Table 3 provides a list of several manufacturers of inductors that are well suited to LTC3520 applications.

Table 3. Inductor Vendor Information

MANUFACTURER	PHONE	WEB SITE
Coilcraft	847-639-6400	www.coilcraft.com
Murata	814-238-0490	www.murata.com
Sumida	847-956-0702	www.sumida.com
TDK	847-803-6296	www.component.tdk.com
TOKO	847-699-7864	www.tokoam.com

APPLICATIONS INFORMATION

Capacitor Vendor Information

Both the input and output capacitors used with the LTC3520 must be low ESR and designed to handle the large AC currents generated by switching converters. The vendors in Table 4 provide capacitors that are well suited to LTC3520 application circuits.

Table 4. Capacitor Vendor Information

MANUFACTURER	WEB SITE	PART NUMBER
Taiyo Yuden	www.t-yuden.com	JMK212BJ226MG-T 22µF, 6.3V
TDK	www.component.tdk.com	C3216X5ROJ106KB 10µF, 6.3V
Sanyo	www.secc.co.jp	6APD10M 10µF, 6.3V
Murata	www.murata.com	GRM21BR60J226ME39 22µF, 6.3V

Closing the Buck-Boost Feedback Loop

The LTC3520 buck-boost converter employs voltage mode PWM control. The control to output gain varies with operational region (buck, boost, or buck-boost), but is usually no greater than 24dB. The output filter exhibits a double pole response as given by the following equations:

$$f_{FILTER\_POLE} = \frac{1}{2\pi\sqrt{LC_{OUT}}} Hz \text{(Buck Mode)}$$

$$f_{FILTER\_POLE} = \frac{1}{2\pi V_{OUT}\sqrt{LC_{OUT}}} Hz \text{(Boost Mode)}$$

where L is the inductance in henries and C_{OUT} is the output capacitance in farads. The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2\pi R_{ESR} C_{OUT}} Hz$$

where R_{ESR} is the equivalent series resistance of the output capacitor. A challenging aspect of the loop dynamics in boost mode is the presence of a right half plane zero at the frequency given by:

$$f_{RHPZ} = \frac{V_{IN}^2}{2\pi I_{OUT} LV_{OUT}} Hz$$

The loop gain is typically rolled off to below unity gain before the worst case right half plane zero frequency.

A simple Type I compensation network as shown in Figure 6 can be utilized to stabilize the buck-boost converter. However, this will yield a relatively low bandwidth and slow transient response. To ensure sufficient phase margin using Type I compensation, the loop must be crossed over a decade before the LC double pole frequency. The unity-gain frequency of the error amplifier with Type I compensation is given by:

$$f_{UG} = \frac{1}{2\pi R1 C_{P1}} Hz$$

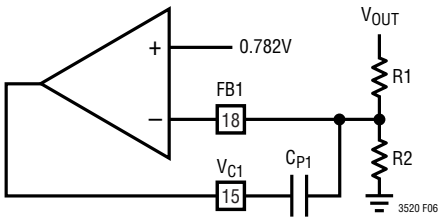


Figure 6. Type I Compensation Network

APPLICATIONS INFORMATION

Most applications require a faster transient response than can be attained using Type I compensation in order to reduce the size of the output capacitor. To achieve a higher loop bandwidth, Type III compensation is required, providing two zeros to compensate for the double pole response of the output filter. Referring to Figure 7, the location of the compensation poles and zeros are given as follows:

$$f_{POLE1} \cong \frac{1}{2\pi(32000)R1C_{P1}} Hz \cong 0Hz$$

$$f_{ZERO1} = \frac{1}{2\pi R_Z C_{P1}} Hz$$

$$f_{ZERO2} = \frac{1}{2\pi R1 C_{Z1}} Hz$$

$$f_{POLE2} = \frac{1}{2\pi R_Z C_{P2}} Hz$$

where all resistances are in ohms and all capacitances are in farads.

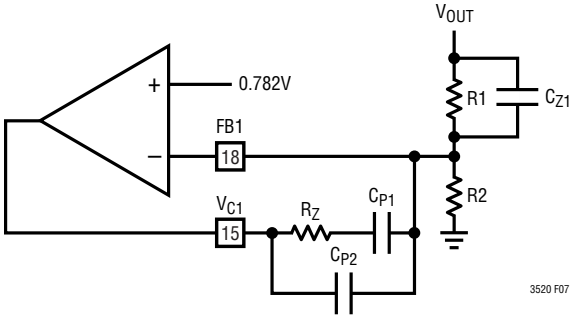


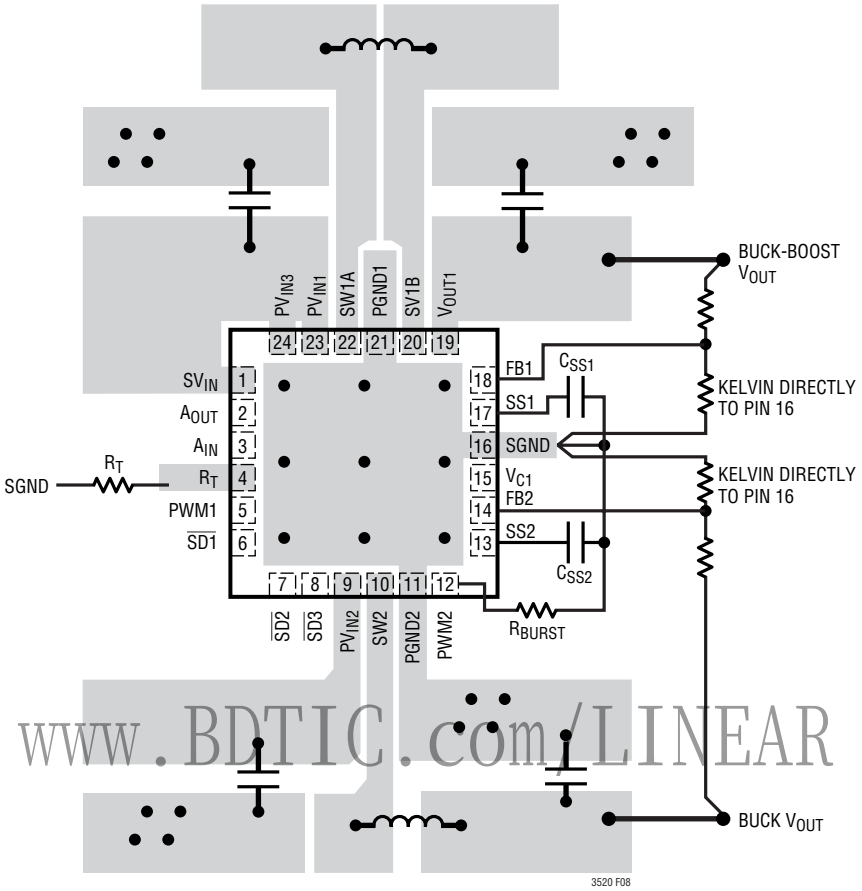
Figure 7. Type III Compensation Network

PCB Layout Considerations

The LTC3520 switches large currents at high frequencies. Special care should be given to the PCB layout to ensure stable, noise-free operation. Figure 8 depicts the recommended PCB layout to be utilized for the LTC3520. A few key guidelines follow:

1. All circulating current paths should be kept as short as possible. This can be accomplished by keeping the routes to all bold components in Figure 8 as short and as wide as possible. Capacitor ground connections should via down to the ground plane by the shortest route possible. The bypass capacitors on PV_{IN1}, PV_{IN2}, and PV_{IN3} should be placed as close to the IC as possible and should have the shortest possible paths to ground.
2. The small signal ground pad (SGND) should have a single-point connection to the power ground. A convenient way to achieve this is to short the pin directly to the Exposed Pad as shown in Figure 8.
3. The components shown in bold and their connections should all be placed over a complete ground plane to reduce the cross-sectional area of circulating current paths.
4. To prevent large circulating currents from disrupting the output voltage sensing, the ground for each resistor divider should be returned directly to the small signal ground pin (SGND).
5. Use of vias in the die attach pad will enhance the thermal environment of the converter especially if the vias extend to a ground plane region on the exposed bottom surface of the PCB.

APPLICATIONS INFORMATION



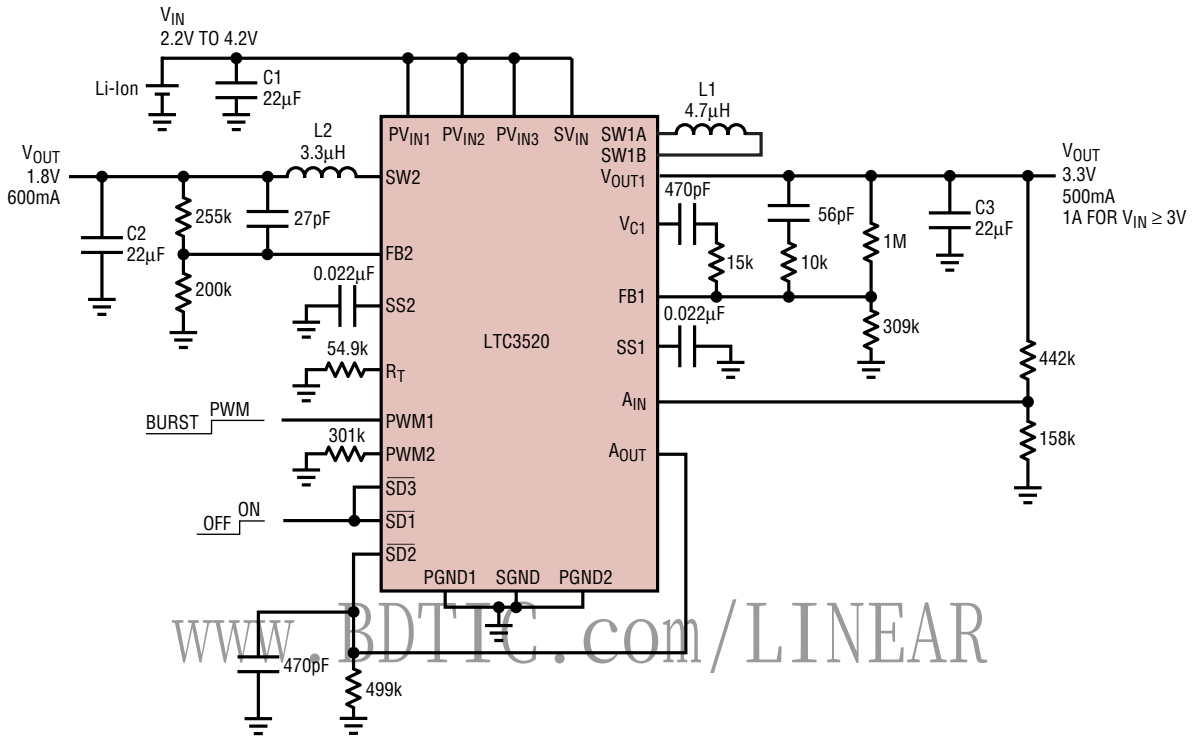
UNINTERRUPTED GROUND PLANE MUST EXIST UNDER ALL COMPONENTS SHOWN IN BOLD AND UNDER TRACES CONNECTING TO THOSE COMPONENTS.

● VIA TO GROUND PLANE

Figure 8. LTC3520 Recommended PCB Layout

TYPICAL APPLICATIONS

Sequenced Buck Converter Start-Up
3.3V at 500mA and 1.8V at 600mA Outputs

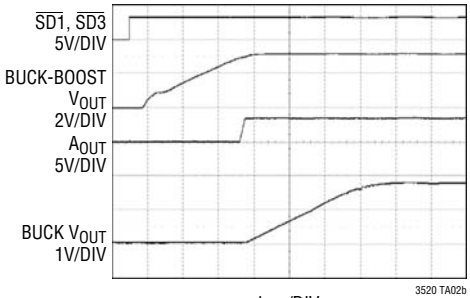


C1, C2, C3: TAIYO YUDEN CERAMIC JMK212BJ226MG-T
L1: TDK RLF7030T-4R7M3R4 4.7µH
L2: TDK RLF7030T-3R3M4R 3.3µH

THE BUCK CONVERTER IS ENABLED WHEN THE BUCK-BOOST OUTPUT VOLTAGE REACHES 3.0V.

3520 TA02a

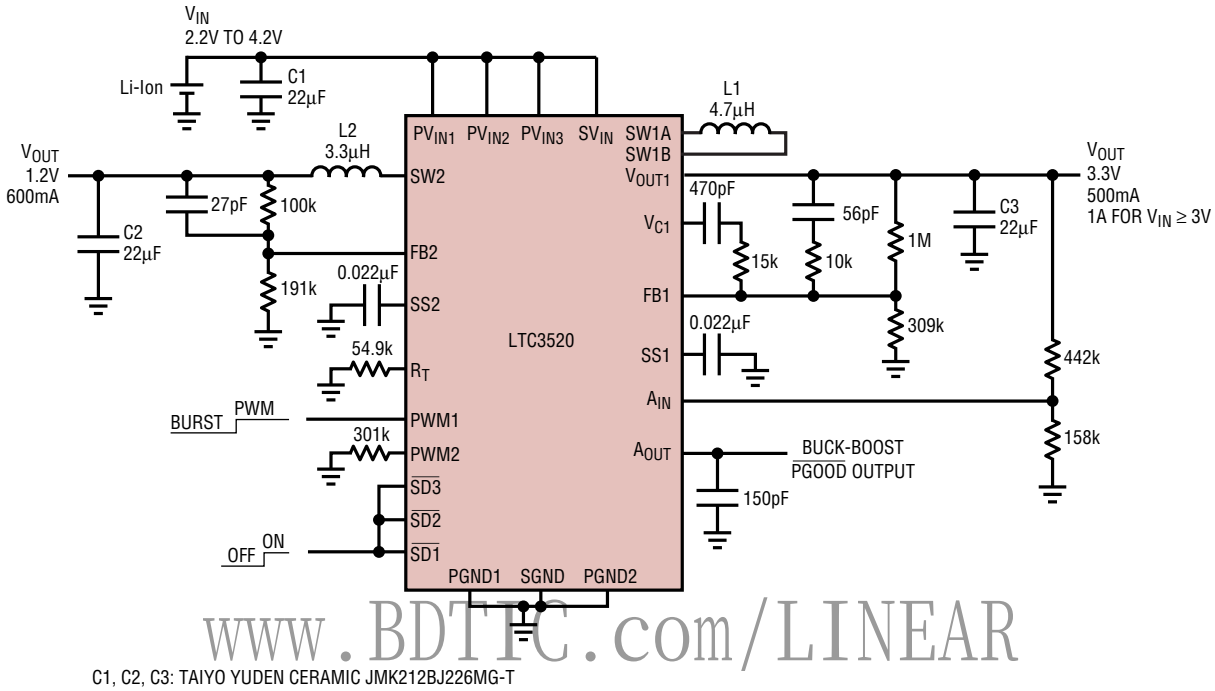
Typical Waveforms During Power-Up



1ms/DIV

TYPICAL APPLICATIONS

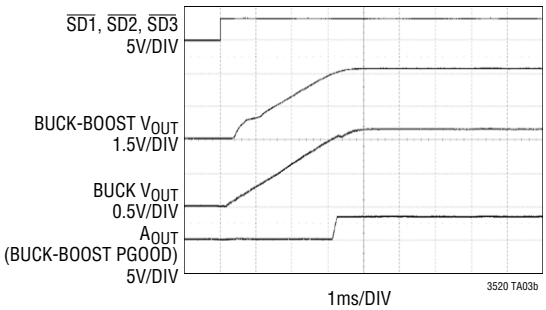
Dual 3.3V at 500mA and 1.2V at 600mA Supplies with Power Good Output



C1, C2, C3: TAIYO YUDEN CERAMIC JMK212BJ226MG-T
L1: TDK RLF7030T-4R7M3R4 4.7µH
L2: TDK RLF7030T-3R3M4R 3.3µH

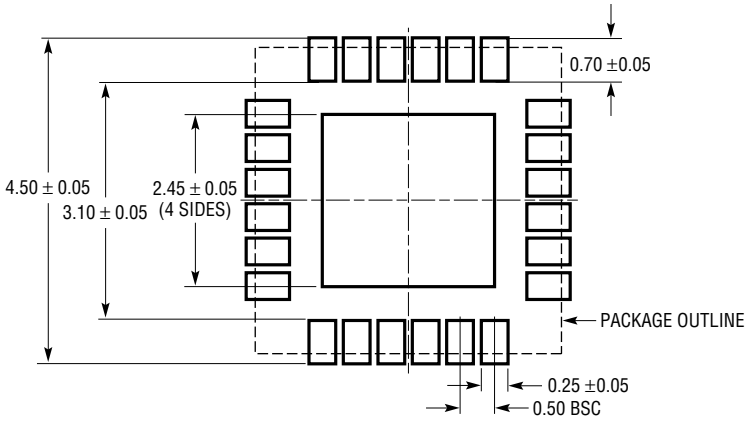
3520 TA03a

Typical Waveforms During Power-Up

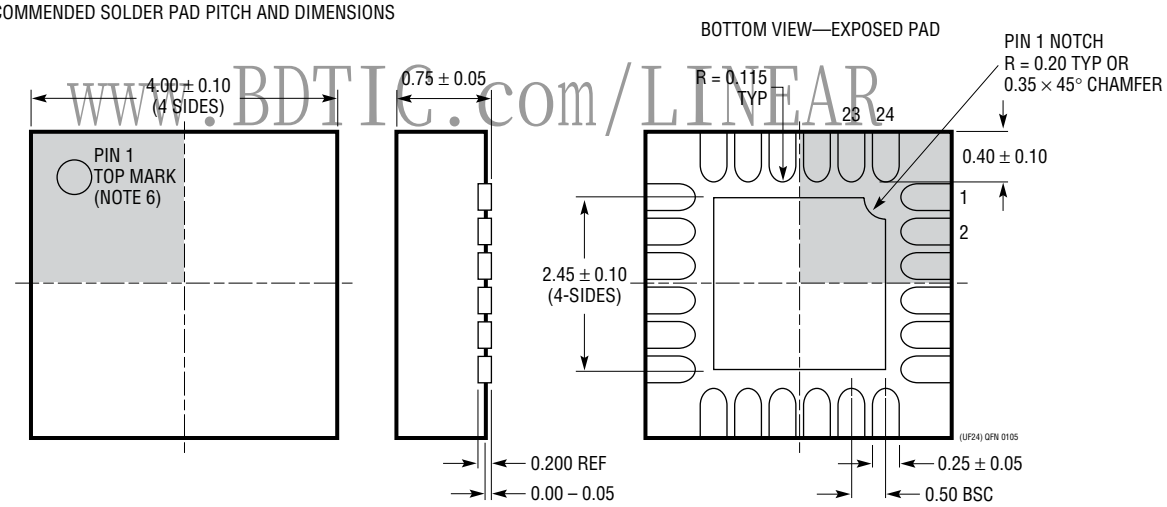


PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



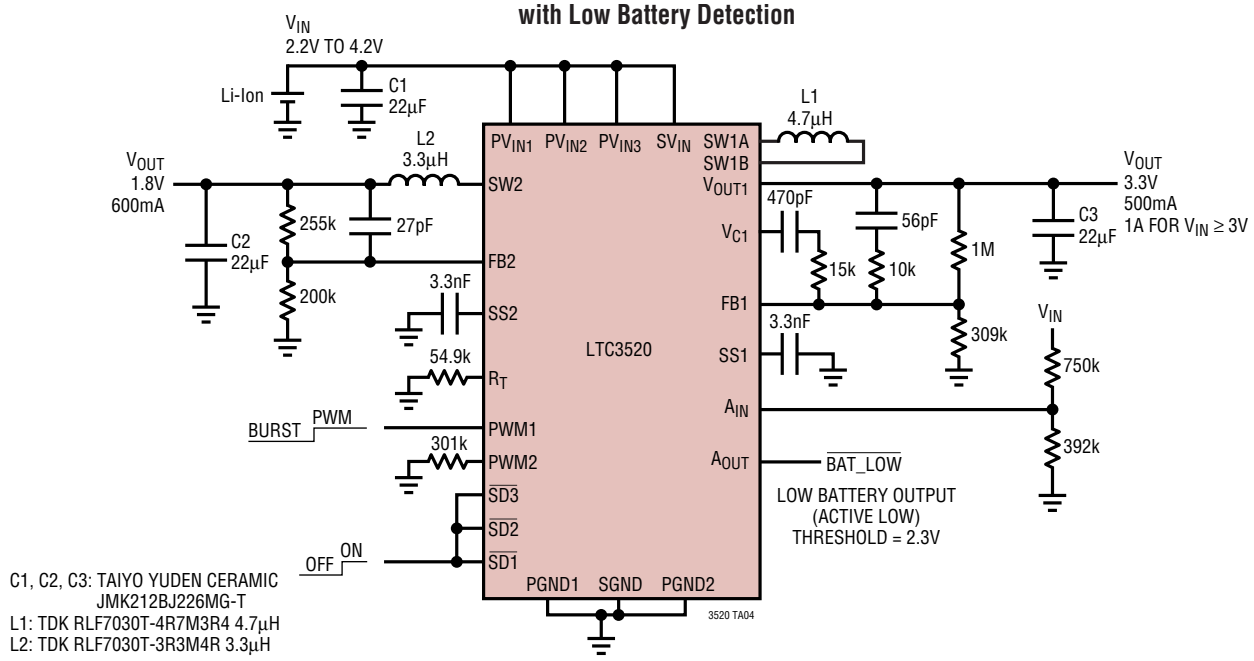
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Li-Ion to 3.3V at 500mA and 1.8V at 600mA with Low Battery Detection



C1, C2, C3: TAIYO YUDEN CERAMIC
JMK212BJ226MG-T
L1: TDK RLF7030T-4R7M3R4 4.7µH
L2: TDK RLF7030T-3R3M4R 3.3µH

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3410/ LTC3410B	300mA (I_{OUT}), 2.25MHz Synchronous Buck DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(RANGE)}$: 0.8V to V_{IN}, I_Q = 26µA, I_{SD} < 1µA, SC70 Packages
LTC3440	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(RANGE)}$: 2.5V to 5.5V, I_Q = 25µA, I_{SD} < 1µA, MS and DFN Packages
LTC3441	1.2A (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 5.5V, $V_{OUT(RANGE)}$: 2.4V to 5.25V, I_Q = 25µA, I_{SD} < 1µA, DFN Package
LTC3442	1.2A (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 5.5V, $V_{OUT(RANGE)}$: 2.4V to 5.25V, I_Q = 35µA, I_{SD} < 1µA, DFN Package
LTC3443	600kHz, 1.2A, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(RANGE)}$: 2.4V to 5.25V, I_Q = 25µA, I_{SD} < 1µA, DFN Package
LTC3444	1.5MHz, 400mA, Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.75V to 5.5V, $V_{OUT(RANGE)}$: 0.5V to 5V, I_{SD} < 1µA, DFN Package
LTC3455	Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger	96% Efficiency, Seamless Transition Between Inputs, I_Q = 110µA, I_{SD} < 2µA, QFN Package
LTC3456	Two Cell Multi-Output DC/DC Converter with USB Power Manager	92% Efficiency, Seamless Transition Between Inputs, I_Q = 180µA, I_{SD} < 1µA, QFN Package
LTC3522	400mA (I_{OUT}) Synchronous Buck-Boost and 200mA Buck DC/DC Converters	V_{IN}: 2.4V to 5.5V, Buck-Boost $V_{OUT(RANGE)}$: 2.2V to 5.25V, Buck $V_{OUT(RANGE)}$: 0.6V to V_{IN}, I_Q = 25µA, I_{SD} < 1µA, QFN Package
LTC3530	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, $V_{OUT(RANGE)}$: 1.8V to 5.5V, I_Q = 40µA, I_{SD} < 1µA, DFN and MSOP Packages
LTC3532	500mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 5.5V, $V_{OUT(RANGE)}$: 2.4V to 5.25V, I_Q = 35µA, I_{SD} < 1µA, DFN and MSOP Packages
LTC3548	400mA/800mA, 2.25MHz Dual Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, DFN and MSOP Packages

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