High Efficiency USB Power Manager + Triple Step-Down DC/DC

FEATURES

Power Manager

- **High Efficiency Switching PowerPath™ Controller with Bat-Track™ Adaptive Output Control**
- **Programmable USB or Wall Current Limit (100mA/500mA/1A)**
- **Full Featured Li-Ion/Polymer Battery Charger**
- 1.5A Maximum Charge Current
- Internal 180mΩ Ideal Diode + External Ideal Diode Controller Powers Load in Battery Mode
- Low No-Load Quiescent Current when Powered from BAT (<32µA)

DC/DCs

- **Triple High Efficiency Step-Down DC/DCs (1A/400mA/400mA I_{OUT})**
- **All Regulators Operate at 2.25MHz**
- Dynamic Voltage Scaling on Two Outputs
- I^2C or Independent Enable, V_{OUT} Controls
- Low No-Load Quiescent Current: 20µA
- 28-Pin (4mm × 5mm × 0.75mm) QFN Package

APPLICATIONS

- HDD-Based MP3 Players, PDAs, GPS, PMPs
- Portable Medical Products
- Handheld Instrumentation
- Other USB-Based Handheld Products

DESCRIPTION

The LTC®3555 family are highly integrated USB compatible power management and battery charger ICs for Li-Ion/Polymer battery applications. They include a high efficiency current limited switching PowerPath manager with automatic load prioritization, a battery charger, an ideal diode and three general purpose synchronous step-down switching regulators.

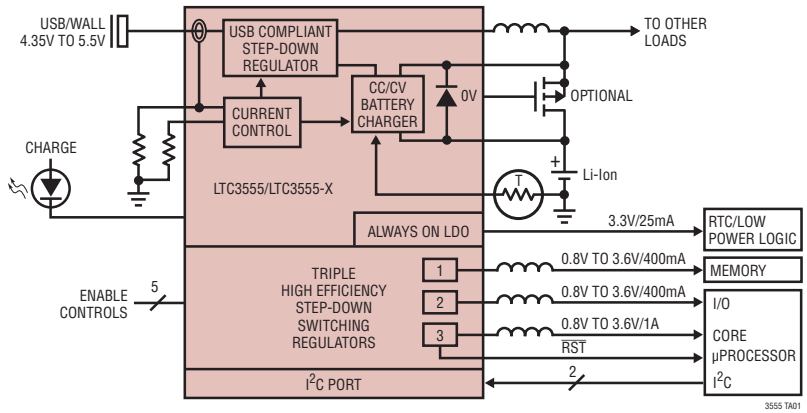
The LTC3555 family limits input current to either 100mA or 500mA for USB applications or 1A for adapter-powered applications. Unlike linear chargers, the LTC3555 family's switching architecture transmits nearly all of the power available from the USB port to the load with minimal loss and heat which eases thermal constraints in small spaces.

Two of the three general purpose switching regulators can provide up to 400mA and the third can deliver 1A. The entire product can be controlled via I^2C or simple I/O. The LTC3555-1/LTC3555-3 versions offer "instant-on" power delivery to the portable product even with a very low battery voltage. The LTC3555-3 version also has a reduced charger float voltage of 4.100V for battery safety and longevity.

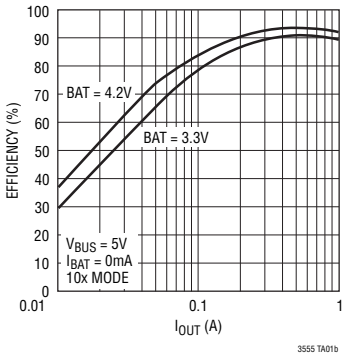
The LTC3555 family is available in the low profile 28-pin (4mm × 5mm × 0.75mm) QFN surface mount package.

TYPICAL APPLICATION

High Efficiency PowerPath Manager and Triple Step-Down Regulator



Switching Regulator Efficiency to System Load (P_{OUT}/P_{BUS})

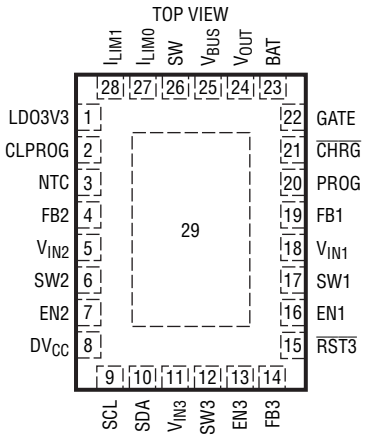


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V_{BUS} (Transient) t < 1ms,
Duty Cycle < 1% ..... –0.3V to 7V
V_{IN1}, V_{IN2}, V_{IN3}, V_{BUS} (Static), DV_{CC},
FB1, FB2, FB3, NTC, BAT, EN1, EN2, EN3,
I_{LIM0}, I_{LIM1}, SCL, SDA, $\overline{RST3}$, $\overline{CHRG}$..... –0.3V to 6V
I_{CLPROG} 3mA
$I_{\overline{RST3}}$, $I_{\overline{CHRG}}$.....50mA
I_{PROG}.....2mA
I_{LDO3V3}.....30mA
I_{SW1}, I_{SW2} 600mA
I_{SW}, I_{SW3}, I_{BAT}, I_{VOUT} 2A
Junction Temperature ..... 125°C
Operating Temperature Range (Note 2).... –40°C to 85°C
Storage Temperature Range..... –65°C to 125°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3555EUFD#PBF	LTC3555EUFD#TRPBF	3555	28-Lead (4mm x 5mm) Plastic QFN	–40°C to 85°C
LTC3555IUFD#PBF	LTC3555IUFD#TRPBF	3555	28-Lead (4mm x 5mm) Plastic QFN	–40°C to 85°C
LTC3555EUFD-1#PBF	LTC3555EUFD-1#TRPBF	35551	28-Lead (4mm x 5mm) Plastic QFN	–40°C to 85°C
LTC3555IUFD-1#PBF	LTC3555IUFD-1#TRPBF	35551	28-Lead (4mm x 5mm) Plastic QFN	–40°C to 85°C
LTC3555EUFD-3#PBF	LTC3555EUFD-3#TRPBF	35553	28-Lead (4mm x 5mm) Plastic QFN	–40°C to 85°C
LTC3555IUFD-3#PBF	LTC3555IUFD-3#TRPBF	35553	28-Lead (4mm x 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, BAT = 3.8V, DV_{CC} = 3.3V, R_{PROG} = 1k, R_{CLPROG} = 3k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PowerPath Switching Regulator							
V_{BUS}	Input Supply Voltage			4.35		5.5	V
I_{BUSLIM}	Total Input Current	1x Mode, V_{OUT} = BAT	●	87	95	100	mA
		5x Mode, V_{OUT} = BAT	●	436	460	500	mA
		10x Mode, V_{OUT} = BAT	●	800	860	1000	mA
		Suspend Mode, V_{OUT} = BAT	●	0.31	0.38	0.50	mA
I_{VBUSQ}	V_{BUS} Quiescent Current	1x Mode, I_{OUT} = 0mA			7		mA
		5x Mode, I_{OUT} = 0mA			15		mA
		10x Mode, I_{OUT} = 0mA			15		mA
		Suspend Mode, I_{OUT} = 0mA			0.044		mA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
h_{CLPROG} (Note 4)	Ratio of Measured V_{BUS} Current to CLPROG Program Current	1x Mode 5x Mode 10x Mode Suspend Mode			224 1133 2140 11.3		mA/mA mA/mA mA/mA mA/mA
$I_{OUT(POWERPATH)}$	V_{OUT} Current Available Before Loading BAT	1x Mode, BAT = 3.3V 5x Mode, BAT = 3.3V 10x Mode, BAT = 3.3V Suspend Mode			135 672 1251 0.32		mA mA mA mA
V_{CLPROG}	CLPROG Servo Voltage in Current Limit	1x, 5x, 10x Modes Suspend Mode			1.188 100		V mV
V_{UVLO_VBUS}	V_{BUS} Undervoltage Lockout	Rising Threshold Falling Threshold		 3.95	4.30 4.00	4.35	V V
$V_{UVLO\_VBUS-BAT}$	V_{BUS} to BAT Differential Undervoltage Lockout	Rising Threshold Falling Threshold			200 50		mV mV
V_{OUT}	V_{OUT} Voltage	1x, 5x, 10x Modes, 0V < BAT < 4.2V, I_{OUT} = 0mA, Battery Charger Off		3.4	BAT + 0.3	4.7	V
		USB Suspend Mode, I_{VOUT} = 250µA		4.5	4.6	4.7	V
f_{OSC}	Switching Frequency			1.8	2.25	2.7	MHz
$R_{PMOS\_POWERPATH}$	PMOS On Resistance				0.18		Ω
$R_{NMOS\_POWERPATH}$	NMOS On Resistance				0.30		Ω
$I_{PEAK\_POWERPATH}$	Peak Switch Current Limit	1x, 5x Modes 10x			2 3		A A
Battery Charger							
V_{FLOAT}	BAT Regulated Output Voltage	LTC3555/LTC3555-1 LTC3555/LTC3555-1 LTC3555-3 LTC3555-3	 ● ●	4.179 4.165 4.079 4.065	4.200 4.200 4.100 4.100	4.221 4.235 4.121 4.135	V V V V
I_{CHG}	Constant Current Mode Charge Current	R_{PROG} = 1k R_{PROG} = 5k		980 185	1022 204	1065 223	mA mA
I_{BAT}	Battery Drain Current	V_{BUS} > V_{UVLO}, Battery Charger Off, I_{VOUT} = 0µA V_{BUS} = 0V, I_{VOUT} = 0µA (Ideal Diode Mode) LTC3555 LTC3555-1/LTC3555-3		2	3.5 27 32	5 38 44	µA µA µA
V_{PROG}	PROG Pin Servo Voltage				1.000		V
V_{PROG_TRKL}	PROG Pin Servo Voltage in Trickle Charge	BAT < V_{TRKL}			0.100		V
$V_{C/10}$	C/10 Threshold Voltage at PROG				100		mV
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				1022		mA/mA
I_{TRKL}	Trickle Charge Current	BAT < V_{TRKL}			100		mA
V_{TRKL}	Trickle Charge Threshold Voltage	BAT Rising		2.7	2.85	3.0	V
ΔV_{TRKL}	Trickle Charge Hysteresis Voltage				135		mV
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–75	–100	–125	mV
t_{TERM}	Safety Timer Termination	Timer Starts when BAT = V_{FLOAT}		3.3	4	5	Hour
t_{BADBAT}	Bad Battery Termination Time	BAT < V_{TRKL}		0.42	0.5	0.63	Hour
$h_{C/10}$	End of Charge Indication Current Ratio	(Note 5)		0.088	0.1	0.112	mA/mA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 5mA			65	100	mV
$I_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Leakage Current	$V_{\overline{CHRG}}$ = 5V				1	µA
R_{ON_CHG}	Battery Charger Power FET On Resistance (Between V_{OUT} and BAT)				0.18		Ω
T_{LIM}	Junction Temperature in Constant Temperature Mode				110		°C
NTC							
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising Threshold Hysteresis		75.0	76.5 1.5	78.0	$\%V_{BUS}$ $\%V_{BUS}$
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling Threshold Hysteresis		33.4	34.9 1.5	36.4	$\%V_{BUS}$ $\%V_{BUS}$
V_{DIS}	NTC Disable Threshold Voltage	Falling Threshold Hysteresis		0.7	1.7 50	2.7	$\%V_{BUS}$ mV
I_{NTC}	NTC Leakage Current	V_{NTC} = V_{BUS} = 5V		–50		50	nA
Ideal Diode							
V_{FWD}	Forward Voltage	V_{BUS} = 0V, I_{VOUT} = 10mA I_{VOUT} = 10mA			2 15		mV mV
$R_{DROPOUT}$	Internal Diode On Resistance, Dropout	V_{BUS} = 0V			0.18		Ω
I_{MAX_DIODE}	Internal Diode Current Limit			1.6			A
Always On 3.3V LDO Supply							
V_{LDO3V3}	Regulated Output Voltage	0mA < I_{LDO3V3} < 25mA		3.1	3.3	3.5	V
R_{CL_LDO3V3}	Closed-Loop Output Resistance				4		Ω
R_{OL_LDO3V3}	Dropout Output Resistance				23		Ω
Logic (I_{LIM0}, I_{LIM1}, EN1, EN2, EN3)							
V_{IL}	Logic Low Input Voltage					0.4	V
V_{IH}	Logic High Input Voltage			1.2			V
I_{PD1}	I_{LIM0}, I_{LIM1}, EN1, EN2, EN3 Pull-Down Currents				2		µA
I^2C Port							
DV_{CC}	Input Supply Voltage			1.6		5.5	V
I_{DVCC}	DV_{CC} Current	SCL/SDA = 0kHz			0.5		µA
V_{DVCC_UVLO}	DV_{CC} UVLO				1.0		V
ADDRESS	I^2C Address				0001 001[0]		
V_{IH}, SDA, SCL	Input High Threshold			70			$\%DV_{CC}$
V_{IL}, SDA, SCL	Input Low Threshold					30	$\%DV_{CC}$
I_{PD2} SDA, SCL	Pull-Down Current				2		µA
V_{OL}	Digital Output Low (SDA)	I_{PULLUP} = 3mA				0.4	V
f_{SCL}	Clock Operating Frequency					400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
t_{HD_STA}	Hold Time After (Repeated) Start Condition			0.6			µs
t_{SU_STA}	Repeated Start Condition Setup Time			0.6			µs

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SU_STD}	Stop Condition Time			0.6			µs
$t_{HD\_DAT(OUT)}$	Data Hold Time			225			ns
$t_{HD\_DAT(IN)}$	Input Data Hold Time			0		900	ns
t_{SU_DAT}	Data Setup Time			100			ns
t_{LOW}	Clock Low Period			1.3			µs
t_{HIGH}	Clock High Period			0.6			µs
t_f	Clock Data Fall Time			20		300	ns
t_r	Clock Data Rise Time			20		300	ns
t_{SP}	Spike Suppression Time					50	ns
General Purpose Switching Regulators 1, 2 and 3							
$V_{IN1,2,3}$	Input Supply Voltage			2.7		5.5	V
$V_{OUTUVLO}$	V_{OUT} UVLO—V_{OUT} Falling V_{OUT} UVLO—V_{OUT} Rising	$V_{IN1,2,3}$ Connected to V_{OUT} Through Low Impedance. Switching Regulators are Disabled in UVLO		2.5	2.6 2.8	 2.9	V V
f_{OSC}	Oscillator Frequency			1.8	2.25	2.7	MHz
$I_{FB1,2,3}$	FBx Input Current	$V_{FB1,2,3}$ = 0.85V		–50		50	nA
$D_{1,2,3}$	Maximum Duty Cycle			100			%
$R_{SW1,2,3\_PD}$	SWx Pull-Down in Shutdown				10		kΩ
General Purpose Switching Regulator 1							
I_{VIN1}	Pulse Skip Mode Input Current Burst Mode Input Current Forced Burst Mode® Input Current LDO Mode Input Current Shutdown Input Current	I_{OUT1} = 0µA (Note 6) I_{OUT1} = 0µA (Note 6) I_{OUT1} = 0µA (Note 6) I_{OUT1} = 0µA (Note 6) I_{OUT1} = 0µA, FB1 = 0V			225 35 20 20	 60 35 35 1	µA µA µA µA µA
I_{LIMSW1}	PMOS Switch Current Limit	Pulse Skip/Burst Mode Operation		600	800	1100	mA
I_{OUT1}	Available Output Current	Pulse Skip/Burst Mode Operation (Note 7) Forced Burst Mode Operation (Note 7) LDO Mode (Note 7)		400 60 50			mA mA mA
V_{FB1}	V_{FB1} Servo Voltage	(Note 8)	●	0.78	0.80	0.82	V
R_{P1}	PMOS $R_{DS(ON)}$				0.6		Ω
R_{N1}	NMOS $R_{DS(ON)}$				0.7		Ω
R_{LDO_CL1}	LDO Mode Closed-Loop R_{OUT}				0.25		Ω
R_{LDO_OL1}	LDO Mode Open-Loop R_{OUT}	(Note 9)			2.5		Ω
General Purpose Switching Regulator 2							
I_{VIN2}	Pulse Skip Mode Input Current Burst Mode Input Current Forced Burst Mode Input Current LDO Mode Input Current Shutdown Input Current	I_{OUT2} = 0µA (Note 6) I_{OUT2} = 0µA (Note 6) I_{OUT2} = 0µA (Note 6) I_{OUT2} = 0µA (Note 6) I_{OUT2} = 0µA, FB2 = 0V			225 35 20 20	 60 35 35 1	µA µA µA µA µA
I_{LIMSW2}	PMOS Switch Current Limit	Pulse Skip/Burst Mode Operation		600	800	1100	mA
I_{OUT2}	Available Output Current	Pulse Skip/Burst Mode Operation (Note 7) Forced Burst Mode Operation (Note 7) LDO Mode (Note 7)		400 60 50			mA mA mA

Burst Mode is a registered trademark of Linear Technology Corporation.

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{FBHIGH2}$	Maximum Servo Voltage	Full Scale (1, 1, 1, 1) (Note 8)	●	0.78	0.80	0.82	V
V_{FBLOW2}	Minimum Servo Voltage	Zero Scale (0, 0, 0, 0) (Note 8)		0.405	0.425	0.445	V
V_{LSB2}	V_{FB2} Servo Voltage Step Size				25		mV
R_{P2}	PMOS $R_{DS(ON)}$				0.6		Ω
R_{N2}	NMOS $R_{DS(ON)}$				0.7		Ω
R_{LDO_CL2}	LDO Mode Closed-Loop R_{OUT}				0.25		Ω
R_{LDO_OL2}	LDO Mode Open-Loop R_{OUT}	(Note 9)			2.5		Ω
General Purpose Switching Regulator 3							
I_{VIN3}	Pulse Skip Mode Input Current Burst Mode Input Current Forced Burst Mode Input Current LDO Mode Input Current Shutdown Input Current	I_{OUT3} = 0µA (Note 6) I_{OUT3} = 0µA (Note 6) I_{OUT3} = 0µA (Note 6) I_{OUT3} = 0µA (Note 6) I_{OUT3} = 0µA, FB3 = 0V			225 35 20 20	 60 35 35 1	µA µA µA µA µA
I_{LIMSW3}	PMOS Switch Current Limit	Pulse Skip/Burst Mode Operation		1500	2000	2800	mA
I_{OUT3}	Available Output Current	Pulse Skip/Burst Mode Operation (Note 7) Forced Burst Mode Operation (Note 7) LDO Mode (Note 7)		1000 150 50			mA mA mA
$V_{FBHIGH3}$	Maximum Servo Voltage	Full Scale (1, 1, 1, 1) (Note 8)	●	0.78	0.80	0.82	V
V_{FBLOW3}	Minimum Servo Voltage	Zero Scale (0, 0, 0, 0) (Note 8)		0.405	0.425	0.445	V
V_{LSB3}	V_{FB} Servo Voltage Step Size				25		mV
R_{P3}	PMOS $R_{DS(ON)}$				0.18		Ω
R_{N3}	NMOS $R_{DS(ON)}$				0.30		Ω
R_{LDOCL3}	LDO Mode Closed Loop R_{OUT}				0.25		Ω
R_{LDOOL3}	LDO Mode Open Loop R_{OUT}	(Note 9)			2.5		Ω
$t_{\overline{RST3}}$	Power On Reset Time for Switching Regulator	V_{FB3} Within 92% of Final Value to $\overline{RST3}$ Hi-Z			230		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3555E/LTC3555E-X are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3555I/LTC3555I-X are guaranteed to meet performance specifications over the full –40°C to 85°C operating temperature range.

Note 3: The LTC3555/LTC3555-X include overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Total input current is the sum of quiescent current, I_{VBUSQ}, and measured current given by:

$V_{CLPROG}/R_{CLPROG} \bullet (h_{CLPROG} + 1)$

Note 5: $h_{C/10}$ is expressed as a fraction of measured full charge current with indicated PROG resistor.

Note 6: FBx above regulation such that regulator is in sleep. Specification does not include resistive divider current reflected back to V_{INx}.

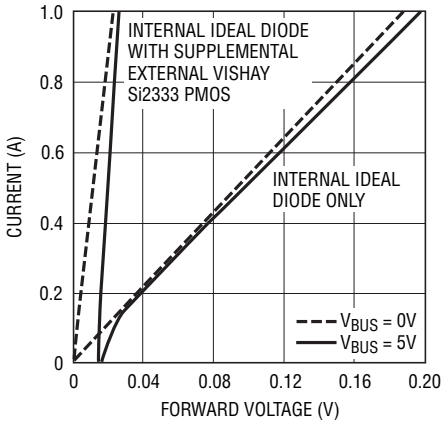
Note 7: Guaranteed by design but not explicitly tested.

Note 8: Applies to pulse skip, Burst Mode operation and forced Burst Mode operation only.

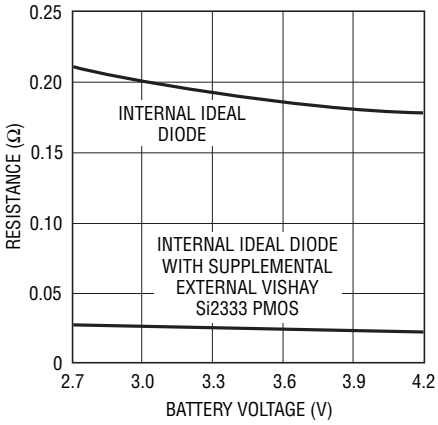
Note 9: Inductor series resistance adds to open-loop R_{OUT}.

TYPICAL PERFORMANCE CHARACTERISTICS

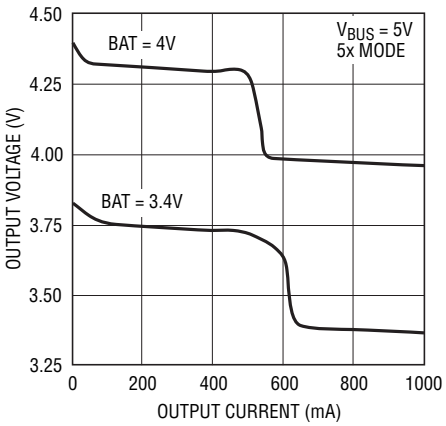
Ideal Diode V-I Characteristics



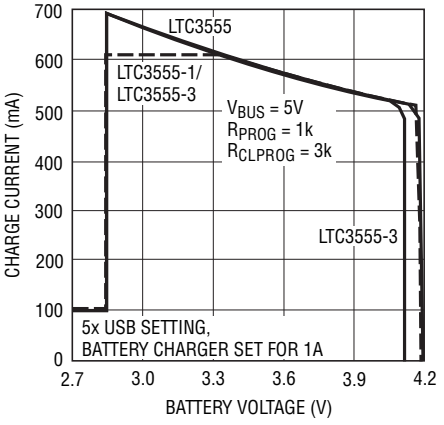
Ideal Diode Resistance vs Battery Voltage



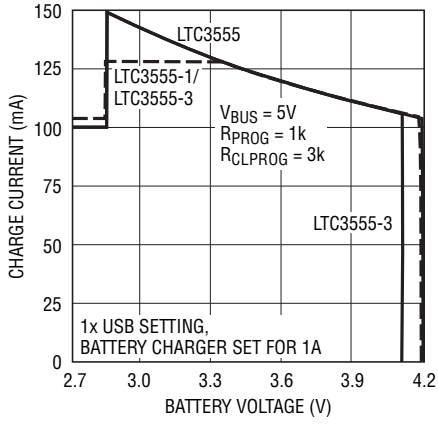
Output Voltage vs Output Current (Battery Charger Disabled)



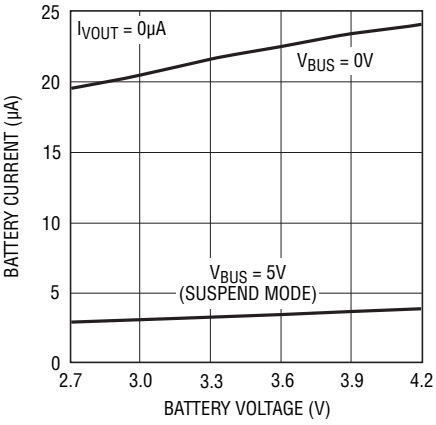
USB Limited Battery Charge Current vs Battery Voltage



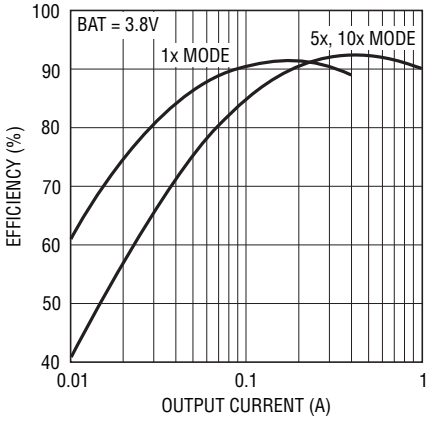
USB Limited Battery Charge Current vs Battery Voltage



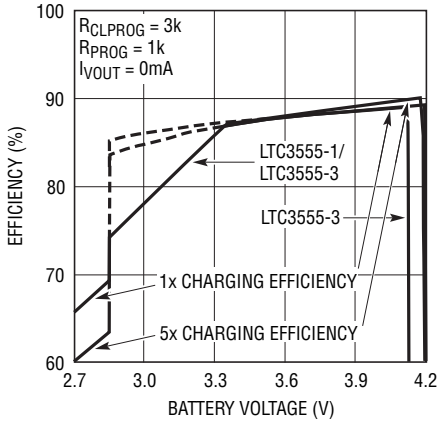
Battery Drain Current vs Battery Voltage



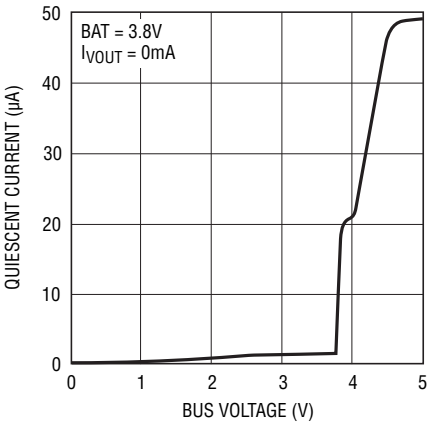
PowerPath Switching Regulator Efficiency vs Output Current



Battery Charging Efficiency vs Battery Voltage with No External Load (P_{BAT}/P_{BUS})

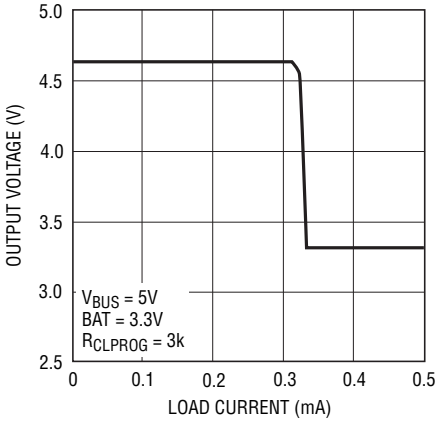


V_{BUS} Current vs V_{BUS} Voltage (Suspend)



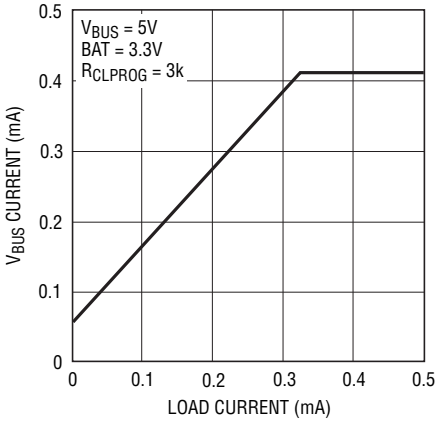
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage vs Load Current in Suspend



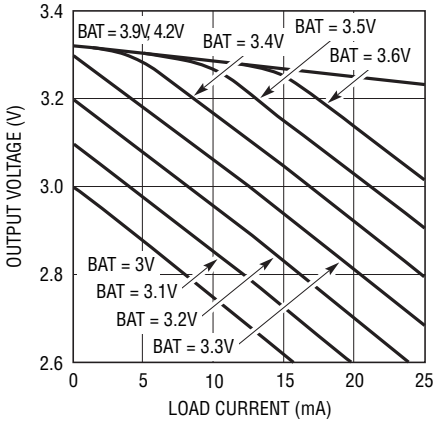
3555 G10

V_{BUS} Current vs Load Current in Suspend



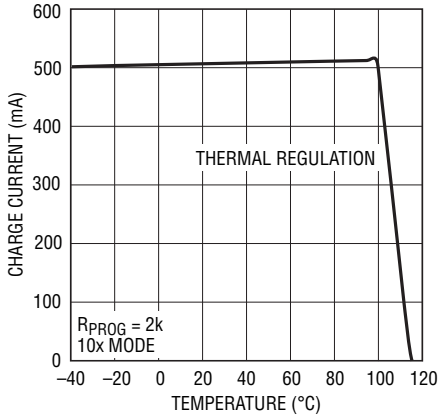
3555 G11

3.3V LDO Output Voltage vs Load Current, V_{BUS} = 0V



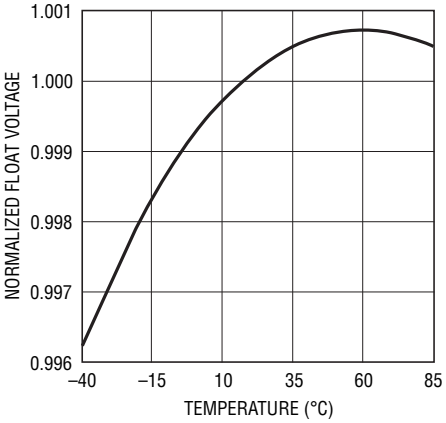
3555 G12

Battery Charge Current vs Temperature



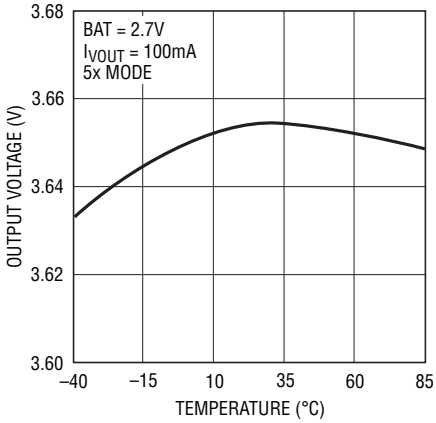
3555 G13

Normalized Battery Charger Float Voltage vs Temperature



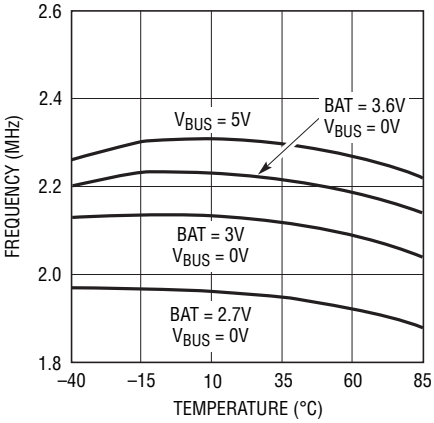
3555 G14

Low-Battery (Instant-On) Output Voltage vs Temperature



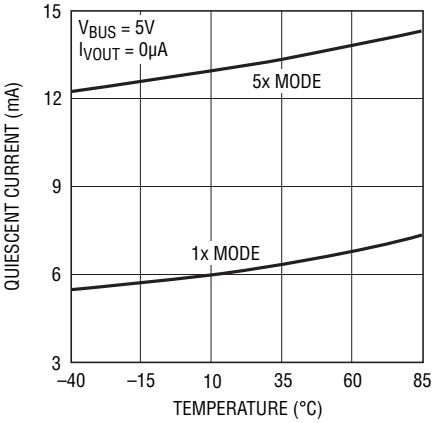
3555 G15

Oscillator Frequency vs Temperature



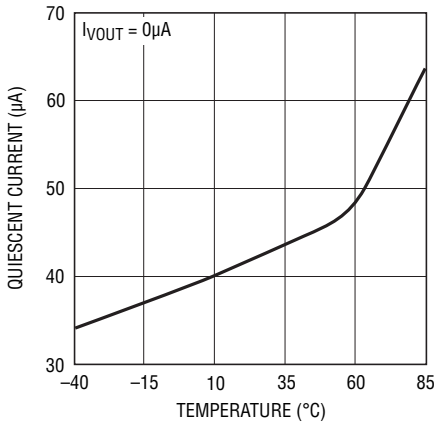
3555 G16

V_{BUS} Quiescent Current vs Temperature



3555 G17

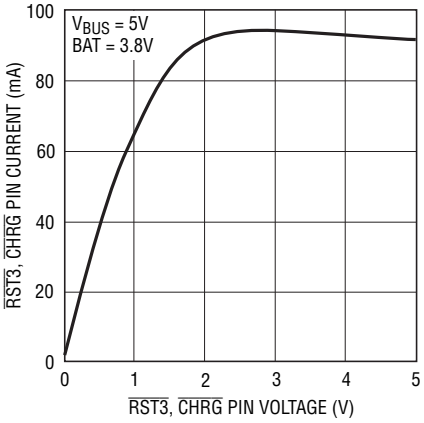
V_{BUS} Quiescent Current in Suspend vs Temperature



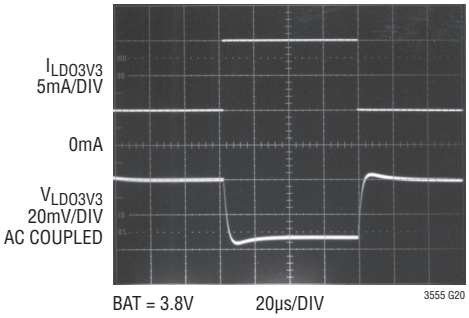
3555 G18

TYPICAL PERFORMANCE CHARACTERISTICS

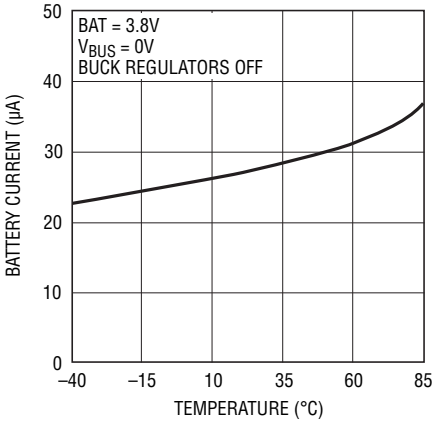
$\overline{RST3}$, $\overline{CHRG}$ Pin Current vs Voltage (Pull-Down State)



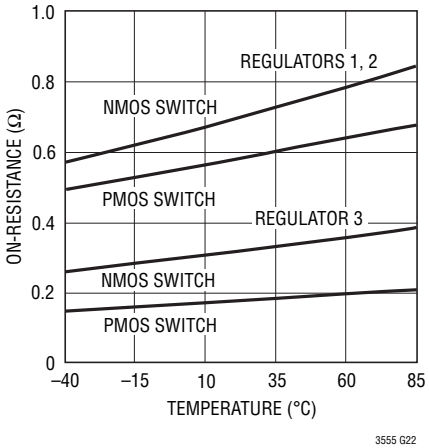
3.3V LDO Step Response (5mA to 15mA)



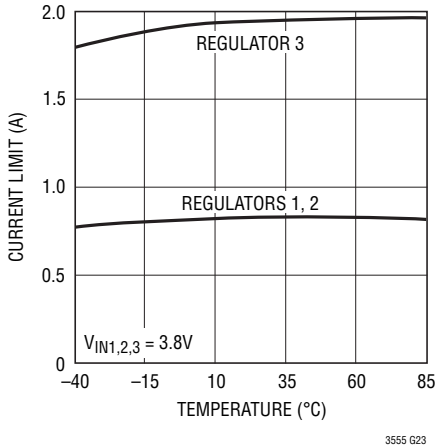
Battery Drain Current vs Temperature



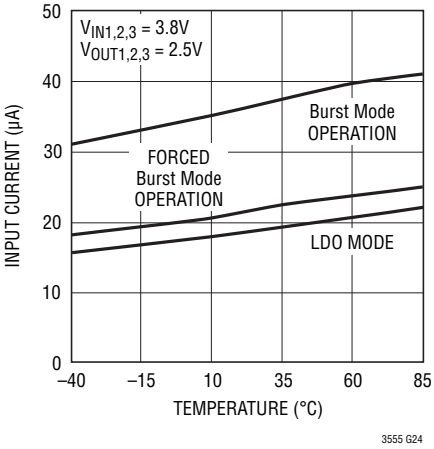
$R_{DS(ON)}$ for Switching Regulator Power Switches vs Temperature



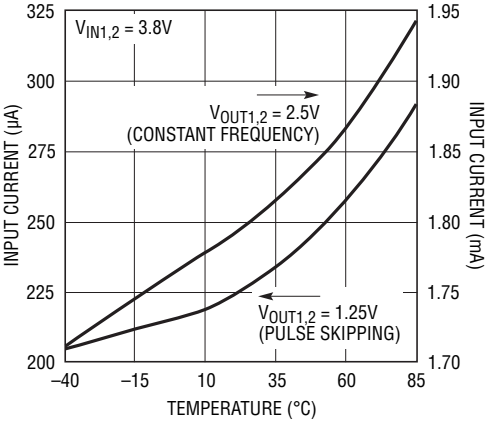
Switching Regulator Current Limit vs Temperature



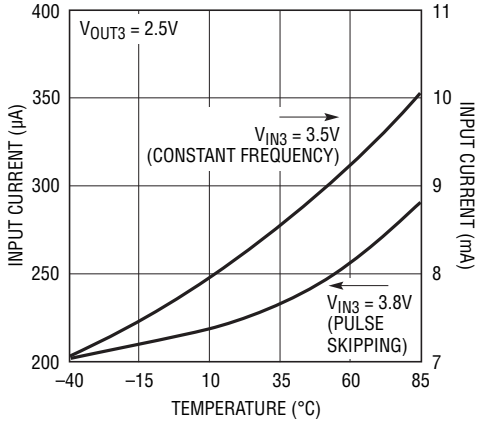
Switching Regulator Low Power Mode Quiescent Currents



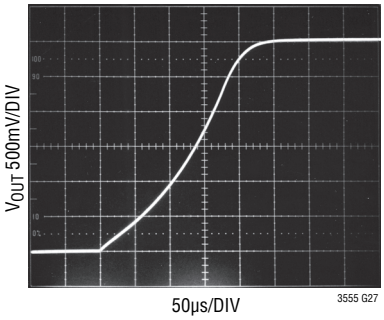
Switching Regulators 1, 2 Pulse Skip Mode Quiescent Currents



Switching Regulator 3 Pulse Skip Mode Quiescent Currents

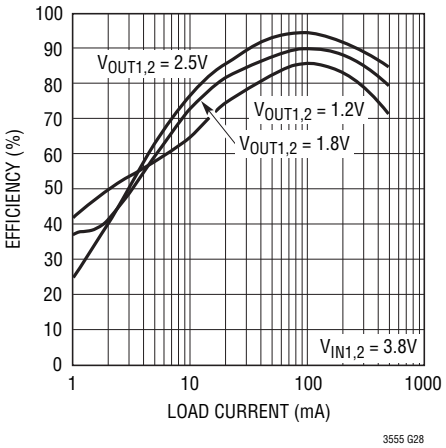


Switching Regulator Soft-Start Waveform

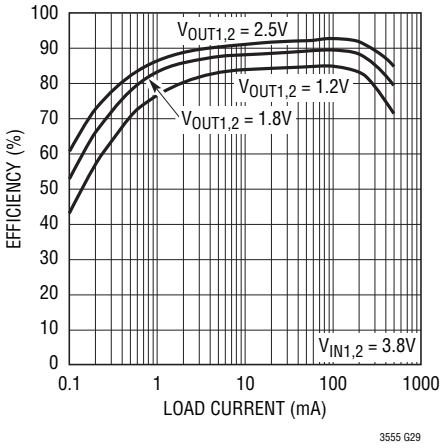


TYPICAL PERFORMANCE CHARACTERISTICS

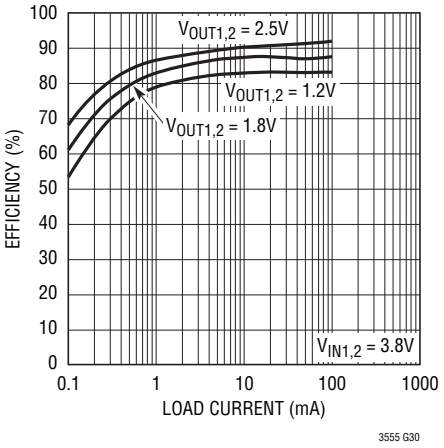
Switching Regulators 1, 2 Pulse Skip Mode Efficiency



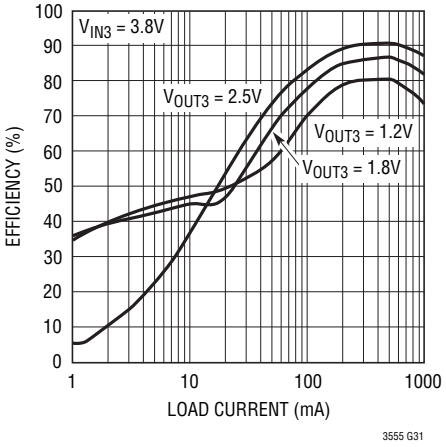
Switching Regulators 1, 2 Burst Mode Efficiency



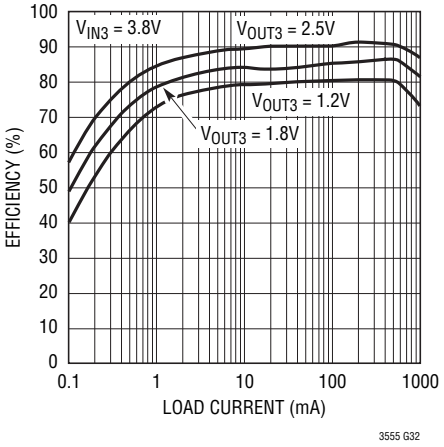
Switching Regulators 1, 2 Forced Burst Mode Efficiency



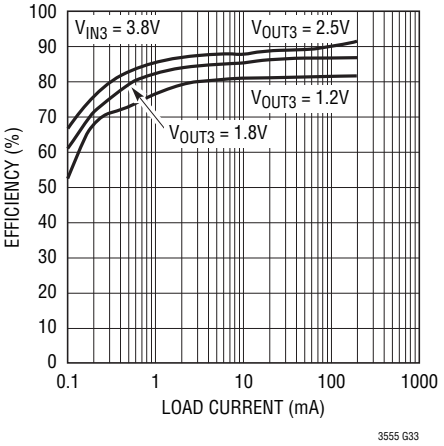
Switching Regulator 3 Pulse Skip Mode Efficiency



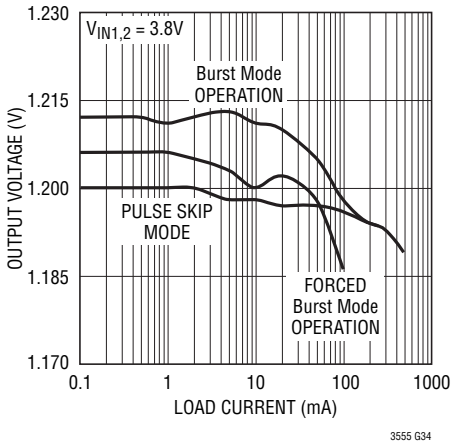
Switching Regulator 3 Burst Mode Efficiency



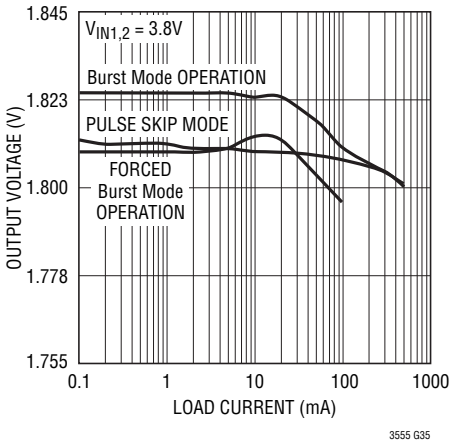
Switching Regulator 3 Forced Burst Mode Efficiency



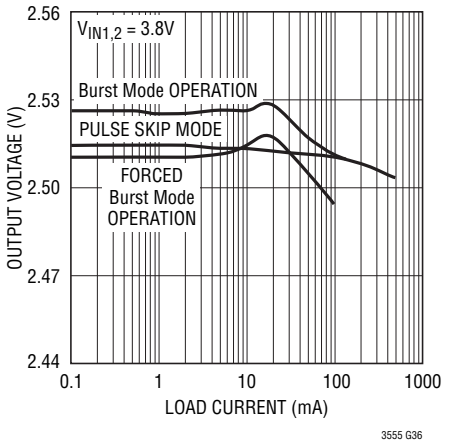
Switching Regulators 1, 2 Load Regulation at $V_{OUT1,2}$ = 1.2V



Switching Regulators 1, 2 Load Regulation at $V_{OUT1,2}$ = 1.8V



Switching Regulators 1, 2 Load Regulation at $V_{OUT1,2}$ = 2.5V



PIN FUNCTIONS

LDO3V3 (Pin 1): 3.3V LDO Output Pin. This pin provides a regulated always-on 3.3V supply voltage. LDO3V3 gets its power from V_{OUT}. It may be used for light loads such as a watchdog microprocessor or real time clock. A 1µF capacitor is required from LDO3V3 to ground. If the LDO3V3 output is not used it should be disabled by connecting it to V_{OUT}.

CLPROG (Pin 2): USB Current Limit Program and Monitor Pin. A resistor from CLPROG to ground determines the upper limit of the current drawn from the V_{BUS} pin. A fraction of the V_{BUS} current is sent to the CLPROG pin when the synchronous switch of the PowerPath switching regulator is on. The switching regulator delivers power until the CLPROG pin reaches 1.188V. Several V_{BUS} current limit settings are available via user input which will typically correspond to the 500mA and 100mA USB specifications. A multi-layer ceramic averaging capacitor or R-C network is required at CLPROG for filtering.

NTC (Pin 3): Input to the Thermistor Monitoring Circuits. The NTC pin connects to a battery's thermistor to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until it re-enters the valid range. A low drift bias resistor is required from V_{BUS} to NTC and a thermistor is required from NTC to ground. If the NTC function is not desired, the NTC pin should be grounded.

FB2 (Pin 4): Feedback Input for Switching Regulator 2. When regulator 2's control loop is complete, this pin servos to 1 of 16 possible set-points based on the commanded value from the I^2C serial port. See Table 4.

V_{IN2} (Pin 5): Power Input for Switching Regulator 2. This pin will generally be connected to V_{OUT}. A 1µF MLCC capacitor is recommended on this pin.

SW2 (Pin 6): Power Transmission Pin for Switching Regulator 2.

EN2 (Pin 7): Logic Input. This logic input pin independently enables switching regulator 2. This pin is logically OR-ed with its corresponding bit in the I^2C serial port. See Table 2.

DV_{CC} (Pin 8): Logic Supply for the I^2C Serial Port. If the serial port is not needed it can be disabled by grounding DV_{CC}. When DV_{CC} is grounded, chip control is automatically passed to the individual logic input pins.

SCL (Pin 9): Clock Input Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{CC}. If DV_{CC} is grounded, the SCL pin is equivalent to the B5 bit in the I^2C serial port. SCL in conjunction with SDA determine the operating modes of switching regulators 1, 2 and 3 when DV_{CC} is grounded. See Tables 2 and 5.

SDA (Pin 10): Data Input Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{CC}. If DV_{CC} is grounded, the SDA pin is equivalent to the B6 bit in the I^2C serial port. SDA in conjunction with SCL determine the operating modes of switching regulators 1, 2 and 3 when DV_{CC} is grounded. See Tables 2 and 5.

V_{IN3} (Pin 11): Power Input for Switching Regulator 3. This pin will generally be connected to V_{OUT}. A 1µF MLCC capacitor is recommended on this pin.

SW3 (Pin 12): Power Transmission Pin for Switching Regulator 3.

EN3 (Pin 13): Logic Input. This logic input pin independently enables switching regulator 3. This pin is logically OR-ed with its corresponding bit in the I^2C serial port. See Table 2.

FB3 (Pin 14): Feedback Input for Switching Regulator 3. When regulator 3's control loop is complete, this pin servos to 1 of 16 possible set-points based on the commanded value from the I^2C serial port. See Table 4.

$\overline{RST3}$ (Pin 15): Logic Output. This in an open-drain output which indicates that switching regulator 3 has settled to its final value. It can be used as a power-on reset for the primary microprocessor or to enable the other switching regulators for supply sequencing.

EN1 (Pin 16): Logic Input. This logic input pin independently enables switching regulator 1. This pin is logically OR-ed with its corresponding bit in the I^2C serial port. See Table 2.

PIN FUNCTIONS

SW1 (Pin 17): Power Transmission Pin for Switching Regulator 1.

V_{IN1} (Pin 18): Power Input for Switching Regulator 1. This pin will generally be connected to V_{OUT}. A 1µF MLCC capacitor is recommended on this pin.

FB1 (Pin 19): Feedback Input for Switching Regulator 1. When regulator 1's control loop is complete, this pin servos to a fixed voltage of 0.8V.

PROG (Pin 20): Charge Current Program and Charge Current Monitor Pin. Connecting a resistor from PROG to ground programs the charge current. If sufficient input power is available in constant-current mode, this pin servos to 1V. The voltage on this pin always represents the actual charge current.

$\overline{CHRG}$ (Pin 21): Open-Drain Charge Status Output. The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{CHRG}$: charging, not charging, unresponsive battery and battery temperature out of range. $\overline{CHRG}$ is modulated at 35kHz and switches between a low and a high duty cycle for easy recognition by either humans or microprocessors. See Table 1. $\overline{CHRG}$ requires a pull-up resistor and/or LED to provide indication.

GATE (Pin 22): Analog Output. This pin controls the gate of an optional external P-channel MOSFET transistor used to supplement the ideal diode between V_{OUT} and BAT. The external ideal diode operates in parallel with the internal ideal diode. The source of the P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. If the external ideal diode FET is not used, GATE should be left floating.

BAT (Pin 23): Single Cell Li-Ion Battery Pin. Depending on available V_{BUS} power, a Li-Ion battery on BAT will either deliver power to V_{OUT} through the ideal diode or be charged from V_{OUT} via the battery charger.

V_{OUT} (Pin 24): Output voltage of the Switching PowerPath Controller and Input Voltage of the Battery Charger. The majority of the portable product should be powered from V_{OUT}. The LTC3555 family will partition the available power between the external load on V_{OUT} and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted power from V_{BUS} or if the V_{BUS} power source is removed. V_{OUT} should be bypassed with a low impedance ceramic capacitor.

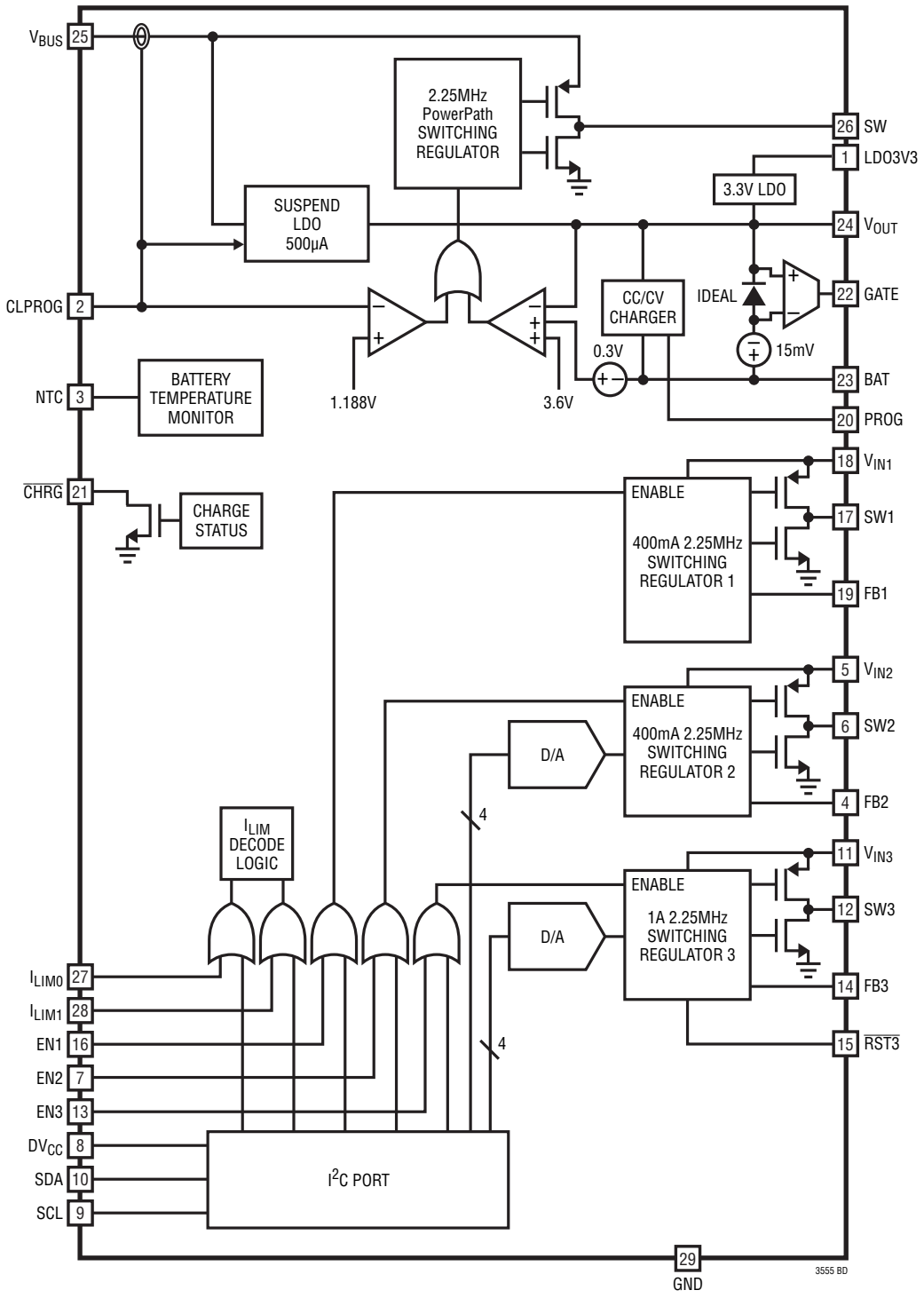
V_{BUS} (Pin 25): Primary Input Power Pin. This pin delivers power to V_{OUT} via the SW pin by drawing controlled current from a DC source such as a USB port or wall adapter.

SW (Pin 26): Power Transmission Pin for the USB Power Path. The SW pin delivers power from V_{BUS} to V_{OUT} via the step-down switching regulator. A 3.3µH inductor should be connected from SW to V_{OUT}.

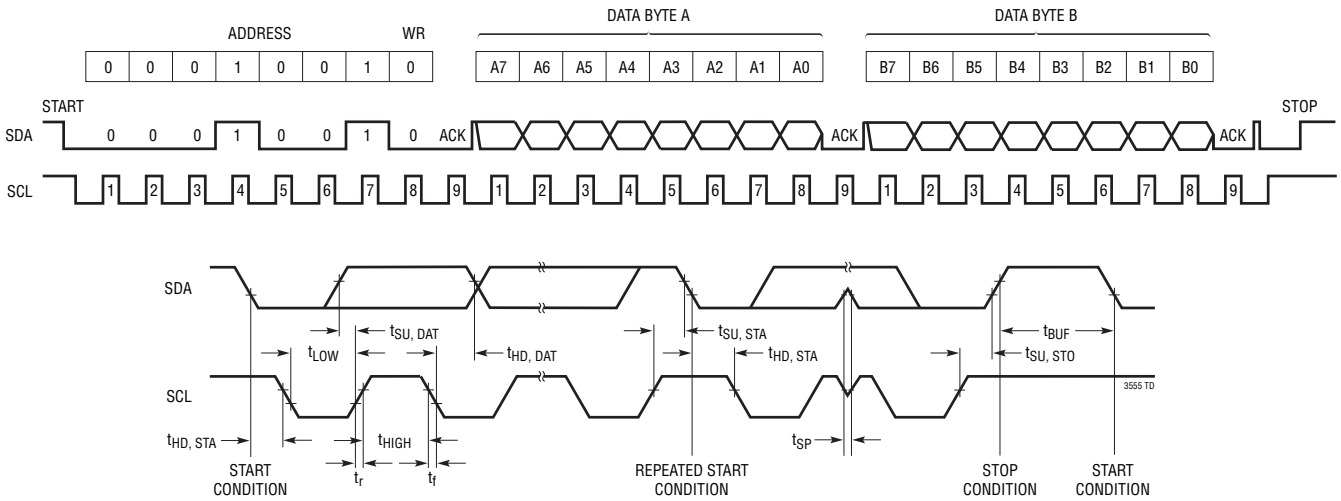
I_{LIM0}, I_{LIM1} (Pins 27, 28): Logic Inputs. I_{LIM0} and I_{LIM1} control the current limit of the PowerPath switching regulator. See Table 3. Both of the I_{LIM0} and I_{LIM1} pins are logically OR-ed with their corresponding bits in the I^2C serial port. See Table 2.

Exposed Pad (Pin 29): Ground. The Exposed Pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the part.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

Introduction

The LTC3555 family are highly integrated power management ICs which include a high efficiency switch mode PowerPath controller, a battery charger, an ideal diode, an always-on LDO and three general purpose step-down switching regulators. The entire chip is controlled by either direct digital control, by an I^2C serial port or both.

Designed specifically for USB applications, the PowerPath controller incorporates a precision average input current step-down switching regulator to make maximum use of the allowable USB power. Because power is conserved, the LTC3555 family allows the load current on V_{OUT} to exceed the current drawn by the USB port without exceeding the USB load specifications.

The PowerPath switching regulator and battery charger communicate to ensure that the input current never violates the USB specifications.

The ideal diode from BAT to V_{OUT} guarantees that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS}.

An "always on" LDO provides a regulated 3.3V from available power at V_{OUT}. Drawing very little quiescent current, this LDO will be on at all times and can be used to supply up to 25mA.

The three general purpose switching regulators can be independently enabled via either direct digital control or by operating the I^2C serial port. Under I^2C control, two of the three switching regulators have adjustable set-points so that voltages can be reduced when high processor performance is not needed. Along with constant frequency PWM mode, all three switching regulators have a low power burst-only mode setting as well as automatic Burst Mode operation and LDO modes for significantly reduced quiescent current under light load conditions.

High Efficiency Switching PowerPath Controller

Whenever V_{BUS} is available and the PowerPath switching regulator is enabled, power is delivered from V_{BUS} to V_{OUT} via SW. V_{OUT} drives the combination of the external load (switching regulators 1, 2 and 3) and the battery charger.

If the combined load does not exceed the PowerPath switching regulator's programmed input current limit, V_{OUT} will track 0.3V above the battery. By keeping the voltage across the battery charger low, efficiency is optimized because power lost to the linear battery charger is minimized. Power available to the external load is therefore optimized.

If the combined load at V_{OUT} is large enough to cause the

OPERATION

switching power supply to reach the programmed input current limit, the battery charger will reduce its charge current by that amount necessary to enable the external load to be satisfied. Even if the battery charge current is set to exceed the allowable USB current, the USB specification will not be violated. The switching regulator will limit the average input current so that the USB specification is never violated. Furthermore, load current at V_{OUT} will always be prioritized and only excess available power will be used to charge the battery.

If the voltage at BAT is below 3.3V, or the battery is not present, and the load requirement does not cause the switching regulator to exceed the USB specification, V_{OUT} will regulate at 3.6V. If the load exceeds the available power, V_{OUT} will drop to a voltage between 3.6V and the battery voltage. If there is no battery present when the load exceeds the available USB power, V_{OUT} can drop toward ground.

The power delivered from V_{BUS} to V_{OUT} is controlled by a 2.25MHz constant-frequency step-down switching regulator. To meet the USB maximum load specification, the switching regulator includes a control loop which ensures that the average input current is below the level programmed at CLPROG.

The current at CLPROG is a fraction (h_{CLPROG}^{-1}) of the V_{BUS} current. When a programming resistor and an averaging capacitor are connected from CLPROG to GND, the voltage on CLPROG represents the average input current of the switching regulator. When the input current approaches the programmed limit, CLPROG reaches V_{CLPROG}, 1.188V, and power out is held constant. The input current limit is programmed by the I_{LIM0} and I_{LIM1} pins or by the I^2C serial port. It can be configured to limit average input current to one of several possible settings as well as be deactivated (USB suspend). The input current limit will be set by the V_{CLPROG} servo voltage and the resistor on CLPROG according to the following expression:

$$I_{VBUS} = I_{VBUSQ} + \frac{V_{CLPROG}}{R_{CLPROG}} \bullet \left(h_{CLPROG} + 1\right)$$

Figure 1 shows the range of possible voltages at V_{OUT} as a function of battery voltage.

The LTC3555 vs the LTC3555-1 and LTC3555-3

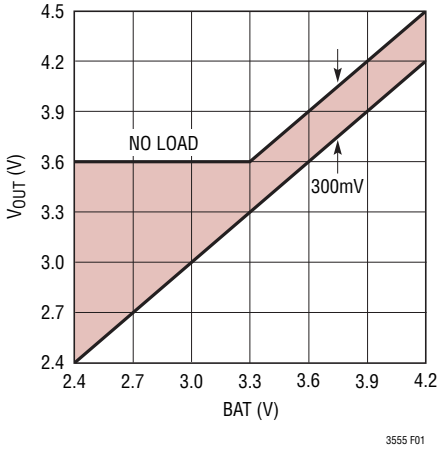


Figure 1. V_{OUT} vs BAT

For very low battery voltages, the battery charger acts like a load and, due to limited input power, its current will tend to pull V_{OUT} below the 3.6V "instant-on" voltage. To prevent V_{OUT} from falling below this level, the LTC3555-1 and LTC3555-3 include an undervoltage circuit that automatic detects that V_{OUT} is falling and reduces the battery charge current as needed. This reduction ensures that load current and output voltage are always prioritized and yet delivers as much battery charge current as possible. The standard LTC3555 does not include this circuit and thus favors maximum charge current at all times over output voltage preservation.

If instant-on operation under low battery conditions is a requirement then the LTC3555-1 or LTC3555-3 should be used. If maximum charge efficiency at low battery voltages is preferred, and instant-on operation is not a requirement, then the standard LTC3555 should be selected. All versions of the LTC3555 family will start up with a removed battery.

The LTC3555-3 has a battery charger float voltage of 4.100V rather than the 4.200V float voltage of the LTC3555 and LTC3555-1.

Ideal Diode from BAT to V_{OUT}

The LTC3555 family has an internal ideal diode as well as a controller for an optional external ideal diode. The ideal diode controller is always on and will respond quickly whenever V_{OUT} drops below BAT.

If the load current increases beyond the power allowed from the switching regulator, additional power will be

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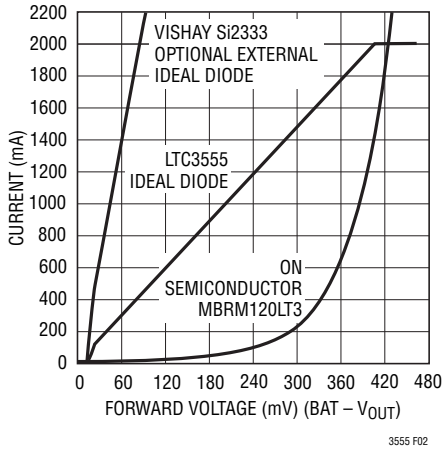
pulled from the battery via the ideal diode. Furthermore, if power to V_{BUS} (USB or wall power) is removed, then all of the application power will be provided by the battery via the ideal diode. The transition from input power to battery power at V_{OUT} will be quick enough to allow only the 10µF capacitor to keep V_{OUT} from drooping. The ideal diode consists of a precision amplifier that enables a large on-chip P-channel MOSFET transistor whenever the voltage at V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at BAT. The resistance of the internal ideal diode is approximately 180mΩ. If this is sufficient for the application, then no external components are necessary. However, if more conductance is needed, an external P-channel MOSFET transistor can be added from BAT to V_{OUT}.

When an external P-channel MOSFET transistor is present, the GATE pin of the LTC3555 family drives its gate for automatic ideal diode control. The source of the external P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. Capable of driving a 1nF load, the GATE pin can control an external P-channel MOSFET transistor having an on-resistance of 40mΩ or lower.



Suspend LDO

If the LTC3555 family is configured for USB suspend mode, the switching regulator is disabled and the suspend LDO provides power to the V_{OUT} pin (presuming there is power available to V_{BUS}). This LDO will prevent the battery from running down when the portable product has access to a suspended USB port. Regulating at 4.6V, this LDO only becomes active when the switching converter is disabled (suspended). To remain compliant with the USB specification, the input to the LDO is current limited so that it will not exceed the 500µA low power suspend specification. If the load on V_{OUT} exceeds the suspend current limit, the additional current will come from the

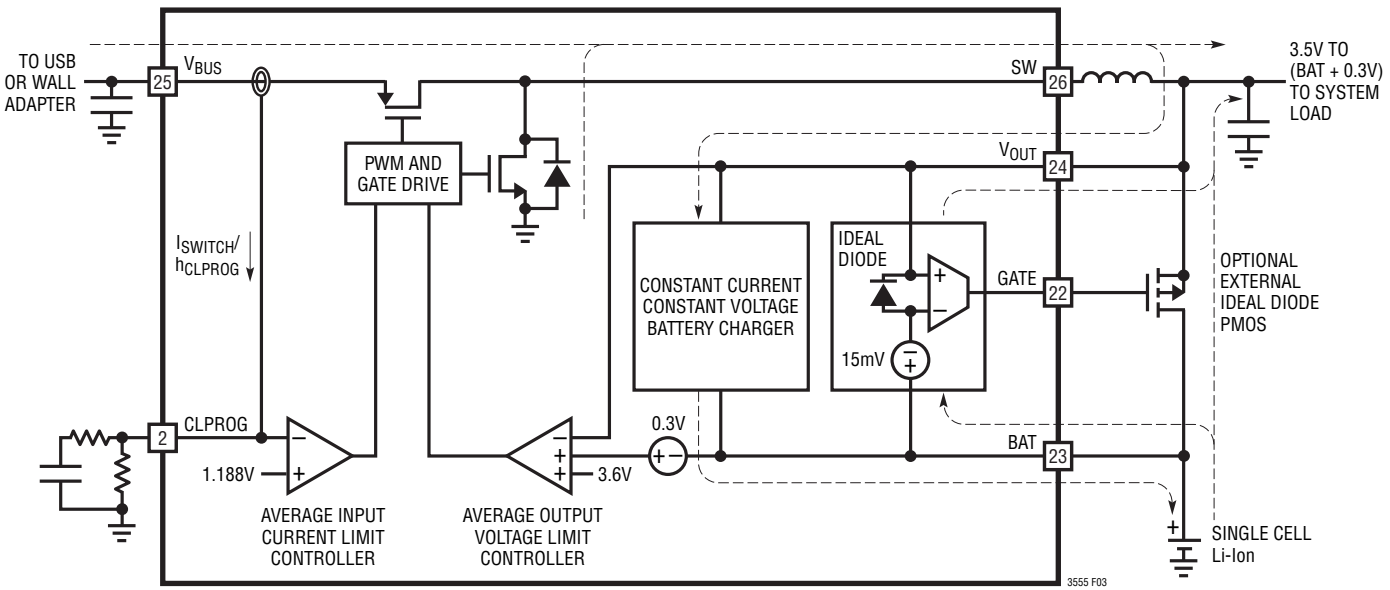


Figure 3. PowerPath Block Diagram

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battery via the ideal diode.

3.3V Always-On LDO Supply

The LTC3555 family includes a low quiescent current low dropout regulator that is always powered. This LDO can be used to provide power to a system pushbutton controller, standby microcontroller or real time clock. Designed to deliver up to 25mA, the always-on LDO requires at least a 1µF low impedance ceramic bypass capacitor for compensation. The LDO is powered from V_{OUT}, and therefore will enter dropout at loads less than 25mA as V_{OUT} falls near 3.3V. If the LDO3V3 output is not used, it should be disabled by connecting it to V_{OUT}.

V_{BUS} Undervoltage Lockout (UVLO)

An internal undervoltage lockout circuit monitors V_{BUS} and keeps the PowerPath switching regulator off until V_{BUS} rises above 4.30V and is about 200mV above the battery voltage. Hysteresis on the UVLO turns off the regulator if V_{BUS} drops below 4.00V or to within 50mV of BAT. When this happens, system power at V_{OUT} will be drawn from the battery via the ideal diode.

Battery Charger

The LTC3555 family includes a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad cell detection and thermistor sensor input for out-of-temperature charge pausing.

Battery Preconditioning

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{TRKL}, typically 2.85V, an automatic trickle charge feature sets the battery charge current to 10% of the programmed value. If the low voltage persists for more than 1/2 hour, the battery charger automatically terminates and indicates via the $\overline{CHRG}$ pin that the battery was unresponsive.

Once the battery voltage is above 2.85V, the battery charger begins charging in full power constant-current mode. The current delivered to the battery will try to reach 1022V/R_{PROG}. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. The USB current limit programming will always be observed and only additional power will be available to charge the battery. When system loads are light, battery charge current will be maximized.

Charge Termination

The battery charger has a built-in safety timer. When the voltage on the battery reaches the pre-programmed float voltage, the battery charger will regulate the battery voltage and the charge current will decrease naturally. Once the battery charger detects that the battery has reached the float voltage, the four hour safety timer is started. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered.

Automatic Recharge

After the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below the recharge threshold which is typically 100mV less than the charger's float voltage. In the event that the safety timer is running when the battery voltage falls below the recharge threshold, it will reset back to zero. To prevent brief excursions below the recharge threshold from resetting the safety timer, the battery voltage must be below the recharge threshold for more than 1.3ms. The charge cycle and safety timer will also restart if the V_{BUS} UVLO cycles low and then high (e.g., V_{BUS} is removed and then replaced), or if the battery charger is cycled on and off by the I^2C port.

Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/1022th of the battery charge current is sent to PROG which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 1022 times the current in the PROG pin. The program resistor and the charge current are calculated using the

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following equations:

$$R_{PROG} = \frac{1022V}{I_{CHG}},\ I_{CHG} = \frac{1022V}{R_{PROG}}$$

In either the constant-current or constant-voltage charging modes, the voltage at the PROG pin will be proportional to the actual charge current delivered to the battery. Therefore, the actual charge current can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1022$$

In many cases, the actual battery charge current, I_{BAT}, will be lower than I_{CHG} due to limited input power available and prioritization with the system load drawn from V_{OUT}.

Charge Status Indication

The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{CHRG}$ which include charging, not charging, unresponsive battery, and battery temperature out of range.

The signal at the $\overline{CHRG}$ pin can be easily recognized as one of the above four states by either a human or a microprocessor. An open-drain output, the $\overline{CHRG}$ pin can drive an indicator LED through a current limiting resistor for human interfacing or simply a pull-up resistor for microprocessor interfacing.

To make the $\overline{CHRG}$ pin easily recognized by both humans and microprocessors, the pin is either low for charging, high for not charging, or it is switched at high frequency (35kHz) to indicate the two possible faults, unresponsive battery and battery temperature out of range.

When charging begins, $\overline{CHRG}$ is pulled low and remains low for the duration of a normal charge cycle. When charging is complete, i.e., the BAT pin reaches the float voltage and the charge current has dropped to one tenth of the programmed value, the $\overline{CHRG}$ pin is released (Hi-Z). If a fault occurs, the pin is switched at 35kHz. While switching, its duty cycle is modulated between a low and high value at a very low frequency. The low and high duty cycles are disparate enough to make an LED appear to be on or off thus giving the appearance of "blinking". Each of the two faults has its own unique "blink" rate for human recognition as well as two unique duty cycles for machine recognition.

The $\overline{CHRG}$ pin does not respond to the C/10 threshold if the LTC3555 family is in V_{BUS} current limit. This prevents false end-of-charge indications due to insufficient power available to the battery charger.

Table 1 illustrates the four possible states of the $\overline{CHRG}$ pin when the battery charger is active.

Table 1. $\overline{CHRG}$ Signal

STATUS	FREQUENCY	MODULATION (BLINK) FREQUENCY	DUTY CYCLES
Charging	0Hz	0Hz (Lo-Z)	100%
Not Charging	0Hz	0Hz (Hi-Z)	0%
NTC Fault	35kHz	1.5Hz at 50%	6.25% to 93.75%
Bad Battery	35kHz	6.1Hz at 50%	12.5% to 87.5%

An NTC fault is represented by a 35kHz pulse train whose duty cycle varies between 6.25% and 93.75% at a 1.5Hz rate. A human will easily recognize the 1.5Hz rate as a "slow" blinking which indicates the out-of-range battery temperature while a microprocessor will be able to decode either the 6.25% or 93.75% duty cycles as an NTC fault.

If a battery is found to be unresponsive to charging (i.e., its voltage remains below 2.85V for 1/2 hour), the $\overline{CHRG}$ pin gives the battery fault indication. For this fault, a human would easily recognize the frantic 6.1Hz "fast" blink of the LED while a microprocessor would be able to decode either the 12.5% or 87.5% duty cycles as a bad battery fault.

Note that the LTC3555 family is a three terminal PowerPath product where system load is always prioritized over battery charging. Due to excessive system load, there may not be sufficient power to charge the battery beyond the trickle charge threshold voltage within the bad battery timeout period. In this case, the battery charger will falsely indicate a bad battery. System software may then reduce the load and reset the battery charger to try again.

Although very improbable, it is possible that a duty cycle reading could be taken at the bright-dim transition (low duty cycle to high duty cycle). When this happens the duty cycle reading will be precisely 50%. If the duty cycle reading is 50%, system software should disqualify it and

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take a new duty cycle reading.

NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack.

To use this feature, connect the NTC thermistor, R_{NTC}, between the NTC pin and ground and a resistor, R_{NOM}, from V_{BUS} to the NTC pin. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25). For applications requiring greater than 750mA of charging current, a 10k NTC thermistor is recommended due to increased interference.

The LTC3555 family will pause charging when the resistance of the NTC thermistor drops to 0.54 times the value of R25 or approximately 5.4k. For a Vishay "Curve 1" thermistor, this corresponds to approximately 40°C. If the battery charger is in constant voltage (float) mode, the safety timer also pauses until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC3555 family is also designed to pause charging when the value of the NTC thermistor increases to 3.25 times the value of R25. For Vishay "Curve 1" this resistance, 32.5k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables the NTC charge pausing function.

Thermal Regulation

To optimize charging time, an internal thermal feedback loop may automatically decrease the programmed charge current. This will occur if the die temperature rises to approximately 110°C. Thermal regulation protects the LTC3555 family from excessive temperature due to high power operation or high ambient thermal conditions and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the part or external components. The benefit of the LTC3555 family thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions with the assurance that the battery charger will automatically reduce the current in worst-case conditions.

I^2C Interface

The LTC3555 family may receive commands from a host (master) using the standard I^2C 2-wire interface. The Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 I^2C accelerator, are required on these lines. The LTC3555 family is a receive-only slave device. The I^2C control signals, SDA and SCL are scaled internally to the DV_{CC} supply. DV_{CC} should be connected to the same power supply as the microcontroller generating the I^2C signals.

The I^2C port has an undervoltage lockout on the DV_{CC} pin. When DV_{CC} is below approximately 1V, the I^2C serial port is cleared and switching regulators 2 and 3 are set to full scale.

Bus Speed

The I^2C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I^2C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

Start and Stop Conditions

A bus-master signals the beginning of a communication to a slave device by transmitting a START condition. A START condition is generated by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high.

Byte Format

Each byte sent to the LTC3555 family must be eight bits long followed by an extra clock cycle for the acknowledge bit to be returned by the LTC3555 family. The data should be sent to the LTC3555 family most significant bit (MSB) first.

Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. An acknowledge (active low)

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Table 2. I²C Serial Port Mapping

A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
Switching Regulator 2 Voltage (See Table 4)				Switching Regulator 3 Voltage (See Table 4)				Disable Battery Charger	Switching Regulator Modes (See Table 5)		Enable Regulator 1	Enable Regulator 2	Enable Regulator 3	Input Current Limit (See Table 3)	

Table 3. USB Current Limit Settings

B1 (I_{LIM1})	B0 (I_{LIM0})	USB SETTING
0	0	1x Mode (USB 100mA Limit)
0	1	10x Mode (Wall 1A Limit)
1	0	Suspend
1	1	5x Mode (USB 500mA Limit)

Table 4. Switching Regulator Servo Voltage

A7	A6	A5	A4	Switching Regulator 2 Servo Voltage
A3	**A2**	**A1**	**A0**	**Switching Regulator 3 Servo Voltage**
0	0	0	0	0.425V
0	0	0	1	0.450V
0	0	1	0	0.475V
0	0	1	1	0.500V
0	1	0	0	0.525V
0	1	0	1	0.550V
0	1	1	0	0.575V
0	1	1	1	0.600V
1	0	0	0	0.625V
1	0	0	1	0.650V
1	0	1	0	0.675V
1	0	1	1	0.700V
1	1	0	0	0.725V
1	1	0	1	0.750V
1	1	1	0	0.775V
1	1	1	1	0.800V

Table 5. General Purpose Switching Regulator Modes

B6 (SDA)*	B5 (SCL)*	Switching Regulator Mode
0	0	Pulse Skip
0	1	Forced Burst Mode Operation
1	0	LDO Mode
1	1	Burst Mode Operation

*SDA and SCL take on this context only when DV_{CC} = 0V.

generated by the slave (LTC3555 family) lets the master know that the latest byte of information was received. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (high) during the acknowledge clock cycle. The slave-receiver must pull down the SDA line during the acknowledge clock pulse so that it remains a stable low during the high period of this clock pulse.

Slave Address

The LTC3555 family responds to only one 7-bit address which has been factory programmed to 0001001. The eighth bit of the address byte (R/W) must be 0 for the LTC3555 family to recognize the address since it is a write only device. This effectively forces the address to be eight bits long where the least significant bit of the address is 0. If the correct seven bit address is given but the R/W bit is 1, the LTC3555 family will not respond.

Bus Write Operation

The master initiates communication with the LTC3555 family with a START condition and a 7-bit address followed by the write bit R/W = 0. If the address matches that of the LTC3555 family, the LTC3555 family returns an acknowledge. The master should then deliver the most significant data byte. Again the LTC3555 family acknowledges and the cycle is repeated for a total of one address byte and two data bytes. Each data byte is transferred to an internal holding latch upon the return of an acknowledge. After both data bytes have been transferred to the LTC3555 family, the master may terminate the communication with a STOP condition. Alternatively, a REPEAT-START condition can be initiated by the master and another chip on the I²C bus can be addressed. This cycle can continue indefinitely and the LTC3555 family will remember the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global STOP condition can

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be sent and the LTC3555 family will update its command latch with the data that it had received.

In certain circumstances the data on the I²C bus may become corrupted. In these cases the LTC3555 family responds appropriately by preserving only the last set of complete data that it has received. For example, assume the LTC3555 family has been successfully addressed and is receiving data when a STOP condition mistakenly occurs. The LTC3555 family will ignore this STOP condition and will not respond until a new START condition, correct address, new set of data and STOP condition are transmitted.

Likewise, with only one exception, if the LTC3555 family was previously addressed and sent valid data but not updated with a STOP, it will respond to any STOP that appears on the bus, independent of the number of REPEAT-STARTS that have occurred. If a REPEAT-START is given and the LTC3555 family successfully acknowledges its address and first byte, it will not respond to a STOP until both bytes of the new data have been received and acknowledged.

Disabling the I²C Port

The I²C serial port can be disabled by grounding the DV_{CC} pin. In this mode, control automatically passes to the individual logic input pins EN1, EN2, EN3, I_{LIM0}, I_{LIM1}, SDA and SCL. Some functionality is not available in this mode such as the programmability of switching regulators 2 and 3's output voltage and the battery charger disable feature. In this mode, both of the programmable switching regulators have a fixed servo voltage of 0.8V.

Because the SDA and SCL pins have no other context when DV_{CC} is grounded, these pins are re-mapped to control the switching regulator mode bits B5 and B6. SCL maps to B5 and SDA maps to B6.

$\overline{RST3}$ Pin

The $\overline{RST3}$ pin is an open-drain output used to indicate that switching regulator 3 has reached its final voltage. $\overline{RST3}$ remains low impedance until regulator 3 reaches 92% of its regulation value. A 230ms delay is included to allow a system microcontroller ample time to reset itself. $\overline{RST3}$ may be used as a power-on reset to the microprocessor powered by regulator 3 or may be used to enable regulators 1 and/or 2 for supply sequencing. $\overline{RST3}$ is an open-drain output and requires a pull-up resistor to the output voltage of regulator 3 or another appropriate power source.

General Purpose Step-Down Switching Regulators

The LTC3555 family contains three general purpose 2.25MHz step-down constant-frequency current mode switching regulators. Two regulators provide up to 400mA and a third switching regulator can produce up to 1A. All three switching regulators can be programmed for a minimum output voltage of 0.8V and can be used to power a microcontroller core, microcontroller I/O, memory, disk drive or other logic circuitry. Two of the switching regulators have I²C programmable set-points for on-the-fly power savings. All three converters support 100% duty cycle operation (low dropout mode) when their input voltage drops very close to their output voltage. To suit a variety of applications, selectable mode functions can be used to trade-off noise for efficiency. Four modes are available to control the operation of the LTC3555 family's general purpose switching regulators. At moderate to heavy loads, the pulse skip mode provides the least noise switching solution. At lighter loads, either Burst Mode operation, forced Burst Mode operation or LDO mode may be selected. The switching regulators include soft-start to limit inrush current when powering on, short-circuit current protection and switch node slew limiting circuitry to reduce radiated EMI. No external compensation components are required. The operating mode of the regulators may be set by either I²C control or by manual control of the SDA and SCL pins if the I²C port is not used. Each converter may be individually enabled by either their external control pins EN1, EN2, EN3 or by the I²C port. Switching regulators 2 and 3 have individual programmable feedback servo voltages via I²C control. The switching regulator input supplies V_{IN1}, V_{IN2} and V_{IN3} will generally be connected to the system load pin V_{OUT}.

Step-Down Switching Regulator Output Voltage Programming

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All three switching regulators can be programmed for output voltages greater than 0.8V. Switching regulators 2 and 3 have I²C programmable set-points while regulator 1 has a single fixed set-point. The full-scale output voltage for each switching regulator is programmed using a resistor divider from the switching regulator output connected to the feedback pins (FB1, FB2 and FB3) such that:

$$V_{OUTX} = V_{FBX}\left(\frac{R1}{R2}+1\right)$$

where V_{FBX} ranges from 0.425V to 0.8V for switching regulators 2 and 3 and V_{FBX} is fixed at 0.8V for switching regulator 1. See Figure 4

Typical values for R1 are in the range of 40k to 1M. The capacitor C_{FB} cancels the pole created by feedback resistors and the input capacitance of the FB pin and also helps to improve transient response for output voltages much greater than 0.8V. A variety of capacitor sizes can be used for C_{FB} but a value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 2pF and 22pF may yield improved transient response.

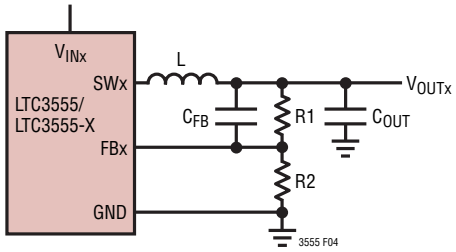

Figure 4. Buck Converter Application Circuit

Step-Down Switching Regulator Operating Modes

The LTC3555 family's general purpose switching regulators include four possible operating modes to meet the noise/power needs of a variety of applications.

In pulse skip mode, an internal latch is set at the start of every cycle which turns on the main P-channel MOSFET switch. During each cycle, a current comparator compares the peak inductor current to the output of an error amplifier. The output of the current comparator resets the internal latch which causes the main P-channel MOSFET switch to turn off and the N-channel MOSFET synchronous rectifier to turn on. The N-channel MOSFET synchronous rectifier turns off at the end of the 2.25MHz cycle or if the current through the N-channel MOSFET synchronous rectifier drops to zero. Using this method of operation, the error amplifier adjusts the peak inductor current to deliver the required output power. All necessary compensation is internal to the switching regulator requiring only a single ceramic output capacitor for stability. At light loads in PWM mode, the inductor current may reach zero on each pulse which will turn off the N-channel MOSFET synchronous rectifier. In this case, the switch node (SW) goes high impedance and the switch node voltage will "ring". This is discontinuous mode operation, and is normal behavior for a switching regulator. At very light loads in pulse skip mode, the switching regulators will automatically skip pulses as needed to maintain output regulation.

At high duty cycles ($V_{OUTx} > V_{INx}/2$) it is possible for the inductor current to reverse, causing the regulator to operate continuously at light loads. This is normal and regulation is maintained, but the supply current will increase to several milliamperes due to continuous switching.

In forced Burst Mode operation, the switching regulators use a constant current algorithm to control the inductor current. By controlling the inductor current directly and using a hysteretic control loop, both noise and switching losses are minimized. In this mode output power is limited. While in forced Burst Mode operation, the output capacitor is charged to a voltage slightly higher than the regulation point. The step-down converter then goes into sleep mode, during which the output capacitor provides the load current. In sleep mode, most of the regulator's circuitry is powered down, helping conserve battery power. When the output voltage drops below a pre-determined value, the switching regulator circuitry is powered on and another burst cycle begins. The duration for which the regulator operates in sleep mode depends on the load current. The sleep time decreases as the load current increases. The maximum output current in forced Burst Mode operation is about 100mA for switching regulators 1 and 2, and about 250mA for switching regulator 3. The step-down switching regulators will not enter sleep mode if the maximum output current is exceeded in forced Burst Mode operation and the output will drop out of regulation. Forced Burst Mode operation provides a significant improvement in efficiency

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at light loads at the expense of higher output ripple when compared to pulse skip mode. For many noise-sensitive systems, forced Burst Mode operation might be undesirable at certain times (i.e., during a transmit or receive cycle of a wireless device), but highly desirable at others (i.e., when the device is in low power standby mode). The I^2C port can be used to enable or disable forced Burst Mode operation at any time, offering both low noise and low power operation when they are needed.

In Burst Mode operation, the switching regulator automatically switches between fixed frequency PWM operation and hysteretic control as a function of the load current. At light loads, the regulators operate in hysteretic mode in much the same way as described for the forced Burst Mode operation. Burst Mode operation provides slightly less output ripple at the expense of slightly lower efficiency than forced Burst Mode operation. At heavy loads the switching regulator operates in the same manner as pulse skip operation at high loads. For applications that can tolerate some output ripple at low output currents, Burst Mode operation provides better efficiency than pulse skip at light loads while still providing the full specified output current of the switching regulator.

Finally, the switching regulators have an LDO mode that gives a DC option for regulating their output voltages. In LDO mode, the switching regulators are converted to linear regulators and deliver continuous power from their SWx pins through their respective inductors. This mode gives the lowest possible output noise as well as low quiescent current at light loads.

The step-down switching regulators allow mode transition on the fly, providing seamless transition between modes even under load. This allows the user to switch back and forth between modes to reduce output ripple or increase low current efficiency as needed.

Step-Down Switching Regulator in Shutdown

The step-down switching regulators are in shutdown when not enabled for operation. In shutdown, all circuitry in the step-down switching regulator is disconnected from the switching regulator input supply leaving only a few nanoamperes of leakage current. The step-down switching regulator outputs are individually pulled to ground through a 10k resistor on the switch pins (SW1-SW3) when in shutdown.

General Purpose Switching Regulator Dropout Operation

It is possible for a switching regulator's input voltage, V_{INx}, to approach its programmed output voltage (e.g., a battery voltage of 3.4V with a programmed output voltage of 3.3V). When this happens, the PMOS switch duty cycle increases until it is turned on continuously at 100%. In this dropout condition, the respective output voltage equals the regulator's input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

Step-Down Switching Regulator Soft-Start Operation

Soft-start is accomplished by gradually increasing the peak inductor current for each switching regulator over a 500µs period. This allows each output to rise slowly, helping minimize the battery surge current. A soft-start cycle occurs whenever a given switching regulator is enabled, or after a fault condition has occurred (thermal shutdown or UVLO). A soft-start cycle is not triggered by changing operating modes. This allows seamless output operation when transitioning between forced Burst Mode, Burst Mode, pulse skip mode or LDO operation.

Step-Down Switching Regulator Switching Slew Rate Control

The step-down switching regulators contain new patent pending circuitry to limit the slew rate of the switch nodes (SWx). This new circuitry is designed to transition the switch nodes over a period of a couple of nanoseconds, significantly reducing radiated EMI and conducted supply noise.

Low Supply Operation

The LTC3555 family incorporates an undervoltage lockout circuit on V_{OUT} which shuts down the general purpose switching regulators when V_{OUT} drops below $V_{OUTUVLO}$. This UVLO prevents unstable operation.

APPLICATIONS INFORMATION

CLPROG Resistor and Capacitor

As described in the High Efficiency Switching PowerPath Controller section, the resistor on the CLPROG pin determines the average input current limit when the switching regulator is set to either the 1x mode (USB 100mA), the 5x mode (USB 500mA) or the 10x mode. The input current will be comprised of two components, the current that is used to drive V_{OUT} and the quiescent current of the switching regulator. To ensure that the USB specification is strictly met, both components of input current should be considered. The Electrical Characteristics table gives values for quiescent currents in either setting as well as current limit programming accuracy. To get as close to the 500mA or 100mA specifications as possible, a 1% resistor should be used. Recall that

$$I_{VBUS} = I_{VBUSQ} + V_{CLPROG}/R_{CLPPROG} \bullet (h_{CLPROG} +1)$$

An averaging capacitor or an R-C combination is required in parallel with the CLPROG resistor so that the switching regulator can determine the average input current. This network also provides the dominant pole for the feedback loop when current limit is reached. To ensure stability, the capacitor on CLPROG should be 0.47µF or larger. Alternatively, faster transient response may be achieved with 0.1µF in series with 8.2Ω.

Choosing the PowerPath Inductor

Because the average input current circuit does not measure reverse current (i.e., current from SW to V_{BUS}), current reversal in the inductor at light loads will contribute an error to the average V_{BUS} current measurement. The error is conservative in that if the current reverses, the voltage at CLPROG will be higher than what would represent the actual average input current drawn. The current available for battery charging plus system load is thus reduced but the USB specification will not be violated.

This reduction in available V_{BUS} current will happen when the peak-peak inductor ripple is greater than twice the average current limit setting. For example, if the average current limit is set to 100mA, the peak-peak ripple should not exceed 200mA. If the input current is less than 100mA, the measurement accuracy may be reduced. However, this will not affect the average current loop since it will not be in regulation.

The LTC3555 family includes a current-reversal comparator which monitors inductor current and disables the synchronous rectifier as current approaches zero. This comparator will minimize the effect of current reversal on the average input current measurement. For some low inductance values, however, the inductor current may still reverse slightly. This value depends on the speed of the comparator in relation to the slope of the current waveform, given by V_L/L. V_L is the voltage across the inductor (approximately $–V_{OUT}$) and L is the inductance value.

An inductance value of 3.3µH is a good starting value. The ripple will be small enough for the regulator to remain in continuous conduction at 100mA average V_{BUS} current. At lighter loads the current-reversal comparator will disable the synchronous rectifier for currents slightly above 0mA. As the inductance is reduced from this value, the LTC3555 family will enter discontinuous conduction mode at progressively higher loads. Ripple at V_{OUT} will increase directly proportionally to the magnitude of inductor ripple. Transient response, however, will improve. The current mode controller controls inductor current to exactly the amount required by the load to keep V_{OUT} in regulation. A transient load step requires the inductor current to change to a new level. Since inductor current cannot change instantaneously, the capacitance on V_{OUT} delivers or absorbs the difference in current until the inductor current can change to meet the new load demand. A smaller inductor changes its current more quickly for a given voltage drive than a larger inductor, resulting in faster transient response. A larger inductor will reduce output ripple and current ripple, but at the expense of reduced transient performance and a physically larger inductor package size. For this reason a larger C_{VOUT} will be required for larger inductor sizes.

The input regulator has an instantaneous peak current clamp to prevent the inductor from saturating during transient load or start-up conditions. The clamp is designed so that it does not interfere with normal operation at high loads and reasonable inductor ripple. It is intended to prevent inductor current runaway in case of a shorted output.

The DC winding resistance and AC core losses of the inductor will affect efficiency, and therefore available output power. These effects are difficult to characterize and vary

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by application. Some inductors that may be suitable for this application are listed in Table 6.

Table 6. Recommended Inductors

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE in mm (L × W × H)	MANUFACTURER
LPS4018	3.3	2.2	0.08	3.9 × 3.9 × 1.7	Coilcraft www.coilcraft.com
D53LC DB318C	3.3 3.3	2.26 1.55	0.034 0.070	5 × 5 × 3 3.8 × 3.8 × 1.8	Toko www.toko.com
WE-TPC Type M1	3.3	1.95	0.065	4.8 × 4.8 × 1.8	Wurth Elektronik www.we-online.com
CDRH6D12 CDRH6D38	3.3 3.3	2.2 3.5	0.0625 0.020	6.7 × 6.7 × 1.5 7 × 7 × 4	Sumida www.sumida.com

V_{BUS} and V_{OUT} Bypass Capacitors

The style and value of capacitors used with the LTC3555 family determine several important parameters such as regulator control-loop stability and input voltage ripple. Because the LTC3555 family uses a step-down switching power supply from V_{BUS} to V_{OUT}, its input current waveform contains high frequency components. It is strongly recommended that a low equivalent series resistance (ESR) multilayer ceramic capacitor be used to bypass V_{BUS}. Tantalum and aluminum capacitors are not recommended because of their high ESR. The value of the capacitor on V_{BUS} directly controls the amount of input ripple for a given load current. Increasing the size of this capacitor will reduce the input ripple.

To prevent large V_{OUT} voltage steps during transient load conditions, it is also recommended that a ceramic capacitor be used to bypass V_{OUT}. The output capacitor is used in the compensation of the switching regulator. At least 4µF of actual capacitance with low ESR are required on V_{OUT}. Additional capacitance will improve load transient performance and stability.

Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions.

There are several types of ceramic capacitors available, each having considerably different characteristics. For example, X7R ceramic capacitors have the best voltage and temperature stability. X5R ceramic capacitors have apparently higher packing density but poorer performance over their rated voltage and temperature ranges. Y5V ceramic capacitors have the highest packing density, but must be used with caution because of their extreme non-linear characteristic of capacitance verse voltage. The actual in-circuit capacitance of a ceramic capacitor should be measured with a small AC signal as is expected in-circuit. Many vendors specify the capacitance versus voltage with a $1V_{RMS}$ AC test signal and as a result, overstate the capacitance that the capacitor will present in the application. Using similar operating conditions as the application, the user must measure or request from the vendor the actual capacitance to determine if the selected capacitor meets the minimum capacitance that the application requires.

General Purpose Switching Regulator Inductor Selection

Many different sizes and shapes of inductors are available from numerous manufacturers. Choosing the right inductor from such a large selection of devices can be overwhelming, but following a few basic guidelines will make the selection process much simpler.

The general purpose step-down converters are designed to work with inductors in the range of 2.2µH to 10µH. For most applications a 4.7µH inductor is suggested for the lower power switching regulators 1 and 2 and 2.2µH is recommended for the more powerful switching regulator 3. Larger value inductors reduce ripple current which improves output ripple voltage. Lower value inductors result in higher ripple current and improved transient response time. To maximize efficiency, choose an inductor with a low DC resistance. For a 1.2V output, efficiency is reduced about 2% for 100mΩ series resistance at 400mA load current, and about 2% for 300mΩ series resistance at 100mA load current. Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the step-down converters.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or Permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar

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electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses, and will not give the best efficiency. The choice of which style inductor to use often depends more on the price vs size, performance and any radiated EMI requirements than on what the LTC3555 family requires to operate.

The inductor value also has an effect on forced Burst Mode and Burst Mode operations. Lower inductor values will cause the Burst and forced Burst Mode switching frequencies to increase.

Table 7 shows several inductors that work well with the LTC3555 family's general purpose regulators. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Table 7. Recommended Inductors

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE in mm (L × W × H)	MANUFACTURER
DE2818C	4.7	1.25	0.072	3.0 × 2.8 × 1.8	Toko
	3.3	1.45	0.053	3.0 × 2.8 × 1.8	www.toko.com
D312C	4.7	0.79	0.24	3.6 × 3.6 × 1.2	
	3.3	0.90	0.20	3.6 × 3.6 × 1.2	
	2.2	1.14	0.14	3.6 × 3.6 × 1.2	
DE2812C	4.7	1.2	0.13*	3.0 × 2.8 × 1.2	
	3.3	1.4	0.10*	3.0 × 2.8 × 1.2	
	2.0	1.8	0.067*	3.0 × 2.8 × 1.2	
CDRH3D16	4.7	0.9	0.11	4 × 4 × 1.8	Sumida
	3.3	1.1	0.085	4 × 4 × 1.8	www.sumida.
	2.2	1.2	0.072	4 × 4 × 1.8	com
CDRH2D11	4.7	0.5	0.17	3.2 × 3.2 × 1.2	
	3.3	0.6	0.123	3.2 × 3.2 × 1.2	
	2.2	0.78	0.098	3.2 × 3.2 × 1.2	
CLS4D09	4.7	0.75	0.19	4.9 × 4.9 × 1	
SD3118	4.7	1.3	0.162	3.1 × 3.1 × 1.8	Cooper
	3.3	1.59	0.113	3.1 × 3.1 × 1.8	www.cooperet.
	2.2	2.0	0.074	3.1 × 3.1 × 1.8	com
SD3112	4.7	0.8	0.246	3.1 × 3.1 × 1.2	
	3.3	0.97	0.165	3.1 × 3.1 × 1.2	
	2.2	1.12	0.14	3.1 × 3.1 × 1.2	
SD12	4.7	1.29	0.117*	5.2 × 5.2 × 1.2	
	3.3	1.42	0.104*	5.2 × 5.2 × 1.2	
	2.2	1.80	0.075*	5.2 × 5.2 × 1.2	
SD10	4.7	1.08	0.153*	5.2 × 5.2 × 1.0	
	3.3	1.31	0.108*	5.2 × 5.2 × 1.0	
	2.2	1.65	0.091*	5.2 × 5.2 × 1.0	
LPS3015	4.7	1.1	0.2	3.0 × 3.0 × 1.5	Coil Craft
	3.3	1.3	0.13	3.0 × 3.0 × 1.5	www.coilcraft.
	2.2	1.5	0.11	3.0 × 3.0 × 1.5	com

*Typical DCR

General Purpose Switching Regulator Input/Output

Capacitor Selection

Low ESR (equivalent series resistance) MLCC capacitors should be used at both switching regulator outputs as well as at each switching regulator input supply (V_{INX}). Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 10µF output capacitor is sufficient for most applications. For good transient response and stability the output capacitor should retain at least 4µF of capacitance over operating temperature and bias voltage. Each switching regulator input supply should be bypassed with a 1µF capacitor. Consult with capacitor manufacturers for detailed information on their selection and specifications of ceramic capacitors. Many manufacturers now offer very thin (<1mm tall) ceramic capacitors ideal for use in height-restricted designs. Table 8 shows a list of several ceramic capacitor manufacturers.

Table 8. Recommended Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

Over-Programming the Battery Charger

The USB high power specification allows for up to 2.5W to be drawn from the USB port (5V × 500mA). The PowerPath switching regulator transforms the voltage at V_{BUS} to just above the voltage at BAT with high efficiency, while limiting power to less than the amount programmed at CLPROG. In some cases the battery charger may be programmed (with the PROG pin) to deliver the maximum safe charging current without regard to the USB specifications. If there is insufficient current available to charge the battery at the programmed rate, the PowerPath regulator will reduce charge current until the system load on V_{OUT} is satisfied and the V_{BUS} current limit is satisfied. Programming the battery charger for more current than is available will not cause the average input current limit to be violated. It will merely allow the battery charger to make use of all available power to charge the battery as quickly as possible, and with minimal power dissipation within the battery charger.

APPLICATIONS INFORMATION

Alternate NTC Thermistors and Biasing

The LTC3555 family provides temperature qualified charging if a grounded thermistor and a bias resistor are connected to NTC. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25) the upper and lower temperatures are pre-programmed to approximately 40°C and 0°C, respectively (assuming a Vishay "Curve 1" thermistor).

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique are given below.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N011-N1002F, used in the following examples, has a nominal value of 10k and follows the Vishay "Curve 1" resistance-temperature characteristic.

In the explanation below, the following notation is used.

R25 = Value of the Thermistor at 25°C

$R_{NTC|COLD}$ = Value of thermistor at the cold trip point

$R_{NTC|HOT}$ = Value of the thermistor at the hot trip point

α_{COLD} = Ratio of $R_{NTC|COLD}$ to R25

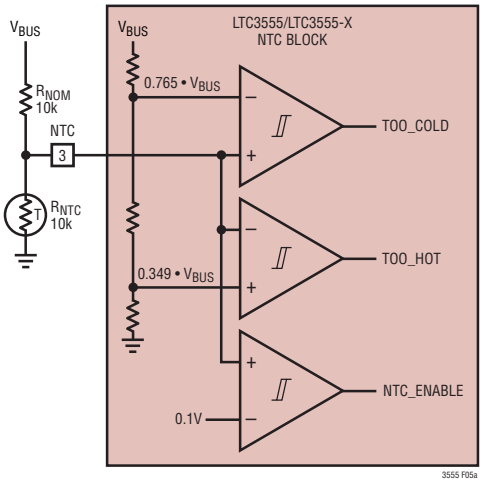
α_{HOT} = Ratio of $R_{NTC|HOT}$ to R25

R_{NOM} = Primary thermistor bias resistor (see Figure 5a)

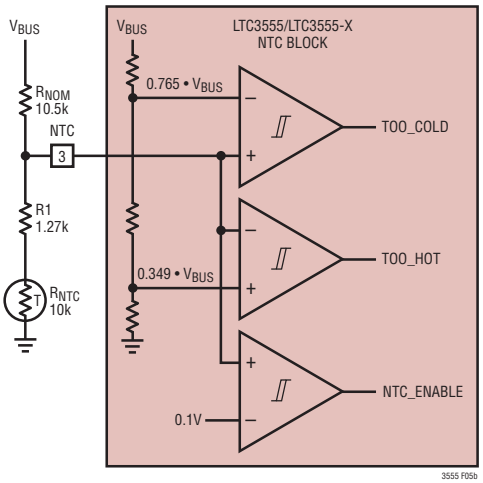
R1 = Optional temperature range adjustment resistor (see Figure 5b)

The trip points for the LTC3555 family's temperature qualification are internally programmed at 0.349 • V_{BUS} for the hot threshold and 0.765 • V_{BUS} for the cold threshold.

Therefore, the hot trip point is set when:



(5a)



(5b)

Figure 5. NTC Circuits

$$\frac{R_{NTC|HOT}}{R_{NOM}+R_{NTC|HOT}} \bullet V_{BUS} = 0.349 \bullet V_{BUS}$$

and the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM}+R_{NTC|COLD}} \bullet V_{BUS} = 0.765 \bullet V_{BUS}$$

Solving these equations for $R_{NTC|COLD}$ and $R_{NTC|HOT}$ results in the following:

$R_{NTC|HOT}$ = 0.536 • R_{NOM}

and

$R_{NTC|COLD}$ = 3.25 • R_{NOM}

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By setting R_{NOM} equal to R25, the above equations result in $\alpha_{HOT} = 0.536$ and $\alpha_{COLD} = 3.25$. Referencing these ratios to the Vishay Resistance-Temperature Curve 1 chart gives a hot trip point of about 40°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 40°C.

By using a bias resistor, R_{NOM}, different in value from R25, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the non-linear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

$$R_{NOM} = \frac{\alpha_{HOT}}{0.536} \bullet R25$$

$$R_{NOM} = \frac{\alpha_{COLD}}{3.25} \bullet R25$$

where α_{HOT} and α_{COLD} are the resistance ratios at the *desired* hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can be chosen, the other is determined by the default ratios designed in the IC. Consider an example where a 60°C hot trip point is desired.

From the Vishay Curve 1 R-T characteristics, α_{HOT} is 0.2488 at 60°C. Using the above equation, R_{NOM} should be set to 4.64k. With this value of R_{NOM}, the cold trip point is about 16°C. Notice that the span is now 44°C rather than the previous 40°C. This is due to the decrease in "temperature gain" of the thermistor as absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 5b. The following formulas can be used to compute the values of R_{NOM} and R1:

$$R_{NOM} = \frac{\alpha_{COLD} - \alpha_{HOT}}{2.714} \bullet R25$$

$$R1 = 0.536 \bullet R_{NOM} - \alpha_{HOT} \bullet R25$$

For example, to set the trip points to 0°C and 45°C with a Vishay Curve 1 thermistor choose:

$$R_{NOM} = \frac{3.266 - 0.4368}{2.714} \bullet 10k = 10.42k$$

the nearest 1% value is 10.5k:

$$R1 = 0.536 \bullet 10.5k - 0.4368 \bullet 10k = 1.26k$$

the nearest 1% value is 1.27k. The final circuit is shown in Figure 5b and results in an upper trip point of 45°C and a lower trip point of 0°C.

USB Inrush Limiting

When a USB cable is plugged into a portable product, the inductance of the cable and the high-Q ceramic input capacitor form an L-C resonant circuit. If the cable does not have adequate mutual coupling or if there is not much impedance in the cable, it is possible for the voltage at the input of the product to reach as high as twice the USB voltage (~10V) before it settles out. In fact, due to the high voltage coefficient of many ceramic capacitors, a nonlinearity, the voltage may even exceed twice the USB voltage. To prevent excessive voltage from damaging the LTC3555 family during a hot insertion, it is best to have a low voltage coefficient capacitor at the V_{BUS} pin to the LTC3555 family. This is achievable by selecting an MLCC capacitor that has a higher voltage rating than that required for the application. For example, a 16V, X5R, 10µF capacitor in a 1206 case would be a better choice than a 6.3V, X5R, 10µF capacitor in a smaller 0805 case.

Alternatively, the following soft connect circuit (Figure 6) can be employed. In this circuit, capacitor C1 holds MP1 off when the cable is first connected. Eventually C1 begins to charge up to the USB input voltage applying increasing gate support to MP1. The long time constant of R1 and C1 prevent the current from building up in the cable too fast thus dampening out any resonant overshoot.

Printed Circuit Board Layout Considerations

In order to be able to deliver maximum current under all conditions, it is critical that the Exposed Pad on the backside of the LTC3555 family package be soldered to the PC board ground. Failure to make thermal contact between the Exposed Pad on the backside of the package and the copper board will result in higher thermal resistances.

Furthermore, due to its high frequency switching circuitry, it is imperative that the input capacitors, inductors and output capacitors be as close to the LTC3555 family as possible and that there be an *unbroken* ground plane under the IC and all of its external high frequency components.

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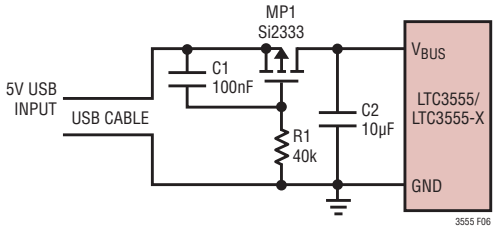


Figure 6. USB Soft Connect Circuit

High frequency currents, such as the V_{BUS}, V_{IN1}, V_{IN2} and V_{IN3} currents on the LTC3555 family, tend to find their way along the ground plane in a myriad of paths ranging from directly back to a mirror path beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur. There should be a group of vias under the grounded backside of the package leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be on the second layer of the PC board.

The GATE pin for the external ideal diode controller has extremely limited drive current. Care must be taken to minimize leakage to adjacent PC board traces. 100nA of leakage from this pin will introduce an offset to the 15mV ideal diode of approximately 10mV. To minimize leakage, the trace can be guarded on the PC board by surrounding it with V_{OUT} connected metal, which should generally be less that one volt higher than GATE.

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3555 family.

1. Are the capacitors at V_{BUS}, V_{IN1}, V_{IN2} and V_{IN3} as close as possible to the LTC3555? These capacitors provide the AC current to the internal power MOSFETs and their drivers. Minimizing inductance from these capacitors to the LTC3555 is a top priority.
2. Are C_{OUT} and L1 closely connected? The (–) plate of C_{OUT} returns current to the GND plane.
3. Keep sensitive components away from the SW pins.

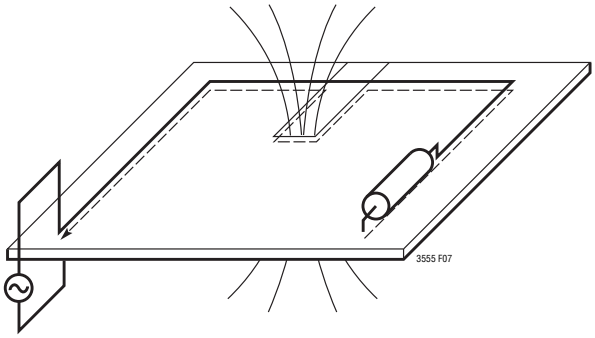


Figure 7. Higher Frequency Ground Currents Follow Their Incident Path. Slices in the Ground Plane Cause High Voltage and Increased Emissions

Battery Charger Stability Considerations

The LTC3555 family's battery charger contains both a constant-voltage and a constant-current control loop. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND. Furthermore, when the battery is disconnected, a 100µF MLCC capacitor in series with a 0.3Ω resistor from BAT to GND is required to prevent oscillation.

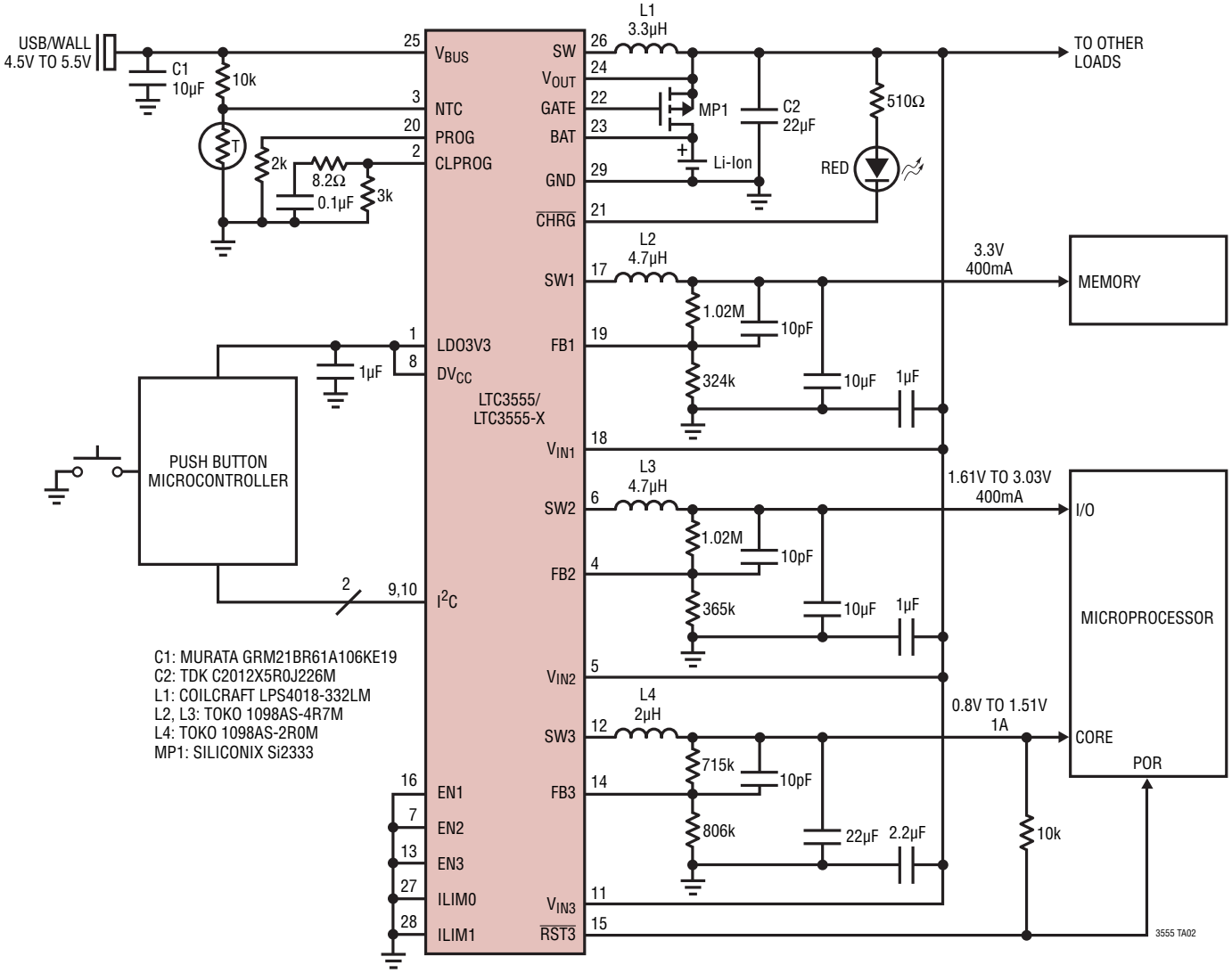
High value, low ESR multilayer ceramic chip capacitors reduce the constant-voltage loop phase margin, possibly resulting in instability. Ceramic capacitors up to 22µF may be used in parallel with a battery, but larger ceramics should be decoupled with 0.2Ω to 1Ω of series resistance.

In constant-current mode, the PROG pin is in the feedback loop rather than the battery voltage. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the battery charger is stable with program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 100kHz \bullet C_{PROG}}$$

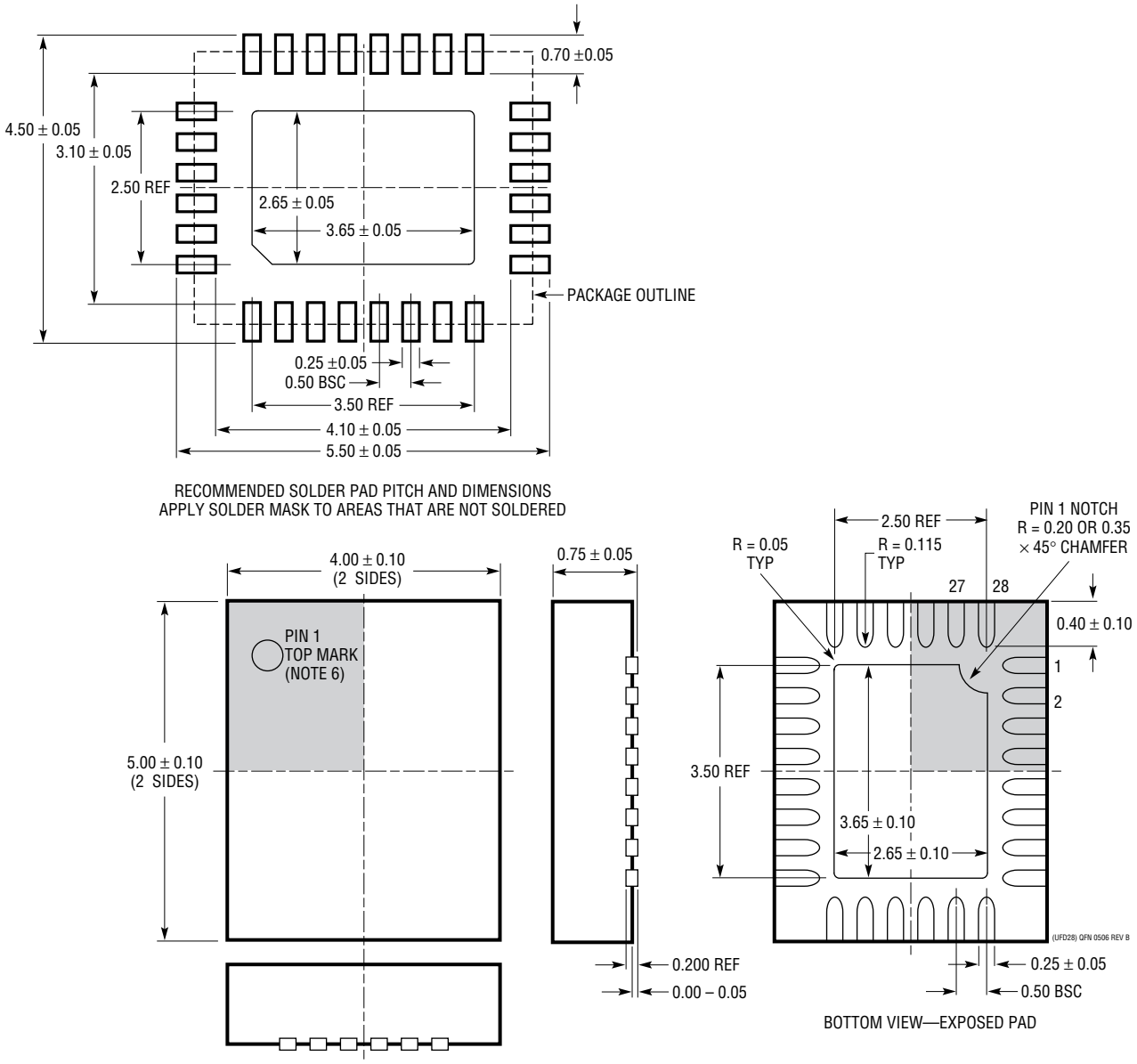
TYPICAL APPLICATION

Watchdog Microcontroller Operation



PACKAGE DESCRIPTION

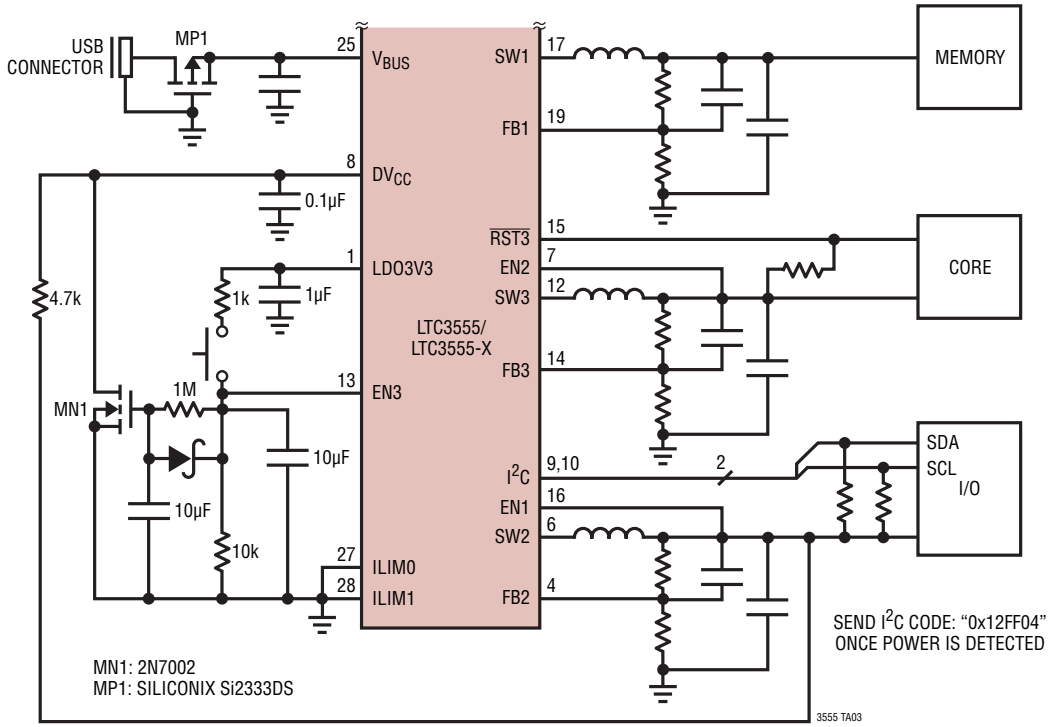
UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Push Button Start with Automatic Sequencing, Reverse Input Voltage Protection and 10 Second Push and Hold Hard Shutdown



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3455	Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger	Seamless Transition Between Input Power Sources: Li-Ion Battery, USB and 5V Wall Adapter. Two High Efficiency DC/DC Converters: Up to 96%. Full Featured Li-Ion Battery Charger with Accurate USB Current Limiting (500mA/100mA). Pin Selectable Burst Mode Operation. Hot Swap™ Output for SDIO and Memory Cards. 24-Lead 4mm × 4mm QFN Package
LTC3456	2-Cell, Multi-Output DC/DC Converter with USB Power Manager	Seamless Transition Between 2-Cell Battery, USB and AC Wall Adapter Input Power Sources. Main Output: Fixed 3.3V Output, Core Output: Adjustable from 0.8V to $V_{BATT(MIN)}$. Hot Swap Output for Memory Cards. Power Supply Sequencing: Main and Hot Swap Accurate USB Current Limiting. High Frequency Operation: 1MHz. High Efficiency: Up to 92%. 24-Lead 4mm × 4mm QFN Package
LTC3552	Standalone Linear Li-Ion Battery Charger with Adjustable Output Dual Synchronous Buck Converter	Synchronous Buck Converter, Efficiency: >90%, Adjustable Outputs at 800mA and 400mA, Charge Current Programmable up to 950mA, USB Compatible, 16-Lead 5mm × 3mm DFN Package
LTC3557/LTC3557-1	USB Power Manager with Li-Ion/Polymer Charger, Triple Synchronous Buck Converter plus LDO	Complete Multi Function PMIC: Linear Power Manager and Three Buck Regulators Charge Current Programmable up to 1.5A from Wall Adapter Input, Thermal Regulation Synchronous Buck Converters Efficiency: >95%, ADJ Outputs: 0.8V to 3.6V at 400mA/400mA/600mA Bat-Track™ Adaptive Output Control, 200mΩ Ideal Diode, 4mm × 4mm QFN-28 Package.
LTC4085	USB Power Manager with Ideal Diode Controller and Li-Ion Charger	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode with <50mΩ option, 4mm × 3mm DFN14 Package
LTC4088/LTC4088-1/ LTC4088-2	High Efficiency USB Power Manager and Battery Charger	Maximizes Available Power from USB Port, Bat-Track, "Instant On" Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always-On LDO, 4mm × 3mm DFN14 Package

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