

### FEATURES

- Eight Independent PSE Channels
- Compliant with IEEE 802.3at Type 1 and 2
- Chipset Provides Electrical Isolation
  - Reduced BOM Cost
  - Eliminates up to 6 High Speed Opto-Couplers
  - Eliminates Isolated 3.3V Power Supply
- Low Power Dissipation
  - 0.25Ω Sense Resistance Per Channel
- Very High Reliability 4-Point PD Detection
  - 2-Point Forced Voltage
  - 2-Point Forced Current
- V<sub>EE</sub> and V<sub>PORT</sub> Monitoring
- 1 Second Rolling I<sub>PORT</sub> Averaging
- Supports 2-Pair and 4-Pair Output Power
- 1MHz I<sup>2</sup>C Compatible Serial Control Interface
- Available In a 40-Lead 6mm × 6mm (LTC4290) and 24-Lead 4mm × 4mm (LTC4271) QFN Package

### APPLICATIONS

- PoE PSE Switches/Routers
- PoE PSE Midspans

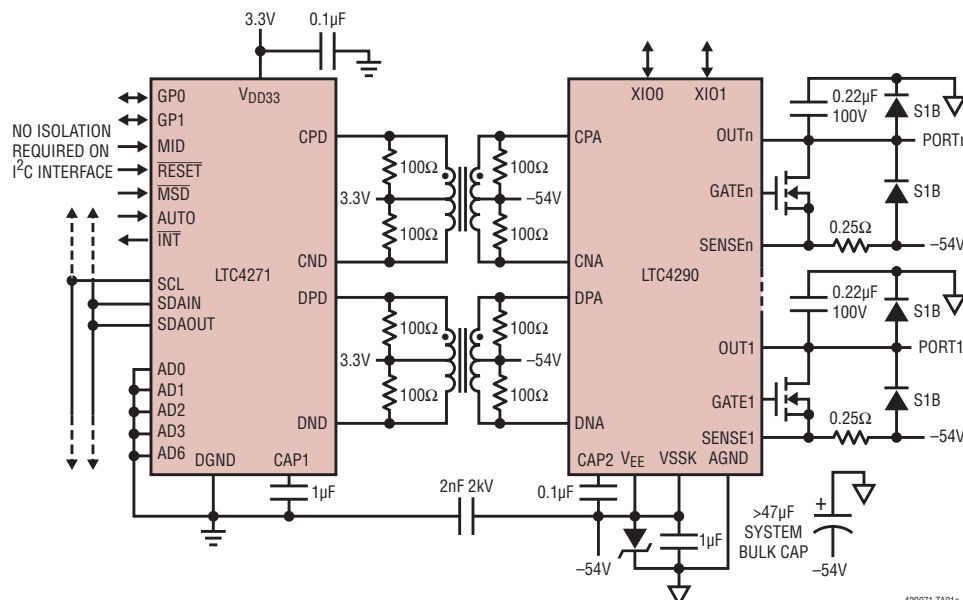
### DESCRIPTION

The LTC<sup>®</sup>4290/LTC4271 chipset is an 8-port power sourcing equipment (PSE) controller designed for use in IEEE 802.3at Type 1 and Type 2 (high power) compliant Power over Ethernet (PoE) systems. Transformer-isolated communication protocol replaces expensive opto-couplers and complex isolated 3.3V supply resulting in significant BOM cost savings. The LTC4290/LTC4271 chipset delivers lowest-in-industry heat dissipation by utilizing low-R<sub>DS(ON)</sub> external MOSFETs and 0.25Ω sense resistors.

Advanced power management features include per-port 12-bit current monitoring ADCs, DAC-programmable current limit, and versatile fast shut-down of preselected ports. Advanced power management host software is available under a no-cost license. PD discovery uses a proprietary dual-mode 4-point detection mechanism ensuring excellent immunity from false PD detection. Midspan PSEs are supported with 2-event classification and a 2 second backoff timer. The LTC4290/LTC4271 includes an I<sup>2</sup>C serial interface operable up to 1MHz.

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### TYPICAL APPLICATION



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## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 4)

### LTC4290

#### Supply Voltages

AGND – V<sub>EE</sub> ..... –0.3V to 80V

VSSK (Note 7) ..... V<sub>EE</sub> – 0.3V to V<sub>EE</sub> + 0.3V

#### Digital Pins

XIO<sub>n</sub> ..... V<sub>EE</sub> – 0.3V to CAP2 + 0.3V

#### Analog Pins

SENSE<sub>n</sub>, GATE<sub>n</sub>, OUT<sub>n</sub> ..... V<sub>EE</sub> – 0.3V to V<sub>EE</sub> + 80V

CAP2 (Note 13) ..... V<sub>EE</sub> – 0.3V to V<sub>EE</sub> + 5V

CPA, CNA, DPA, DNA ..... V<sub>EE</sub> – 0.3V to V<sub>EE</sub> + 0.3

#### Operating Ambient Temperature Range

LTC4290I ..... –40°C to 85°C

Junction Temperature (Note 2) ..... 125°C

Storage Temperature Range ..... –65°C to 150°C

(Note 1)

### LTC4271

#### Supply Voltages

V<sub>DD</sub> – DGND ..... –0.3V to 3.6V

#### Digital Pins

SCL, SDA<sub>IN</sub>, SDA<sub>OUT</sub>,  $\overline{\text{INT}}$ ,  $\overline{\text{RESET}}$ ,  $\overline{\text{MSD}}$ , AD<sub>n</sub>, AUTO,

MID, GP<sub>n</sub> ..... DGND – 0.3V to V<sub>DD</sub> + 0.3V

#### Analog Pins

CAP1 (Note 13) ..... –0.3V to DGND + 2V

CPD, CND, DPD, DND ..... DGND – 0.3V to V<sub>DD</sub> + 0.3V

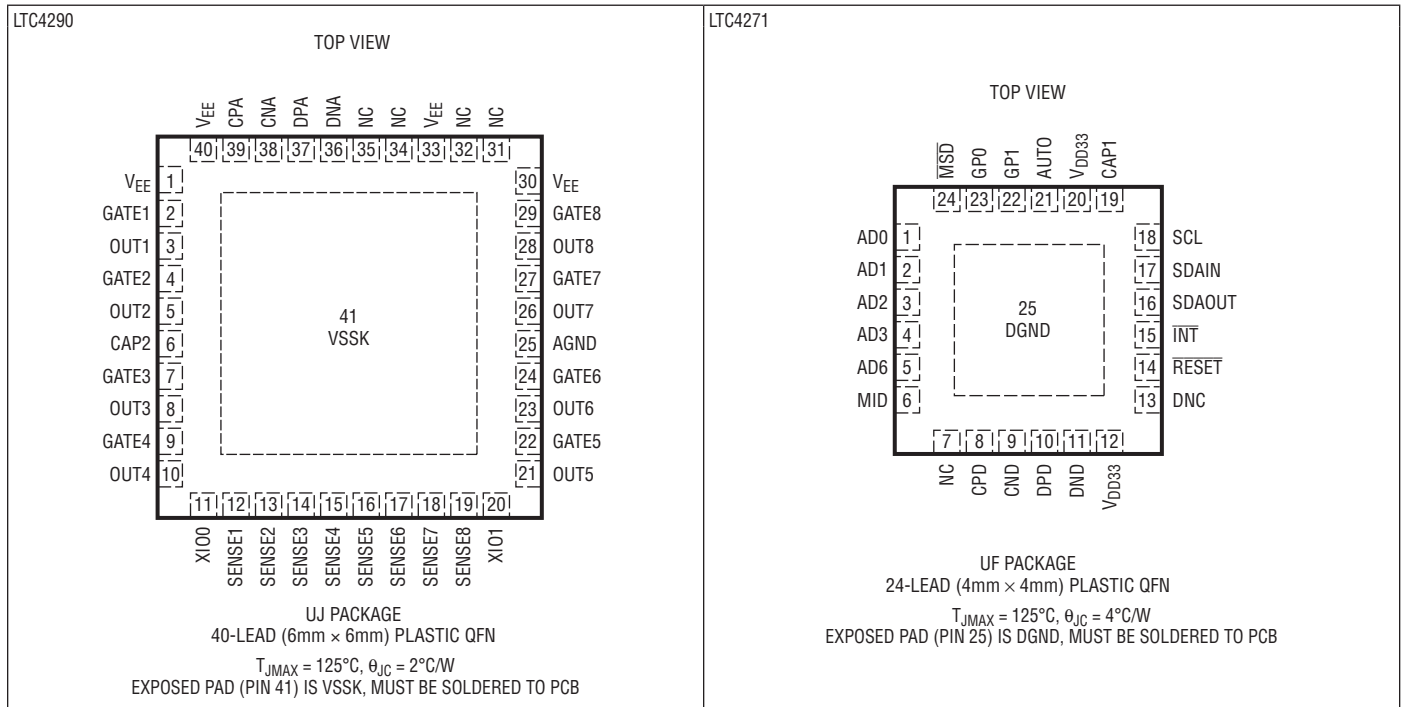
#### Operating Ambient Temperature Range

LTC4271I ..... –40°C to 85°C

Junction Temperature (Note 2) ..... 125°C

Storage Temperature Range ..... –65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	MAX PWR	TEMPERATURE RANGE
LTC4271IUF#PBF	LTC4271IUF#TRPBF	4271	24-Lead (4mm × 4mm) Plastic QFN		-40°C to 85°C
LTC4290BIUJ#PBF	LTC4290BIUJ#TRPBF	LTC4290BUJ	40-Lead (6mm × 6mm) Plastic QFN	25.5W	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $\text{AGND} - V_{EE} = 54\text{V}$  and  $V_{DD} - \text{DGND} = 3.3\text{V}$  unless otherwise noted. (Notes 3 & 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{EE}$	Main PoE Supply Voltage	$\text{AGND} - V_{EE}$ For IEEE Type 1 Compliant Output	● 45		57	V
		For IEEE Type 2 Compliant Output	● 51		57	V
	Undervoltage Lock-Out	$\text{AGND} - V_{EE}$	● 20	25	30	V
$V_{DD}$	$V_{DD}$ Supply Voltage	$V_{DD} - \text{DGND}$	● 3.0	3.3	3.6	V
	Undervoltage Lock-Out	$V_{DD} - \text{DGND}$		2.7		V
$V_{CAP1}$	Internal Regulator Supply Voltage	$V_{CAP1} - \text{DGND}$		1.84		V
$V_{CAP2}$	Internal Regulator Supply Voltage	$V_{CAP2} - V_{EE}$		4.3		V
$I_{EE}$	$V_{EE}$ Supply Current	$(\text{AGND} - V_{EE}) = 55\text{V}$	●	9	15	mA
$R_{EE}$	$V_{EE}$ Supply Resistance	$V_{EE} < 15\text{V}$	●		12	k $\Omega$
$I_{DD}$	$V_{DD}$ Supply Current	$(V_{DD} - \text{DGND}) = 3.3\text{V}$	●	10	15	mA

### Detection

	Detection Current – Forced Current	First Point, $\text{AGND} - V_{OUTn} = 9\text{V}$ Second Point, $\text{AGND} - V_{OUTn} = 3.5\text{V}$	● 220 ● 143	240 160	260 180	$\mu\text{A}$ $\mu\text{A}$
	Detection Voltage – Forced Voltage	$\text{AGND} - V_{OUTn}$ , $5\mu\text{A} \leq I_{OUTn} \leq 500\mu\text{A}$ First Point Second Point	● 7 ● 3	8 4	9 5	V V
	Detection Current Compliance	$\text{AGND} - V_{OUTn} = 0\text{V}$	●	0.8	0.9	mA
$V_{OC}$	Detection Voltage Compliance	$\text{AGND} - V_{OUTn}$ , Open Port	●	10.4	12	V
	Detection Voltage Slew Rate	$\text{AGND} - V_{OUTn}$ , $C_{PORT} = 0.15\mu\text{F}$	●		0.01	V/ $\mu\text{s}$
	Min. Valid Signature Resistance		● 15.5	17	18.5	k $\Omega$
	Max. Valid Signature Resistance		● 27.5	29.7	32	k $\Omega$

### Classification

$V_{CLASS}$	Classification Voltage	$\text{AGND} - V_{OUTn}$ , $0\text{mA} \leq I_{OUTn} \leq 50\text{mA}$	● 16.0		20.5	V
	Classification Current Compliance	$V_{OUTn} = \text{AGND}$	● 53	61	67	mA
	Classification Threshold Current	Class 0-1	● 5.5	6.5	7.5	mA
		Class 1-2	● 13.5	14.5	15.5	mA
		Class 2-3	● 21.5	23	24.5	mA
		Class 3-4	● 31.5	33	34.9	mA
		Class 4-Overcurrent	● 45.2	48	50.8	mA
$V_{MARK}$	Classification Mark State Voltage	$\text{AGND} - V_{OUTn}$ , $0.1\text{mA} \leq I_{CLASS} \leq 5\text{mA}$	● 7.5	9	10	V
	Mark State Current Compliance	$V_{OUTn} = \text{AGND}$	● 53	61	67	mA

### Gate Driver

	GATE Pin Pull-Down Current	Port Off, $V_{GATEn} = V_{EE} + 5\text{V}$	● 0.4			mA
		Port Off, $V_{GATEn} = V_{EE} + 1\text{V}$	● 0.08	0.12		mA
	GATE Pin Fast Pull-Down Current	$V_{GATEn} = V_{EE} + 5\text{V}$		30		mA
	GATE Pin On Voltage	$V_{GATEn} - V_{EE}$ , $I_{GATEn} = 1\mu\text{A}$	● 8	12	14	V

### Output Voltage Sense

$V_{PG}$	Power Good Threshold Voltage	$V_{OUTn} - V_{EE}$	● 2	2.4	2.8	V
	OUT Pin Pull-Up Resistance to AGND	$0\text{V} \leq (\text{AGND} - V_{OUT}) \leq 5\text{V}$	● 300	500	700	k $\Omega$

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{CUT}}$	Overcurrent Sense Voltage	$V_{\text{SENSEn}} - V_{EE}$ , $h_{\text{pen}} = 0\text{Fh}$ , $cutn = \text{D4h}$	● 89	94	99	mV
		$h_{\text{pen}} = 0\text{Fh}$ , $cutn = \text{E2h}$ (Note 12)	● 152	159	168	mV
	Overcurrent Sense in AUTO Pin Mode	Class 0, Class 3	● 89	94	99	mV
		Class 1	● 26	28	30	mV
		Class 2	● 49	52	55	mV
		Class 4	● 152	159	168	mV
$V_{\text{LIM}}$	Active Current Limit in 802.3af Compliant Mode	$V_{\text{SENSEn}} - V_{EE}$ , $h_{\text{pen}} = 0\text{Fh}$ , $limn = 80\text{h}$ , ( $\text{AGND} - V_{EE}$ ) = 55V $V_{EE} < V_{\text{OUT}} < \text{AGND} - 29\text{V}$ $\text{AGND} - V_{\text{OUT}} = 0\text{V}$ (Note 12)	● 102	106	112	mV
			● 25		50	mV
	Active Current Limit in High Power Mode	$h_{\text{pen}} = 0\text{Fh}$ , $limn = \text{C0h}$ , ( $\text{AGND} - V_{EE}$ ) = 55V $V_{\text{OUT}} - V_{EE} = 0 - 10\text{V}$ $V_{EE} + 23\text{V} < V_{\text{OUT}} < \text{AGND} - 29\text{V}$ $\text{AGND} - V_{\text{OUT}} = 0\text{V}$ (Note 12)	● 204	212	225	mV
		● 102	106	115	mV	
		● 25		50	mV	
$V_{\text{LIM}}$	Active Current Limit in AUTO Pin Mode	$V_{EE} < V_{\text{OUT}} < \text{AGND} - 10\text{V}$ , ( $\text{AGND} - V_{EE}$ ) = 55V Class 0 to Class 3	● 102	106	112	mV
		Class 4	● 204	212	225	mV
$V_{\text{MIN}}$	DC Disconnect Sense Voltage	$V_{\text{SENSE}} - V_{EE}$ , $rdis \text{ Bit} = 0$	● 2.6	3.8	4.9	mV
		$V_{\text{SENSE}} - V_{EE}$ , $rdis \text{ Bit} = 1$ (Note 12)	● 1.3	1.9	2.45	mV
$V_{\text{SC}}$	Short-Circuit Sense	$V_{\text{SENSEn}} - V_{EE} - V_{\text{LIM}}$ (Note 12) $rdis \text{ Bit} = 0$	● 125	200	255	mV
		$rdis \text{ Bit} = 1$	● 70	100	125	mV

**Port Current Readback**

Resolution	No Missing Codes, Reported as 14 Bits		12	Bits
LSB Weight	$V_{\text{SENSEn}} - V_{EE}$		30.518	$\mu\text{V}/\text{LSB}$
Conversion Period			25.1	ms/ Convert

**Port Voltage Readback**

Resolution	No Missing Codes, Reported as 14 Bits		12	Bits
LSB Weight	$V_{\text{SENSEn}} - V_{EE}$		5.8350	mV/LSB

**Digital Interface**

$V_{\text{ILD}}$	Digital Input Low Voltage	$\text{ADn}$ , $\overline{\text{RESET}}$ , $\overline{\text{MSD}}$ , $\text{GPn}$ , $\text{AUTO}$ , $\text{MID}$ (Note 6)	●		0.8	V
	I <sup>2</sup> C Input Low Voltage	$\text{SCL}$ , $\text{SDAIN}$ (Note 6)	●		1.0	V
$V_{\text{IHD}}$	Digital Input High Voltage	(Note 6)	●	2.2		V
	Digital Output Voltage Low	$I_{\text{SDAOUT}} = 3\text{mA}$ , $I_{\text{INT}} = 3\text{mA}$	●		0.4	V
		$I_{\text{SDAOUT}} = 5\text{mA}$ , $I_{\text{INT}} = 5\text{mA}$	●		0.7	V
	Internal Pull Up to $V_{\text{DD}}$	$\text{ADn}$ , $\overline{\text{RESET}}$ , $\overline{\text{MSD}}$ , $\text{GPn}$			50	$\text{k}\Omega$
	Internal Pull Down To $\text{DGND}$	$\text{AUTO}$ , $\text{MID}$			50	$\text{k}\Omega$

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>XIO</b>						
$V_{OLX}$	XIO Digital Output Low	$V_{XIO_n} - V_{EE}$ , $I_{XIO_n} = 5\text{mA}$	●		0.7	V
$V_{OHX}$	XIO Digital Output High	$V_{XIO_n} - V_{EE}$ , $I_{XIO_n} = 100\mu\text{A}$	●	3.5		V
	XIO Digital Input Low Voltage	$V_{XIO_n} - V_{EE}$	●		0.8	V
	XIO Digital Input High Voltage	$V_{XIO_n} - V_{EE}$	●	3.4		V
	Internal Pull Up to CAP2	X100, XIO1		50		k $\Omega$

### PSE Timing Characteristics

$t_{DET}$	Detection Time	Beginning To End of Detection (Note 7)		220		ms	
$t_{CLE}$	Class Event Duration	(Note 7)		12		ms	
$t_{CLEON}$	Class Event Turn On Duration	$C_{PORT} = 0.6\mu\text{F}$ (Note 7)	●		0.1	ms	
$t_{ME}$	Mark Event Duration	(Note 7, Note 11)		8.6		ms	
$t_{MEL}$	Last Mark Event Duration	(Note 7, Note 11)	●	16	22	ms	
$t_{PON}$	Power On Delay in AUTO Pin Mode	From End of Valid Detect to Application of Power to Port (Note 7)	●		60	ms	
	Turn-On Rise Time	( $AGND - V_{OUT}$ ): 10% to 90% of ( $AGND - V_{EE}$ ) $C_{PORT} = 0.15\mu\text{F}$ (Note 7)	●	15	24	$\mu\text{s}$	
	Turn-On Ramp Rate	$C_{PORT} = 0.15\mu\text{F}$ (Note 7)	●		10	V/ $\mu\text{s}$	
$t_{TOCL}$	Turn-On Class Transition	$C_{PORT} = 0.15\mu\text{F}$ (Note 7)	●		0.1	ms	
$t_{ED}$	Fault Delay	From $I_{CUT}$ or $I_{LIM}$ Fault to Next Detect (Note 7)	●	1.0	1.1	s	
	Midspan Mode Detection Backoff	$R_{PORT} = 15.5\text{k}\Omega$ (Note 7)	●	2.3	2.5	2.7	s
	Power Removal Detection Delay	From Power Removal After $t_{DIS}$ to Next Detect (Note 7)	●	1.0	1.3	2.5	s
$t_{START}$	Maximum Current Limit Duration During Port Start-Up	(Note 7)	●	52	59	66	ms
$t_{CUT}$	Maximum Overcurrent Duration After Port Start-Up	(Note 7)	●	52	59	66	ms
	Maximum Overcurrent Duty Cycle	(Note 7)	●	5.8	6.3	6.7	%
$t_{LIM}$	Maximum Current Limit Duration After Port Start-Up – $t_{LIM}$ Enabled	$t_{LIM} = 1$ (Note 7, Note 12)	●	10	12	14	ms
	Maximum Current Limit Duration After Port Start-Up – $t_{LIM}$ as $t_{CUT}$	$t_{LIM} = 0$ (Note 7, Note 12)	●	52	59	66	ms
$t_{MPS}$	Maintain Power Signature (MPS) Pulse Width Sensitivity	Current Pulse Width to Reset Disconnect Timer (Note 7, Note 8)	●	1.6		3.6	ms
$t_{DIS}$	Maintain Power Signature (MPS) Dropout Time	(Note 7, Note 5)	●	320	350	380	ms
$t_{MSD}$	Masked Shut Down Delay	(Note 7)			6.5	$\mu\text{s}$	
	I <sup>2</sup> C Watchdog Timer Duration	(Note 7)	●	1.5	2	3	s
	Minimum Pulse Width for Masked Shut Down	(Note 7)	●	3		$\mu\text{s}$	
	Minimum Pulse Width for $\overline{\text{RESET}}$	(Note 7)	●	4.5		$\mu\text{s}$	

## ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>I<sup>2</sup>C Timing</b>							
f <sub>SCLK</sub>	Clock Frequency	(Note 7)	●			1	MHz
t <sub>1</sub>	Bus Free Time	Figure 5 (Notes 7, 9)	●	480			ns
t <sub>2</sub>	Start Hold Time	Figure 5 (Notes 7, 9)	●	240			ns
t <sub>3</sub>	SCL Low Time	Figure 5 (Notes 7, 9)	●	480			ns
t <sub>4</sub>	SCL High Time	Figure 5 (Notes 7, 9)	●	240			ns
t <sub>5</sub>	SDAIN Data Hold Time	Figure 5 (Notes 7, 9)	●	60			ns
t <sub>5</sub>	Data Clock to SDAOUT Valid	Figure 5 (Notes 7, 9)	●			130	ns
t <sub>6</sub>	Data Set-Up Time	Figure 5 (Notes 7, 9)	●	80			ns
t <sub>7</sub>	Start Set-Up Time	Figure 5 (Notes 7, 9)	●	240			ns
t <sub>8</sub>	Stop Set-Up Time	Figure 5 (Notes 7, 9)	●	240			ns
t <sub>r</sub>	SCL, SDAIN Rise Time	Figure 5 (Notes 7, 9)	●			120	ns
t <sub>f</sub>	SCL, SDAIN Fall Time	Figure 5 (Notes 7, 9)	●			60	ns
	Fault Present to $\overline{\text{INT}}$ Pin Low	(Notes 7, 9, 10)	●			150	ns
	Stop Condition to $\overline{\text{INT}}$ Pin Low	(Notes 7, 9, 10)	●			1.5	μs
	ARA to $\overline{\text{INT}}$ Pin High Time	(Notes 7, 9)	●			1.5	μs
	SCL Fall to ACK Low	(Notes 7, 9)	●			130	ns

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. With the exception of ( $\text{V}_{\text{DD}} - \text{DGND}$ ), exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $140^\circ\text{C}$  when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 3:** All currents into device pins are positive; all currents out of device pins are negative.

**Note 4:** The LTC4290 operates with a negative supply voltage (with respect to AGND). To avoid confusion, voltages in this data sheet are referred to in terms of absolute magnitude.

**Note 5:** t<sub>DJS</sub> is the same as t<sub>MPO</sub> defined by IEEE 802.3

**Note 6:** The LTC4271 digital interface operates with respect to DGND. All logic levels are measured with respect to DGND.

**Note 7:** Guaranteed by design, not subject to test.

**Note 8:** The IEEE 802.3 specification allows a PD to present its Maintain Power Signature (MPS) on an intermittent basis without being disconnected. In order to stay powered, the PD must present the MPS for t<sub>MPS</sub> within any t<sub>MPO</sub> time window.

**Note 9:** Values Measured at V<sub>ILD</sub> and V<sub>IHD</sub>

**Note 10:** If a fault condition occurs during an I<sup>2</sup>C transaction, the  $\overline{\text{INT}}$  pin will not be pulled down until a stop condition is present on the I<sup>2</sup>C bus.

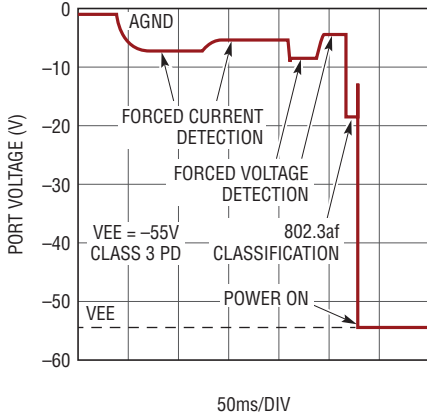
**Note 11:** Load characteristics of the LTC4290 during Mark:  $7\text{V} < (\text{AGND} - \text{V}_{\text{OUTn}}) < 10\text{V}$  or  $\text{I}_{\text{OUT}} < 50\mu\text{A}$ .

**Note 12:** See the LTC4271 Software Programming documentation for information on serial bus usage and device configuration and status registers.

**Note 13:** Do not source or sink current from CAP1 and CAP2.

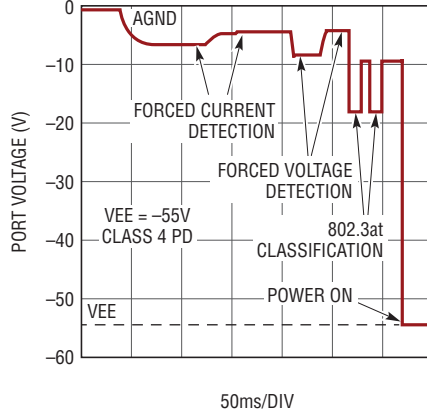
## TYPICAL PERFORMANCE CHARACTERISTICS

**802.3af Power On Sequence in AUTO Pin Mode**



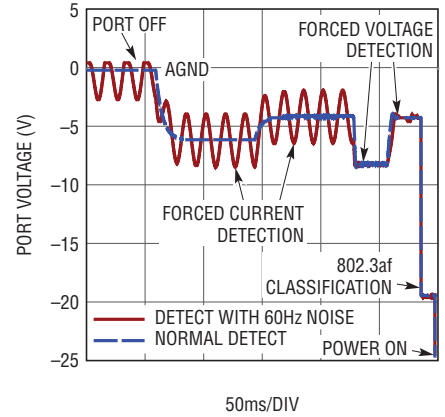
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**802.3at Power On Sequence in AUTO Pin Mode**



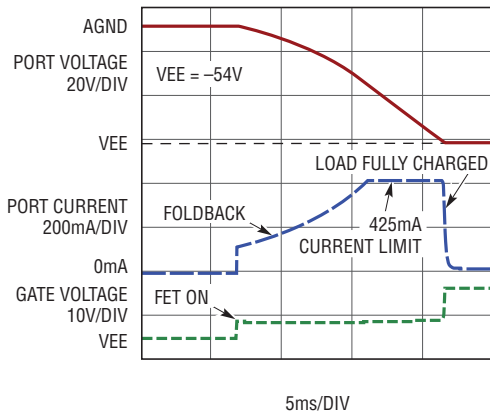
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**Power On Sequence with 10Vpp 60Hz Noise**



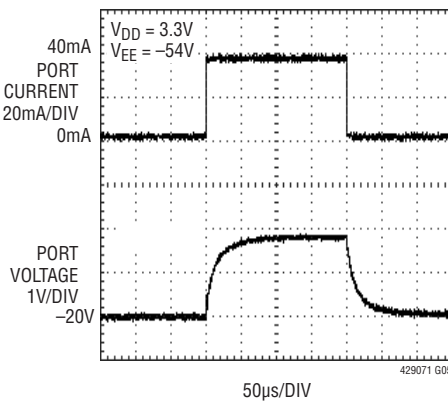
429071 G03

**Powering Up into a 180µF Load**



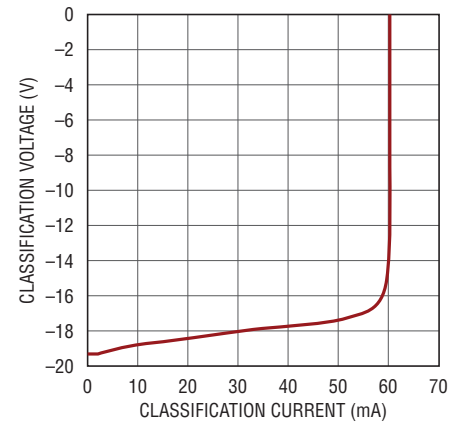
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**Classification Transient Response to 40mA Load Step**



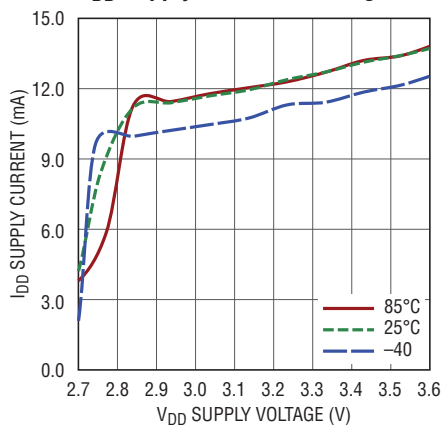
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**Classification Current Compliance**



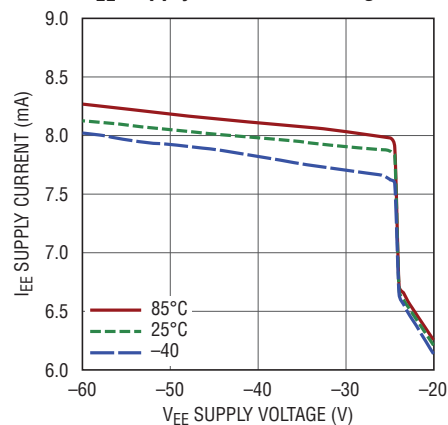
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**V<sub>DD</sub> Supply Current vs Voltage**



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**V<sub>EE</sub> Supply Current vs Voltage**

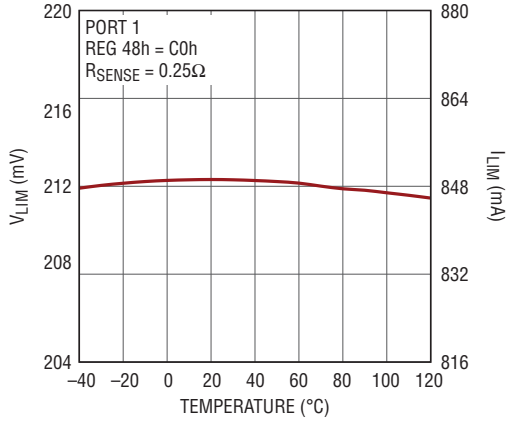


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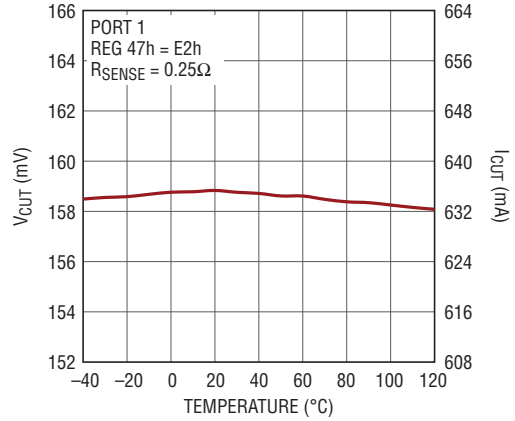
# TYPICAL PERFORMANCE CHARACTERISTICS

**802.3at  $I_{LIM}$  Threshold vs Temperature**



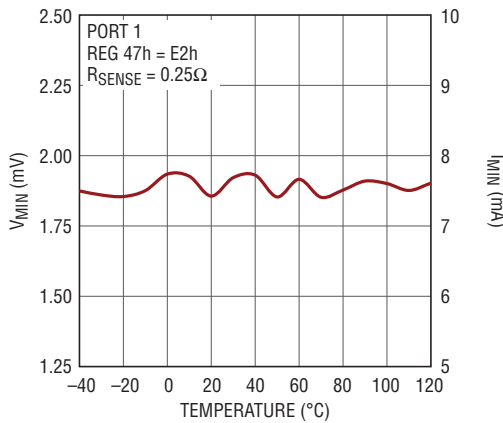
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**802.3at  $I_{CUT}$  Threshold vs Temperature**



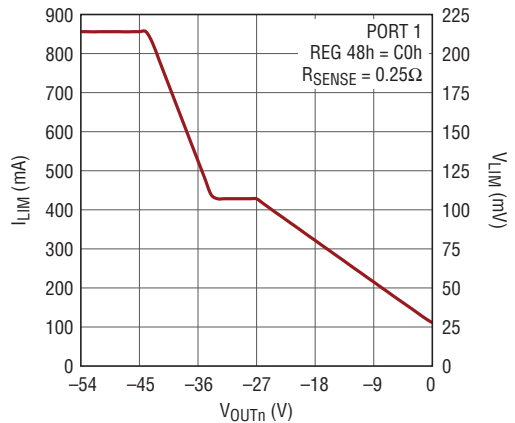
429071 G10

**DC Disconnect Threshold vs Temperature**



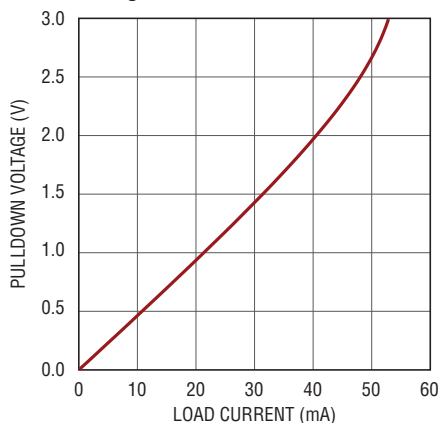
429071 G11

**802.3at Current Limit Foldback**



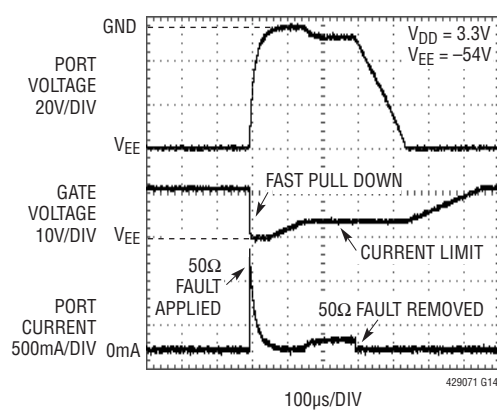
429071 G12

**$\overline{INT}$  and SDAOUT Pull Down Voltage vs Load Current**



429071 G13

**MOSFET Gate Drive With Fast Pull Down**



429071 G14

## TEST TIMING DIAGRAMS

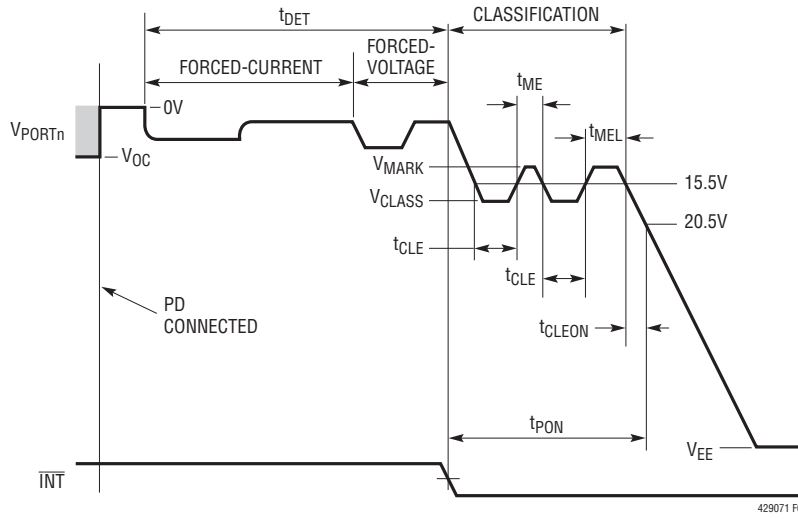


Figure 1. Detect, Class and Turn-On Timing in AUTO Pin or Semi-auto Modes

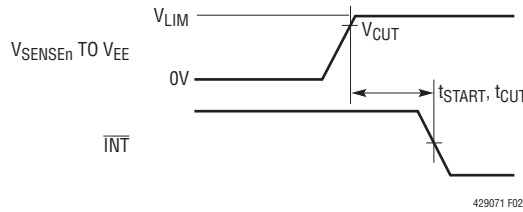


Figure 2. Current Limit Timing

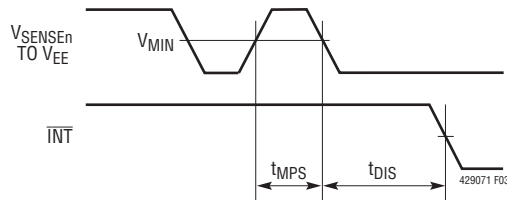


Figure 3. DC Disconnect Timing

# TEST TIMING DIAGRAMS

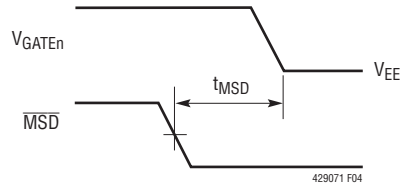


Figure 4. Shut Down Delay Timing

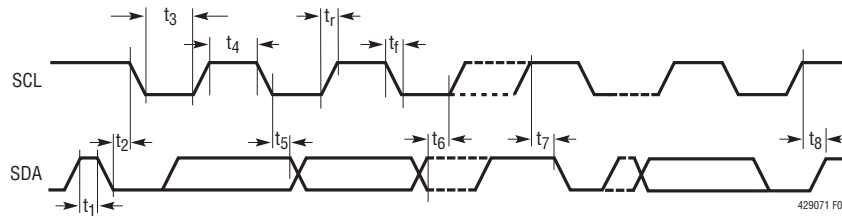


Figure 5. I<sup>2</sup>C Interface Timing

# I<sup>2</sup>C TIMING DIAGRAMS

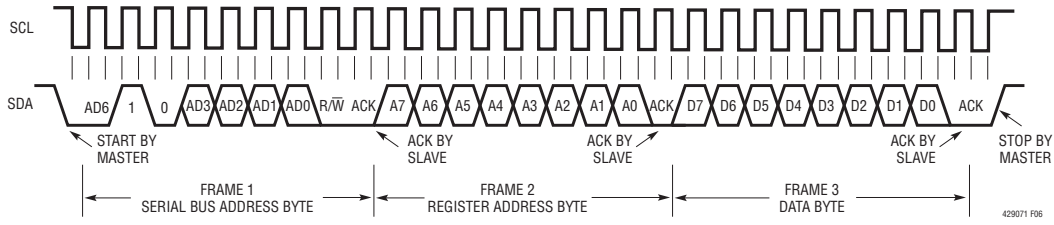


Figure 6. Writing to a Register

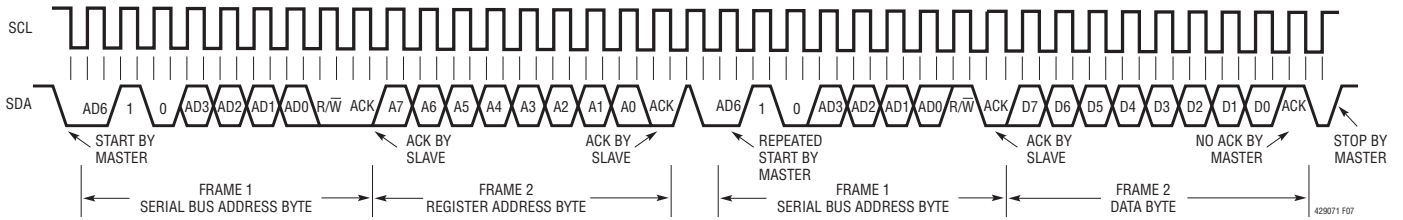


Figure 7. Reading from a Register

## I<sup>2</sup>C TIMING DIAGRAMS

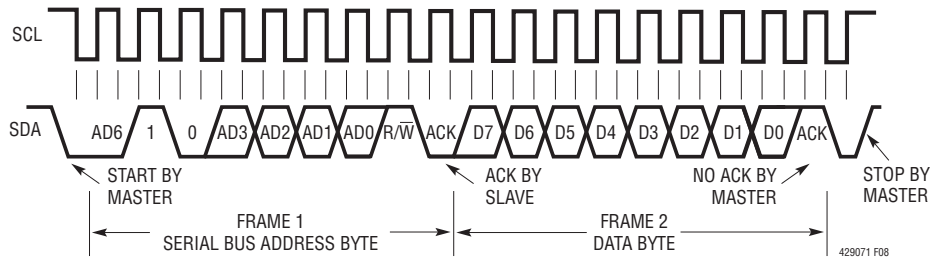


Figure 8. Reading the Interrupt Register (Short Form)

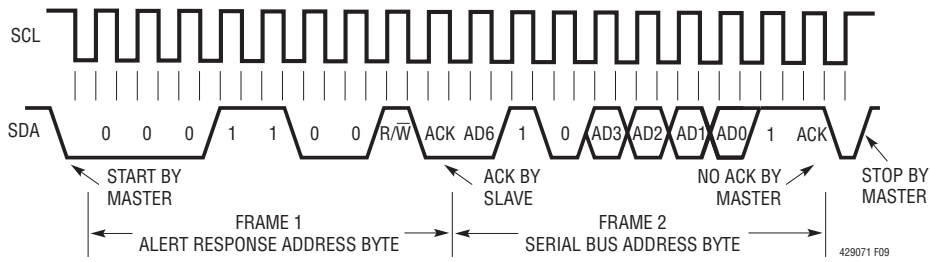


Figure 9. Reading from Alert Response Address

## PIN FUNCTIONS

### LTC4290

**V<sub>EE</sub> (Pins 1, 30, 33, 40):** Main PoE Supply Input. Connect to a –45V to –57V supply, relative to AGND. Voltage depends on PSE type (Type 1 or Type 2).

**GATEn (Pins 2, 4, 7, 9, 22, 24, 27, 29):** Port n Gate Drive. GATEn should be connected to the gate of the external MOSFET for port n. When the MOSFET is turned on, the gate voltage is driven to 12V (typ) above V<sub>EE</sub>. During a current limit condition, the voltage at GATEn will be reduced to maintain constant current through the external MOSFET. If the fault timer expires, GATEn is pulled down, turning the MOSFET off and recording a port fault event. If the port is unused, float the GATEn pin.

**OUTn (Pins 3, 5, 8, 10, 21, 23, 26, 28):** Port n Output Voltage Monitor. OUTn should be connected to the output port. A current limit foldback circuit limits the power dissipation in the external MOSFET by reducing the current limit threshold when the drain-to-source voltage exceeds 10V. The port n Power Good bit is set when the voltage from OUTn to V<sub>EE</sub> drops below 2.4V (typ). A 500k resistor is connected internally from OUTn to AGND when the port is idle. If the port is unused, the OUTn pin must be floated.

**CAP2 (Pin 6):** Analog Internal 4.3V Power Supply Bypass Capacitor. Connect 0.1μF ceramic cap to V<sub>EE</sub>.

**XI00 (Pin 11):** General Purpose Digital Input Output. Logic signal between V<sub>EE</sub> and V<sub>EE</sub> + 4.3V. Internal pull up.

**SENSEn (Pins 12, 13, 14, 15, 16, 17, 18, 19):** Port n Current Sense Input. SENSEn monitors the external MOSFET current via a 0.5Ω or 0.25Ω sense resistor between SENSEn and V<sub>EE</sub>. Whenever the voltage across the sense resistor exceeds the overcurrent detection threshold V<sub>CUT</sub>, the current limit fault timer counts up. If the voltage across the sense resistor reaches the current limit threshold V<sub>LIM</sub>, the GATEn pin voltage is lowered to maintain constant current in the external MOSFET. See Applications Information for further details. If the port is unused, the SENSEn pin must be tied to V<sub>EE</sub>.

**XI01 (Pin 20):** General Purpose Digital Input Output. Logic signal between V<sub>EE</sub> and V<sub>EE</sub> + 4.3V. Internal pull up.

**AGND (Pin 25):** Analog Ground. Connect AGND to the return for the V<sub>EE</sub> supply.

**DNA (Pin 36):** Data Transceiver Negative Input Output (Analog). Connect to DND through a data transformer.

**DPA (Pin 37):** Data Transceiver Positive Input Output (Analog). Connect to DPD through a data transformer.

**CNA (Pin 38):** Clock Transceiver Negative Input Output (Analog). Connect to CND through a data transformer.

**CPA (Pin 39):** Clock Transceiver Positive Input Output (Analog). Connect to CPD through a data transformer.

**VSSK (Exposed Pad Pin 41):** Kelvin Sense to V<sub>EE</sub>. Connect to sense resistor common node. Do not connect directly to V<sub>EE</sub> plane. See Layout Guide.

### Common Pins

**NC, DNC (LTC4271 Pins 7, 13; LTC4290 Pins 31, 32, 34, 35):** All pins identified with “NC” or “DNC” must be left unconnected.

### LTC4271

**AD0 (Pin 1):** Address Bit 0. Tie the address pins high or low to set the starting I<sup>2</sup>C serial address to which the LTC4271 responds. The chip will respond to this address plus the next two incremental addresses. The base address of the first four ports will be (A<sub>6</sub>10A<sub>3</sub>A<sub>2</sub>A<sub>1</sub>A<sub>0</sub>)b. The second and third groups of four ports will respond at the next two logical addresses. Internally pulled up to V<sub>DD</sub>.

**AD1 (Pin 2):** Address Bit 1. See AD0.

**AD2 (Pin 3):** Address Bit 2. See AD0.

**AD3 (Pin 4):** Address Bit 3. See AD0.

**AD6 (Pin 5):** Address Bit 6. See AD0.

**MID (Pin 6):** Midspan Mode Input. When high, the LTC4271 acts as a midspan device. Internally pulled down to DGND.

**CPD (Pin 8):** Clock Transceiver Positive Input Output (Digital). Connect to CPA through a data transformer.

## PIN FUNCTIONS

**CND (Pin 9):** Clock Transceiver Negative Input Output (Digital). Connect to CNA through a data transformer.

**DPD (Pin 10):** Data Transceiver Positive Input Output (Digital). Connect to DPA through a data transformer.

**DND (Pin 11):** Data Transceiver Negative Input Output (Digital). Connect to DNA through a data transformer.

**V<sub>DD33</sub> (Pins 12, 20):** V<sub>DD</sub> IO Power Supply. Connect to a 3.3V power supply relative to DGND. V<sub>DD33</sub> must be bypassed to DGND near the LTC4271 with at least a 0.1μF capacitor.

**RESET (Pin 14):** Reset Input, Active Low. When the RESET pin is low, the LTC4290/LTC4271 is held inactive with all ports off and all internal registers reset to their power-up states. When RESET is pulled high, the LTC4271 begins normal operation. RESET can be connected to an external capacitor or RC network to provide a power turn-on delay. Internal filtering of the RESET pin prevents glitches less than 1μs wide from resetting the LTC4290/LTC4271. Internally pulled up to V<sub>DD</sub>.

**INT (Pin 15):** Interrupt Output, Open Drain. INT will pull low when any one of several events occur in the LTC4271. It will return to a high impedance state when bits 6 or 7 are set in the Reset PB register (1Ah). The INT signal can be used to generate an interrupt to the host processor, eliminating the need for continuous software polling. Individual INT events can be disabled using the INT Mask register (01h). See LTC4271 Software Programming documentation for more information. The INT pin is only updated between I<sup>2</sup>C transactions.

**SDAOUT (Pin 16):** Serial Data Output, Open Drain Data Output for the I<sup>2</sup>C Serial Interface Bus. The LTC4271 uses two pins to implement the bidirectional SDA function to simplify optoisolation of the I<sup>2</sup>C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.

**SDAIN (Pin 17):** Serial Data Input. High impedance data input for the I<sup>2</sup>C serial interface bus. The LTC4271 uses two pins to implement the bidirectional SDA function to simplify optoisolation of the I<sup>2</sup>C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.

**SCL (Pin 18):** Serial Clock Input. High impedance clock input for the I<sup>2</sup>C serial interface bus. The SCL pin should be connected directly to the I<sup>2</sup>C SCL bus line. SCL must be tied high if the I<sup>2</sup>C serial interface bus is not used.

**CAP1 (Pin 19):** Core Power Supply Bypass Capacitor. Connect a 1μF Bypass capacitance to DGND for the internal 1.8V regulator. Do not use other capacitor values.

**AUTO (Pin 21):** AUTO Pin Mode Input. AUTO pin mode allows the LTC4271 to detect and power up a PD even if there is no host controller present on the I<sup>2</sup>C bus. The AUTO pin determines the state of the internal registers when the LTC4271 is reset or comes out of V<sub>DD</sub> UVLO (see LTC4271 Software Programming documentation). The states of these register bits can subsequently be changed via the I<sup>2</sup>C interface. Internally pulled down to DGND. Must be tied locally to either V<sub>DD</sub> or DGND.

**GP1 (Pin 22):** General Purpose Digital Input Output for customer applications. Referenced to DGND.

**GP0 (Pin 23):** General Purpose Digital Input Output for customer applications. Referenced to DGND.

**MSD (Pin 24):** Maskable Shutdown Input. Active low. When pulled low, all ports that have their corresponding mask bit set in the mconfig register (17h) will be reset. Internal filtering of the MSD pin prevents glitches less than 1μs wide from resetting ports. The MSD Pin Mode register can configure the MSD pin polarity. Internally pulled up to V<sub>DD</sub>.

**DGND (Exposed Pad Pin 25):** Digital Ground. DGND should be connected to the return from the V<sub>DD</sub> supply.





## APPLICATIONS INFORMATION

### PoE BASICS

Common Ethernet data connections consist of two or four twisted pairs of copper wire (commonly known as CAT-5 cable), transformer-coupled at each end to avoid ground loops. PoE systems take advantage of this coupling arrangement by applying voltage between the center-taps of the data transformers to transmit power from the PSE to the PD without affecting data transmission. Figure 10 shows a high level PoE system schematic.

To avoid damaging legacy data equipment that does not expect to see DC voltage, the PoE spec defines a protocol that determines when the PSE may apply and remove power. Valid PDs are required to have a specific 25k common mode resistance at their input. When such a PD is connected to the cable, the PSE detects this signature resistance and turns on the power. When the PD is later disconnected, the PSE senses the open circuit and turns power off. The PSE also turns off power in the event of a current fault or short circuit.

When a PD is detected, the PSE optionally looks for a classification signature that tells the PSE the maximum power the PD will draw. The PSE can use this information to allocate power among several ports, to police the current consumption of the PD, or to reject a PD that will draw more power than the PSE has available. The classification step is optional; if a PSE chooses not to classify a PD, it must assume that the PD is a 13W (full 802.3af power) device.

### New in 802.3at

The newer 802.3at standard supersedes 802.3af and brings several new features:

- A PD may draw as much as 25.5W. Such PDs (and the PSEs that support them) are known as Type 2. Older 13W 802.3af equipment is classified as Type 1. Type 1 PDs will work with all PSEs; Type 2 PDs may require Type 2 PSEs to work properly. The LTC4290/LTC4271

is designed to work in both Type 1 and Type 2 PSE designs, and also supports non-standard configurations at higher power levels.

- The Classification protocol is expanded to allow Type 2 PSEs to detect Type 2 PDs, and to allow Type 2 PDs to determine if they are connected to a Type 2 PSE. Two versions of the new Classification protocol are available: an expanded version of the 802.3af Class Pulse protocol, and an alternate method integrated with the existing LLDP protocol (using the Ethernet data path). The LTC4290/LTC4271 fully supports the new Class Pulse protocol and is also compatible with the LLDP protocol (which is implemented in the data communications layer, not in the PoE circuitry).
- Fault protection current levels and timing are adjusted to reduce peak power in the MOSFET during a fault; this allows the new 25.5W power levels to be reached using the same MOSFETs as older 13W designs.

### BACKWARD COMPATIBILITY

The LTC4290/LTC4271 chipset is designed to be backward compatible with the LTC4266, operating in Type 2 mode, without software changes; only minor layout changes are required to implement a fully compliant IEEE 802.3at design.

Some LTC4266 registers have been obsoleted in the LTC4290/LTC4271 chipset. The obsoleted registers are not required for 802.3at compliant PSE operation. For more details about software differences between the LTC4266 and LTC4290/LTC4271, refer to the LTC4271 Software Programming document.

Operation with high power mode disabled is obsoleted in the LTC4290/LTC4271 chipset. All operations previously available in low power mode are fully implemented as a subset of the high power mode capabilities.

## APPLICATIONS INFORMATION

### OPERATING MODES

The LTC4290/LTC4271 includes eight independent ports, each of which can operate in one of four modes: manual, semi-auto, AUTO pin, or shutdown.

**Table 1. Operating Modes**

MODE	AUTO PIN	OPMD	DETECT/CLASS	POWER-UP	AUTOMATIC $I_{\text{CUT}}/I_{\text{LIM}}$ ASSIGNMENT
AUTO Pin	1	11b	Enabled at Reset	Automatically	Yes
Reserved	0	11b	N/A	N/A	N/A
Semi-auto	0	10b	Host Enabled	Upon Request	No
Manual	0	01b	Once Upon Request	Upon Request	No
Shutdown	0	00b	Disabled	Disabled	No

In manual mode, the port waits for instructions from the host system before taking any action. It runs a single detection or classification cycle when commanded to by the host, and reports the result in its Port Status register. The host system can command the port to turn on or off the power at any time.

In semi-auto mode, the port repeatedly attempts to detect and classify any PD attached to it. It reports the status of these attempts back to the host, and waits for a command from the host before turning on power to the port. The host must enable detection (and optionally classification) for the port before detection will start.

AUTO pin mode operates the same as semi-auto mode except it will automatically turn on the power to the port if detection is successful. AUTO pin mode will autonomously set the  $I_{\text{CUT}}$  and  $I_{\text{LIM}}$  values based on the class result. This operational mode is only valid if the AUTO pin is high at reset or power-up and remains high during operation.

In shutdown mode, the port is disabled and will not detect or power a PD.

Regardless of which mode it is in, the LTC4290/LTC4271 will remove power automatically from any port that generates a current limit fault. It will also automatically remove power from any port that generates a disconnect event if disconnect detection is enabled. The host controller may also command the port to remove power at any time.

### Reset and the AUTO/MID Pins

The initial LTC4290/LTC4271 configuration depends on the state of the AUTO and MID pins during reset. Reset occurs at power-up, or whenever the RESET pin is pulled low or the global Reset All bit is set. Changing the state of AUTO or MID after power-up will not properly change the port behavior of the LTC4290/LTC4271 until a reset occurs.

Although typically used with a host controller, the LTC4290/LTC4271 can also be used in a standalone mode with no connection to the serial interface. If there is no host present, the AUTO pin must be tied high so that, at reset, all ports will be configured to operate automatically. Each port will detect and classify repeatedly until a PD is discovered, set  $I_{\text{CUT}}$  and  $I_{\text{LIM}}$  according to the classification results, apply power to valid PDs, and remove power when a PD is disconnected.

Table 2 shows the  $I_{\text{CUT}}$  and  $I_{\text{LIM}}$  values that will be automatically set in standalone (AUTO pin) mode, based on the discovered class.

**Table 2.  $I_{\text{CUT}}$  and  $I_{\text{LIM}}$  Values in Standalone Mode**

CLASS	$I_{\text{CUT}}$	$I_{\text{LIM}}$
Class 1	112mA	425mA
Class 2	206mA	425mA
Class 3 or 0	375mA	425mA
Class 4	638mA	850mA

The automatic setting of  $I_{\text{CUT}}$  and  $I_{\text{LIM}}$  values only occurs if the LTC4290/LTC4271 is reset with the AUTO pin high.

If the standalone application is a midspan, the MID pin must be tied high to enable correct midspan detection timing.

## APPLICATIONS INFORMATION

### DETECTION

#### Detection Overview

To avoid damaging network devices that were not designed to tolerate DC voltage, a PSE must determine whether the connected device is a real PD before applying power. The IEEE specification requires that a valid PD have a common-mode resistance of  $25k \pm 5\%$  at any port voltage below 10V. The PSE must accept resistances that fall between 19k and 26.5k, and it must reject resistances above 33k or below 15k (shaded regions in Figure 11). The PSE may choose to accept or reject resistances in the undefined areas between the must-accept and must-reject ranges. In particular, the PSE must reject standard computer network ports, many of which have  $150\Omega$  common-mode termination resistors that will be damaged if power is applied to them (the black region at the left of Figure 11).

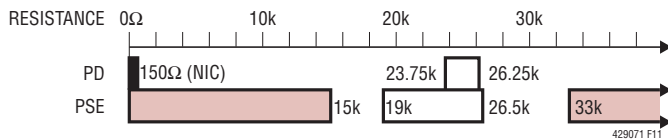


Figure 11. IEEE 802.3af Signature Resistance Ranges

#### 4-Point Detection

The LTC4290/LTC4271 uses a 4-point detection method to discover PDs. False-positive detections are minimized by checking for signature resistance with both forced-current and forced-voltage measurements.

Initially, two test currents are forced onto the port (via the OUTn pin) and the resulting voltages are measured. The detection circuitry subtracts the two V-I points to determine the resistive slope while removing offset caused by series diodes or leakage at the port (see Figure 12). If the forced-current detection yields a valid signature resistance, two test voltages are then forced onto the port and the result-

ing currents are measured and subtracted. Both methods must report valid resistances for the port to report a valid detection. PD signature resistances between 17k and 29k (typically) are detected as valid and reported as Detect Good in the corresponding Port Status register. Values outside this range, including open and short circuits, are also reported. If the port measures less than 1V at the first forced-current test, the detection cycle will abort and Short Circuit will be reported. Table 3 shows the possible detection results.

Table 3. Detection Status

MEASURED PD SIGNATURE	DETECTION RESULT
Incomplete or Not Yet Tested	Detect Status Unknown
$< 2.4k$	Short Circuit
Capacitance $> 2.7\mu F$	$C_{PD}$ too High
$2.4k < R_{PD} < 17k$	$R_{SIG}$ too Low
$17k < R_{PD} < 29k$	Detect Good
$> 29k$	$R_{SIG}$ too High
$> 50k$	Open Circuit
Voltage $> 10V$	Port Voltage Outside Detect Range

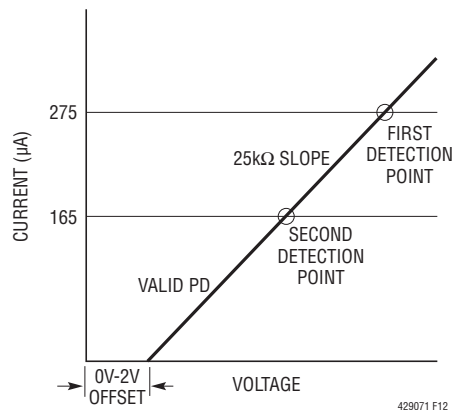


Figure 12. PD Detection

## APPLICATIONS INFORMATION

### More on Operating Modes

The port's operating mode determines when the LTC4290/LTC4271 runs a detection cycle. In manual mode, the port will idle until the host orders a detect cycle. It will then run detection, report the results, and return to idle to wait for another command.

In semi-auto mode, the LTC4290/LTC4271 autonomously polls a port for PDs, but it will not apply power until commanded to do so by the host. The Port Status register is updated at the end of each detection cycle.

If a valid signature resistance is detected and classification is enabled, the port will classify the PD and report that result as well. The port will then wait for at least 100ms (or 2 seconds if midspan mode is enabled), and will repeat the detection cycle to ensure that the data in the Port Status register is up-to-date.

If the port is in semi-auto mode and high power operation is enabled, the port will not turn on in response to a power-on command unless the current detect result is detect good. Any other detect result will generate a  $t_{\text{START}}$  fault if a power-on command is received. In high power mode the port must be placed in manual mode to force a port on regardless of detect outcome.

Behavior in AUTO pin mode is similar to semi-auto; however, after detect good is reported and the port is classified (if classification is enabled), it is automatically powered on without further intervention. In standalone (AUTO pin) mode, the  $I_{\text{CUT}}$  and  $I_{\text{LIM}}$  thresholds are automatically set; see the Reset and the AUTO/MID Pins section for more information.

The signature detection circuitry is disabled when the port is initially powered up with the AUTO pin low, in shutdown mode, or when the corresponding Detect Enable bit is cleared.

### Detection of Legacy PDs

Proprietary PDs that predate the original IEEE 802.3af standard are commonly referred to today as legacy devices. One type of legacy PD uses a large common mode capacitance ( $>10\mu\text{F}$ ) as the detection signature. Note that PDs in this range of capacitance are defined as invalid, so a PSE that detects legacy PDs is technically noncompliant with the IEEE spec. The LTC4290/LTC4271 can be configured to detect this type of legacy PD. Legacy detection is disabled by default, but can be manually enabled on a per-port basis. When enabled, the port will report Detect Good when it sees either a valid IEEE PD or a high-capacitance legacy PD. With legacy mode disabled, only valid IEEE PDs will be recognized.

## CLASSIFICATION

### 802.3af Classification

A PD may optionally present a classification signature to the PSE to indicate the maximum power it will draw while operating. The IEEE specification defines this signature as a constant current draw when the PSE port voltage is in the  $V_{\text{CLASS}}$  range (between 15.5V and 20.5V), with the current level indicating one of 5 possible PD classes. Figure 13 shows a typical PD load line, starting with the slope of the 25k signature resistor below 10V, then transitioning to the classification signature current (in this case, Class 3) in the  $V_{\text{CLASS}}$  range. Table 4 shows the possible classification values.

**Table 4. 802.3af and 802.3at Classification Values**

CLASS	RESULT
Class 0	No Class Signature Present; Treat Like Class 3
Class 1	3W
Class 2	7W
Class 3	13W
Class 4	25.5W (Type 2)

## APPLICATIONS INFORMATION

If classification is enabled, the port will classify the PD immediately after a successful detection cycle in semi-auto or AUTO pin modes, or when commanded to in manual mode. It measures the PD classification signature by applying 18V for 12ms (both values typical) to the port via the OUTn pin and measuring the resulting current; it then reports the discovered class in the Port Status register. If the LTC4290/LTC4271 is in AUTO pin mode, it will additionally use the classification result to set the  $I_{CUT}$  and  $I_{LIM}$  thresholds. See the Reset and the AUTO/MID Pin section for more information.

The classification circuitry is disabled when the port is initially powered up with the AUTO pin low, in shutdown mode, or when the corresponding Class Enable bit is cleared.

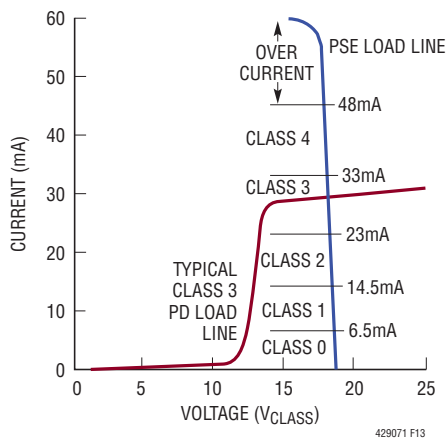


Figure 13. PD Classification

### 802.3at 2-Event Classification

The 802.3at specification defines two methods of classifying a Type 2 PD. LTC4290/LTC4271 parts support 802.3at 2-event classification.

One method adds extra fields to the Ethernet LLDP data protocol; although the LTC4290/LTC4271 is compatible with this classification method, it cannot perform classification directly since it doesn't have access to the data

path. LLDP classification requires the PSE to power the PD as a standard 802.3af (Type 1) device. It then waits for the host to perform LLDP communication with the PD and update the PSE port data. The LTC4290/LTC4271 supports changing the  $I_{LIM}$  and  $I_{CUT}$  levels on the fly, allowing the host to complete LLDP classification.

The second 802.3at classification method, known as 2-event classification or ping-pong, is supported by the LTC4290/LTC4271. A Type 2 PD that is requesting more than 13W will indicate Class 4 during normal 802.3af classification. If the LTC4290/LTC4271 sees Class 4, it forces the port to a specified lower voltage (called the mark voltage, typically 9V), pauses briefly, and then re-runs classification to verify the Class 4 reading (Figure 1). It also sets a bit in the High Power Status register to indicate that it ran the second classification cycle. The second cycle alerts the PD that it is connected to a Type 2 PSE which can supply Type 2 power levels.

2-event ping-pong classification is enabled by setting a bit in the port's High Power Mode register. Note that a ping-pong enabled port only runs the second classification cycle when it detects a Class 4 device; if the first cycle returns Class 0 to 3, the port determines it is connected to a Type 1 PD and does not run the second classification cycle.

### Invalid Type 2 Class Combinations

The 802.3at specification defines a Type 2 PD class signature as two consecutive Class 4 results; a Class 4 followed by a Class 0-3 is not a valid signature. In AUTO pin mode, the LTC4290/LTC4271 will power a detected PD regardless of the classification results, with one exception: if the PD presents an invalid Type 2 signature (Class 4 followed by Class 0 to 3), the LTC4290/LTC4271 will not provide power and will restart the detection process. To aid in diagnosis, the Port Status register will always report the results of the last class pulse, so an invalid Class 4–Class 2 combination would report a second class pulse was run in the High Power Status register (which implies that the first cycle found class 4), and Class 2 in the Port Status register.

## APPLICATIONS INFORMATION

### POWER CONTROL

The primary function of the LTC4290/LTC4271 is to control the delivery of power to the PSE port. It does this by controlling the gate drive voltage of an external power MOSFET while monitoring the current via an external sense resistor and the output voltage at the OUT pin. This circuitry serves to couple the raw  $V_{EE}$  input supply to the port in a controlled manner that satisfies the PDs power needs while minimizing both power dissipation in the MOSFET and disturbances on the  $V_{EE}$  backplane.

### Inrush Control

Once the command has been given to turn on a port, the LTC4290/LTC4271 ramps up the GATE pin of that port's external MOSFET in a controlled manner. Under normal power-up circumstances, the MOSFET gate will rise until the port current reaches the inrush current limit level (typically 425mA), at which point the GATE pin will be servoed to maintain the specified  $I_{INRUSH}$  current. During this inrush period, a timer ( $t_{START}$ ) runs. When output charging is complete, the port current will fall and the GATE pin will be allowed to continue rising to fully enhance the MOSFET and minimize its on-resistance. The final  $V_{GS}$  is nominally 12V. The inrush period is maintained until the  $t_{START}$  timer expires. At this time if the inrush current limit level is still exceeded, the port will be turned back off and a  $t_{START}$  fault reported.

### Current Limit

Each LTC4290/LTC4271 port includes two current limiting thresholds ( $I_{CUT}$  and  $I_{LIM}$ ), each with a corresponding timer ( $t_{CUT}$  and  $t_{LIM}$ ). Setting the  $I_{CUT}$  and  $I_{LIM}$  thresholds depends on several factors: the class of the PD, the voltage of the main supply ( $V_{EE}$ ), the type of PSE (Type 1 or Type 2), the sense resistor (0.5 $\Omega$  or 0.25 $\Omega$ ), the SOA of the MOSFET, and whether or not the system is required to enforce class current levels.

Per the IEEE specification, the LTC4290/LTC4271 will allow the port current to exceed  $I_{CUT}$  for a limited period of time before removing power from the port, whereas it will actively control the MOSFET gate drive to keep the port current below  $I_{LIM}$ . The port does not take any action to limit the current when only the  $I_{CUT}$  threshold is exceeded, but does start the  $t_{CUT}$  timer. If the current drops below the  $I_{CUT}$  current threshold before its timer expires, the  $t_{CUT}$  timer counts back down, but at 1/16 the rate that it counts up. If the  $t_{CUT}$  timer reaches 60ms (typical) the port is turned off and the port  $t_{CUT}$  fault is set. This allows the current limit circuitry to tolerate intermittent overload signals with duty cycles below about 6%; longer duty cycle overloads will turn the port off.

The  $I_{LIM}$  current limiting circuit is always enabled and actively limiting port current. The  $t_{LIM}$  timer is enabled only when the  $t_{LIM}$  Enable bit is set. This allows  $t_{LIM}$  to be set to a shorter value than  $t_{CUT}$  to provide more aggressive MOSFET protection and turn off a port before MOSFET damage can occur. The  $t_{LIM}$  timer starts when the  $I_{LIM}$  threshold is exceeded. When the  $t_{LIM}$  timer reaches 12ms (typical) the port is turned off and the port  $t_{LIM}$  fault is set. When the  $t_{LIM}$  Enable bit is disabled  $t_{LIM}$  behaviors are tracked by the  $t_{CUT}$  timer, which counts up during both  $I_{LIM}$  and  $I_{CUT}$  events.

$I_{CUT}$  is typically set to a lower value than  $I_{LIM}$  to allow the port to tolerate minor faults without current limiting.

Per the IEEE specification, the LTC4290/LTC4271 will automatically set  $I_{LIM}$  to 425mA (shown in bold in Table 5) during inrush at port turn-on, and then switch to the programmed  $I_{LIM}$  setting once inrush has completed. To maintain IEEE compliance,  $I_{LIM}$  should be kept at 425mA for all Type 1 PDs, and 850mA if a Type 2 PD is detected.  $I_{LIM}$  is automatically reset to 425mA when a port turns off.

## APPLICATIONS INFORMATION

**Table 5. Example Current Limit Settings**

I <sub>LIM</sub> (mA)	INTERNAL REGISTER SETTING (hex)	
	R <sub>SENSE</sub> = 0.5Ω	R <sub>SENSE</sub> = 0.25Ω
53	88	
106	08	88
159	89	
213	80	08
266	8A	
319	09	89
372	8B	
<b>425</b>	<b>00</b>	<b>80</b>
478	8E	
531	92	8A
584	CB	
638	10	90
744	D2	9A
<b>850</b>	<b>40</b>	<b>C0</b>
956	4A	CA
1063	50	D0
1169	5A	DA
1275	60	E0
1488	52	49
1700		40
1913		4A
2125		50
2338		5A
2550		60
2975		52

### I<sub>LIM</sub> Foldback

The LTC4290/LTC4271 features a two-stage foldback circuit that reduces the port current if the port voltage falls below the normal operating voltage. This keeps MOSFET power dissipation at safe levels for typical 802.3af MOSFETs, even at extended 802.3at power levels. Current limit and foldback behavior are programmable on a per-port basis.

Table 5 gives examples of recommended I<sub>LIM</sub> register settings.

The LTC4290/LTC4271 will support current levels well beyond the maximum values in the 802.3at specification.

The shaded areas in Table 5 indicate settings that may require a larger external MOSFET, additional heat sinking, or setting t<sub>LIM</sub> Enable.

### MOSFET Fault Detection

LTC4290/LTC4271 PSE ports are designed to tolerate significant levels of abuse, but in extreme cases it is possible for the external MOSFET to be damaged. A failed MOSFET may short source to drain, which will make the port appear to be on when it should be off; this condition may also cause the sense resistor to fuse open, turning off the port but causing the LTC4290 SENSE pin to rise to an abnormally high voltage. A failed MOSFET may also short from gate to drain, causing the LTC4290 GATE pin to rise to an abnormally high voltage. The LTC4290 OUT, SENSE and GATE pins are designed to tolerate up to 80V faults without damage.

If the LTC4290/LTC4271 sees any of these conditions for more than 180μs, it disables all port functionality, reduces the gate drive pull-down current for the port and reports a FET Bad fault. This is typically a permanent fault, but the host can attempt to recover by resetting the port, or by resetting the entire chip if a port reset fails to clear the fault. If the MOSFET is in fact bad, the fault will quickly return, and the port will disable itself again. The remaining ports of the LTC4290/LTC4271 are unaffected.

An open or missing MOSFET will not trigger a FET Bad fault, but will cause a t<sub>START</sub> fault if the LTC4290/LTC4271 attempts to turn on the port.

### Port Current Readback

The LTC4290/LTC4271 measures the current at each port with an internal A/D converter. Port data is only valid when the port power is on and reads zero at all other times. The converter has two modes:

- 100ms mode: Samples are taken continuously and the measured value is updated every 100ms
- 1s mode: Samples are taken continuously; a moving 1 second average is updated every 100ms

## APPLICATIONS INFORMATION

### Port Current Policing

The LTC4290/LTC4271 can augment  $t_{CUT}$  current monitoring with a policing function to track the one second current averages. A port violating the user-specified Port Police Threshold will be shut off with both a  $t_{CUT}$  and Police event recorded. A port current Police event can be differentiated from a port  $t_{CUT}$  violation by reading both events bits; both bits are set for a Police violation while only the  $t_{CUT}$  bit is set for  $t_{CUT}$  timer violations.

### Port Voltage Readback

The LTC4290/LTC4271 measures the output voltage at each port with an internal A/D converter. Port data is only valid when the port power is on and reads zero at all other times.

### Disconnect

The LTC4290/LTC4271 monitors powered ports to ensure the PD continues to draw the minimum specified current. A disconnect timer counts up whenever port current is below 7.5mA (typ), indicating that the PD has been disconnected. If the  $t_{DIS}$  timer expires, the port will be turned off and the disconnect bit in the fault event register will be set. If the current returns before the  $t_{DIS}$  timer runs out, the timer resets. As long as the PD exceeds the minimum current level more often than  $t_{DIS}$ , it will remain powered.

Although not recommended, the DC disconnect feature can be disabled by clearing the corresponding enable bits. Note that this defeats the protection mechanisms built into the IEEE specification, since a powered port will stay powered after the PD is removed. If the still-powered port is subsequently connected to a non-PoE data device, the device may be damaged.

The LTC4290/LTC4271 does not include AC disconnect circuitry, but includes AC Disconnect Enable bits to maintain compatibility with the LTC4259A. If the AC Disconnect Enable bits are set, DC disconnect will be used.

### Masked Shutdown

The LTC4290/LTC4271 provides a low latency port shedding feature to quickly reduce the system load when required. By allowing a pre-determined set of ports to be turned off, the current on an overloaded main power supply can be reduced rapidly while keeping high priority devices powered. Each port can be configured to high or low priority; all low-priority ports will shut down within 6.5 $\mu$ s after the  $\overline{MSD}$  pin is pulled low, high priority ports will remain powered. If a port is turned off via  $\overline{MSD}$ , the corresponding Detection and Classification Enable bits are cleared, so the port will remain off until the host explicitly re-enables detection.

In the LTC4290/LTC4271 chipset the active level of  $\overline{MSD}$  is register configurable as active high or low. The default is LTC4266-compatible active low behavior.

### $V_{EE}$ Readback

The LTC4290/LTC4271 measures the  $V_{EE}$  voltage with an internal 12-bit A/D converter.

### General Purpose IO

Two sets of general purpose IO pins are available in the LTC4290/LTC4271 chipset. The first set of general purpose IO are GP1 and GP0. These fully bidirectional IO are 3.3V CMOS IO on the LTC4271 chip.

The second set of general purpose IO pins are XIO1 and XIO0. These fully bidirectional IO are 4.3V CMOS IO on the LTC4290 chip.

### Code Download

LTC4271 firmware is field-upgradable by downloading and executing RAM images. RAM images are volatile and must be re-downloaded after each  $V_{DD}$  power cycle, but will remain valid during reset and  $V_{EE}$  power events. Contact Linear Technology for code download procedures and RAM images.



## APPLICATIONS INFORMATION

### SERIAL DIGITAL INTERFACE

#### Overview

The LTC4290/LTC4271 communicates with the host using a standard SMBus/I<sup>2</sup>C 2-wire interface. The LTC4290/LTC4271 is a slave-only device, and communicates with the host master using the standard SMBus protocols. Interrupts are signaled to the host via the  $\overline{\text{INT}}$  pin. The Timing Diagrams (Figures 5 through 9) show typical communication waveforms and their timing relationships. More information about the SMBus data protocols can be found at [www.smbus.org](http://www.smbus.org).

The LTC4290/LTC4271 requires both the  $V_{\text{DD}}$  and  $V_{\text{EE}}$  supply rails to be present for the serial interface to function.

#### Bus Addressing

The LTC4290/LTC4271's primary 7-bit serial bus address is  $A_610A_3A_2A_1A_0b$ , with bit 6 controlled by AD6 and the lower four bits set by the AD3-AD0 pins; this allows up to 16 LTC4290/LTC4271s, on a single bus. Sixteen LTC4290/LTC4271 are equivalent to 32 quad PSEs or 128 ports. All LTC4290/LTC4271s also respond to the broadcast address 0110000b, allowing the host to write the same command (typically configuration commands) to multiple LTC4290/LTC4271s in a single transaction. If the LTC4290/LTC4271 is asserting the  $\overline{\text{INT}}$  pin, it will also respond to the alert response address (0001100b) per the SMBus specification.

Each LTC4290/LTC4271 is logically composed of two quads of four ports each. Each quad occupies separate, contiguous I<sup>2</sup>C addresses. The AD6, AD3-0 pins set the address of the base quad while the second quad is consecutively numbered. I<sup>2</sup>C addresses outside of the  $x10xxxxb$  range are considered illegal and will not respond. Each internal quad is independent of the other quad, with the exception of writes to the Chip Reset,  $\overline{\text{MSD}}$  Inversion and General Purpose Input Output registers. These registers are global in nature and will affect all quads.

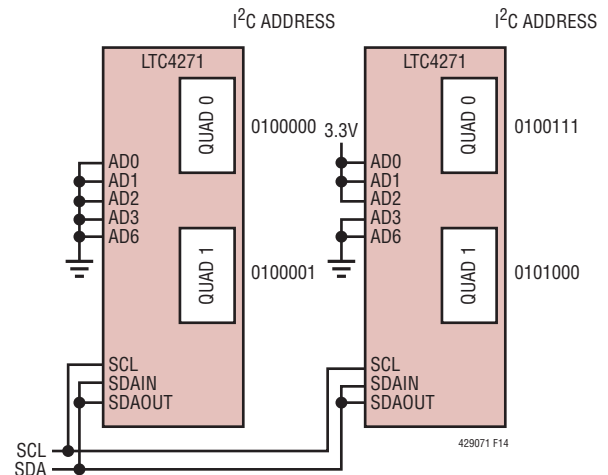


Figure 14. Example I<sup>2</sup>C Bus Addressing

#### Interrupts and SMBAlert

Most LTC4290/LTC4271 port events can be configured to trigger an interrupt, asserting the  $\overline{\text{INT}}$  pin and alerting the host to the event. This removes the need for the host to poll the LTC4290/LTC4271, minimizing serial bus traffic and conserving host CPU cycles. Multiple LTC4290/LTC4271s can share a common  $\overline{\text{INT}}$  line, with the host using the SMBAlert protocol (ARA) to determine which LTC4290/LTC4271 caused an interrupt.

#### Register Description

For information on serial bus usage and device configuration and status, refer to the LTC4271 Software Programming documentation.

#### ISOLATION REQUIREMENTS

IEEE 802.3 Ethernet specifications require that network segments (including PoE circuitry) be electrically isolated from the chassis ground of each network interface device. However, network segments are not required to be isolated from each other, provided that the segments are connected to devices residing within a single building on a single power distribution system.

## APPLICATIONS INFORMATION

For simple devices such as small PoE switches, the isolation requirement can be met by using an isolated main power supply for the entire device. This strategy can be used if the device has no electrically conducting ports other than twisted-pair Ethernet. In this case, the SDAIN and SDAOUT pins can be tied together and will act as a standard I<sup>2</sup>C/SMBus SDA pin.

If the device is part of a larger system, contains additional external non-Ethernet ports, or must be referenced to protective ground for some other reason, the Power over Ethernet subsystem must be electrically isolated from the rest of the system.

The LTC4290/LTC4271 chipset simplifies PSE isolation by allowing the LTC4271 chip to reside on the non-isolated side. There it can receive power from the main logic supply and connect directly to the I<sup>2</sup>C/SMBus bus. Isolation between the LTC4271 and LTC4290 is implemented using a proprietary transformer-based communication protocol. Additional details are provided in the Serial Bus Isolation section of this data sheet.

### EXTERNAL COMPONENT SELECTION

#### Power Supplies and Bypassing

The LTC4290/LTC4271 requires two supply voltages to operate.  $V_{DD}$  requires 3.3V (nominally) relative to DGND.  $V_{EE}$  requires a negative voltage of between -45V and -57V for Type 1 PSEs or -51V to -57V for Type 2 PSEs, relative to AGND.

#### Digital Power Supply

$V_{DD}$  provides digital power for the LTC4271 processor, and draws a maximum of 15mA. A ceramic decoupling cap of at least 0.1 $\mu$ F should be placed from  $V_{DD}$  to DGND, as close as practical to each LTC4271 chip. A 1.8V core voltage supply is generated internally and requires a 1 $\mu$ F ceramic decoupling cap between the CAP1 pin and DGND.

In the LTC4290/LTC4271,  $V_{DD}$  should be delivered by the host controller's non-isolated 3.3V supply. To maintain required isolation AGND and DGND must not be connected in any way.

#### Main PoE Power Supply

$V_{EE}$  is the main isolated PoE supply that provides power to the PDs. Because it supplies a relatively large amount of power and is subject to significant current transients, it requires more design care than a simple logic supply. For minimum IR loss and best system efficiency, set  $V_{EE}$  near maximum amplitude (57V), leaving enough margin to account for transient over or undershoot, temperature drift, and the line regulation specifications of the particular power supply used.

Bypass capacitance between AGND and  $V_{EE}$  is very important for reliable operation. If a short circuit occurs at one of the output ports it can take as long as 1 $\mu$ s for the LTC4290 to begin regulating the current. During this time the current is limited only by the small impedances in the circuit and a high current spike typically occurs, causing a voltage transient on the  $V_{EE}$  supply and possibly causing the LTC4290/LTC4271 to reset due to a UVLO fault. A 1 $\mu$ F, 100V X7R capacitor placed near the  $V_{EE}$  pin along with an electrolytic bulk capacitor of at least 47 $\mu$ F is recommended to minimize spurious resets.

#### Serial Bus Isolation

The LTC4290/LTC4271 chipset uses transformers to isolate the LTC4271 from the LTC4290. In this case, the SDAIN and SDAOUT pins can be shorted to each other and tied directly to the I<sup>2</sup>C/SMBus bus. The transformers should be 10BASE-T or 10/100BASE-T with a 1:1 turns ratio. It is important that the selected transformers do not have common-mode chokes. These transformers typically provide 1500V of isolation between the LTC4271 and the LTC4290. For proper operation strict layout guidelines must be met.

## APPLICATIONS INFORMATION

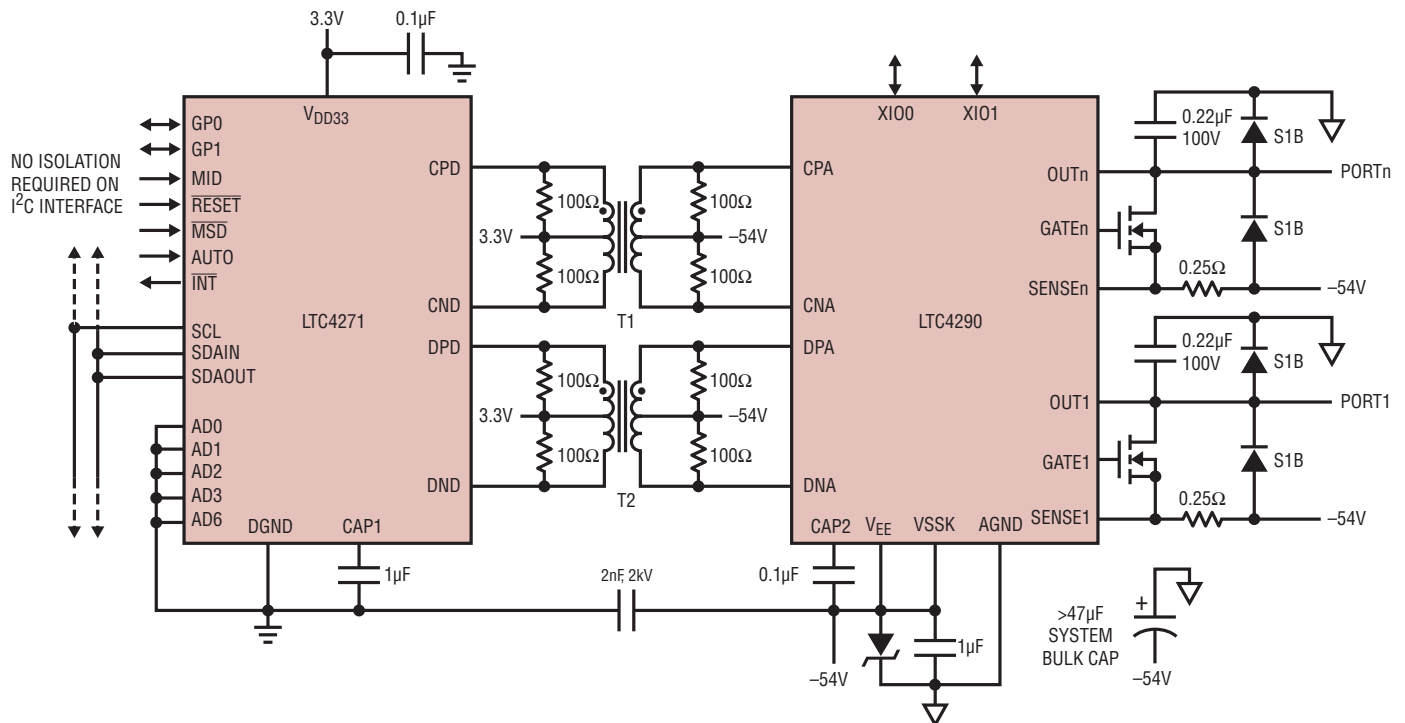


Figure 15. LTC4290/LTC4271 Proprietary Isolation

## External MOSFET

Careful selection of the power MOSFET is critical to system reliability. LTC recommends either Fairchild IRFM120A, FDT3612, FDMC3612 or Philips PHT6NQ10T for their proven reliability in Type 1 and Type 2 PSE applications. SOA curves are not a reliable specification for MOSFET selection. Contact LTC Applications before using a MOSFET other than one of these recommended parts.

## Sense Resistor

The LTC4290/LTC4271 is designed to use 0.25Ω current sense resistors to reduce power dissipation. Four commonly available 1Ω resistors (sized according to power dissipation) can be used in parallel in place of a single

0.25Ω resistor. In order to meet the  $I_{CUT}$  and  $I_{LIM}$  accuracy required by the IEEE specification, the sense resistors should have  $\pm 1\%$  tolerance or better, and no more than  $\pm 200\text{ppm}/^\circ\text{C}$  temperature coefficient. In addition, the sense resistors must meet strict layout guidelines.

## Port Output Cap

Each port requires a 0.22µF cap across its outputs to keep the LTC4290 stable while in current limit during startup or overload. Common ceramic capacitors often have significant voltage coefficients; this means the capacitance is reduced as the applied voltage increases. To minimize this problem, X7R ceramic capacitors rated for at least 100V are recommended and must be located close to the PSE.

## APPLICATIONS INFORMATION

### ESD/Cable Discharge Protection

Ethernet ports can be subject to significant ESD events when long data cables, each potentially charged to thousands of volts, are plugged into the low impedance of the RJ45 jack. To protect against damage, each port requires a pair of clamp diodes; one to AGND and one to  $V_{EE}$  (Figure 16). An additional surge suppressor is required for each LTC4290 chip from  $V_{EE}$  to AGND. The diodes at the ports steer harmful surges into the supply rails, where they are absorbed by the surge suppressor and the  $V_{EE}$  bypass capacitance. The surge suppressor has the additional benefit of protecting the LTC4290 from transients on the  $V_{EE}$  supply.

S1B diodes work well as port clamp diodes, and an SMAJ58A or equivalent is recommended for the  $V_{EE}$  surge suppressor.

### LAYOUT GUIDELINES

Strict adherence to board layout, parts placement and routing guidelines is critical for optimal current reading accuracy, IEEE compliance, system robustness, and thermal dissipation. Refer to the DC1842A Demo Board as a layout reference. Contact LTC Applications to obtain a full set of layout guidelines, example layouts and BOMs.

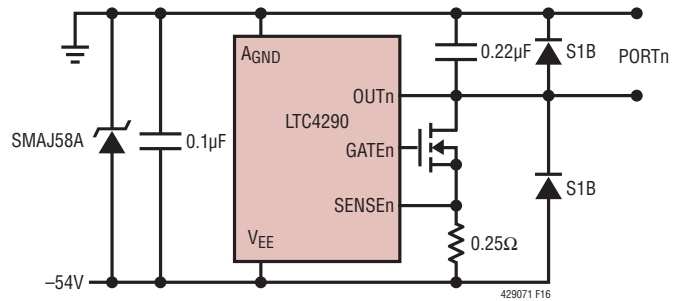
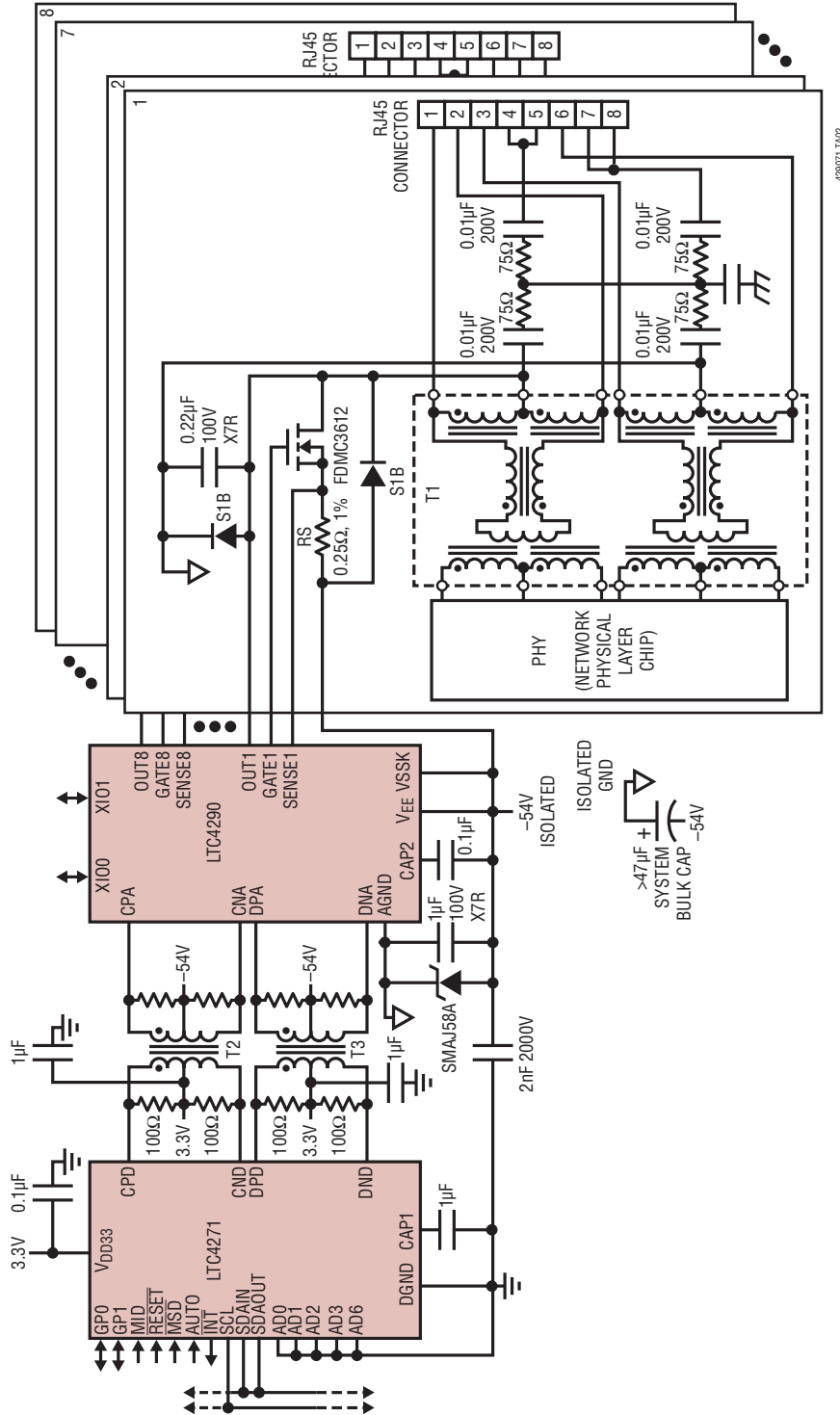


Figure 16. LTC4290 Discharge Protection

TYPICAL APPLICATION

Complete 8-Port PSE



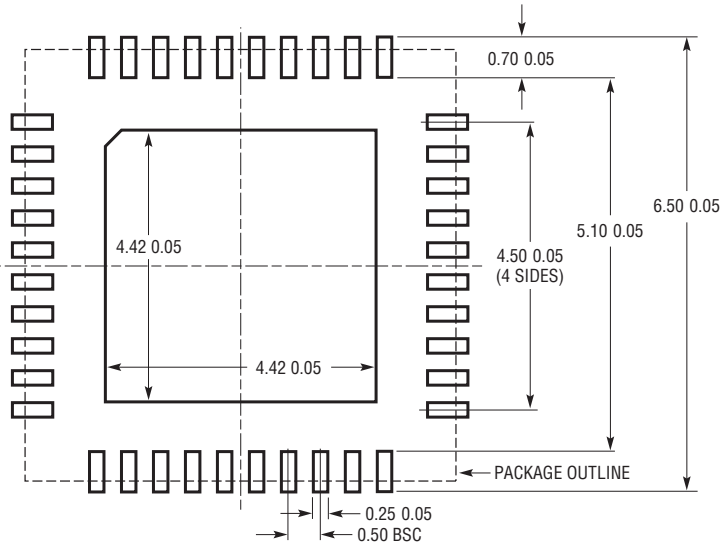
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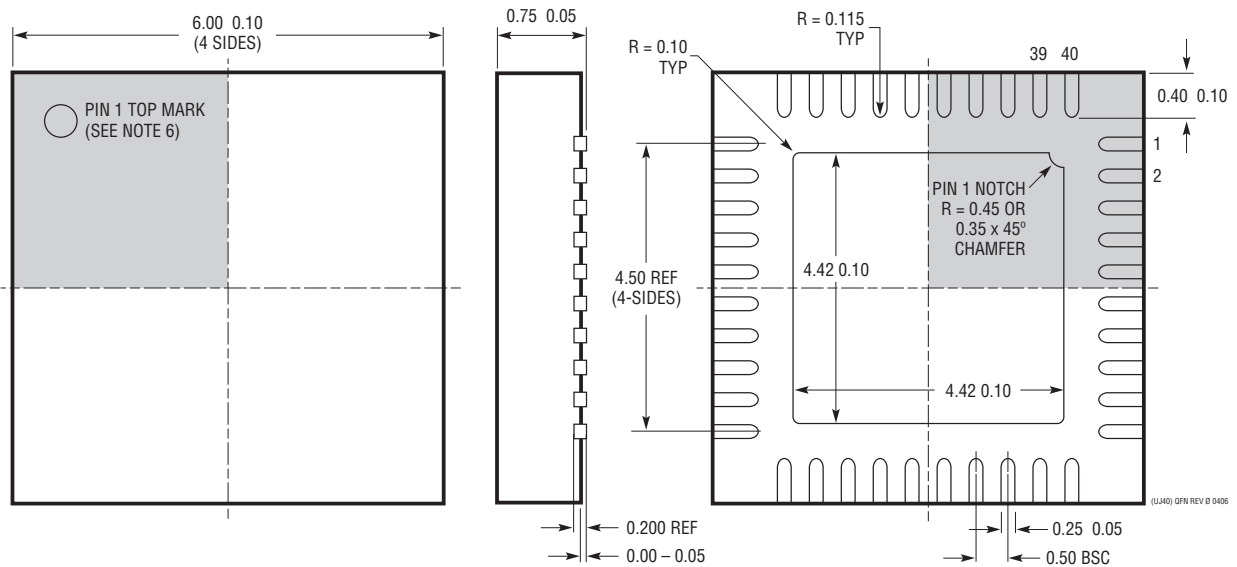
# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

**UJ Package**  
**40-Lead Plastic QFN (6mm × 6mm)**  
 (Reference LTC DWG # 05-08-1728 Rev 0)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS  
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

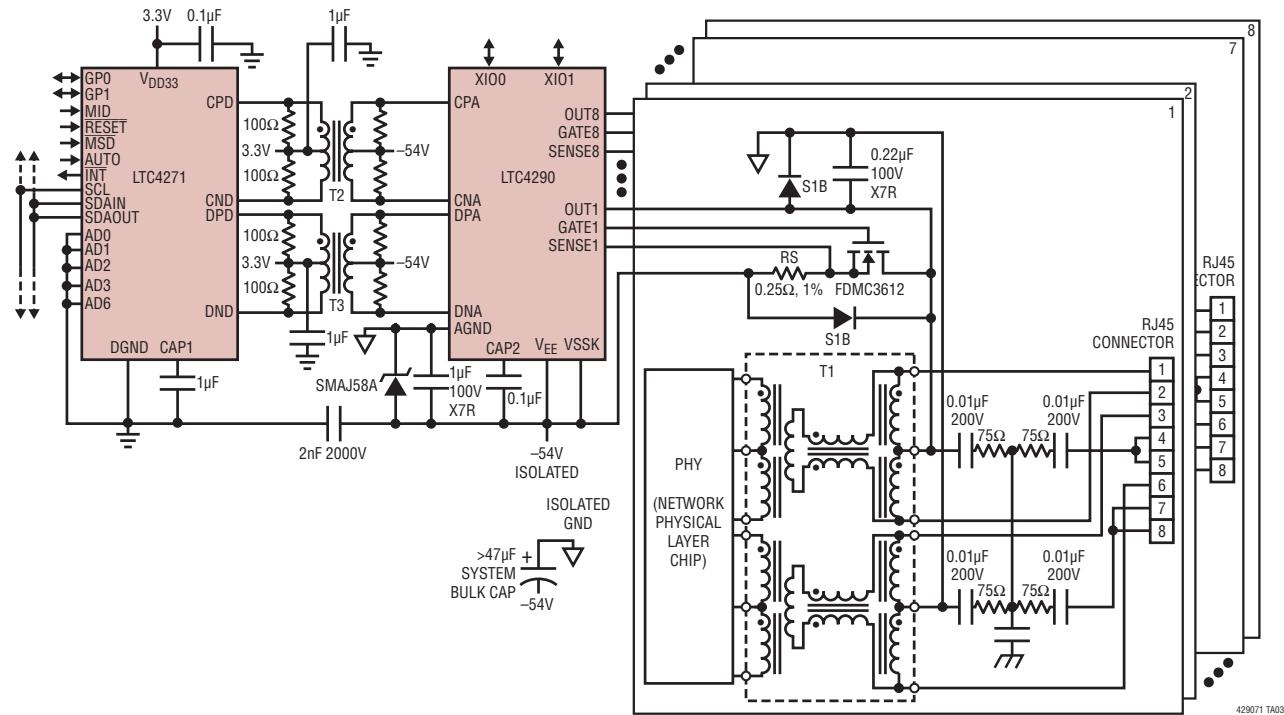


- NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS
  4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
  5. EXPOSED PAD SHALL BE SOLDER PLATED
  6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

BOTTOM VIEW—EXPOSED PAD

## TYPICAL APPLICATION

Complete 8-Port PSE



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4257-1	IEEE 802.3af PD Interface Controller	Internal 100V, 400mA Switch, Dual Current Limit, Programmable Class
LTC4263	Single IEEE 802.3af PSE Controller	Internal FET Switch
LTC4263-1	High Power Single PoE PSE Controller	With Internal FET Switch
LTC4265	IEEE 802.3at PD Interface Controller	Internal 100V, 1A Switch, 2-Event Classification Recognition
LTC4266	Quad IEEE 802.3at PoE PSE Controller	With Programmable $I_{CUT}/I_{LIM}$ , 2-Event Classification, and Port Current and Voltage Monitoring
LTC4267	IEEE 802.3af PD Interface With Integrated Switching Regulator	Internal 100V, 400mA Switch, Dual Inrush Current, Programmable Class
LTC4267-1	IEEE 802.3af PD Interface With Integrated Switching Regulator	Internal 100V, 400mA Switch, Programmable Class, 200kHz Constant Frequency PWM
LTC4267-3	IEEE 802.3af PD Interface With Integrated Switching Regulator	Internal 100V, 400mA Switch, Programmable Class, 300kHz Constant Frequency PWM
LTC4269-1	IEEE 802.3af PD Interface With Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, Aux Support
LTC4269-2	IEEE 802.3af PD Interface With Integrated Forward Switching Regulator	2-Event Classification, Programmable Class, Synchronous Forward Controller, 100kHz to 500kHz, Aux Support
LTC4270/ LTC4271	12-Port PoE/PoE+/LTPoE++™ PSE Controller	Transformer Isolation, Supports Type 1, Type 2 and LTPoE++ PDs
LTC4274	Single IEEE 802.3at PoE PSE Controller	With Programmable $I_{CUT}/I_{LIM}$ , 2-Event Classification, and Port Current and Voltage Monitoring
LTC4278	IEEE 802.3af PD Interface With Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, 12V Aux Support
LTC4311	SMBus/ I <sup>2</sup> C Accelerator	Improved I <sup>2</sup> C Rise Time, Ensures Data Integrity

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