MF0UN(H)00

MIFARE Ultralight Nano

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1. General description

NXP Semiconductors developed the MIFARE Ultralight Nano MF0UN(H)00 for use in a contactless smart ticket, smart card or token in combination with a Proximity Coupling Device (PCD). The MF0UN(H)00 is designed to work in an ISO/IEC 14443 Type A compliant environment (see Ref. 1). The target applications include single trip or limited use tickets in public transportation networks, loyalty cards or day passes for events. The MF0UN(H)00 serves as a replacement for conventional ticketing solutions such as paper tickets, magnetic stripe tickets or coins. It is also a perfect ticketing counterpart to contactless card families such as MIFARE DESFire or MIFARE Plus.

The MIFARE Ultralight Nano is succeeding the MIFARE Ultralight ticketing IC and is fully functional backwards compatible. Its enhanced feature and command set enable more efficient implementations and offer more flexibility in system designs.

The mechanical and electrical specifications of MIFARE Ultralight Nano are tailored to meet the requirements of inlay and paper ticket manufacturers.

### 1.1 Contactless energy and data transfer

In a contactless system, the MF0UN(H)00 is connected to a coil with a few turns. The MF0UN(H)00 fits the TFC.0 (Edmondson) and TFC.1 (ISO) ticket formats as defined in Ref. 7.

The MF0UN(H)00 chip, which is available with 17 pF or 50 pF on-chip resonance capacitor, supports both TFC.1 and TFC.0 ticket formats.

1.2 Anticollision

An intelligent anticollision function allows more than one card to operate in the field simultaneously. The anticollision algorithm selects each card individually. It ensures that the execution of a transaction with a selected card is performed correctly without interference from another card in the field.

Fig 1.   Contactless system
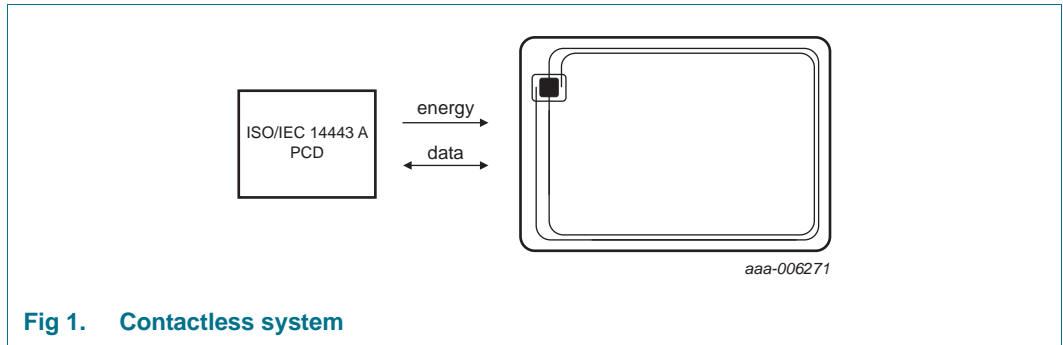
1.3   Simple integration and user convenience

The MF0UN(H)00 is designed for simple integration and user convenience which allows complete ticketing transactions to be handled in less than 35 ms.

1.4   Security

- Manufacturer programmed 7-byte UID for each device
- 32-bit user definable One-Time Programmable (OTP) area
- Field programmable read-only locking function per page
- Pre-programmed ECC-based originality signature, offering the possibility for customizing and permanent locking

1.5   Naming conventions

Table 1.   Naming conventions

MF0UN(H)x001Dyy	Description
MF	MIFARE product family
0	Ultralight product family
UN	Product: MIFARE Ultralight Nano
H	If present, defining high input capacitance H... 50 pF input capacitance
x	One character identifier defining the memory size 0... 448 bit total memory, 320 bit free user memory
Dyy	yy defining the delivery type UF... bare die, 75 μm thickness, Au bumps, e-map file UD... bare die, 120 μm thickness, Au bumps, e-map file

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2. Features and benefits

- Contactless transmission of data and supply energy

- Operating frequency of 13.56 MHz
- Data integrity of 16-bit CRC, parity, bit coding, bit counting
- 7 byte serial number (cascade level 2 according to ISO/IEC 14443-3)
- Originality signature

- Operating distance up to 100 mm depending on antenna geometry and reader configuration
- Data transfer of 106 kbit/s
- True anticollision

- Typical ticketing transaction: < 35 ms

2.1 EEPROM

- 448-bit, organized in 14 pages with 4 bytes per page
- 320-bit freely available user Read/Write area (10 pages)
- 32-bit user definable One-Time Programmable (OTP) area
- Pre-programmed ECC-based originality signature
- Data retention time of 10 years

- Backwards compatible to MF0ICU1 within the available memory
- Field programmable read-only locking function per page
- Anti-tearing support for OTP area and lock bits
- Possibility for customizing and permanently locking the ECC signature
- Write endurance 100.000 cycles

3. Applications

- Public transportation - Single trip ticketing

- Event ticketing

4. Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance MF0UN00	[1]	-	17.0	-	pF
C_i	input capacitance MF0UNH00	[1]	-	50.0	-	pF
f_i	input frequency		-	13.56	-	MHz
EEPROM characteristics						
t_{ret}	retention time	T_{amb} = 22 °C	10	-	-	year
$N_{endu(W)}$	write endurance	T_{amb} = 22 °C	100000	-	-	cycle

[1] T_{amb} = 22 °C, f = 13.56 MHz, V_{LaLb} = 1.5 V RMS

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5. Ordering information

Table 3.   Ordering information

| Type number	Package			
	Name	**Description**		**Version**
MF0UN0001DUF	FFC Bump	8 inch wafer, 75 μm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 320 bit user memory, 17 pF input capacitance		-
MF0UN0001DUD	FFC Bump	8 inch wafer, 120 μm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 320 bit user memory, 17 pF input capacitance		-
MF0UNH0001DUF	FFC Bump	8 inch wafer, 75 μm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 320 bit user memory, 50 pF input capacitance		-
MF0UNH0001DUD	FFC Bump	8 inch wafer, 120 μm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 320 bit user memory, 50 pF input capacitance		-

6. Block diagram

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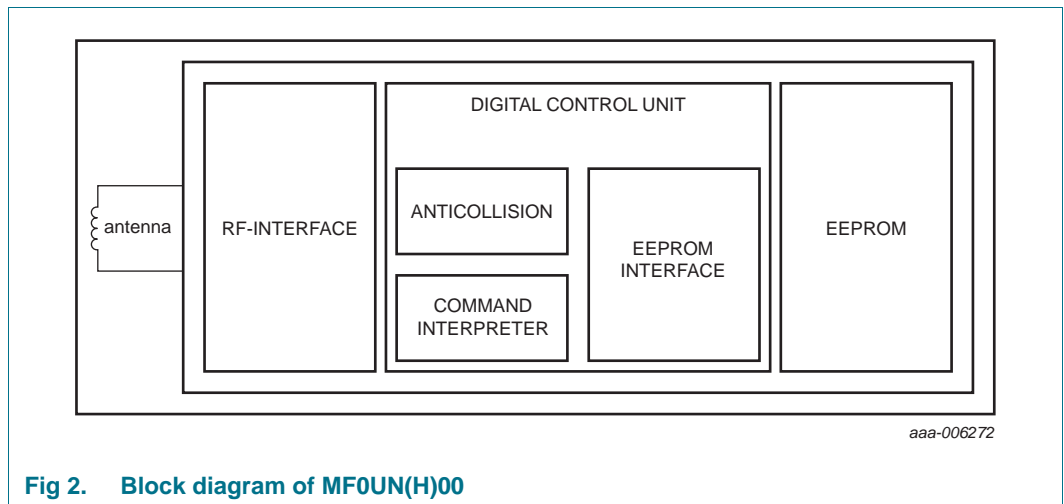
Fig 2.   Block diagram of MF0UN(H)00

7. Pinning information

7.1 Pinning
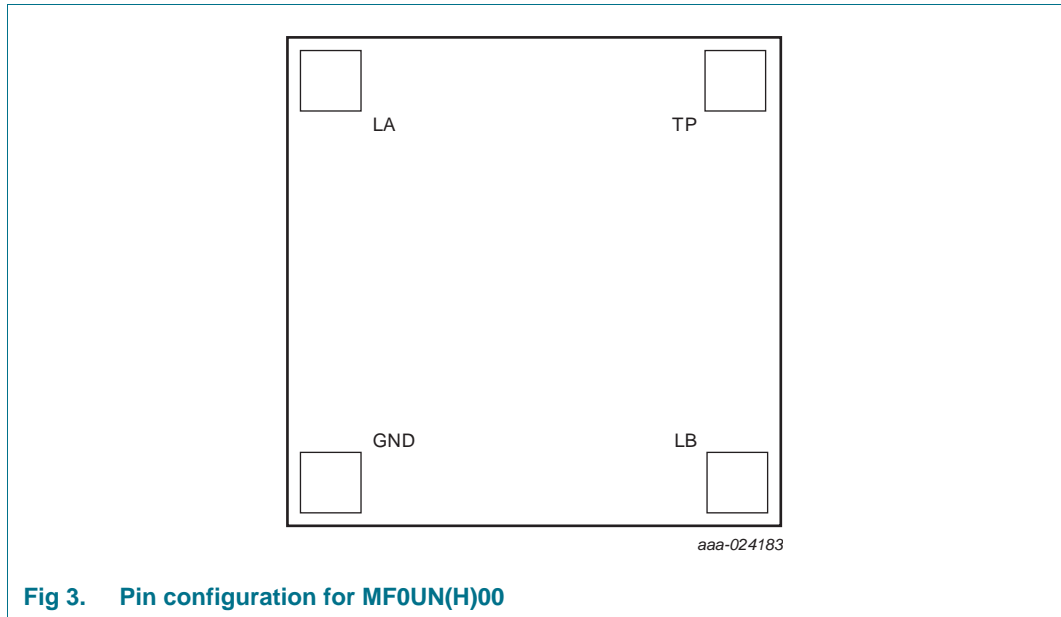
The pinning for the MF0UN(H)00DAx is shown Figure 3.

aaa-024183

Fig 3.   Pin configuration for MF0UN(H)00

Table 4.   Pin allocation table

Pin	Symbol	
LA	LA	antenna coil connection LA
LB	LB	antenna coil connection LB
TP	TP	test pad, unconnected at delivery
GND	GND	ground pad, unconnected at delivery

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8. Functional description

8.1 Block description

The MF0UN(H)00 chip consists of a 448-bit EEPROM, RF interface and Digital Control Unit (DCU). Energy and data are transferred via an antenna consisting of a coil with a few turns which is directly connected to the MF0UN(H)00. No further external components are necessary. Refer to Ref. 2 for details on antenna design.

- RF interface:
  - modulator/demodulator
  - rectifier
  - clock regenerator
  - Power-On Reset (POR)
  - voltage regulator
- Anticollision: multiple cards may be selected and managed in sequence
- Command interpreter: processes memory access commands that the MF0ICU1 supports
- EEPROM interface
- EEPROM: 448 bit, organized in 14 pages of 4 byte per page.
  - 80 bit reserved for manufacturer and configuration data
  - 16 bit used for the read-only locking mechanism
  - 32 bit available as OTP area
  - 320 bit user programmable read/write memory

8.2 RF interface

The RF-interface is based on the ISO/IEC 14443 Type A standard for contactless smart cards.

During operation, the reader generates an RF field. This RF field must always be present (with short pauses for data communication), as it is used for both communication and as power supply of the card.

For both directions of data communication, there is one start bit at the beginning of each frame. Each byte is transmitted with an odd parity bit at the end. The LSB of the byte with the lowest address of the selected block is transmitted first. The maximum length of a PCD to PICC frame is 163 bits (16 data bytes + 2 CRC bytes = $16 \times 9 + 2 \times 9 + 1$ start bit). The maximum length of a frame from PICC to PCD is 307 bits (32 data bytes + 2 CRC bytes = $32 \times 9 + 2 \times 9 + 1$ start bit).

For a multi-byte parameter, the least significant byte is always transmitted first. As an example, take reading from the memory using the READ command. Byte 0 from the addressed block is transmitted first after which, byte 1 to byte 3 are transmitted. The same sequence continues for the next block and all subsequent blocks.
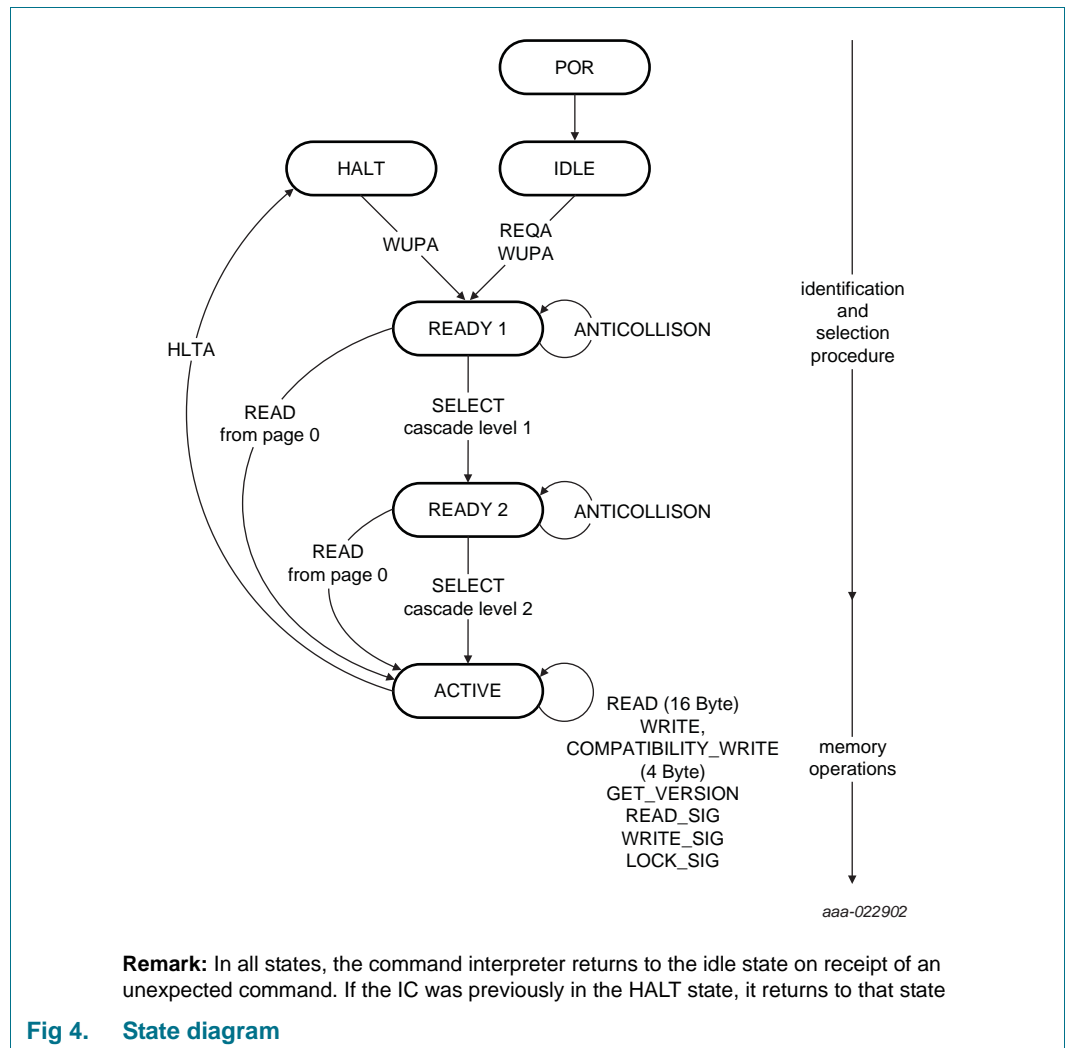
8.3 Data integrity

Following mechanisms are implemented in the contactless communication link between reader and card to ensure very reliable data transmission:

- 16 bits CRC per block
- parity bits for each byte
- bit count checking
- bit coding to distinguish between "1", "0" and "no information"
- channel monitoring (protocol sequence and bit stream analysis)

8.4 Communication principle

The reader initiates the commands and the Digital Control Unit of the MF0UN(H)00 controls them. The command response is depending on the state of the IC and for memory operations also on the access conditions valid for the corresponding page.

Remark: In all states, the command interpreter returns to the idle state on receipt of an unexpected command. If the IC was previously in the HALT state, it returns to that state

Fig 4.   State diagram

8.4.1 IDLE state

After a power-on reset (POR), the MF0UN(H)00 switches to the IDLE state. It only exits this state when a REQA or a WUPA command is received from the PCD. Any other data received while in this state is interpreted as an error and the MF0UN(H)00 remains in the IDLE state.

Refer to Ref. 4 for implementation hints for a card polling algorithm that respects relevant timing specifications from ISO/IEC 14443 Type A.

After a correctly executed HLTA command out of the ACTIVE state, the default waiting state changes from the IDLE state the HALT state. This state can then be exited with a WUPA command or power-on reset only.

8.4.2 READY1 state

In this state, the PCD resolves the first part of the UID (3 bytes) using the ANTICOLLISION or SELECT commands in cascade level 1. This state is exited correctly after execution of either of the following commands:

- SELECT command from cascade level 1: the PCD switches the MF0UN(H)00 into READY2 state where the second part of the UID is resolved.
- READ command (from address 0): all anticollision mechanisms are bypassed and the MF0UN(H)00 switches directly to the ACTIVE state.

Remark: If more than one MF0UN(H)00 is in the PCD field, a READ command from address 0 selects all MF0UN(H)00 devices.
Any other data received in the READY1 state is interpreted as an error and, depending on its previous state, the MF0UN(H)00 returns to either the IDLE state or HALT state.

8.4.3 READY2 state

In this state, the MF0UN(H)00 supports the PCD in resolving the second part of its UID (4 bytes) with the cascade level 2 ANTICOLLISION command. This state is usually exited using the cascade level 2 SELECT command.

Alternatively, READY2 state can be skipped using a READ command (from address 0) as described for the READY1 state.

Remark: The response of the MF0UN(H)00 to the cascade level 2 SELECT command is the select acknowledge (SAK) byte. In accordance with ISO/IEC 14443, this byte indicates if the anticollision cascade procedure has finished. It also defines the type of device selected for the MIFARE architecture platform. The MF0UN(H)00 is now uniquely selected and only this device communicates with the PCD even when other contactless devices are present in the PCD field. If more than one MF0ULx1 is in the PCD field, a READ command from address 0 selects all MF0ULx1 devices. In this case, a collision occurs.
Any other data received when the device is in this state is interpreted as an error and, depending on its previous state, the MF0UN(H)00 returns to either the IDLE state or HALT state.

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8.4.4 ACTIVE state

All memory operations and other functions like the originality signature read-out are operated in the ACTIVE state.

The ACTIVE state is gratefully exited with the HLTA command and upon reception the MF0UN(H)00 transits to the HALT state.
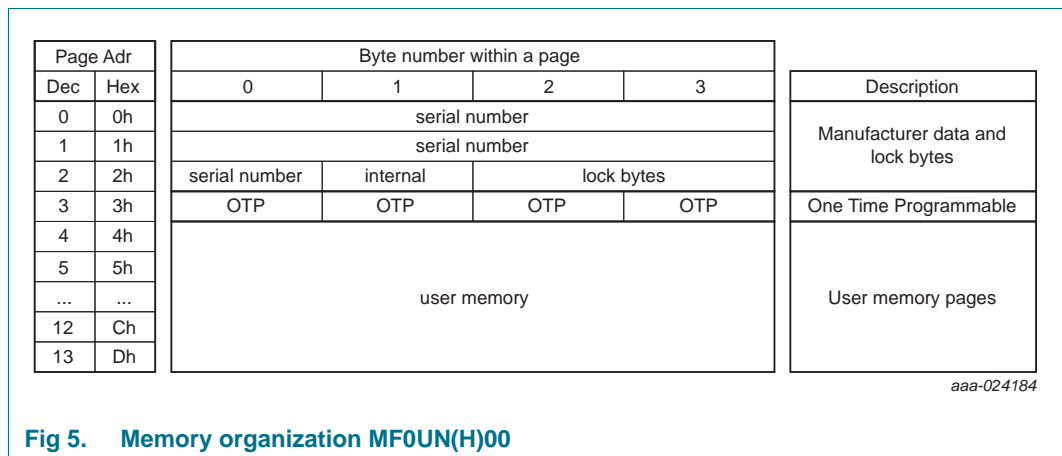
Any other data received when the device is in this state is interpreted as an error. Depending on its previous state the MF0UN(H)00 returns to either the IDLE state or HALT state.

8.4.5 HALT state

The HALT and IDLE states constitute the two wait states implemented in the MF0UN(H)00. An already processed MF0UN(H)00 can be set into the HALT state using the HLTA command. In the anticollision phase, this state helps the PCD to distinguish between processed cards and cards yet to be selected. The MF0UN(H)00 can only exit this state on execution of the WUPA command. Any other data received when the device is in this state is interpreted as an error and the MF0UN(H)00 state remains unchanged. Refer to Ref. 4 for correct implementation of an anticollision procedure based on the IDLE and HALT states and the REQA and WUPA commands.

8.5 Memory organization

The EEPROM memory is organized in pages with 4 bytes per page. The MF0UN(H)00 has 14d pages in total. The memory organization can be seen in Figure 5, the functionality of the different memory sections is described in the following sections.

Page Adr		Byte number within a page				Description
Dec	Hex	0	1	2	3	
0	0h	serial number				Manufacturer data and lock bytes
1	1h	serial number				
2	2h	serial number	internal	lock bytes		
3	3h	OTP	OTP	OTP	OTP	One Time Programmable
4	4h	user memory				User memory pages
5	5h					
...	...					
12	Ch					
13	Dh					

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Fig 5.   Memory organization MF0UN(H)00

8.5.1 UID/serial number

The unique 7-byte serial number (UID) and its two check bytes are programmed into the first 9 bytes of memory covering page addresses 00h, 01h and the first byte of page 02h. The second byte of page address 02h is reserved for internal data. These bytes are programmed and write protected in the production test.
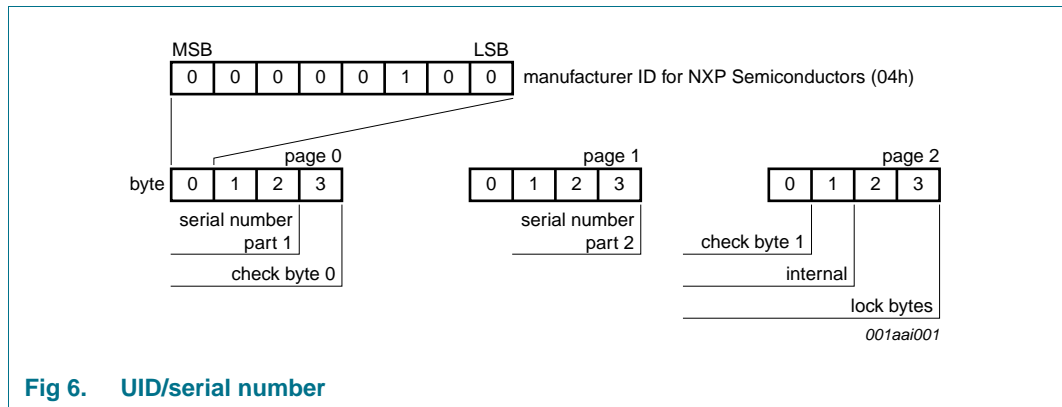

Fig 6.   UID/serial number

In accordance with ISO/IEC 14443-3 check byte 0 (BCC0) is defined as CT $\oplus$ SN0 $\oplus$ SN1 $\oplus$ SN2. Check byte 1 (BCC1) is defined as SN3 $\oplus$ SN4 $\oplus$ SN5 $\oplus$ SN6.

SN0 holds the Manufacturer ID for NXP Semiconductors (04h) in accordance with ISO/IEC 14443-3 and ISO/IEC 7816-6 AMD.1

8.5.2 Lock byte 0 and byte 1

The bits of byte 2 and byte 3 of page 02h represent the field programmable read-only locking mechanism. Each page from 03h (OTP) to 0Dh can be individually locked by setting the corresponding locking bit Lx to logic 1b to prevent further write access. The locking bits for pages Eh and Fh are set to 1b already to indicate that those pages are not available in the MF0UN(H)00. After locking, the corresponding page becomes read-only memory.

The three least significant bits of lock byte 0 are the block-locking bits. Bit 2 deals with pages 0Ah to 0Fh, bit 1 deals with pages 04h to 09h and bit 0 deals with page 03h (OTP). Once the block-locking bits are set, the locking configuration for the corresponding memory area is frozen.
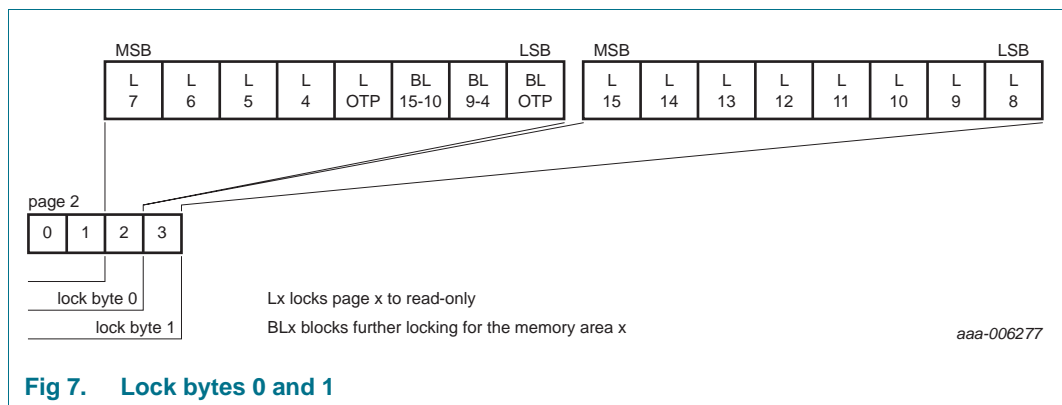

Fig 7.   Lock bytes 0 and 1

For example if BL15-10 is set to logic 1, then bits L15 to L10 (lock byte 1, bit[7:2]) can no longer be changed. A WRITE command or COMPATIBILITY_WRITE command to page 02h, sets the locking and block-locking bits. Byte 2 and byte 3 of the WRITE or COMPATIBILITY_WRITE command, and the contents of the lock bytes are bit-wise OR'ed and the result then becomes the new content of the lock bytes. This process is irreversible. If a bit is set to logic 1, it cannot be changed back to logic 0.

The contents of bytes 0 and 1 of page 02h are unaffected by the corresponding data bytes of the WRITE or COMPATIBILITY_WRITE command.

The default values of lock byte 0 is 00h and the default value of lock byte 1 is C0h. This indicates that pages Eh and Fh are not available for writing because of the smaller memory size.

Any write operation to the lock bytes 0 and 1, features anti-tearing support.

Remark: Setting a lock bit to 1 immediately prevents write access to the respective page

8.5.3 OTP bytes

Page 03h is the OTP page and it is preset so that all bits are set to logic 0 after production. These bytes can be bit-wise modified using the WRITE or COMPATIBILITY_WRITE command.

Fig 8.　OTP bytes
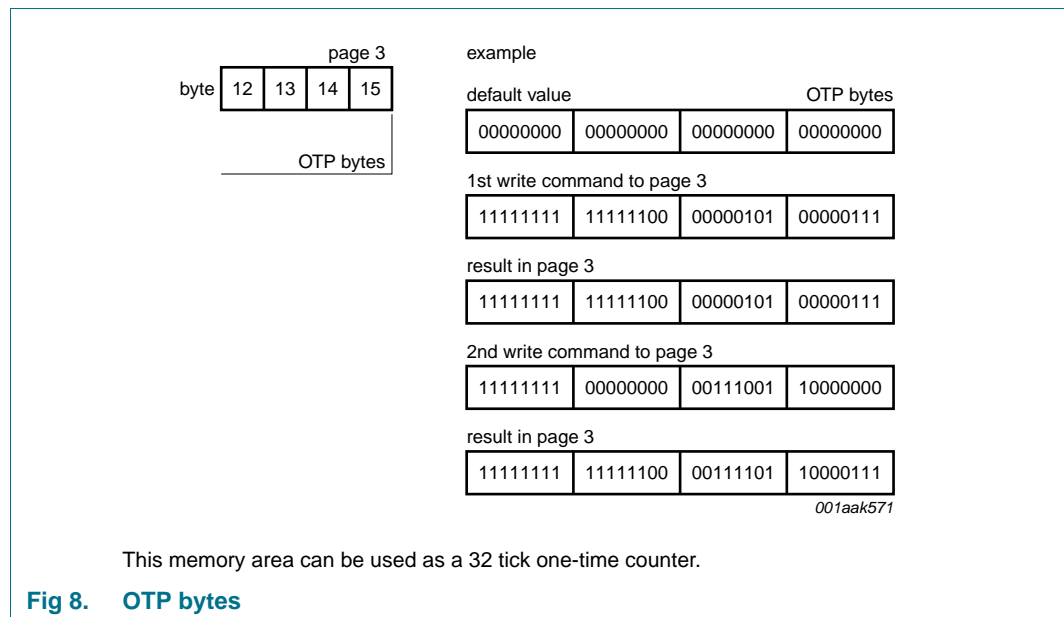
The parameter bytes of the WRITE command and the current contents of the OTP bytes are bit-wise OR'ed. The result is the new OTP byte contents. This process is irreversible and once a bit is set to logic 1, it cannot be changed back to logic 0.

The default value of the OTP bytes is 00 00 00 00h.

Any write operation to the OTP bytes features anti-tearing support.

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8.5.4 Data pages

Pages 04h to 0Dh for the MF0UN(H)00 are the user memory read/write area.

Remark: The default content of the data blocks at delivery is not defined.

8.6 Originality signature

The MIFARE Ultralight Nano offers a feature to verify the origin of a ticket with a certain confidence using the UID and an originality signature which is stored in a hidden part of memory. The originality signature can be read with the READ_SIG command. This check can also be performed on personalized tickets.

The MIFARE Ultralight Nano provides the possibility to customize the originality signature to personalize the IC individually for a specific application.

At delivery, the MIFARE Ultralight Nano is pre-programmed with the NXP originality signature described below. This signature is locked in the dedicated memory. If needed, the signature can be unlocked with the LOCK_SIG command and re-programmed with a custom-specific signature using the WRITE_SIG command during the personalization process by the customer. The signature can be permanently locked afterwards with the LOCK_SIG command to avoid further modifications.

Remark: If no customized originality signature is required, it is recommended to permanently lock the NXP signature during the initialization process with the LOCK_SIG command.

8.6.1 Originality Signature at delivery

At delivery, the MIFARE Ultralight Nano is programmed with an NXP originality signature based on standard Elliptic Curve Cryptography (ECC curve secp128r1), according to the ECDSA algorithm. The use of a standard algorithm and curve ensures easy software integration of the originality check procedure in PCDs without specific hardware requirements.

Each MIFARE Ultralight Nano UID is signed with an NXP private key and the resulting 32-byte signature is stored in a hidden part of the MIFARE Ultralight Nano memory during IC production.

This signature can be retrieved using the READ_SIG command and can be verified in the PCD by using the corresponding ECC public key provided by NXP. In case the NXP public key is stored in the PCD, the complete signature verification procedure can be performed offline.

To verify the signature (for example with the use of the public domain crypto library OpenSSL) the tool domain parameters shall be set to secp128r1, defined within the standards for elliptic curve cryptography SEC (Ref. 8).

Details on how to check the NXP signature value are provided in following application note (Ref. 6). It is foreseen to offer an online and offline way to verify originality of MIFARE Ultralight Nano.

9. Command overview

The MIFARE Ultralight ticket activation follows the ISO/IEC 14443 Type A. After the MIFARE Ultralight ticket has been selected, it can either be deactivated using the ISO/IEC 14443 HLTA command, or the MIFARE Ultralight commands can be performed. For more details about the card activation, refer to Ref. 1.

9.1 MIFARE Ultralight Nano command overview

All available commands for the MIFARE Ultralight are shown in Table 5.

Table 5.   Command overview

Command[1]	ISO/IEC 14443	Command code (hexadecimal)
Request	REQA	26h (7 bit)
Wake-up	WUPA	52h (7 bit)
Anticollision CL1	Anticollision CL1	93h 20h
Select CL1	Select CL1	93h 70h
Anticollision CL2	Anticollision CL2	95h 20h
Select CL2	Select CL2	95h 70h
Halt	HLTA	50h 00h
GET_VERSION[2]	-	60h
READ	-	30h
WRITE	-	A2h
COMP_WRITE	-	A0h
READ_SIG[2]	-	3Ch
WRITE_SIG[2]	-	A9h
LOCK_SIG[2]	-	ACh

[1]   Unless otherwise specified, all commands use the coding and framing as described in Ref. 1.

[2]   this command is new in MIFARE Ultralight Nano compared to MIFARE Ultralight

9.2 Timing

The command and response timings shown in this document are not to scale and values are rounded to 1 µs.

All given command and response transmission times refer to the data frames including start of communication and end of communication. A PCD data frame, contains the start of communication (1 "start bit") and the end of communication (one logic 0 + 1 bit length of unmodulated carrier). A PICC data frame, contains the start of communication (1 "start bit") and the end of communication (1 bit length of no subcarrier).

The minimum command response time is specified according to Ref. 1 as an integer **n** which specifies the PCD to PICC frame delay time. The frame delay time from PICC to PCD has a minimum n of 9. The maximum command response time is specified as a time-out value. Depending on the command, the T_{ACK} value specified for command responses defines the PCD to PICC frame delay time. It does it for either the 4-bit ACK value specified in Section 9.3 or for a data frame.

All command timings are according to ISO/IEC 14443-3 frame specification as shown for the Frame Delay Time in Figure 9. For more details, refer to Ref. 1.
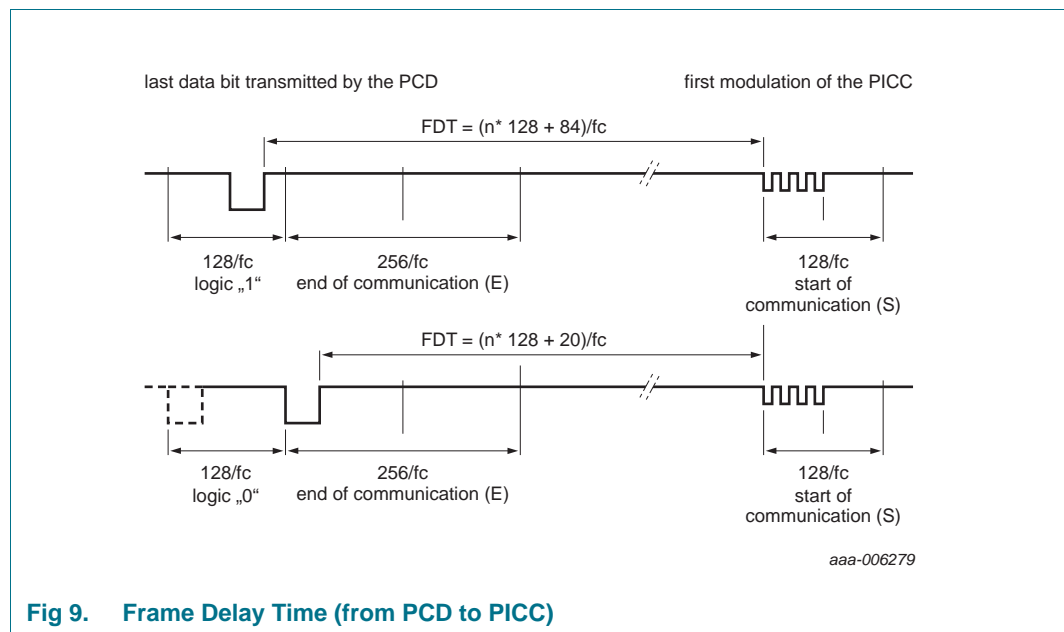

last data bit transmitted by the PCD   first modulation of the PICC

FDT = (n* 128 + 84)/fc

128/fc logic „1"   256/fc end of communication (E)   128/fc start of communication (S)

FDT = (n* 128 + 20)/fc

128/fc logic „0"   256/fc end of communication (E)   128/fc start of communication (S)

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Fig 9.   Frame Delay Time (from PCD to PICC)

Remark: Due to the coding of commands, the measured timings usually excludes (a part of) the end of communication. Consider this factor when comparing the specified times with the measured times.

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9.3 MIFARE Ultralight ACK and NAK

The MIFARE Ultralight uses a 4-bit ACK / NAK as shown in Table 6.

Table 6.   ACK and NAK values

Code (4-bit)	ACK/NAK
Ah	Acknowledge (ACK)
0h	NAK for invalid argument (i.e. invalid page address)
1h	NAK for parity or CRC error
5h, 7h	NAK for EEPROM write error

9.4 ATQA and SAK responses

For details on the type identification procedure, refer to Ref. 3.

The MF0UN(H)00 replies to a REQA or WUPA command with the ATQA value shown in Table 7. It replies to a Select CL2 command with the SAK value shown in Table 8. The 2-byte ATQA value is transmitted with the least significant byte first (44h).

Table 7.   ATQA response of the MF0UN(H)00

Sales type	Hex value	Bit number															
		16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MF0UN(H)00	00 44h	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

Table 8.   SAK response of the MF0UN(H)00

Sales type	Hex value	Bit number							
		8	7	6	5	4	3	2	1
MF0UN(H)00	00h	0	0	0	0	0	0	0	0

Remark: The ATQA coding in bits 7 and 8 indicate the UID size according to ISO/IEC 14443.

Remark: The bit numbering in the ISO/IEC 14443 starts with LSB = bit 1 and not with LSB = bit 0. So 1 byte counts bit 1 to bit 8 instead of bit 0 to 7.

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10. MIFARE Ultralight Nano commands

10.1 GET_VERSION

The GET_VERSION command is used to retrieve information on the MIFARE family, product version, storage size and other product data required to identify the MF0UN(H)00.

This command is available on other MIFARE products to have a common way of identifying products across platforms and evolution steps.

The GET_VERSION command has no arguments and replies the version information for the specific MF0UN(H)00 type. The command structure is shown in Figure 10 and Table 9.

Table 10 shows the required timing.
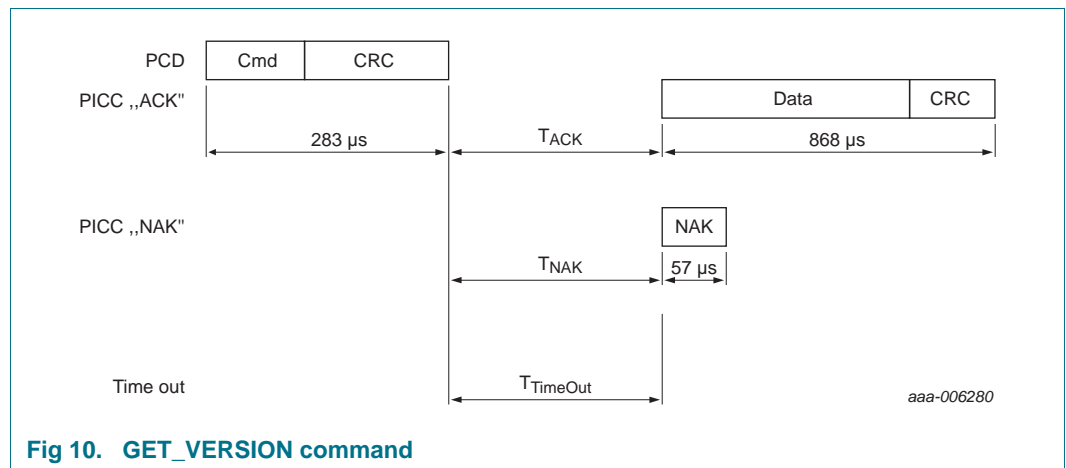
Fig 10. GET_VERSION command

Table 9.   GET_VERSION command

Name	Code	Description	Length
Cmd	60h	Get product version	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
Data	-	Product version information	8 bytes
NAK	see Table 6	see Section 9.3	4-bit

Table 10.   GET_VERSION timing
These times exclude the end of communication of the PCD.

	T_{ACK} min	T_{ACK} max	T_{NAK} min	$T_{NAK max}$	$T_{TimeOut}$
GET_VERSION	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	5 ms

Table 11.   GET_VERSION response for MF0UN(H)00

Byte no.	Description	MF0UN00	MF0UNH00	Interpretation
0	fixed header	00h	00h	
1	vendor ID	04h	04h	NXP Semiconductors
2	product type	03h	03h	MIFARE Ultralight
3	product subtype	01h	02h	17 pF / 50pF
4	major product version	02h	02h	Nano
5	minor product version	00h	00h	V0
6	storage size	0Bh	0Bh	see following explanation
7	protocol type	03h	03h	ISO/IEC 14443-3 compliant

The most significant 7 bits of the storage size byte are interpreted as an unsigned integer value n. As a result, it codes the total available user memory size as 2^n. If the least significant bit is 0b, the user memory size is exactly 2^n. If the least significant bit is 1b, the user memory size is between 2^n and 2^{n+1}.

The user memory for the MF0UN(H)00 is 40 bytes. This memory size is between 32d bytes and 64d bytes. Therefore, the most significant 7 bits of the value 0Bh, are interpreted as 5d and the least significant bit is 1b.

10.2 READ

The READ command requires a start page address, and returns the 16 bytes of four MIFARE Ultralight pages. For example if address (Addr) is 03h then pages 03h, 04h, 05h, 06h are returned. A rollover mechanism is implemented if the READ command address is near the end of the accessible memory area. For details on those cases see the description below. The command structure is shown in Figure 11 and Table 12. Table 13 shows the required timing.
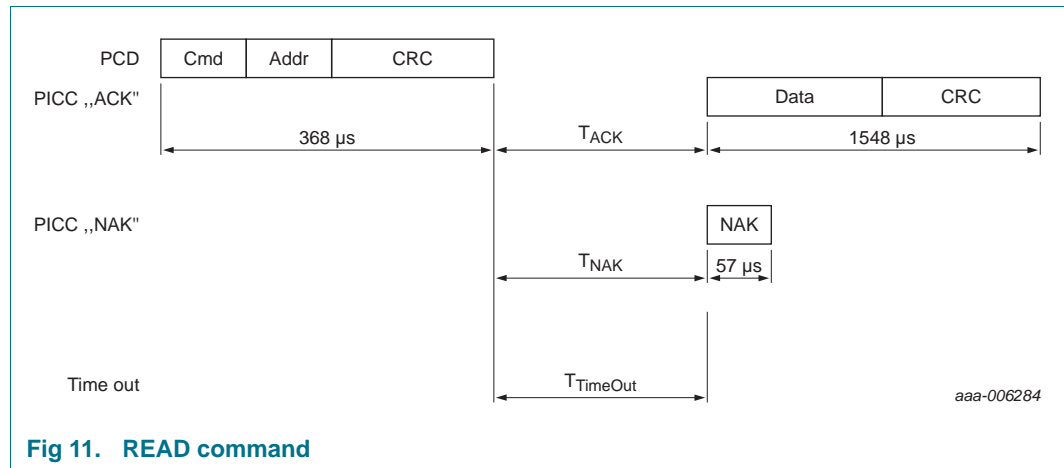

Fig 11. READ command

Table 12. READ command

Name	Code	Description	Length
Cmd	30h	read four pages	1 byte
Addr	-	start page address	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
Data	-	Data content of the addressed pages	16 bytes
NAK	see Table 6	see Section 9.3	4-bit

Table 13. READ timing
These times exclude the end of communication of the PCD.

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
READ	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	5 ms

In the initial state of the MF0UN(H)00, the following memory pages are allowed as Addr parameter to the READ command.

- page address 00h to 0Fh

Addressing a memory page beyond the limits above results in a NAK response from the MF0UN(H)00.

Remark: Although the used memory area is only ranging from pages 0h to Dh, the remaining 2 pages Eh and Fh can be addressed for backwards compatibility reasons. Those 2 pages are locked and read always as 00000000h.

A roll-over mechanism is implemented to continue reading from page 00h once the end of the accessible memory is reached. For example, reading from address Dh on a MF0UN(H)00 results in pages 0D, 0Eh, 0Fh and 00h being returned.

10.3 WRITE

The WRITE command requires a block address, and writes 4 bytes of data into the addressed MIFARE Ultralight Nano page. The WRITE command is shown in Figure 12 and Table 14. Table 15 shows the required timing.
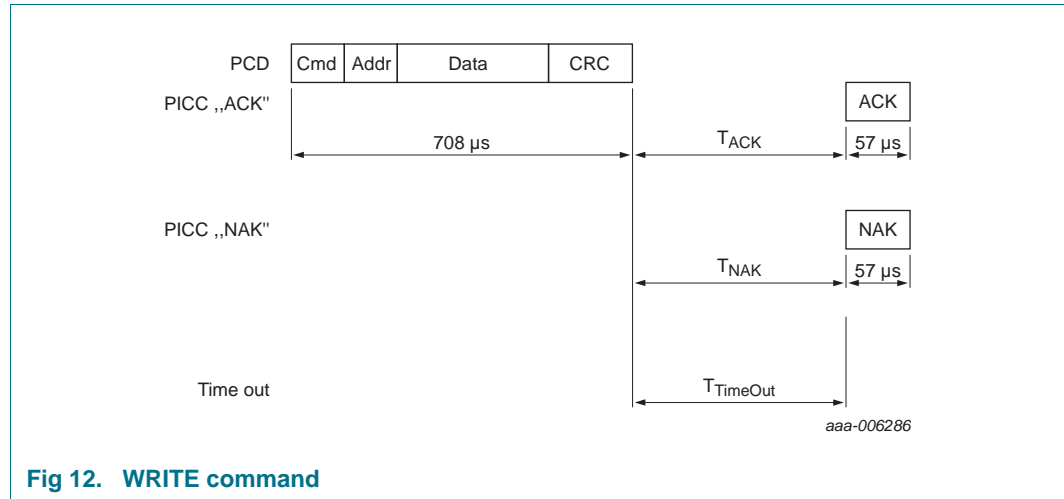

Fig 12. WRITE command

Table 14.   WRITE command

Name	Code	Description	Length
Cmd	A2h	write one page	1 byte
Addr	-	page address	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
Data	-	data	4 bytes
NAK	see Table 6	see Section 9.3	4-bit

Table 15.   WRITE timing
These times exclude the end of communication of the PCD.

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
WRITE	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	5 ms

In the initial state of the MF0UN(H)00, the following memory pages are valid Addr parameters to the WRITE command.

- page address 02h to 0Dh

Addressing a memory page beyond the limits above results in a NAK response from the MF0UN(H)00.

Pages which are locked against writing cannot be reprogrammed using any write command. The locking mechanisms include lock bits as well.

The MF0UN(H)00 features tearing protected write operations to specific memory content. The following pages are protected against tearing events during a WRITE operation:

- page 2 containing lock bits
- page 3 containing OTP bits

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10.4 COMPATIBILITY_WRITE

The COMPATIBILITY_WRITE command is implemented to accommodate the established MIFARE Classic PCD infrastructure. Even though 16 bytes are transferred to the MF0UN(H)00, only the least significant 4 bytes (bytes 0 to 3) are written to the specified address. Set all the remaining bytes, 04h to 0Fh, to logic 00h. The COMPATIBILITY_WRITE command is shown in Figure 13 and Table 14. Table 17 shows the required timing.
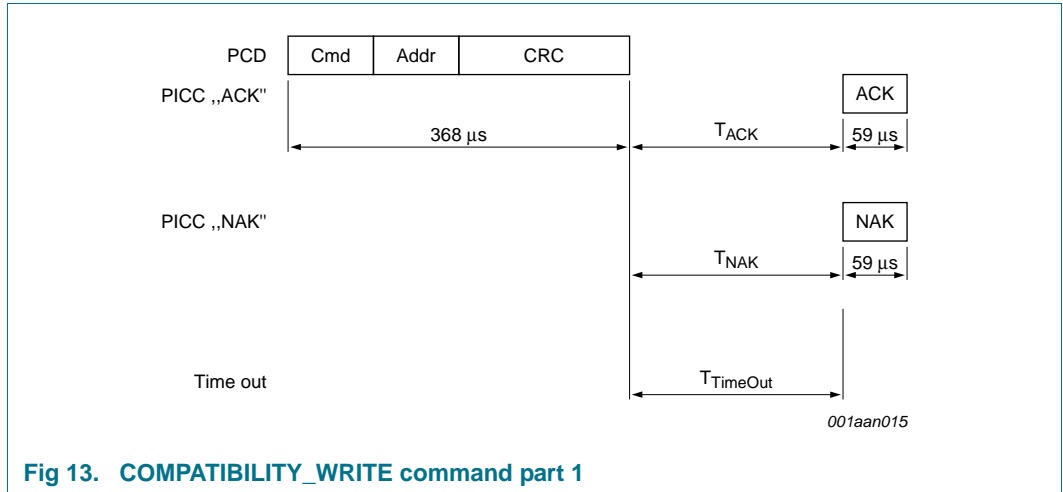

Fig 13. COMPATIBILITY_WRITE command part 1
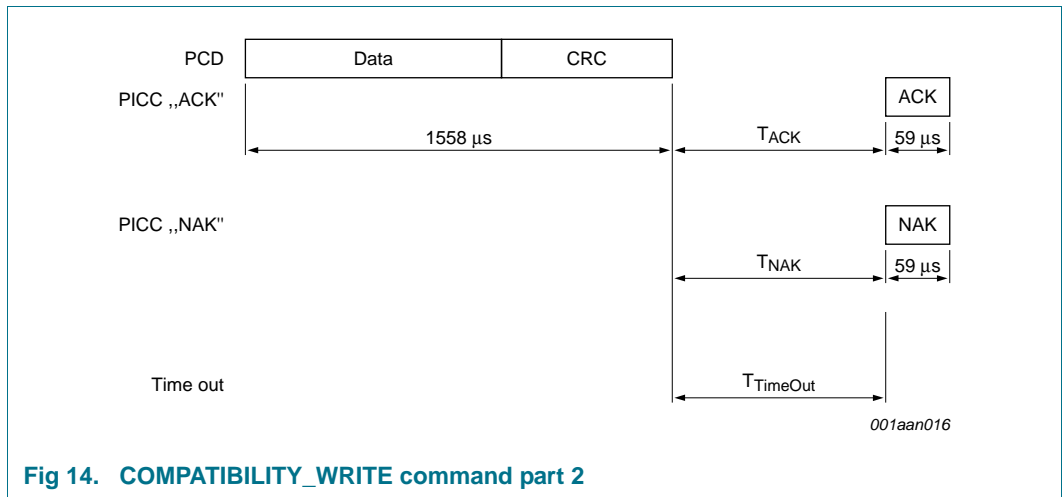
Fig 14. COMPATIBILITY_WRITE command part 2

Table 16.   COMPATIBILITY_WRITE command

Name	Code	Description	Length
Cmd	A0h	compatibility write	1 byte
Addr	-	page address	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
Data	-	16-byte Data, only least significant 4 bytes are written	16 bytes
NAK	see Table 6	see Section 9.3	4-bit

Table 17.   COMPATIBILITY_WRITE timing

These times exclude the end of communication of the PCD.

	T_{ACK} min	T_{ACK} max	$T_{NAK\ min}$	$T_{NAK\ max}$	$T_{TimeOut}$
COMPATIBILITY_WRITE part 1	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	5 ms
COMPATIBILITY_WRITE part 2	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	10 ms

In the initial state of the MF0UN(H)00, the following memory pages are valid Addr parameters to the COMPATIBILITY_WRITE command.

- page address 02h to 0Dh

Addressing a memory page beyond the limits above results in a NAK response from the MF0UN(H)00.

Pages which are locked against writing cannot be reprogrammed using any write command. The locking mechanisms include lock bits as well.

The MF0UN(H)00 features tearing protected write operations to specific memory content. The following pages are protected against tearing events during a COMPATIBILITY_WRITE operation:

- page 2 containing lock bits
- page 3 containing OTP bits

10.5 READ_SIG

The READ_SIG command returns an IC-specific, 32-byte ECC signature, to verify NXP Semiconductors as the silicon vendor. The signature is programmed at chip production and cannot be changed afterwards. The command structure is shown in Figure 15 and Table 18.

Table 19 shows the required timing.
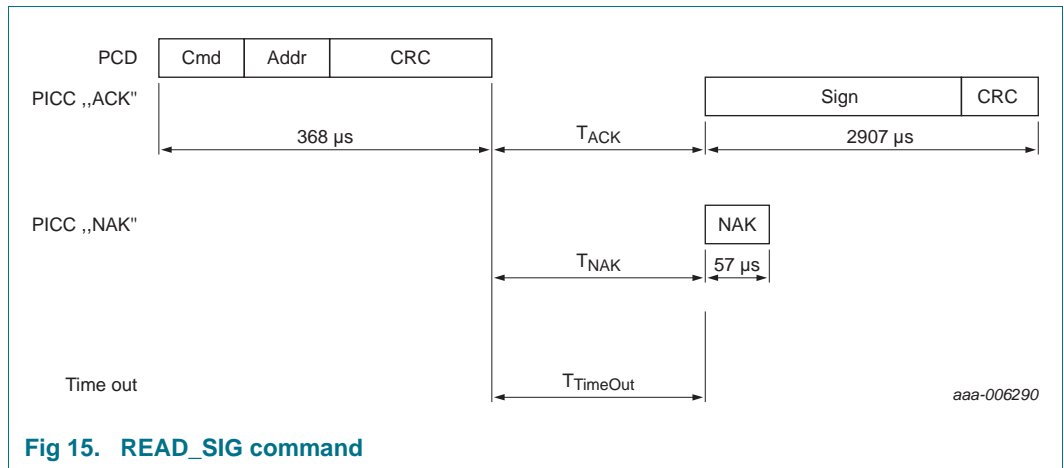
Fig 15.   READ_SIG command

Table 18.   READ_SIG command

Name	Code	Description	Length
Cmd	3Ch	read ECC signature	1 byte
Addr	00h	RFU, is set to 00h	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
Sign	-	ECC signature	32 bytes
NAK	see Table 6	see Section 9.3	4-bit

Table 19.   READ_SIG timing
These times exclude the end of communication of the PCD.

	T_{ACK} **min**	T_{ACK} **max**	$T_{NAK\ min}$	$T_{NAK\ max}$	$T_{TimeOut}$
READ_SIG	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	5 ms

Ref. 6 describes the signature verification procedure.

10.6 WRITE_SIG

The WRITE_SIG command allows the writing of a customized originality signature into the dedicated originality signature memory.

The WRITE_SIG command requires an originality signature block address, and writes 4 bytes of data into the addressed originality signature block. The WRITE_SIG command is shown in Figure 16 and Table 20.

Table 21 shows the required timing.
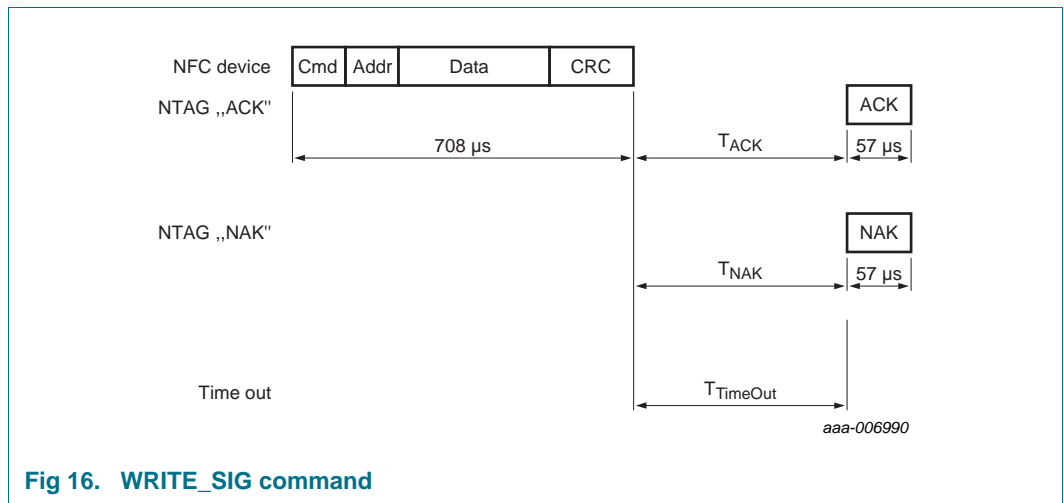
Fig 16. WRITE_SIG command

Table 20. WRITE_SIG command

Name	Code	Description	Length
Cmd	A9h	write one originality signature block	1 byte
Addr	-	block address	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
Data	-	signature bytes to be written	4 bytes
NAK	see Table 6	see Section 9.3	4 bit

Table 21. WRITE_SIG timing
These times exclude the end of communication of the PCD.

	$T_{ACK/NAK}$ **min**	$T_{ACK/NAK}$ **max**	$T_{TimeOut}$
WRITE_SIG	n=9	$T_{TimeOut}$	10 ms

In the initial state of MIFARE Ultralight Nano, the following originality signature blocks are valid Addr parameters to the WRITE_SIG command.

- originality signature block address 00h to 07h for MF0UN(H)00

Addressing a memory block beyond the limits above results in a NAK response from MIFARE Ultralight Nano.

Table 22.   Blocks for the WRITE_SIG command

Originality signature block	Byte 0	Byte 1	Byte 2	Byte 3
00h				MSByte
01h				
...				
06h				
07h	LSByte			

If the originality signature is locked or permanently locked, a WRITE_SIG command results in a NAK response from the MIFARE Ultralight Nano.

10.7 LOCK_SIG

The LOCK_SIG command allows to unlock, lock or permanently lock the dedicated originality signature memory.

The originality signature memory can only be unlocked if the originality signature memory is not permanently locked.

Permanently locking of the originality signature with the LOCK_SIG command is irreversible and the originality signature memory can never be unlocked and reprogrammed again.

The LOCK_SIG command is shown in Figure 17 and Table 23. Table 24 shows the required timing.
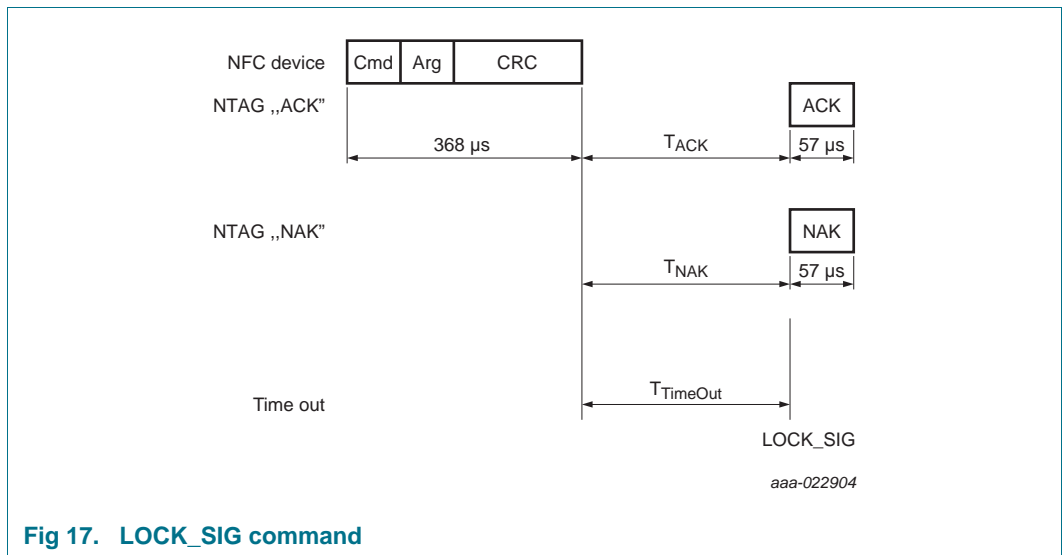
Fig 17. LOCK_SIG command

Table 23. LOCK_SIG command

Name	Code	Description	Length
Cmd	ACh	Lock signature	1 byte
Arg	-	Lock action: 00h ... unlock 01h ... lock 02h ... permanently lock	1 byte
CRC	-	CRC according to Ref. 1	2 bytes
NAK	see Table 6	see Section 9.3	4 bit

Table 24. LOCK_SIG timing

These times exclude the end of communication of the PCD.

	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
LOCK_SIG	n=9	$T_{TimeOut}$	10 ms

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11. Limiting values

Stresses exceeding one or more of the limiting values, can cause permanent damage to the device. Exposure to limiting values for extended periods can affect device reliability.

Table 25. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter		Min	Max	Unit
I_I	input current		-	40	mA
P_{tot}/pack	total power dissipation per package		-	120	mW
T_{stg}	storage temperature		−55	125	°C
T_{amb}	ambient temperature		−25	70	°C
V_{ESD}	electrostatic discharge voltage on LA/LB	[1]	2	-	kV

[1]   ANSI/ESDA/JEDEC JS-001; Human body model: C = 100 pF, R = 1.5 kΩ

12. Characteristics

Table 26. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance MF0UN00	[1]	-	17.0	-	pF
C_i	input capacitance MF0UNH00	[1]	-	50.0	-	pF
f_i	input frequency		-	13.56	-	MHz
EEPROM characteristics						
t_{ret}	retention time	T_{amb} = 22 °C	10	-	-	year
$N_{endu(W)}$	write endurance	T_{amb} = 22 °C	100000	-	-	cycle

[1] T_{amb} = 22 °C, f = 13.56 MHz, V_{LaLb} = 1.5 V RMS

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13. Wafer specification

Table 27.   Wafer specifications MF0ULx1

Wafer	
diameter	200 mm typical (8 inches)
maximum diameter after foil expansion	210 mm
die separation process	laser dicing
thicknessMF0ULx101DUD	120 μm $\pm$ 15 μm
MF0ULx101DUF	75 μm $\pm$ 10 μm
flatness	not applicable
Potential Good Dies per Wafer (PGDW)	112373
Wafer backside	
material	Si
treatment	ground and stress relieve
roughness	R_a max = 0.5 μm
	R_t max = 5 μm
Chip dimensions	
step size[1]MF0UN(H)00	x = 528 μm
	y = 524 μm
gap between chips[1]	typical = 20 μm
	minimum = 5 μm
Passivation	
type	sandwich structure
material	PSG / nitride
thickness	500 nm / 600 nm
Au bump (substrate connected to VSS)	
material	> 99.9 % pure Au
hardness	35 to 80 HV 0.005
shear strength	> 70 MPa
height	18 μm
height uniformity	within a die = $\pm$2 μm
	within a wafer = $\pm$3 μm
	wafer to wafer = $\pm$4 μm
flatness	minimum = $\pm$1.5 μm
size	LA, LB, GND, TP[2] = 60 μm $\times$ 60 μm
size variation	$\pm$5 μm
under bump metallization	sputtered TiW

[1]   The step size and the gap between chips may vary due to changing foil expansion

[2]   Pads GND and TP are disconnected when wafer is sawn

13.1 Fail die identification

Electronic wafer mapping covers the electrical test results and the results of mechanical/visual inspection. No ink dots are applied.

14. Bare die outline

For more details on the wafer delivery forms, see Ref. 5.

	X [µm]	y [µm]
Chip Step	528[1]	524[1]
Bump size		
LA, LB, GND,TP	60	60

typ. 20.0[1]
min. 5.0

typ. 20.0[1]
min. 5.0

LA   TP

442.0   typ. 524.0[1]

43.0

GND   LB

43.0

466.0

Y

(2)

X   typ. 528.0[1]

aaa-022905

Fig 18.   Bare die outline MF0UN(H)00
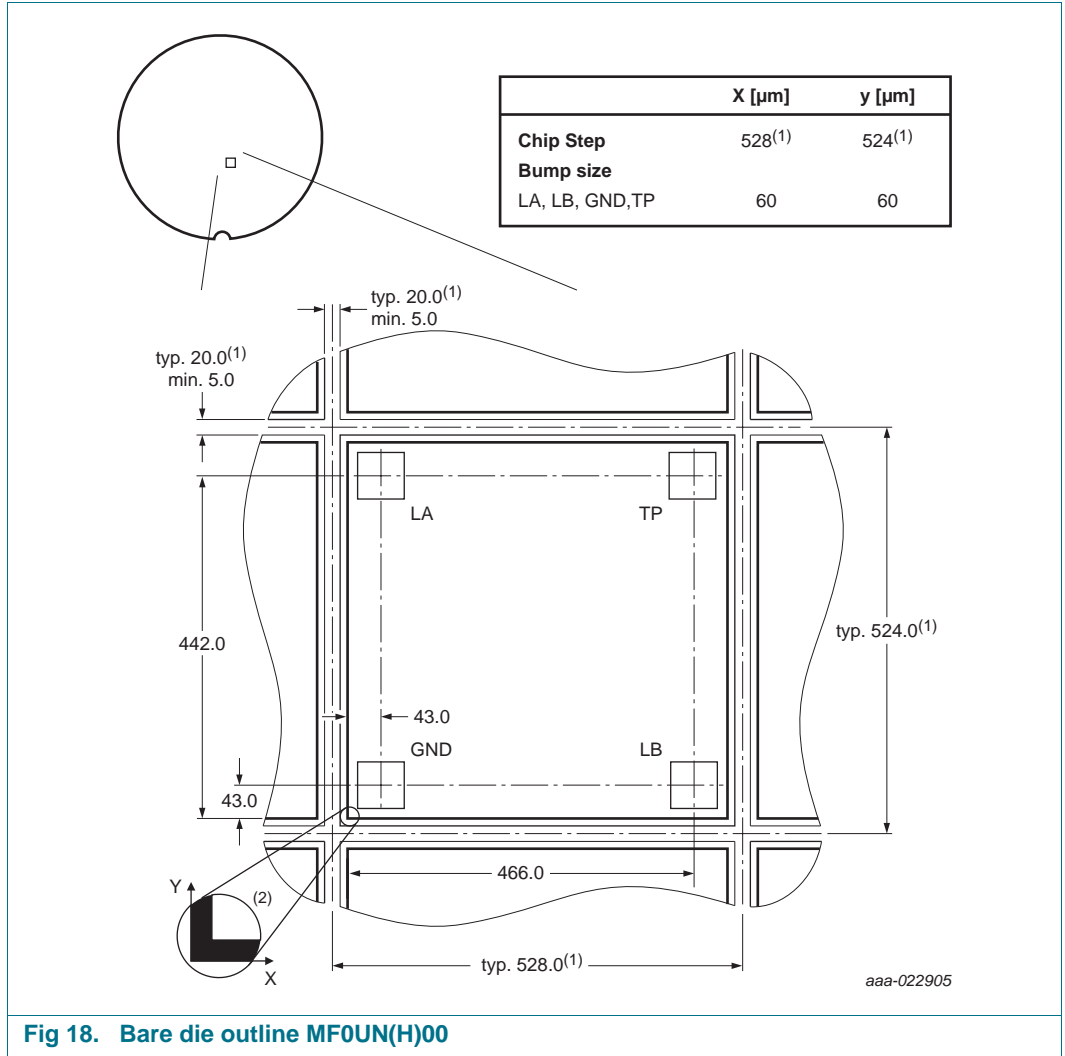
15. Abbreviations

Table 28.   Abbreviations and symbols

Acronym	Description
ACK	Acknowledge
ATQA	Answer to request: Type A
CRC	Cyclic Redundancy Check
CT	Cascade Tag (value 88h) as defined in ISO/IEC 14443-3 Type A
ECC	Elliptic Curve Cryptography
EEPROM	Electrically Erasable Programmable Read-Only Memory
FDT	Frame Delay Time
FFC	Film Frame Carrier
IC	Integrated Circuit
LCR	L = inductance, Capacitance, Resistance (LCR meter)
LSB	Least Significant Bit
LSByte	Least Significant Byte
MSByte	Most Significant Byte
NAK	Not acknowledge
NV	Non-Volatile memory
OTP	One Time Programmable
PCD	Proximity Coupling Device (contactless reader)
PICC	Proximity Integrated Circuit Card (contactless card)
REQA	Request command: Type A
RF	Radio Frequency
RMS	Root Mean Square
SAK	Select acknowledge: Type A
SECS-II	SEMI Equipment Communications Standard part 2
TiW	Titanium Tungsten
UID	Unique identifier
WUPA	Wake-Up Protocol: Type A

16. References

[1] ISO/IEC 14443 — International Organization for Standardization

[2] MIFARE (Card) Coil Design Guide — Application note, BU-ID Document number 0117**[1]

[3] MIFARE Type Identification Procedure — Application note, BU-ID Document number 0184**[1]

[4] MIFARE ISO/IEC 14443 PICC Selection — Application note, BU-ID Document number 1308**[1]

[5] General specification for 8" wafer on UV-tape with electronic fail die marking — Delivery Type Description, BU-ID Document number 1093**[1]

[6] AN11341 MIFARE Ultralight Originality Signature Validation — Application note, BU-ID Document number 2591**

[7] ISO/IEC 15457-1 Identification cards — Thin flexible cards

[8] Certicom Research. SEC 2 — Recommended Elliptic Curve Domain Parameters, version 2.0, January 2010

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1. ** ... document version number

17. Revision history

Table 29. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MF0UN(H)00 v.3.1	20160907	Product data sheet	-	MF0UN(H)00 v.3.0
Modifications:	Table 27 "Wafer specifications MF0ULx1": PGDW value added			
MF0UN(H)00 v.3.0	20160721	Product data sheet	-	344820
Modifications:	• Section 5 "Ordering information": updated • Data sheet status changed into Product data sheet and security status into COMPANY PUBLIC			
344820	20160518	Preliminary data sheet	-	-
	• Initial version			

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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20. Tables

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