

# NPIC6C596A-Q100

Power logic 8-bit shift register; open-drain outputs

Rev. 1 — 18 October 2013

Product data sheet

## 1. General description

The NPIC6C596A-Q100 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and open-drain outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset  $\overline{MR}$  input. A LOW on  $\overline{MR}$  resets both the shift register and storage register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register. To provide additional hold time in cascaded applications, the serial output QS7 is clocked out on the falling edge of SHCP. Data in the storage register drives the gate of the output extended-drain NMOS (EDNMOS) transistor whenever the output enable input ( $\overline{OE}$ ) is LOW. A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the registers. The open-drain outputs are 33 V/100 mA continuous current extended-drain NMOS transistors designed for use in systems that require moderate load power such as LEDs. Integrated voltage clamps in the outputs, provide protection against inductive transients. These voltage clamps make the device suitable for power driver applications such as relays, solenoids and other low-current or medium-voltage loads.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Wide supply range 2.3 V to 5.5 V
- Low  $R_{DSon}$
- Eight Power EDNMOS transistor outputs of 100 mA continuous current
- 250 mA current limit capability
- Output clamping voltage 33 V
- 30 mJ avalanche energy capability
- Enhanced cascading for multiple stages
- All registers cleared with single input
- Low power consumption
- ESD protection:
  - ◆ HBM AEC-Q100-002 revision D exceeds 2500 V
  - ◆ CDM AEC-Q100-011 revision B exceeds 1000 V



### 3. Applications

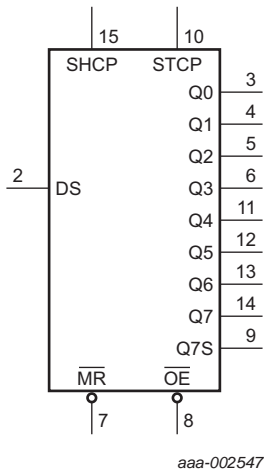
- LED sign
- Graphic status panel
- Fault status indicator

### 4. Ordering information

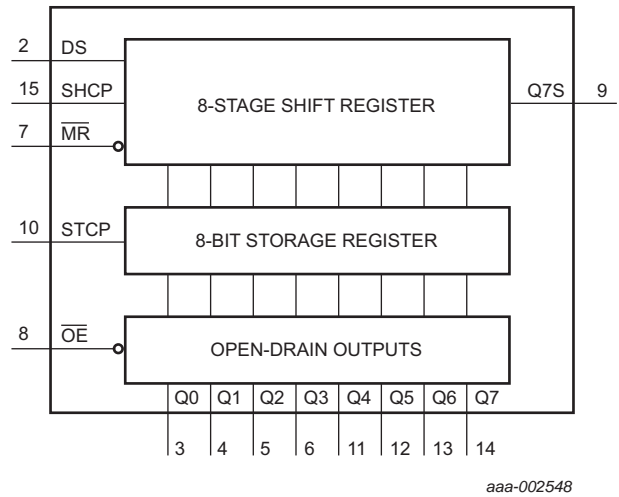
**Table 1. Ordering information**

Type number	Package			Version
	Temperature range	Name	Description	
NPIC6C596AD-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
NPIC6C596APW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
NPIC6C596ABQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

### 5. Functional diagram



**Fig 1. Logic symbol**



**Fig 2. Functional diagram**

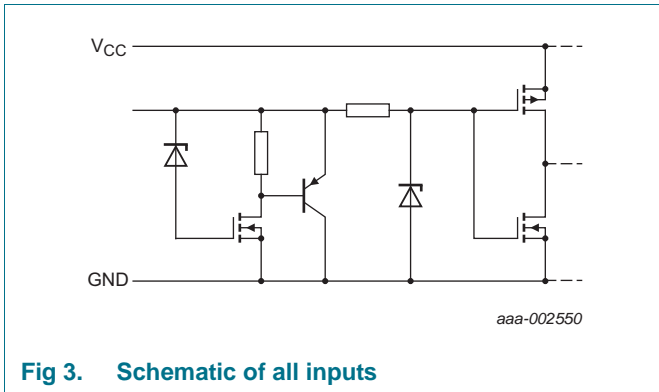


Fig 3. Schematic of all inputs

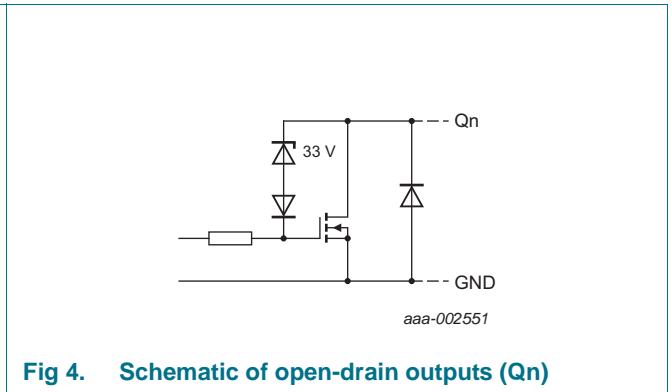


Fig 4. Schematic of open-drain outputs (Qn)

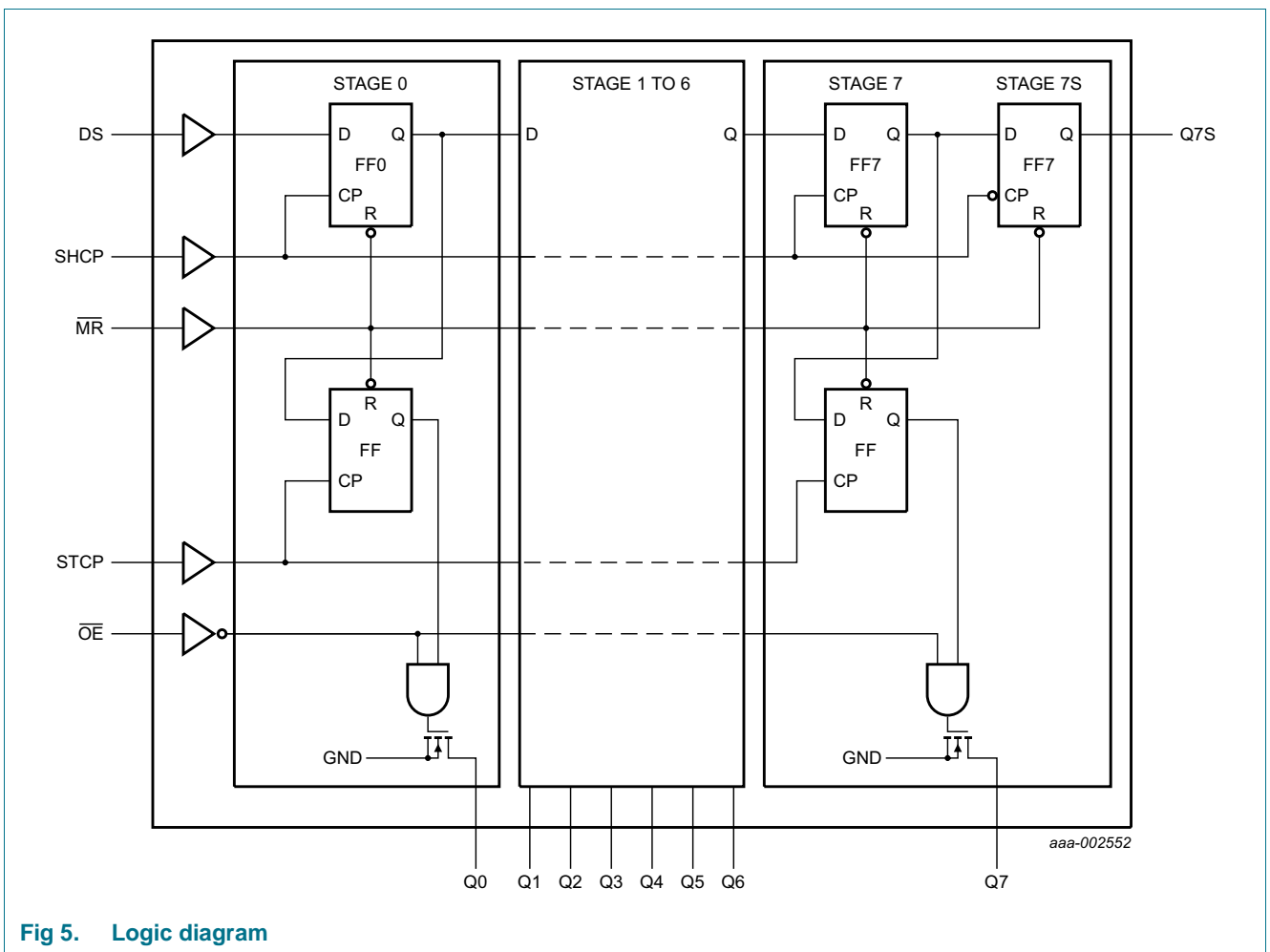


Fig 5. Logic diagram

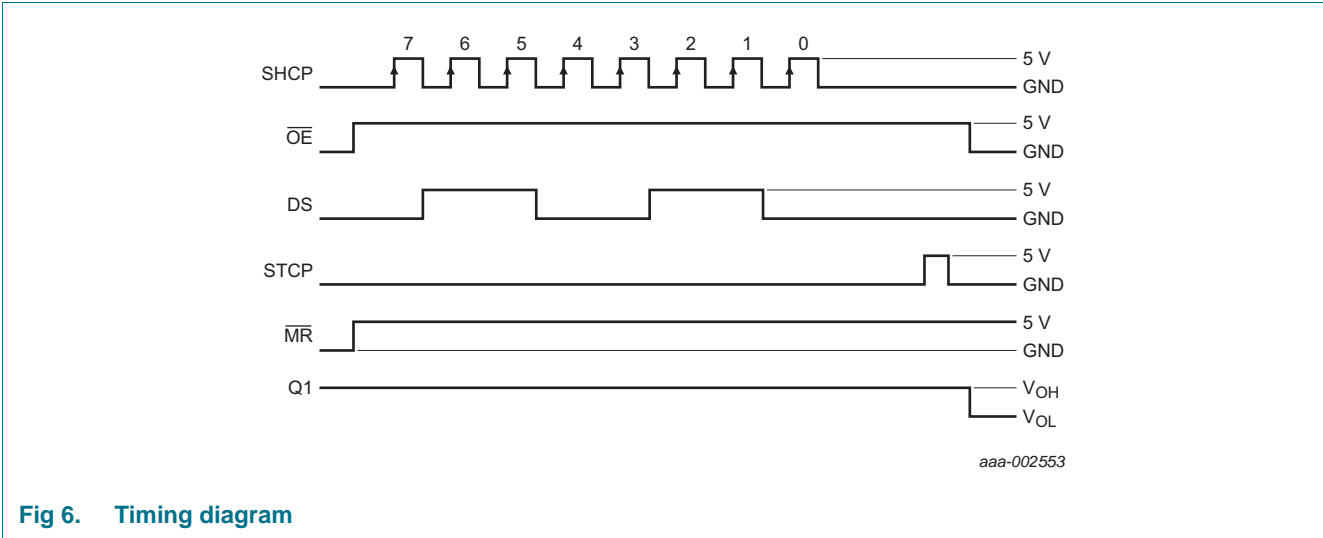


Fig 6. Timing diagram

## 6. Pinning information

### 6.1 Pinning

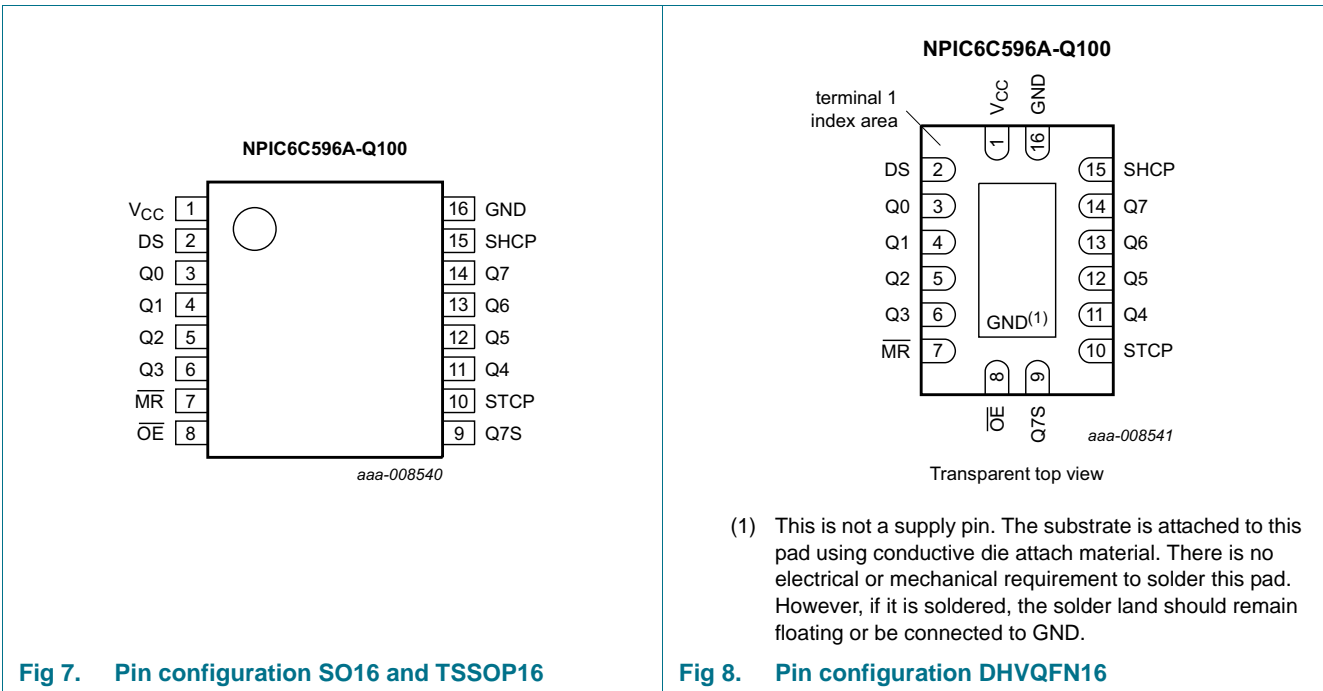


Fig 7. Pin configuration SO16 and TSSOP16

Fig 8. Pin configuration DHVQFN16

## 6.2 Pin description

**Table 2.** Pin description

Symbol	Pin	Description
$V_{CC}$	1	supply voltage
DS	2	serial data input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	3, 4, 5, 6, 11, 12, 13, 14	parallel data output (open-drain)
$\overline{MR}$	7	master reset (active LOW)
$\overline{OE}$	8	output enable input (active LOW)
Q7S	9	serial data output
STCP	10	storage register clock input
SHCP	15	shift register clock input
GND	16	ground (0 V)

## 7. Limiting values

**Table 3.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.3	+7.0	V
$V_{DS}$	drain-source voltage	power EDNMOS drain-source voltage	[1]	+33	V
$I_{d(SD)}$	source-drain diode current	continuous	-	250	mA
		pulsed	[2]	500	mA
$I_D$	drain current	$T_{amb} = 25\text{ °C}$			
		continuous; each output; all outputs on	-	100	mA
		pulsed; each output; all outputs on	[2]	250	mA
$I_{DM}$	peak drain current	single output; $T_{amb} = 25\text{ °C}$	[2]	250	mA
$E_{AS}$	non-repetitive avalanche energy	single pulse; see <a href="#">Figure 9</a>	[3]	30	mJ
$I_{AL}$	avalanche current	see <a href="#">Figure 9</a>	[3]	200	mA
$T_{stg}$	storage temperature		-65	+150	°C

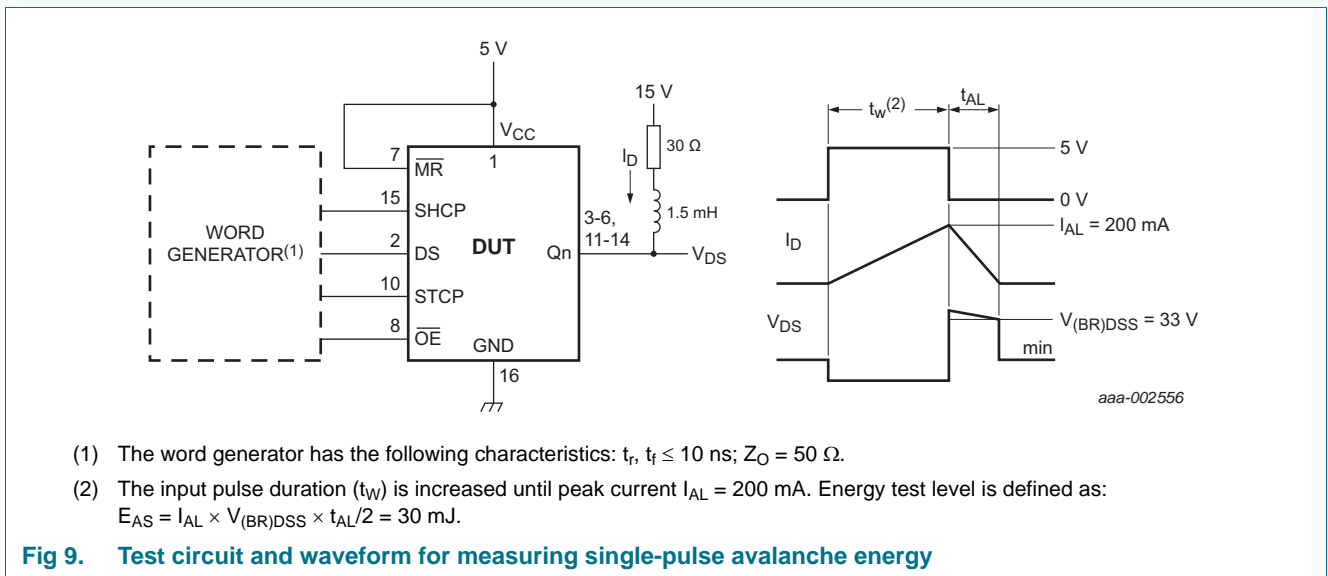
**Table 3. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[4]			
		SO16	-	800	mW	
		TSSOP16	-	725	mW	
		DHVQFN16	-	1825	mW	
		T <sub>amb</sub> = 125 °C	[4]			
		SO16	-	160	mW	
		TSSOP16	-	145	mW	
DHVQFN16	-	365	mW			

- [1] Each power EDNMOS source is internally connected to GND.
- [2] Pulse duration ≤ 100 μs and duty cycle ≤ 2 %.
- [3] V<sub>DS</sub> = 15 V; starting junction temperature (T<sub>J</sub>) = 25 °C; L = 1.5 H; avalanche current (I<sub>AL</sub>) = 200 mA.
- [4] For SO16 packages: above 25 °C the value of P<sub>tot</sub> derates linearly with 6.4 mW/°C.  
 For TSSOP16 packages: above 25 °C the value of P<sub>tot</sub> derates linearly with 5.8 mW/°C.  
 For DHVQFN16 packages: above 25 °C the value of P<sub>tot</sub> derates linearly with 14.6 mW/°C.

**7.1 Test circuit and waveform**



## 8. Recommended operating conditions

**Table 4. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.3	-	5.5	V
$V_I$	input voltage		0	-	5.5	V
$I_D$	drain current	pulsed drain output current; $V_{CC} = 5\text{ V}$ ; $T_{amb} = 25\text{ °C}$ ; all outputs on	[1][2]	-	250	mA
$T_{amb}$	ambient temperature		-40	-	+125	°C

[1] Pulse duration  $\leq 100\ \mu\text{s}$  and duty cycle  $\leq 2\%$ .

[2] Technique should limit  $T_j - T_{amb}$  to  $10\text{ °C}$  maximum.

## 9. Static characteristics

**Table 5. Static characteristics**

At recommended operating conditions unless otherwise specified. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = 25\text{ °C}$			Unit
			Min	Typ[1]	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 3.0\text{ V}$ to $5.5\text{ V}$	$0.85V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 3.0\text{ V}$ to $5.5\text{ V}$	-	-	$0.15V_{CC}$	V
$V_{OH}$	HIGH-level output voltage	serial data output Q7S; $V_I = V_{IH}$ or $V_{IL}$ $I_O = -20\ \mu\text{A}$ ; $V_{CC} = 3.0\text{ V}$	2.64	4.49	-	V
		$I_O = -4\text{ mA}$ ; $V_{CC} = 3.0\text{ V}$	2.4	4.2	-	V
$V_{OL}$	LOW-level output voltage	serial data output Q7S; $V_I = V_{IH}$ or $V_{IL}$ $I_O = 20\ \mu\text{A}$ ; $V_{CC} = 3.0\text{ V}$	-	0.005	0.12	V
		$I_O = 4\text{ mA}$ ; $V_{CC} = 3.0\text{ V}$	-	0.3	0.6	V
$I_I$	input leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{CC}$	-	-	1	$\mu\text{A}$
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 1\text{ mA}$	33	37	-	V
$V_{SD}$	source-drain voltage	diode forward voltage; $I_F = 100\text{ mA}$	-	0.85	1.2	V
$I_{CC}$	supply current	logic supply current; $V_{CC} = 5.5\text{ V}$ ; $V_I = V_{CC}$ or GND				
		all outputs off	-	0.004	200	$\mu\text{A}$
		all outputs on [2]	-	0.006	500	$\mu\text{A}$
		all outputs off; SHCP = 5 MHz; $C_L = 30\text{ pF}$ ; see Figure 14 and Figure 16	-	0.75	5	mA
$I_{O(nom)}$	nominal output current	$V_{DS} = 0.5\text{ V}$ ; $T_{amb} = 85\text{ °C}$ ; $I_{out} = I_D$ [3][4][5]	-	140	-	mA
$I_{DSX}$	drain cut-off current	$V_{CC} = 5.5\text{ V}$ ; $V_{DS} = 30\text{ V}$	-	0.002	0.2	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}$ ; $V_{DS} = 30\text{ V}$ ; $T_{amb} = 125\text{ °C}$	-	0.15	0.3	$\mu\text{A}$

**Table 5. Static characteristics ...continued**

At recommended operating conditions unless otherwise specified. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
R <sub>DSon</sub>	drain-source on-state resistance	see <a href="#">Figure 17</a> and <a href="#">Figure 18</a> <sup>[3][4]</sup>				
		V <sub>CC</sub> = 3.0 V; I <sub>D</sub> = 50 mA	-	3.0	11	Ω
		V <sub>CC</sub> = 3.0 V; I <sub>D</sub> = 50 mA; T <sub>amb</sub> = 125 °C		5.4	14	Ω
		V <sub>CC</sub> = 3.0 V; I <sub>D</sub> = 100 mA	-	3.1	12	Ω

- [1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 5.0 V.
- [2] Output currents below 250 mA current limit.
- [3] Technique should limit T<sub>j</sub> – T<sub>amb</sub> to 10 °C maximum.
- [4] These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
- [5] Nominal output current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T<sub>amb</sub> = 85 °C.

## 10. Dynamic characteristics

**Table 6. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); For test circuit, see [Figure 14](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	$\overline{OE}$ to Qn; I <sub>D</sub> = 75 mA; see <a href="#">Figure 10</a> and <a href="#">Figure 19</a>	-	97	-	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	$\overline{OE}$ to Qn; I <sub>D</sub> = 75 mA; see <a href="#">Figure 10</a> and <a href="#">Figure 19</a>	-	9	-	ns
t <sub>r</sub>	rise time	$\overline{OE}$ to Qn; I <sub>D</sub> = 75 mA; see <a href="#">Figure 10</a> and <a href="#">Figure 19</a>	-	60	-	ns
t <sub>f</sub>	fall time	$\overline{OE}$ to Qn; I <sub>D</sub> = 75 mA; see <a href="#">Figure 10</a> and <a href="#">Figure 19</a>	-	18	-	ns
t <sub>pd</sub>	propagation delay	SHCP to Q7S; I <sub>D</sub> = 75 mA; see <a href="#">Figure 11</a> <sup>[2]</sup>	-	5	-	ns
f <sub>max</sub>	maximum frequency	SHCP; I <sub>D</sub> = 75 mA; see <a href="#">Figure 11</a> <sup>[3]</sup>	-	-	10	MHz
t <sub>rr</sub>	reverse recovery time	I <sub>F</sub> = 100 mA; dI/dt = 10 A/μs; see <a href="#">Figure 13</a> <sup>[4][5]</sup>	-	120	-	ns
t <sub>a</sub>	reverse recovery current rise time	I <sub>F</sub> = 100 mA; dI/dt = 10 A/μs; see <a href="#">Figure 13</a> <sup>[4][5]</sup>	-	100	-	ns
t <sub>su</sub>	set-up time	DS to SHCP; see <a href="#">Figure 12</a>	15	-	-	ns
t <sub>h</sub>	hold time	DS to SHCP; see <a href="#">Figure 12</a>	15	-	-	ns
t <sub>W</sub>	pulse width		40	-	-	ns

- [1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 5.0 V.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SHCP → Q7S propagation delay and setup time plus some timing margin.
- [4] Technique should limit T<sub>j</sub> – T<sub>amb</sub> to 10 °C maximum.
- [5] These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.



10.1 Test circuits and waveforms

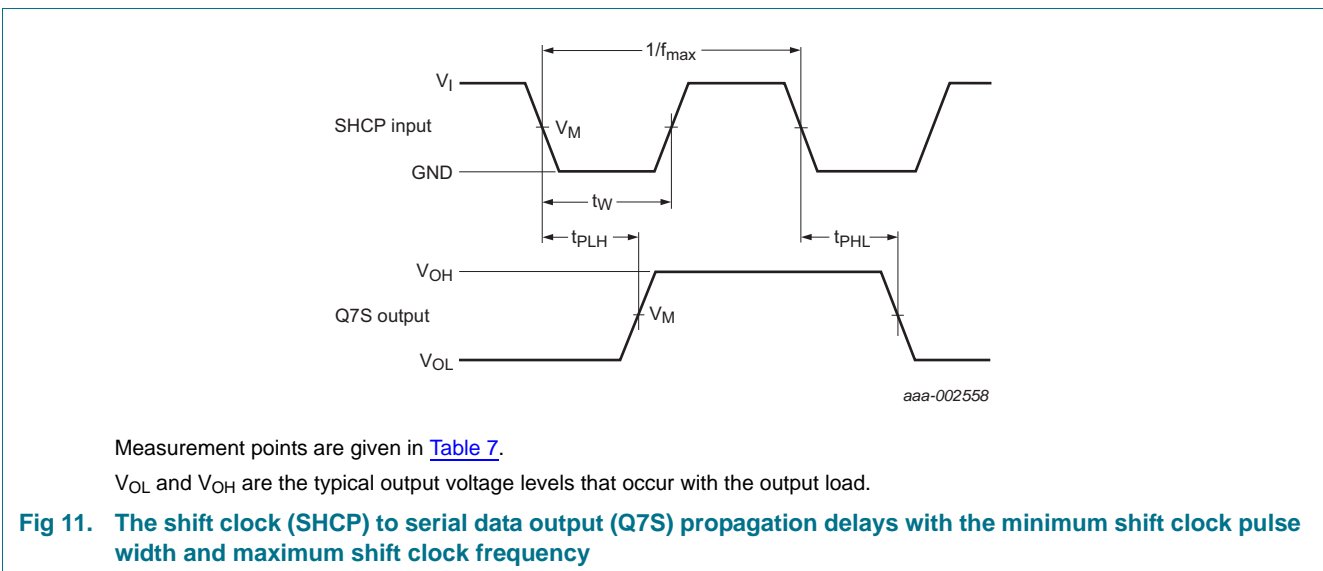
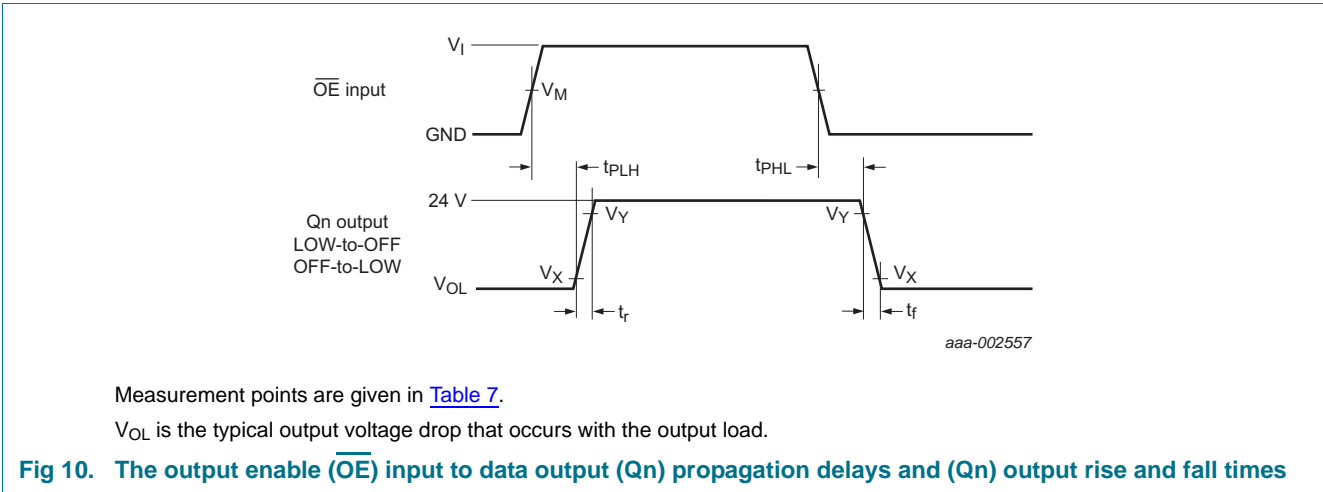
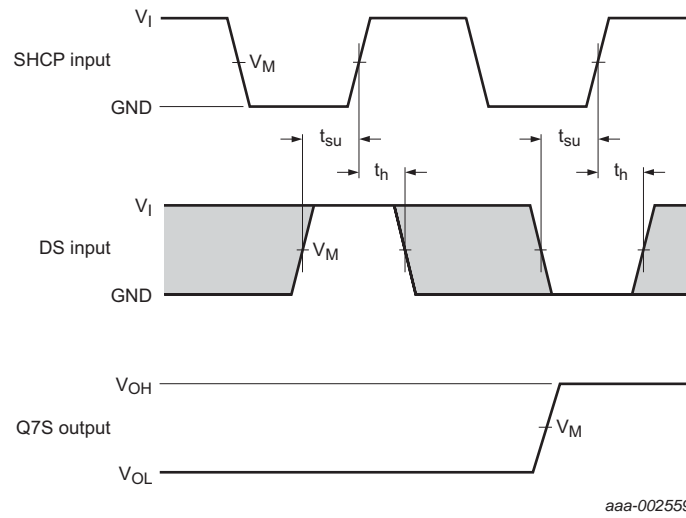


Table 7. Measurement points

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
5 V	$0.5V_{CC}$	$0.5V_{DS}$	$0.1V_{DS}$	$0.9V_{DS}$

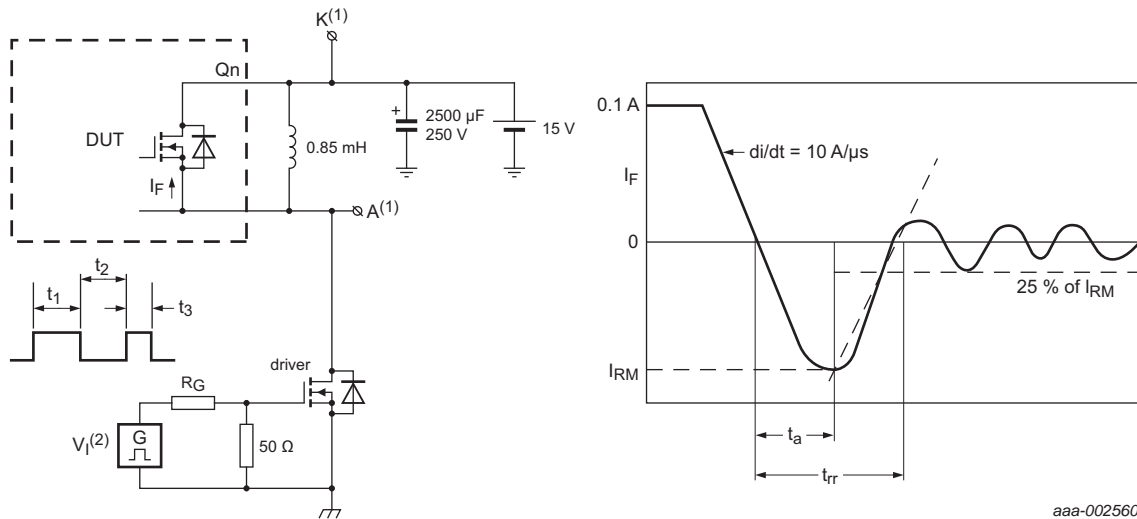


Measurement points are given in [Table 8](#).  
 The shaded areas indicate when the input is permitted to change for predictable output performance.  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

**Fig 12. The data set-up and hold times for the serial data input (DS)**

**Table 8. Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
5 V	$0.5V_{CC}$	$0.5V_{CC}$



- (1) The open-drain Qn terminal under test is connected to testpoint K. All other terminals are connected together and connected to testpoint A.
- (2) The  $V_I$  amplitude and  $R_G$  are adjusted for  $di/dt = 10 \text{ A}/\mu\text{s}$ . A  $V_I$  double-pulse train is used to set  $I_F = 0.1 \text{ A}$ , where  $t_1 = 10 \mu\text{s}$ ,  $t_2 = 7 \mu\text{s}$  and  $t_3 = 3 \mu\text{s}$ .

**Fig 13. Test circuit and waveform for measuring reverse recovery current**

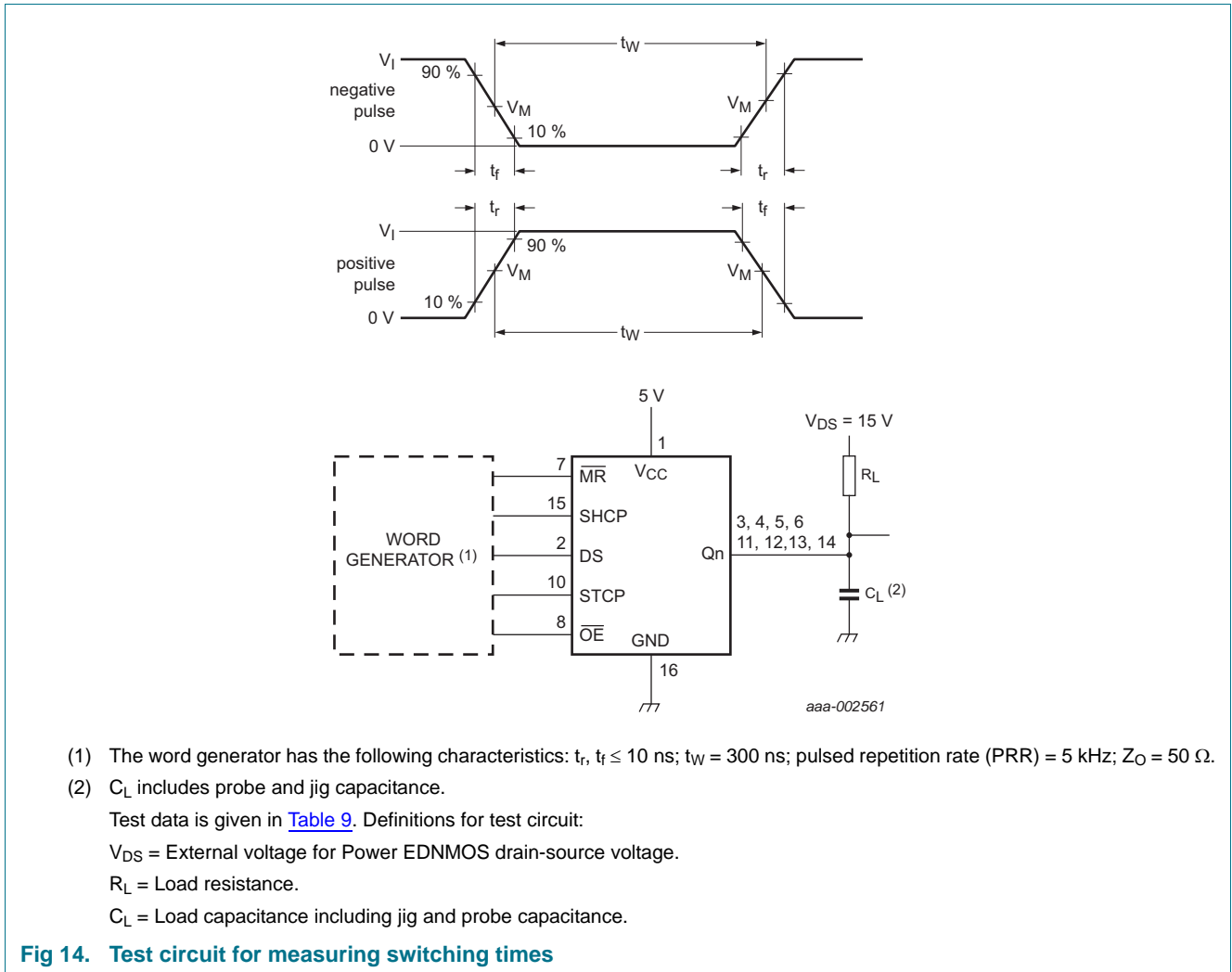
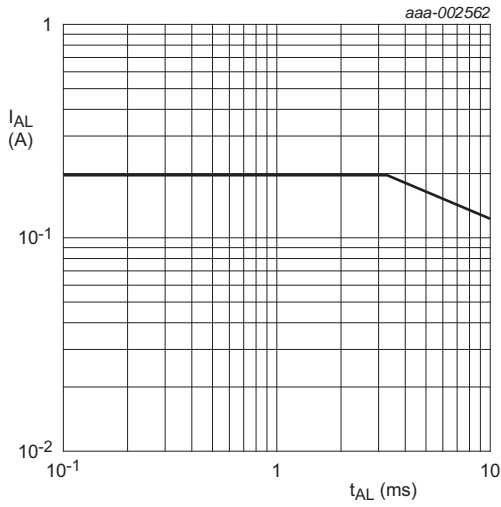


Fig 14. Test circuit for measuring switching times

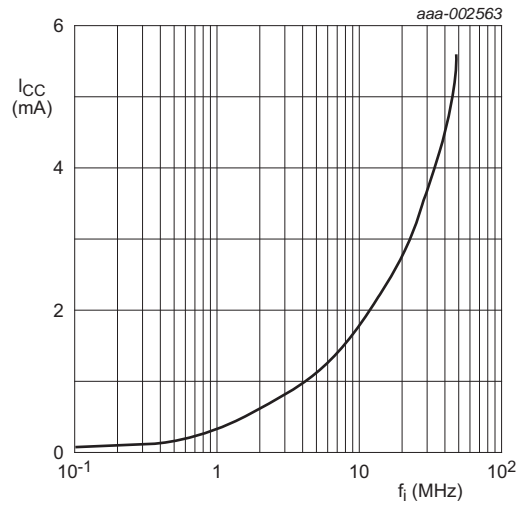
Table 9. Test data

Supply voltage	Input			Load	
	$V_I$	$t_r, t_f$	$V_M$	$C_L$	$R_L$
5 V	5 V	$\leq 10$ ns	50%	30 pF	200 $\Omega$



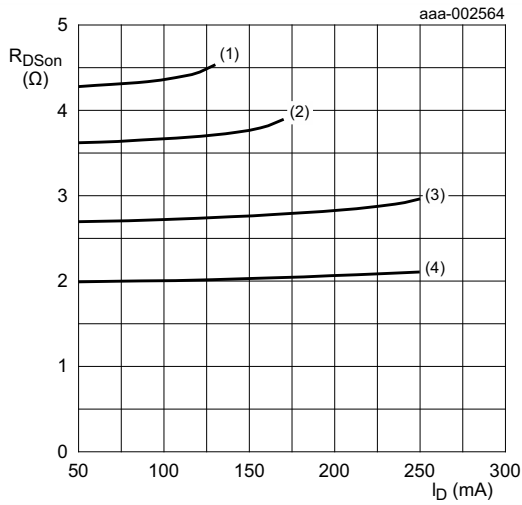
$T_{amb} = 25\text{ }^{\circ}\text{C}$ .

**Fig 15. Avalanche current (peak) versus time duration of avalanche**



$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 5\text{ V}$ .

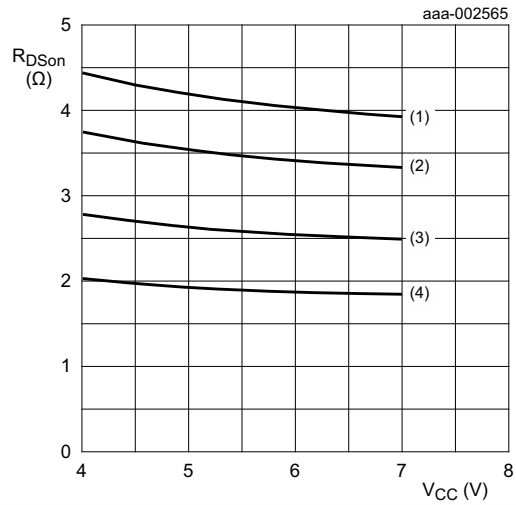
**Fig 16. Supply current versus frequency**



$V_I = V_{CC}$  or GND and  $V_O = \text{GND}$  or  $V_{CC}$ .

- (1)  $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

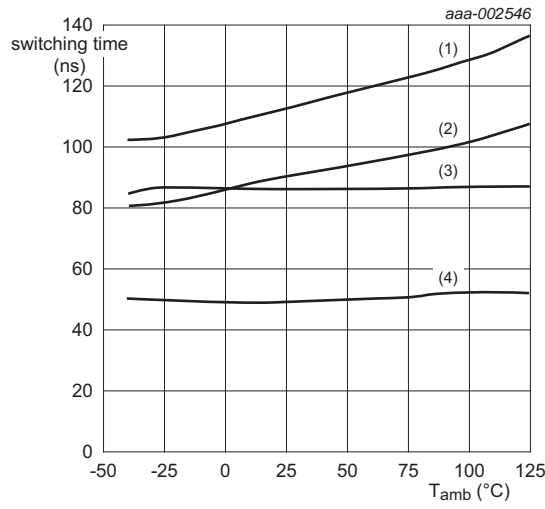
**Fig 17. Drain-source on-state resistance versus drain current**



$V_I = V_{CC}$  or GND and  $V_O = \text{open circuit}$ .

- (1)  $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

**Fig 18. Static drain-source on-state resistance versus supply voltage**



Technique should limit  $T_J - T_C$  to 10 °C maximum.

- (1)  $t_{PLH}$ .
- (2)  $t_r$ .
- (3)  $t_f$ .
- (4)  $t_{PHL}$ .

**Fig 19. Switching time versus case temperature**

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

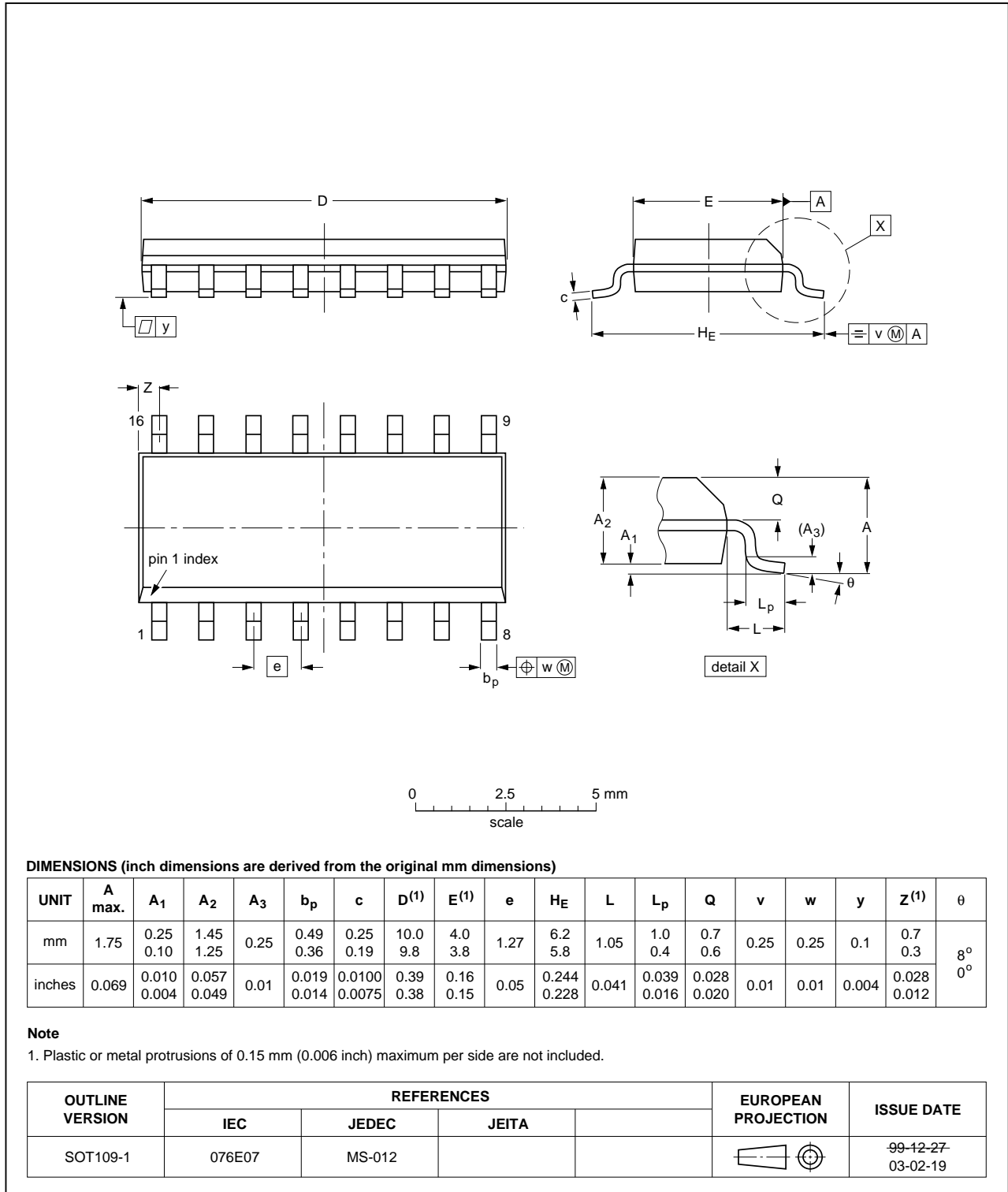


Fig 20. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

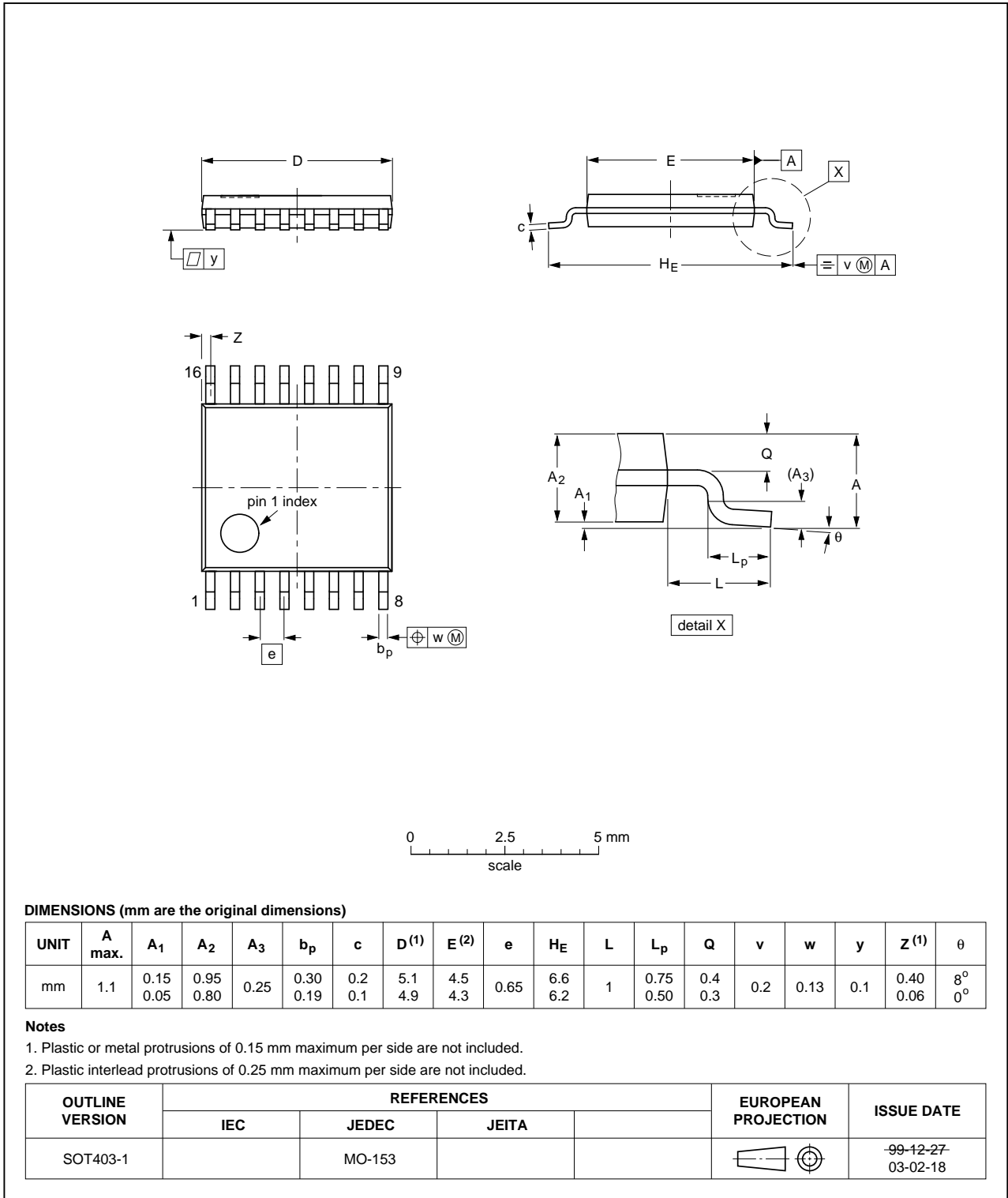


Fig 21. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

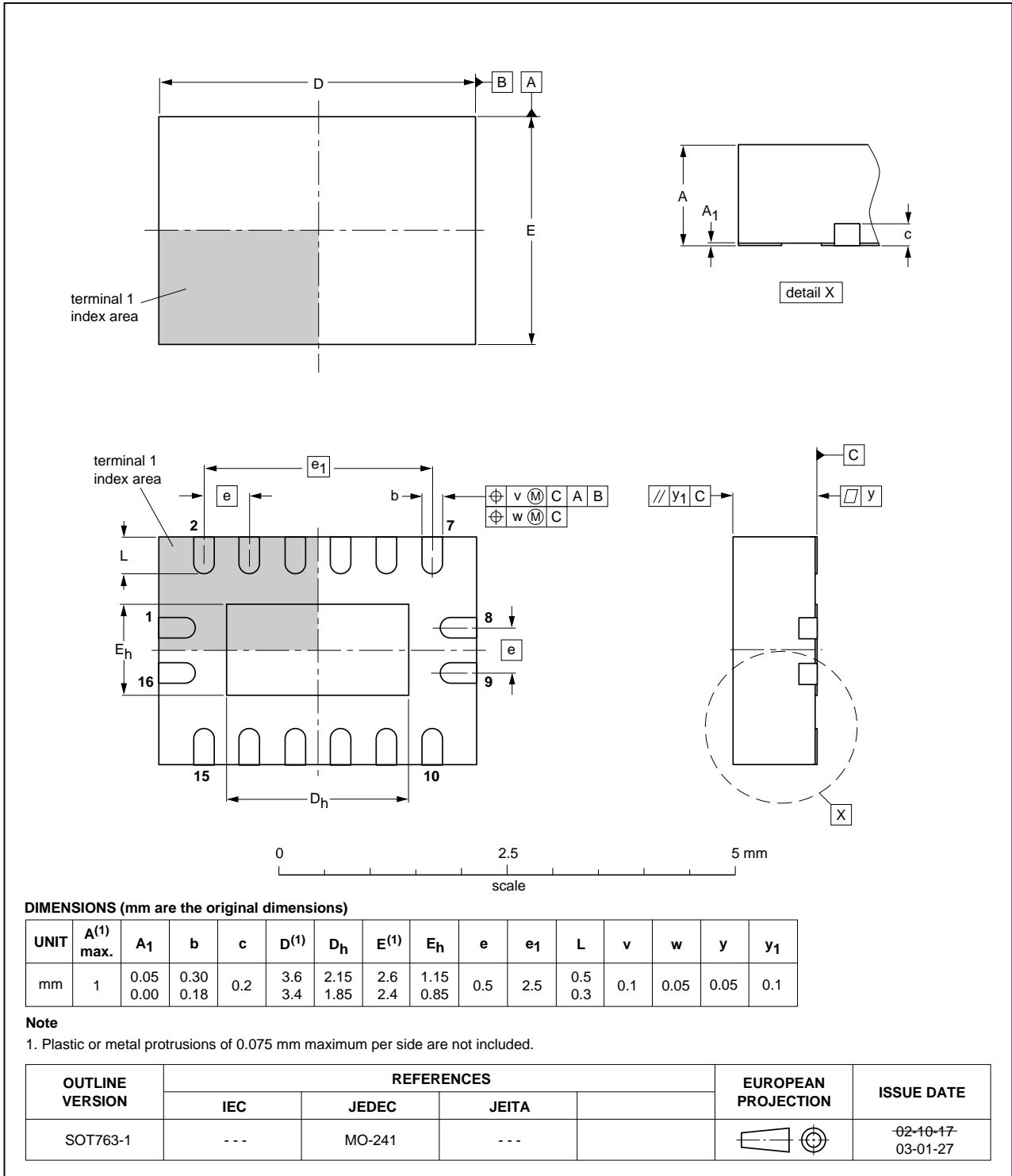


Fig 22. Package outline SOT763-1 (DHVQFN16)



## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
EDNMOS	Extended Drain Negative Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NPIC6C596A_Q100 v.1	20131018	Product data sheet	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 14.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 14.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

#### 14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 15. Contact information

---

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 16. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Applications</b> .....	<b>2</b>
<b>4</b>	<b>Ordering information</b> .....	<b>2</b>
<b>5</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>6</b>	<b>Pinning information</b> .....	<b>4</b>
6.1	Pinning .....	4
6.2	Pin description .....	5
<b>7</b>	<b>Limiting values</b> .....	<b>5</b>
7.1	Test circuit and waveform .....	6
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>7</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>7</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>8</b>
10.1	Test circuits and waveforms .....	9
<b>11</b>	<b>Package outline</b> .....	<b>14</b>
<b>12</b>	<b>Abbreviations</b> .....	<b>17</b>
<b>13</b>	<b>Revision history</b> .....	<b>17</b>
<b>14</b>	<b>Legal information</b> .....	<b>18</b>
14.1	Data sheet status .....	18
14.2	Definitions .....	18
14.3	Disclaimers .....	18
14.4	Trademarks .....	19
<b>15</b>	<b>Contact information</b> .....	<b>19</b>
<b>16</b>	<b>Contents</b> .....	<b>20</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 18 October 2013

Document identifier: NPIC6C596A\_Q100