Features

- Logic Doubling®
  - Bury Either Register or COM While Using the Other for Output
  - Independent Feedback Allows Double Latch Functions per Macrocell
  - Enhanced Routing Resources
  - 5 Product Terms per Macrocell, Expandable up to 40 Product Terms
  - D/T/L Configurable Flip-flops
  - Global and/or per Macrocell Register Control Signals
  - Multiple Global and per Macrocell Clocks
  - Global and/or per Macrocell Output Enable
- EEPROM CPLDs
  - Pin-compatible with Industry-standard Devices
  - Completely Reprogrammable
  - 10,000 Program/Erase Cycles
  - 20-year Data Retention for ATF15xxAS/ASV Devices
  - 10-year Data Retention for ATF15xxBE Devices
  - 2000V ESD Protection
  - 200 mA Latch-up Immunity
  - 100% Tested
- Advanced Features for ATF15xxBE
  - Extremely Low Power
  - Individually-programmable Pin-keeper Option on Inputs and I/Os
  - Individually-programmable Schmitt Trigger Option on Inputs and I/Os
  - Individually-programmable Input and I/O Pull-up Option
  - OTF (On-the-Fly) Configuration Mode
  - DRA (Direct Reconfiguration Access)
  - 2 Independent I/O Banks
- Advanced Features for ATF15xxAS/ASV Devices
  - Input Transition Detection Standby/5 µA typical for “L” Version
  - Pin-controlled Standby Mode
  - Globally Programmable Pin-keeper Inputs and I/Os
  - Per Macrocell Low-power Option
  - Power-up Reset Hysteresis Option

ATF15xx CPLD Family Overview

3614A–PLD–12/05

Description

The Atmel ATF15xx family of Complex Programmable Logic Devices (CPLDs) delivers enhanced functionality and flexibility with no additional design effort. Our superior Logic Doubling® architecture consists of wider fan-in, additional global routing and clock options, and macrocell enhancements that allow PLD designers to pack in more logic, particularly shifters and latches. This dense packing of logic stretches CPLD resources by as much as 200% or more, enabling the use of a smaller device or spare room for revisions.

The newest member of this family – ATF15xxBE – utilizes advance CMOS design techniques to achieve ultra-low power consumption, making it the best choice for power sensitive and battery operated applications. With the new in-system configuration features, many configuration related design challenges can be easily solved.

Factory programming is available, so for old or new designs, prototypes or production, look to Atmel's growing line of pin-compatible CPLDs.

Figure 1. Atmel MacroCell Block Diagram

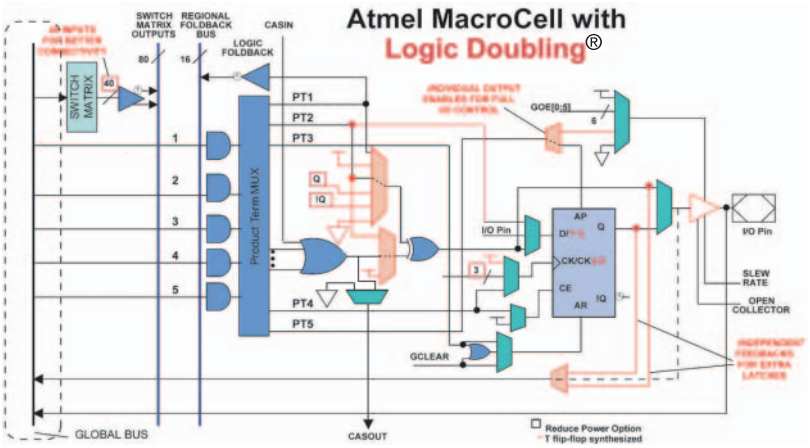

Table 1. ATF15xx CPLD Product Offering

V_{CC} (V)	Device	Macrocells	Speed (ns)	Power
1.8	ATF1502BE	32	5/7	Ultra Low
	ATF1504BE(1)	64	7	Ultra Low
	ATF1508BE(1)	128	7	Ultra Low
	ATF1516BE(1)	256	7	Ultra Low
3.3	ATF1502ASV	32	15/20	Std
	ATF1504ASV/ASVL	64	15/20	Std/Low
	ATF1508ASV/ASVL	128	15/20	Std/Low
5V	ATF1502AS/ASL	32	7/10/15/25	Std/Low
	ATF1504AS/ASL	64	7/10/15/20/25	Std/Low
	ATF1508AS/ASL	128	7/10/15/20/25	Std/Low

Note: 1. Device is not available at press time.