AN-8039

Using the FDDS100H06_F085 in Automotive Systems

Background

Smart high-side switches are a standard building block in today's automotive power distribution and electrical control systems. High and medium current devices with diagnostic features have virtually eliminated fuses and resettable breakers in load management.

In power distribution, single circuits and the associated wiring are protected using smart high-side switches. In body, lighting, and power train; individual loads are driven with smart devices that may include diagnostics using current sensing, and/or fixed parameter diagnostics with status feedback, and/or self-protection features. Autonomous self-protection is almost universal.

Medium Power Load Management

The FDDS100H06_F085 is an AECQ101-grade, smart, high-side switch designed to drive medium power electrical loads and provide diagnostic feedback with a microprocessor-compatible logic level interface. This includes fixed limits for open-load, over-current, and other failure conditions indicated via a status line. There are also autonomous self-protection functions to prevent damage to the device for conditions such as over temperature, shorted load, load dump, and over-voltage.

Overview

Physical Construction

The FDDS100H06_F085 is monolithic (single silicon IC) design, packaged in a 5-lead DPak. The center lead, pin 3, is trimmed and not used to contact the PCB. The TAB is electrically common with pin 3. The package drawing is included in the datasheet.

Table 1. Pin Definitions

Pin #	Name	I/O	Description
1	GND	P	Ground
2	IN	A	Input; activates the power switch in case of logic HIGH
3	VBB	P	Supply voltage; pin 3 and TAB are internally shorted.
4	ST	A	Fault signal feedback LOW on failure
5	OUT	A	Output to loads

Pin Functions

IN - The input pin can be driven with a 3V to 5V logic level output from devices like microcontrollers, provided the V_{OH} output at 3V conforms to the V_{OHmin} > 2.9V as specified for typical HC logic families (*see example V_{OH} minimum for the 74VHC00).*

ST - The status output is an open-drain configuration and requires a pull-up resistor. This allows multiple devices to be wire OR'ed where multiple loads do not require individual diagnostic recognition. Open-load detection can still be accomplished individually by polling of the input and status pins.

The output minimum voltage specified on the status pin relates to the Zener protection diode and is compatible with 3V to 5V logic levels. This should be pulled up to the logic V_{CC} voltage.

VBB – The tab and pin 3 are electrically common; however, pin 3 is a cut lead and not used for electrical connection. Therefore, power for the device must be provided at the tab. The tab pad can also be used with thermal vias and additional PCB radiation area for heat dissipation.

OUT – The output pin is connected to the source of the embedded N-channel MOSFET to source current to the load. The OUT pin is sensed internally for open-load and short-circuit protections.

GND – The ground circuit does not have a large current as it is used only for the internal logic. The ground pin may require added protection for reverse battery, per Section 6.

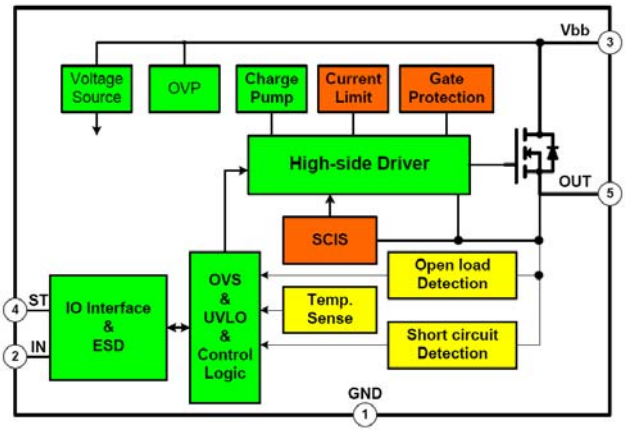


Figure 1. Block Diagram

1. General Applications

1.1. Example Circuit

The FDDS100H06_F085 can be used as a single-load device with individual diagnostics or with combined diagnostic feedback. The device is controlled and monitored via logic signals by a microprocessor, which can provide diagnostic information for user maintenance or service tools. The typical application circuit (*see Figure 2*) is a resistive or inductive load with a steady state current of 0.5A to 3.5A. This includes many types of filaments, LED lamps, and solenoids.

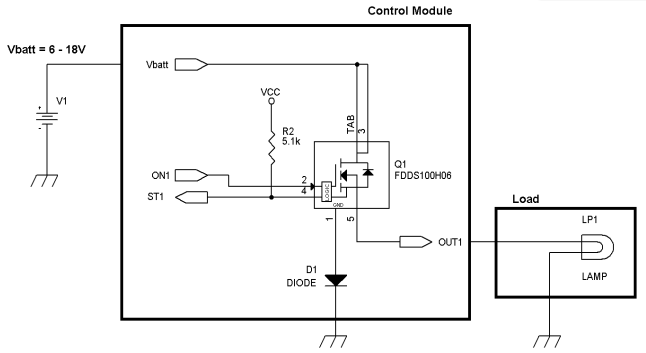


Figure 2. Basic Circuit

1.2. Schematic Design Considerations

IN - The IN pin has a static protection network consisting of a Zener/resistor/Zener network referenced to ground. In the event of an open circuit on the IN pin, the output defaults to OFF due to the fixed current source. No external pull-down is required.

Some design requirements include pin-to-pin short-circuit soft failure (i.e. detected, but isolated failure effect). For the FDDS100H06_F085 and pin-compatible parts, the cut tab pin 3 is V_{BB}. If this is shorted to pin 2, V_{BB} can be applied directly to the output port pin of the control device, normally a micro controller. Unlimited short-circuit current from VBB is normally catastrophic to a micro pin.

The solution is to place a series protection resistor in the IN circuit to limit the current. A 2.2kΩ resistor limits the short-circuit current at 16V into a 5V micro pin structure to:

$$\text{Isht pin} = (16\text{-}5)\text{V} / 2.2\text{k}\Omega \quad (1)$$

$$\text{Isht pin} = 5\text{mA} \quad (2)$$

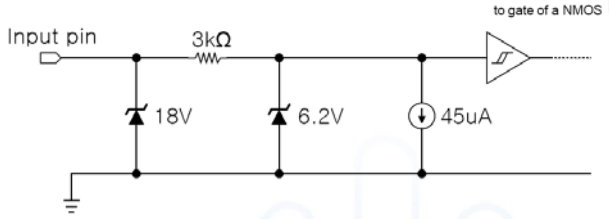


Figure 3. IN Circuit

ST – The same VBB pin to pin short from pin 3 to pin 4 can cause a microcontroller failure; however, a simple series resistor to protect the logic input of a microcontroller can be added to prevent this. Consult the allowed per-pin clamping current of the logic control device.

VBB – VBB should be protected from the noise and fluctuations expected on unregulated vehicle power lines. High-frequency noise should be bypassed using local ceramic capacitors for each device, such as C2 in Figure 4.

Because switching a load and/or lamp inrush can cause dips on VBB, a capacitor to stabilize the supply voltage should be used. A bulk capacitor C1 (*see Figure 4*) may be sized for multiple devices. Please note the topologies in Section 6 on reverse battery. Special consideration may be needed if polarized capacitors are used on VBB.

When driving multiple high-side switches with a single bulk capacitor, turn-on and turn-off of the load channels can be desynchronized to reduce the VBB capacitor size.

OUT – Care should be taken to prevent noise and transients from the adjacent circuits or the external wiring system from coupling onto the output.

Special attention should be given to the device ESD rating of 4kV. To meet standard OEM-type ESD tests on module pins, a small capacitor may be required on the output pin, preferably located near the module connector.

If a pull-up on the output is used, it needs to be reverse-battery protected and powered from a switched power source to minimize ignition OFF current draw.

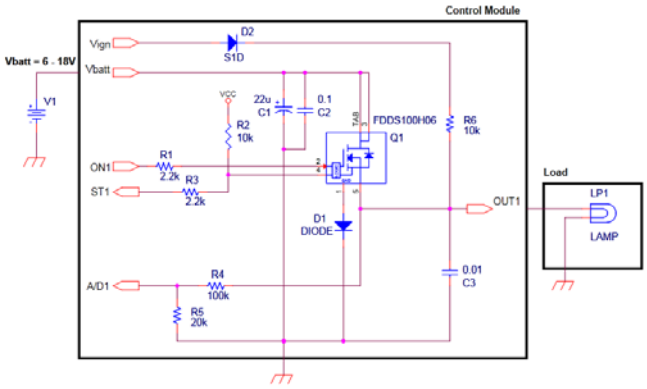


Figure 4. Improved Circuit

1.3. Example PCB Footprint

The minimum footprint recommendations are shown in the datasheet. Additional thermal dissipation using thermal vias and PCB radiation areas are well-established practices for power devices such as load switches. Because the tab is VBB, an electrically common radiation area can be used for multiple devices. Circuit layout patterns and symbols for

PCB Artist (freeware from Advanced Circuits) are available for this device at: www.4pcb.com(1). An extensive library of Fairchild automotive MOSFETs, high-voltage gate drivers, and smart high-side switch components are available as part of the free download. Figure 5 is an example of a thermally enhanced PCB footprint using thermal vias and a bottom-side radiation land pattern.

Note:

1. Fairchild is not responsible for the content of this website.

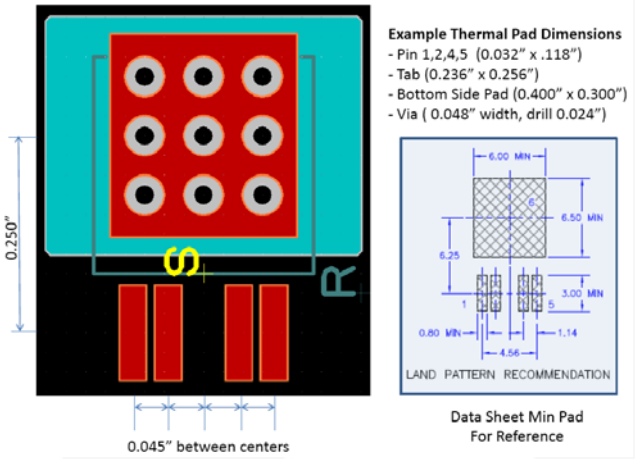


Figure 5. PCB Footprint

2. Load Capability

2.1. Lamp / Resistive Loads

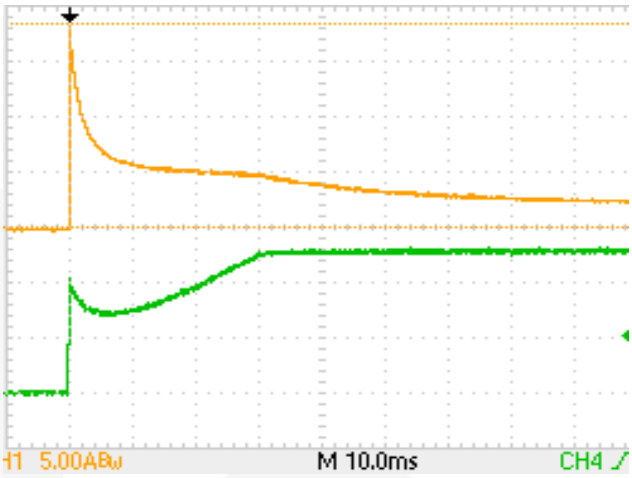
2.1.1. Steady-State Current

Lamp and resistive loads should have a steady-state current between 0.5A and 3.5A to allow open-load detection and to avoid setting the short-circuit current limit. When driving LED-based lamps, a parasitic load can be added to the lamp assembly to achieve the minimum current.

2.1.2. Filament-Type Inrush

The short-circuit delay time, $t_{d(SC)}$ is typically 250µs. This allows a short inrush for filament-type lamps. Generally, the FDDS100H06_F085 is capable of driving 10W filament bulbs at a device temperature of 85°C with V_{BB} = 16V. Cold filament temperatures increase the inrush current and should be reviewed as part of the system design process. To accommodate high inrush, multiple retries on turn-on can be used to "warm" the filament.

Figure 6 shows a typical inrush event at 25°C for the STOP filament of a type-1157 dual-filament (stop/tail) bulb.

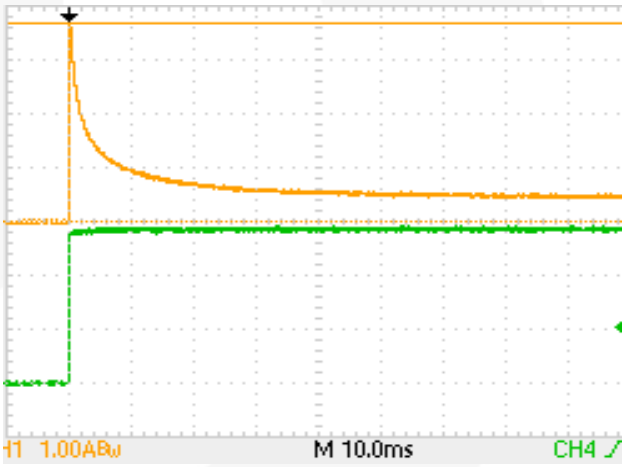


Lamp Current – 5A per/div Applied V_{BB} – 5V per/div

Figure 6. 1157 STOP Filament Inrush

Note the droop on V_{BB} in this example is due to limiting in the power supply source.

Figure 7 shows a typical inrush event at 25°C for the TAIL filament of a type-1157 dual filament (stop/tail) bulb.



Lamp Current – 1A per/div Applied V_{BB} – 5V per/div

Figure 7. 1157 TAIL Filament Inrush

2.2. Inductive / Solenoid Loads

The FDDS100H06_F085 can drive solenoid / inductive loads with a nominal resistance of >4Ω in 12V systems and >8Ω in 24V systems.

2.2.1. Inductive Voltage Clamp Level

The inductive clamp voltage $V_{ON(cl)}$ is referenced from the output to VBB. When driving a grounded load, the negative voltage that the output is clamped to:

$$V_{OUT(cl)} = V_{BB} - V_{ON(cl)} \quad (3)$$

As V_{BB} increases, the ON current in the inductive load increases, lengthening the clamp time (*see Section 2.2.2*) and the Unsuppressed Inductive Spike (UIS) energy. Figure 8 shows V_{OUT} versus V_{BB}, where $V_{ON(cl)} = (V_{BB}-V_{OUT})$ *(refer to Appendix 1)*.

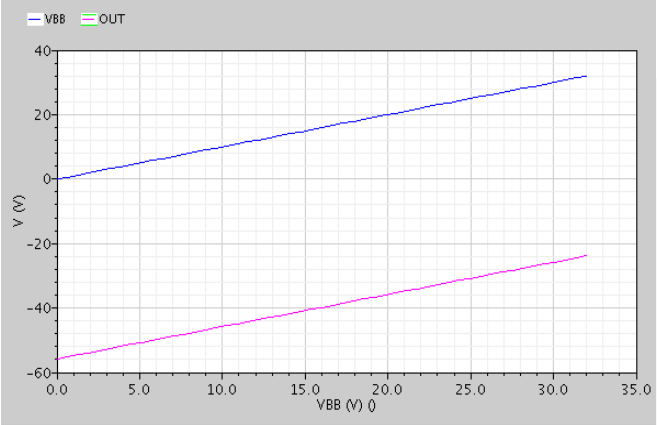


Figure 8. V_{OUT} vs. V_{BB}

2.2.2. Clamp (t_{cl} – Inductive Load)

The active clamp voltage is less than the device avalanche breakdown. In MOSFETs, the time in avalanche is referred to as t_{av}. This is similar to the time in clamp (t_{cl}) for the smart high-side switch.

Table 2. Common Equivalent Terms

Smart Switch	MOSFETS
t_{cl}	t_{av}
Clamp	Avalanche
$V_{ON}(cl)$	BVD_{SS}
V_{OUT}	V_{drain}

Figure 9 and Figure 10 show a constant $V_{ON(cl)}$ for V_{BB} =12V (I_{lpeak} = 1A) and V_{BB} = 30V (I_{lpeak} = 2.4A), respectively, driving the same inductive load.

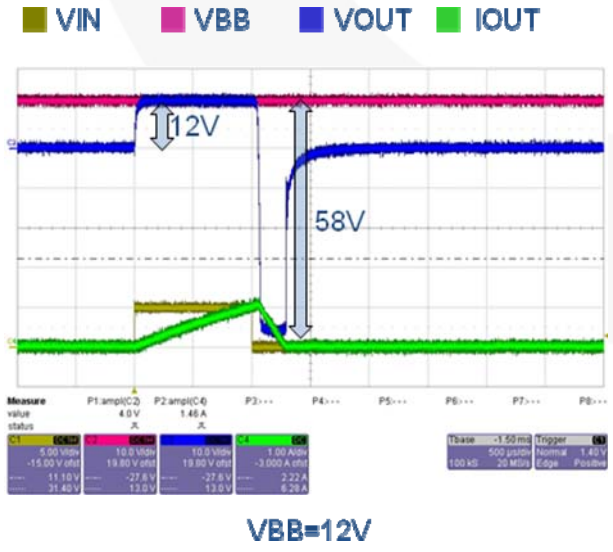


Figure 9. V_{OUT} and I_{OUT} at V_{BB} = 12V

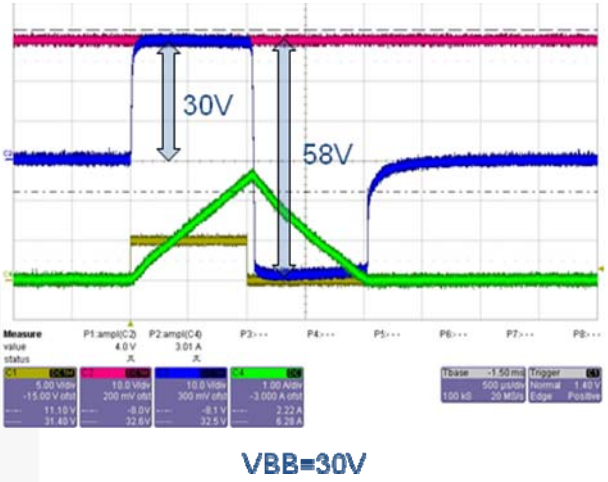


Figure 10. V_{OUT} and I_{OUT} at V_{BB} = 30V

When the output is turned OFF and the device is in a clamp condition, the current loop is the same as in the ON condition; that is, the source of the clamping current is from V_{BB}, flowing through the inductor to ground.

The Il_{peak} at turn off, and thus the stored energy being greater for V_{BB} = 30V than for V_{BB} =12V, causes a longer clamp time. The datasheet limits of $V_{ON(cl)}$ are listed at a test current of 40mA over the full temperature range. Of interest for UIS capability, in Section 2.2.3 are the values of the peak inductor current at 150°C. Table 3 shows estimated $V_{ON(cl)}$ values of interest.

Table 3. $V_{ON(cl)}$ vs. Temperature

T_J	I_{cl}	$V_{ON(cl)}$		
Deg °C	Amps	Min. (V)	Typ.(V)	Max. (V)
-40	0.04	50.0	56.3	62.7
25	0.04	50.3	56.6	63.0
150	0.04	52.3	58.9	63.8
150	2.80	56.0	60.5	65.5

The time for the energy in the inductor to discharge across the device (time in clamp) is calculated as:

$$t_{cl} = L/R \bullet \ln[(I_{pk} \bullet R) / (V_{ON(cl)} - V_{BB}) +1] \quad (4)$$

where R is the series resistance of the inductor inclusive of parasitic current paths, such as PCB traces and wiring.

2.2.3. Inductive Transient Energy (UIS)

The energy stored in the inductor is dissipated across the device for time t_{cl}. This can be approximated as:

$$E_{as} = [\tfrac{1}{2} \bullet I_{pk} \bullet L/R \bullet V_{ON(cl)}] \bullet \ln[I_{pk} \bullet R/(V_{ON(cl)}-V_{BB}) + 1] \quad (5)$$

or, by substituting Equation 4 for t_{cl}:

$$E_{as} = \tfrac{1}{2} \bullet t_{cl} \bullet I_{pk} \bullet V_{ON(cl)} \quad (6)$$

The energy stored in the inductor is calculated as:

$$E_{tot} = ½ \bullet I\text{^}2 \bullet L \quad (7)$$

The voltage source, V_{BB}, is in the current loop during a UIS event, thus the E_{as} energy can be greater than the total energy stored in the inductor for low R values.

2.2.4. Repetitive UIS

Referring to AN-7515 on multiple or repetitive UIS, the same approach can be used for the FDDS100H06_F085 as for a discrete MOSFET. This analysis sums the total thermal load for conduction, switching, and repetitive UIS power to determine the maximum die temperature. Then, the "last pulse" analysis is used to determine if the device operates safely based on the single-pulse UIS rating. In the below example, it is determined that the repetitive conduction, switching, and repetitive UIS losses create a maximum die temperature of 150°C or less.

The final UIS event can then be plotted on the single-pulse UIS curve (I_{MAX} and t_{cl}). This example last event falls within the UIS single-event capability.

EXAMPLE:

The load parameters are R=5Ω, L=30.0mH, with an I_{pk}=3.2A (at V_{BB}=16V). $V_{ON}(cl)_{min}$ at 150°C (~56V) is used to give the largest t_{cl} value. The clamp time is calculated as:

$$t_{cl} = L/R \bullet \ln[(I_{pk} \bullet R) / (V_{ON(cl)} - V_{BB}) +1] \quad (8)$$

$$t_{cl} = 30m/5 \bullet \ln[(3.2 \bullet 5) / (56 – 16) +1] \quad (9)$$

$$t_{cl} = 2.02ms \quad (10)$$

Using the peak current, this point is plotted on the UIS curve (in purple in Figure 11) and falls below the device rating curve for a single pulse below 150°C.

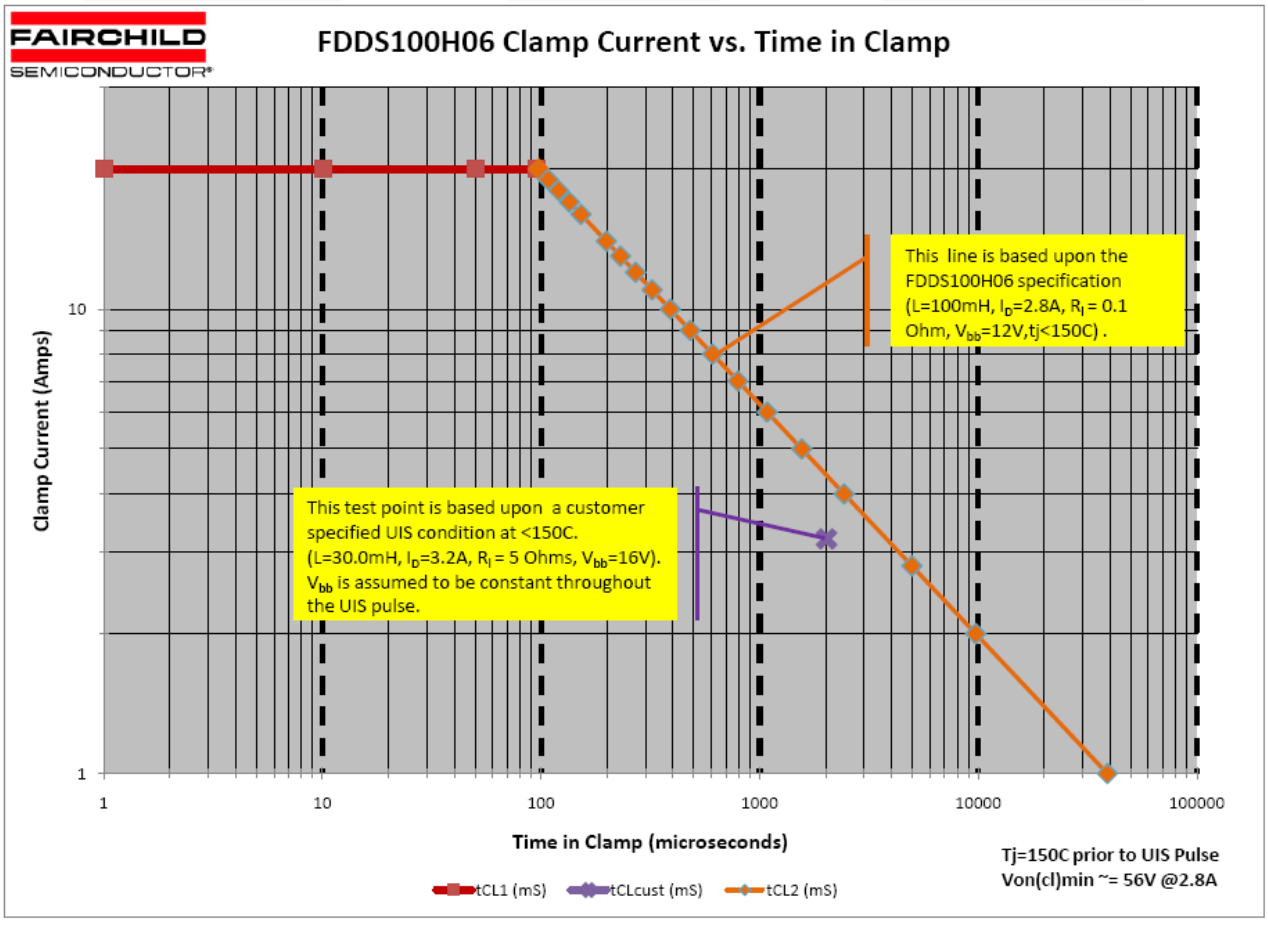


Figure 11. Clamp Current vs. t_{cl}

Note:

2. The red horizontal section of the t_{cl} plot is limited by the maximum device current.

2.2.5. Total Average Power Dissipation

In calculating device thermal rise prior to the last E_{as} event, the repetitive E_{ar} is assumed to be the same as E_{as}.

The E_{ar} can be calculated as:

$$E_{ar} = ½ \bullet t_{cl} \bullet I_{pk} \bullet V_{ON(cl)} \quad (11)$$

$$E_{ar} = ½ \bullet 2.21ms \bullet 3.2A \bullet 52V \quad (12)$$

$$E_{ar} = 185mJ \quad (13)$$

The inductor stored energy in the Section 2.2.4 example is:

$$E_L = ½ \bullet I\text{^}2 \bullet L \quad (14)$$

$$E_L = ½ \bullet (3.2A)^2 \bullet 30mH \quad (15)$$

$$E_L = 154mJ \quad (16)$$

Note:

3. The total inductor stored energy is less than the E_{ar} energy. Multiplying the E_{ar} value by the repetition rate provides a power level due to E_{ar}.

For f_{ar} = 5Hz:

$$P_{ar} = 154mJ \bullet 5Hz \quad (17)$$

$$P_{ar} = 0.77W \quad (18)$$

Total average power dissipation is the sum of conduction losses, switching losses, and repetitive E_{ar} losses:

$$P_{total} = P_{ar} + P_{cond} + P_{switching} \quad (19)$$

3. OFF-State Performance

3.1. Output Leakage and I_{BBOFF}

Ignition OFF current draw is a key design concern for systems that support continuously available power for "wake-up" or reserved auxiliary power functions. Examples are interior lighting, stop lamp, and E-flasher illumination that must function when ignition is off.

The output leakage into the load is the major source of I_{BB} current draw when the output is OFF at normal temperatures. In addition to output leakage across the MOSFET, I_{BBOFF} consists of leakage current draw from the IC. Generally:

- The IC portion of leakage decreases for increasing temperature;
- The MOSFET portion of the leakage increases with increasing temperature; and
- Except for high temperature, I_{BBOFF} is constant over supply voltages up to 37V.

They nominal I_{BBOFF} characteristics are shown in Figure 12 for -40°C, 25°C, and 150°C.

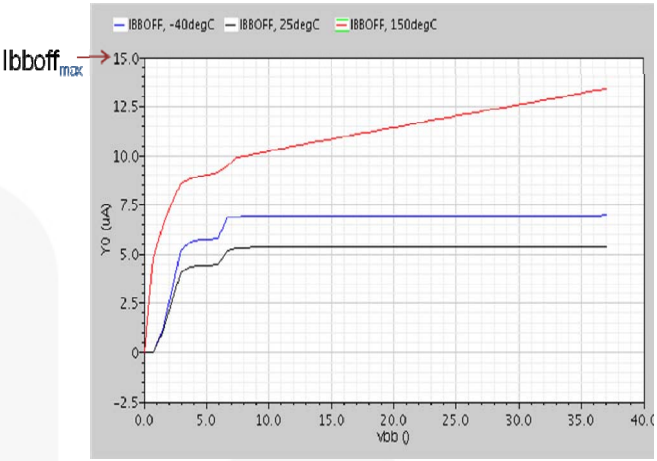


Figure 12. Tri-Temperature I_{BB0FF} vs. V_{BB}

Note:

4. $Ibboff_{max}$ over the full temperature range is 15µA.

3.2. Input and Status Pin Leakage

3.2.1. Input

The IN pin is high impedance. In the LOW state, the pin current is negligible (<1µA).

3.2.2. Status

The ST pin is an open-drain output (*refer to Section 5.6*). Under normal operating conditions, this is HIGH, assuming an external pull-up resistor is present. The leakage into the ST pin in the OFF state is negligible (<1µA).

4. Diagnostic Capability

The basic diagnostic functions when the under-voltage and over-voltage are not valid are summarized in Table 4. The short-circuit and over-current functions (V_{DSON} > 4V) are dependent on $t_{d(SC)}$.

Table 4. Diagnostic Summary

	Within t_{dsc}	After t_{dsc}
Thermal Shutdown	Shutdown	Shutdown
Under-Voltage	Shutdown	Shutdown
Over-Voltage	Shutdown	Shutdown
V_{DSON} >4V	Current Limit	Shutdown by V_{DSON} Detection >4V

4.1. Open-Load When ON

For resistive loads such as solenoids and filament type bulbs, per the open-load portion of Table 5, Line 2 and the specification limit $I_{L(oL)max}$; open-load detection during the ON state requires a minimum current of 400mA to ensure proper diagnostic status feedback (ST). A load current of

less than 20mA, $I_{L(oL)min}$ is assured to cause a LOW output on the ST pin.

Table 5. Truth Table

Sense Current Fault Conditions	State	Input Level	Output Level	Status Pin
Normal Operation $I_{OUT} > I_{L(OL)MAX}$	OFF	LOW	LOW	HIGH
	ON	HIGH	HIGH	HIGH
Open Load $I_{OUT} < I_{L(OL)MIN}$	OFF	LOW	X	X
	ON	HIGH	HIGH	LOW

Note:
5. X=indeterminate; don't care.

There are two open-load delay times (*see Table 6*).

- The initial open-load $t_{d(ST)}$ is typically 380µs. This delay is from the instant the IN pin is changed from LOW to HIGH and when the ST indicates an open-load condition. Note that $t_{d(ST)max}$ = 750µs.
- The open-load detection time, when the device is in the ON state, is $t_{d(ON\_OL)}$, as shown in Table 6. This is a maximum of 90µs. This delay is the same when an open load becomes valid when ON, i.e. $t_{d(ON\_Nor)}$ is also 90µs maximum.

Table 6. Open-Load Status Pin Timing

Open-Load Status Pin Timing		T_J= -40~150°C	Min.	Typ.	Max.
Input Open-Load Delay	$t_{D(ST)}$		80	380	750
Delay for Status while On (with Open Load)	$t_{D(ON\_OL)}$	Normal → Open-Load	10	30	90
	$t_{D(ON\_NOR)}$	Open-Load → Normal	10	30	90

4.2. Open-Load When OFF

Referring to Table 5; to detect open loads in the OFF State, a pull-up resistor (R_{diag}) must be placed on the output. An A/D channel can read the voltage level of the output to provide open-load detection using a set voltage threshold. R_{diag} should be powered from a switched power source, with reverse battery protection, to minimize ignition OFF current draw and leakage paths, as shown in Figure 13.

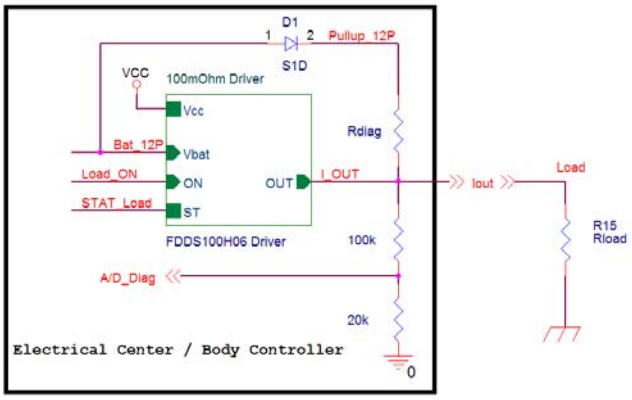


Figure 13. Open-Load in OFF Configuration

4.3. Applications with LEDs

4.3.1. Resistor / Diode or Local Current Regulation Open Load Detection

The simplest form of LED lighting uses a series resistor to regulate the current at nominal DC voltage. Optionally, diodes are used to provide reverse protection and 'or'ing for multifunction, such as combined STOP/TAIL. More complex schemes may include current regulation blocks in series with the LED strings. Both are compatible with the FDDS100H06_F085 open-load detection.

ON State - In some cases, a parasitic resistive load (R_{open}) may be required at the LED to ensure a minimum current draw at minimum battery voltage.

OFF State – To detect open loads in OFF state, the technique in Section 5.2 is used; adding a pull-up resistor (R_{diag}) on the output and employing an A/D channel. For LEDs, this also requires the parasitic resistor to ground (R_{open}) to bring the voltage to ground when the load is connected normally. R_{open} overcomes the large voltage drop across the LED diodes in series *(see Figure 14)*.

4.3.2. Open Load of LEDs with PWM

PWM is often used to provide varying degrees of luminance in both bulbs and LEDs for backlight dimming or combined STOP/TAIL. In combination STOP/TAIL lamps, the TAIL function is achieved by a PWM of 15 to 20%. To detect an open load in ON state, the minimum PWM "on" portion must be longer than $t_{d(ST)}$ maximum, specified at 750µs. For example, if 200Hz (5ms period) is used for the PWM frequency, the minimum allowable duty cycle with open-load detection would be:

$$PWM_{min} = t_{d(ST)} \bullet f \bullet 100\ (\%) \quad (20)$$

or

$$PWM_{min} = 15\% \quad (21)$$

Assuming the status output, ST, is read synchronously with the PWM input signal after $t_{d(ST)}$ has elapsed. One method is to read the ST output signal prior to changing the IN signal from HIGH to LOW within the PWM interrupt routine.

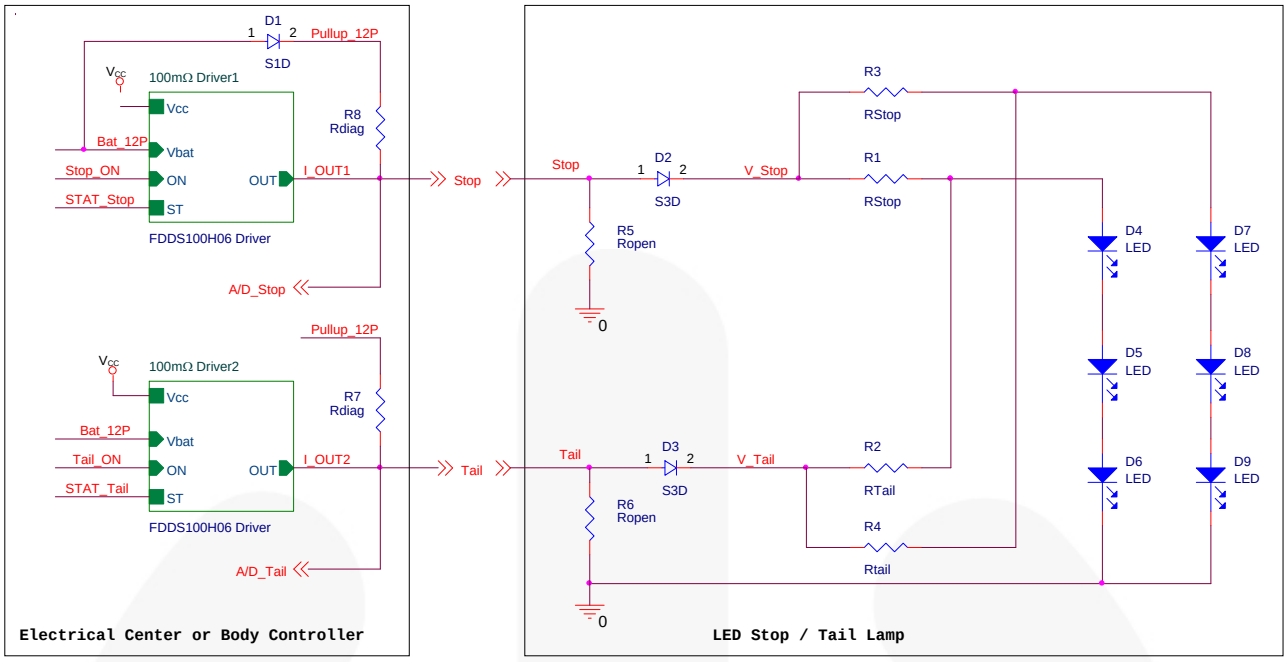


Figure 14. Resistor / Diode LED Typical Configuration

4.3.3. Short Circuit to Ground

During the initial turn-on period, $t_{d(SC)}$, the over-current function is active (*see Section 4.5*). After $t_{d(SC)}$, if the FDDS100H06_F085 is in ON state and the output voltage is less than $V_{ON(sc)}$; the output is turned off. This is indicated on the ST pin as a fault condition. This is a latched function and requires cycling the input (IN pin) to turn the output back on if the short is removed. $V_{ON(sc)}$ is nominally 4V when V_{BB} > 7V. The internal reference for short to ground decreases linearly with V_{BB} below 7V. Figure 15 shows the typical $V_{ON(sc)}$ vs. V_{BB}.

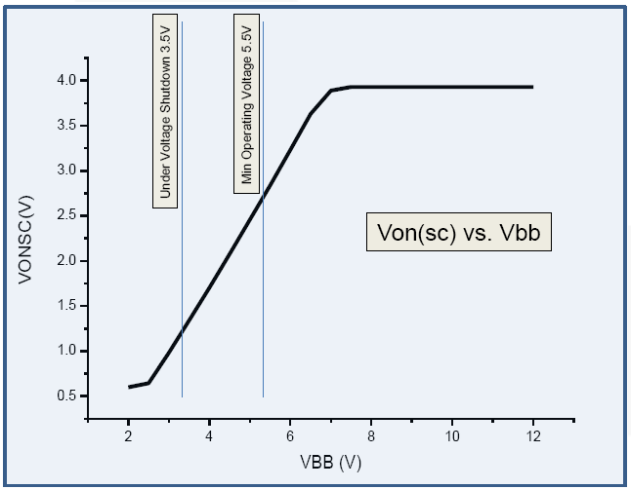


Figure 15. V_{ON}(sc) vs. V_{BB} at Low Voltage

4.4. Over-Current

During the initial $t_{d(SC)}$, when the device is switched to the ON state (IN = 1); the output current is limited to $I_{l(SCP)}$. The complete conditions where $I_{l(SCP)}$ is active are:

- $V_{OUT} > V_{ON(sc)}$; where ($V_{ON(sc)nom}$ = 4V), no short on output
- t_{ON} (time elapsed after IN is triggered from LOW to HIGH) < $t_{d(SC)}$
- T_J (junction temperature) <T_{SD} (thermal shutdown temperature)
- $V_{BB} > V_{BB(u);}$ under-voltage not valid
- $V_{BB} < V_{BB(sd)}$; over-voltage not valid

This is indicated on the ST pin as a fault condition. This is not a latched function. The $I_{L(SCP)}$ limit is a minimum of 4A at 150°C. This value increases as temperature decreases, allowing larger inrush currents at low temperatures.

4.5. Short Circuit to VBB

Refer to the Table 5 and the condition listed as open load in the ON state. A short to VBB is generally not detected by the internal logic. When a hard short to VBB is present, as shown in Figure 16, it is much less than the R_{dson}. Current through the short-circuit path flows to the load, bypassing the MOSFET. A hard short to VBB may be detected in the ON condition by the $I_{L(ol)}$ limit as an open-load condition, setting ST to LOW state. For a nominal R_{dson} of 80mΩ, this requires a short to VBB of 1mΩ to 21mΩ [$I_{l(ol)}$ 20 to 480mA] at 14V.

Generally, a short to VBB is best accomplished externally in combination with open-load detection in the OFF state, as shown in Section 4.2, using an A/D channel.

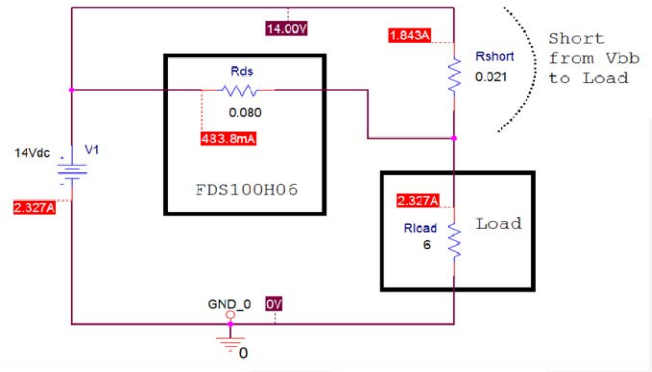


Figure 16. Hard Short to VBB

4.6. Under-Voltage

An under-voltage condition turns off the output and disables the charge pump per the limits of $V_{BB(u)}$ of the datasheet. There is a nominal 0.7V hysteresis in the under-voltage limit. If the IN pin is HIGH and V_{BB} returns to a value greater than $V_{BB(u\ rst)}$, the IN pin must be cycled to restart the output. For the output to turn on, the applied voltage must increase above $V_{BB(ucp)}$, which is the voltage at which the charge pump is activated. The typical values for $V_{BB(u)}$ and $V_{BB(u\ rst)}$ over-temperature are shown in Figure 17.

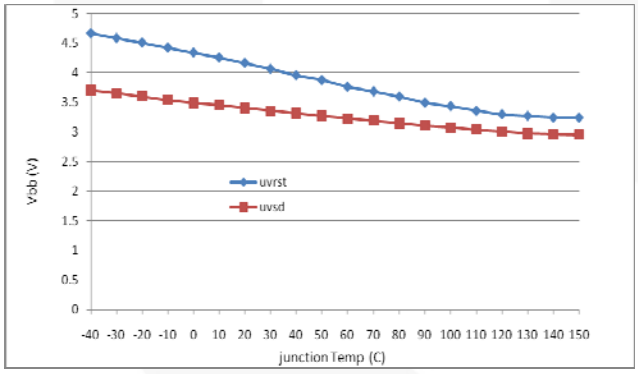


Figure 17. $V_{BB(u)}$ and $V_{BB(urst)}$ vs. Temperature

The ST pin remains HIGH during an under-voltage event. *Refer to timing figures of the datasheet for the ST response to under-voltage.*

Ideally, the under-voltage limit of the device is a secondary means of disabling the load. Monitoring V_{BB} by the user system and providing a soft shutdown below the $V_{BB(ON)min}$ of 5.5V minimum operating range is preferred.

4.7. Multiple Devices with Wired-OR Status Lines

The status line can be connected to multiple devices in a wired-OR configuration to reduce I/O pin count. This is useful where diagnosis of multiple loads can be accomplished by polling or if separate diagnosis is not required.

An example would be a tail lamp with two separately driven bulbs, where either one being open would be indicated as a single diagnostic error. In the case of a shorted load during the ON time, polling can be used to determine which channel should be disabled.

5. Autonomous Protection Features

The FDDS100H06_F085 is designed for 12V and 24V systems. The maximum recommended operating V_{BB} is 34V for full device protection.

5.1. Thermal Shutdown

Thermal shutdown occurs typically at $t_{(jt)}$ = 170°C. Repetitively cycling the part in and out of thermal shutdown is not recommended. *Refer to the timing figures of the device datasheet for thermal shutdown and the ST and output response versus IN.*

The IN pin does not have to be cycled to restore the output state after a thermal shutdown. By design, there is an approximate 10°C hysteresis on thermal shutdown recovery.

5.2. Over-Voltage Shutdown and Protection Limits

If the IN pin is HIGH, the over-voltage detection turns the output to the OFF state per the $V_{BB(SD)}$ limit. The output remains OFF unless the VBB pin surpasses the $V_{BB(AZ)}$ limit; at which point, the avalanche threshold across the output is reached.

After the over-voltage limit $V_{BB(SD)}$ is exceeded, V_{BB} must decrease to below the $V_{BB(RS)}$ limit to reactivate the device. The IN pin does not have to be cycled after over-voltage for the output to be restored.

Refer to the timing figures of the datasheet for the output voltage versus V_{BB} response for over-voltage events with the IN pin OFF and ON.

By design: $V_{BB(RS)} < V_{BB(SD)} < V_{BB(AZ)}$

6. Reverse Battery

The strategy for reverse battery depends on the nature of the load and the application electrical architecture. There are three common conditions: 1) The load can operate under reverse battery, such as a filament lamp or mirror heater element, without damage to the component or the controls. 2) The load is self protected against reverse battery, as in an LED lamp with series rectifiers. 3) The load requires reverse-battery protection as part of the controls to prevent damage or unacceptable behavior.

6.1. With Negative Load Current Allowed During Reverse Battery

6.1.1. Diode and Resistor Options on GND Pin

For details on reverse protection of the IC, refer to AN-9739 — Reverse Battery Protection of Smart Switches.

The FDDS100H06_F085 datasheet shows two options for protection of the IC; using a resistor of 150Ω or a diode in the ground pin. These two options are shown in Figure 18.

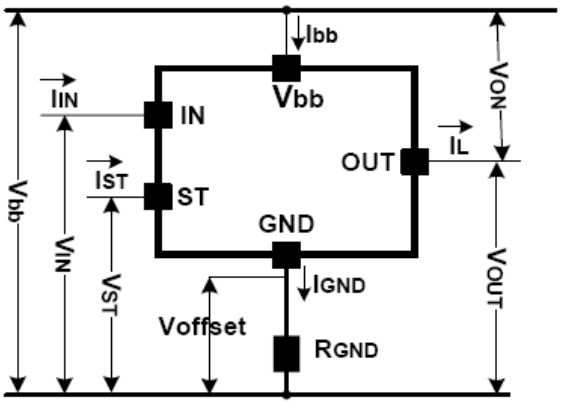
6.1.2. Diode and Resistor Thermal Implications

Allowing load conduction in the reverse-battery condition has thermal implications. Experimental data taken of the resistor versus the diode configuration is shown in Table 7 using a test PCB. This shows the temperature measured at the center of the top surface of the package at the conditions listed. Note that using the resistor option also has greater heating in the resistor itself.

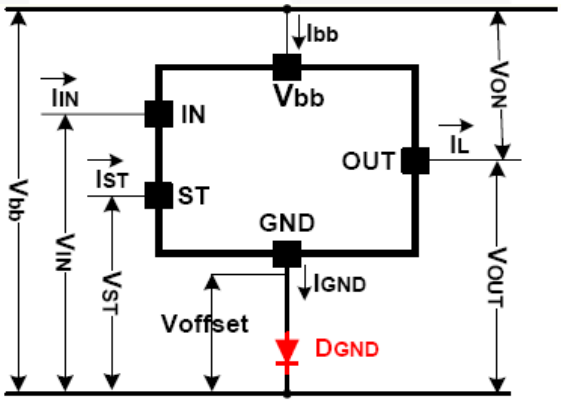
Table 7. Device Thermal Rise in Reverse Battery

Conditions	Measured Temperature at Center of IC	
	Resistor	Diode
V_{BATT} = -18V, T_A=25°C Electronic Load = 1.5A, Measured Time > 20 Minutes	81.0°C	56.2°C

Tradeoffs for the two configurations are summarized in Figure 18. Note that the diode adds a ground shift in the normal operating condition that changes IN pin thresholds. This is generally acceptable for V_{CC} = 5V logic; however, addition of the diode may come close to the guaranteed limits for logic HIGH with V_{CC} =3.3V logic.



Type	Advantage	Disadvantage
1. Limiting current through control IC 2. Current through main body diode	Low Voffset (Maximum 0.3V @2mA)	Large size resistor More than 0.5W



Type	Advantage	Disadvantage
1. Blocking current through Control IC 2. Current through main body diode	Small diode size Safer than figure #4	slightly expensive High Voffset by schottky diode(Maximum 0.5V)

Figure 18. Resistor and Diode in Ground Comparison

6.2. Load Current Not Allowed During Reverse Battery

By not allowing conduction through either the power device or the control section of the IC, the thermal dissipation in reverse battery is negated. Additionally, the diode or resistor in the ground pin of the IC is not required.

6.2.1. Reverse Protection in V_{BATT} with Remote Load Ground

A common method of providing a low-voltage drop reverse battery blocking device is with a P-channel MOSFET in the V_{BATT} supply to the control module, which supplies the VBB pin.

This approach has the benefit of scalability, as the PFET can be selected to protect multiple devices. DPak devices are available for this specific application with a V_{ds} rating of 35V with extended gate voltages (V_{gss}) up to +/-25V, such as the FDD6637_F085. This is shown in Figure 19. An R_{dson}, typically in the ~12mΩ range or less, is sufficient to handle four FDDS100H06_F085 devices operating on a common, protected supply rail.

6.2.2. Reverse Battery Protection in Ground Circuit

Reverse-battery protection in the common ground line can be used in systems where the main electrical supply loop is completely isolated from the surroundings and all low-impedance sneak paths can be eliminated. The ground reverse-battery protection is a mirror image of the reverse protection in the power rail (V_{BATT}). This configuration has the advantage of using a N-channel MOSFET, which provides better economics for lower R_{dson} ratings. A single device can be used to provide global reverse protection to multiple drivers and loads. A device with a 30V V_{BSS} is usually sufficient, such as the FDD8896_F085. This is shown in Figure 20.

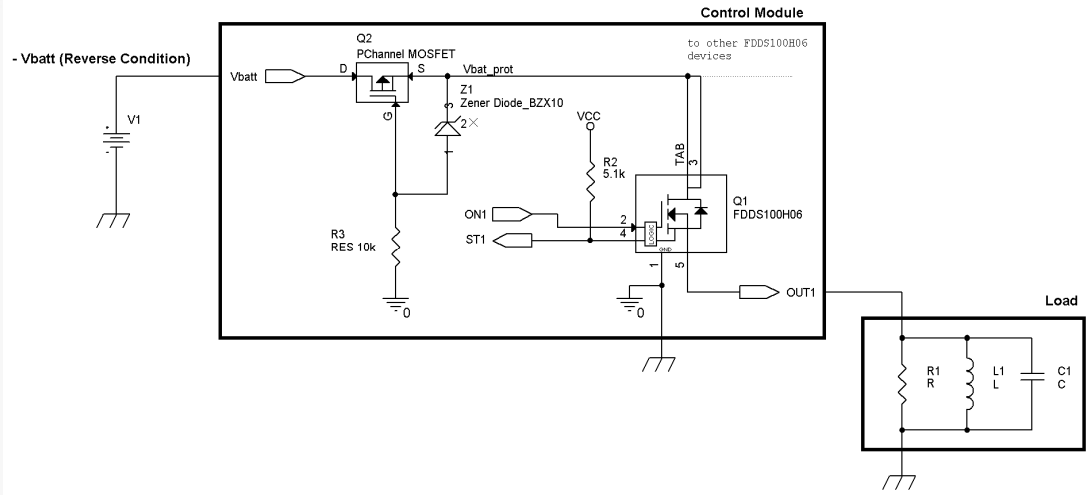


Figure 19. Reverse FET in the Power Line (using the P-Channel MOSFET)

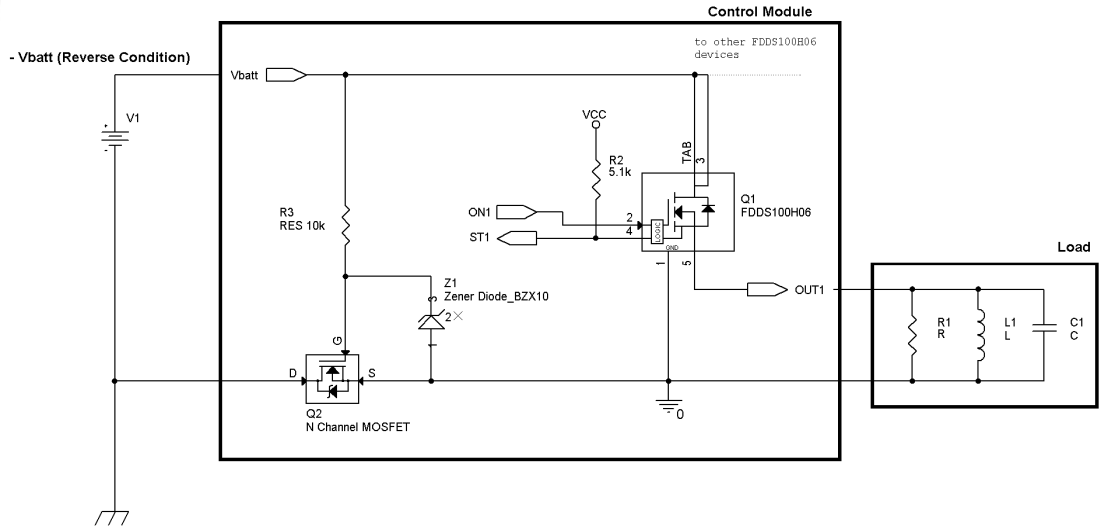


Figure 20. Reverse FET in the Ground Line (using the N-Channel MOSFET)

References

AN-9739 — Reverse-Battery Protection of Smart Switches

AN-7515 — Combined Single-Pulse and Repetitive UIS Rating System

Related Datasheets

http://www.fairchildsemi.com/ds/FD/FDD6637_F085.pdf

http://www.fairchildsemi.com/ds/74/74VHC00.pdf

http://www.fairchildsemi.com/ds/FD/FDD8896_F085.pdf

Appendix1 — $V_{ON(cl)}$ Test Circuit