Limitations in nRF24Z1 Firmware rev. 2.0 vs. nRF24Z1 Product Specification rev. 3.1

Function	Reference to description in nRF24Z1 Preliminary Product Specification, rev 3.1
For VDD less than 2.5V, a 100nF capacitor must be connected between IREF and VSS pin, to avoid an error in wakeup from power down	Minimum supply voltage, on page 1 and other pages, and ch 18 Application example
Audio rates less than 32kHz should not be used, due to poor performance with low link quality	please see register TXSTA bits 6:5 Audio rate scale factor =1 is recommended
ARX SPDIO pin is incorrectly set to output low, when S/PDIF is not enabled	please see table 7.3
Access to ATX 2-wire slave interface may occasionally disturb audio when audio rate is 32kHz.	please see ch. 7.4.3 2-wire slave interface
LNKSTA register is not available via ARX slave interface	please see Table 8-5
Link broken interrupt is not available on ARX side.	please see ch. 9 Interrupts
First interrupt after power on / RESET may be false and should be ignored	please see ch. 9 Interrupts
Occasionally VDD_PA may not go off in sleep mode	please see ch. 11 Power down control
Z1 does not enter Power down mode immediately in link locate mode, only in audio streaming mode. In link locate mode, power down is initiated after specified wake time has expired.	please see ch. 11 Power down control
When the automatic power down mechanism is active, alternative requests for power down will be ignored until the specific timeout period (TX/RXWTI) has elapsed.	please see ch. 11 Power down control
2-wire slave interface should not be active during power down or when waking up from power down	please see ch. 11 Power down control
When a slave interface command is aborted due to relink, TXCSTATE, LNKCSTATE or RXCSTATE status value is incorrectly set to 0.	please se table 12.1

RXLTI register is not covered by RXCSTATE status.	please se table 12.1
RX spur drifts in test mode	relates to single channel test in RX mode, i.e. TESTREG=0x63 and TESTCH.7=0, please see ch. 13

Table-1 : nRF24Z1 functions which are not available in Firmware rev. 2.0

1.1. Complete list of restricted register settings in Firmware rev 2.0:

Register	Restriction
TXSTA	generally scaled rates are not recommended, i.e. bits 6:5 should be set to binary 10
TESTREG, TESTCH	TESTREG=0x63 and TESTCH.7=0 is not recommended

Table-2 : nRF24Z1 limitations on use of registers in Firmware rev. 2.0

All registers not mentioned in Table 2 have no limitations and are free to use.