AN1230
APPLICATION NOTE

LNB SUPPLY AND CONTROL VOLTAGE REGULATOR (PARALLEL INTERFACE)

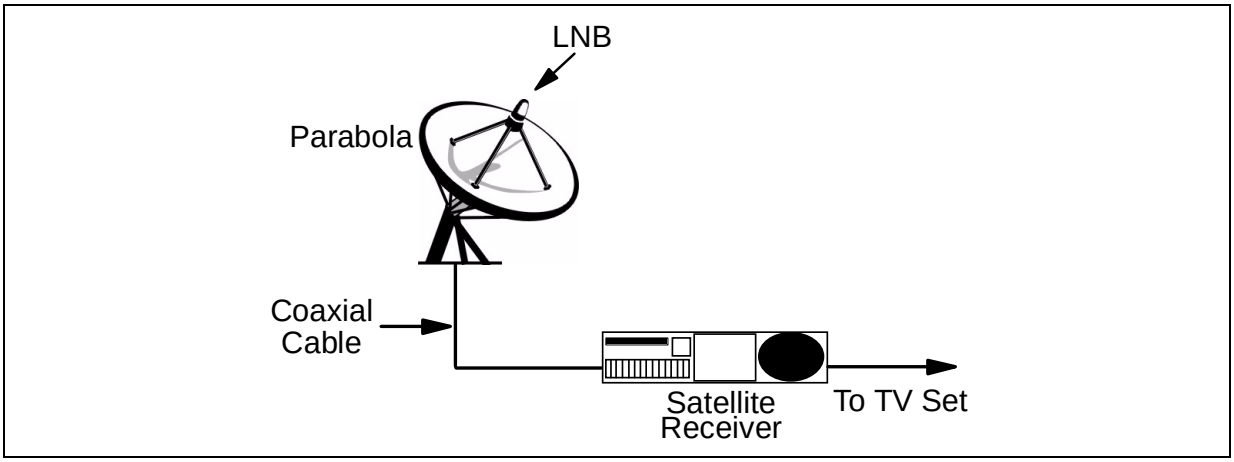
F. Lentini - G. Benenati

1. ABSTRACT

LNBP is the integrated solution for supplying/interfacing satellite LNB modules. It gives good performances in a simple and economical way, with a minimum use of external components. It is comprised of functions that realize LNB supplying/interfacing in accordance to the international standards.

2. INTRODUCTION.

Figure 1: Basic Satellite Installation



A typical satellite receiver system is formed by these blocks (reported in figure 1):

1. The **parabola** is the antenna of the system and focuses the satellite signal to the LNB;
2. The **LNB** (low noise block) is placed on the focus of the parabola and converts the incoming signal in the 10GHz range to a lower frequency signal (in the 1-2GHz range) called "first conversion signal". This allows the signal to be carried by an inexpensive coaxial cable towards the receiver. Additionally, it improves the first conversion signal level by a built-in low noise amplifier. A universal LNB can change the type of polarization (horizontal or vertical) or operative band by command signals sent by the receiver;
3. The **coaxial cable** joins the LNB to the receiver and carries out 3 functions:
   a) to transfer the first conversion signal from the LNB to the receiver;
   b) to transfer the command signals from the receiver to the LNB to change polarization or signal band;
   c) to carry the DC voltage to supply the LNB.
4. The **receiver** converts the first conversion signal into control signals for the TV system. The receiver provides for that provides for two important features:

a) to supply the LNB block;
b) to generate all the signals/voltages that LNB needs to operate correctly.

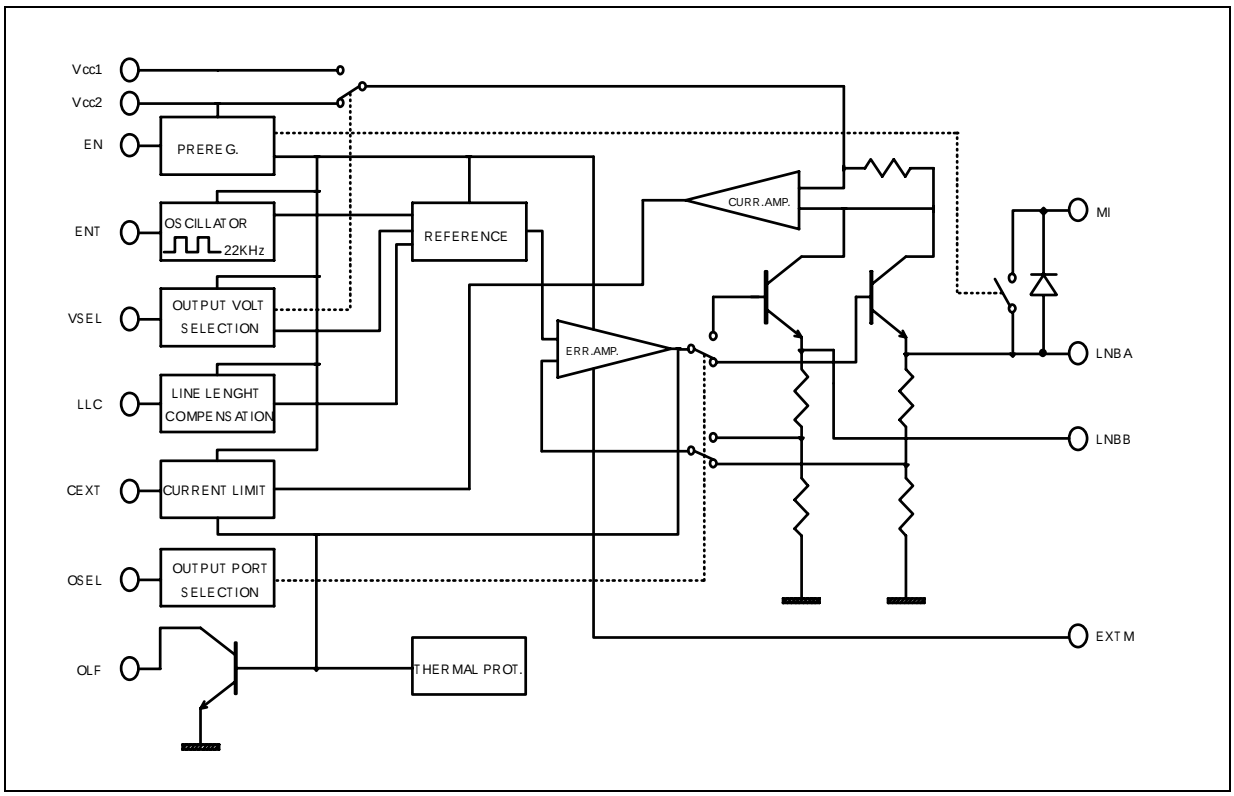
5. The **supply/interface block** is placed inside the receiver. It must perform the following functions:
   a) be ready to accept future digital standards with an external modulation input and fast oscillator start-up;
   b) implement the loop-through function in slave condition for single dish, multiple receiver system;
   c) accept the paralleling of 2 or more receivers and, in this condition. avoid the flow of reverse current from the output to the GND;
   d) give accurate, thermal compensated outputs with the possibility to compensate the DC voltage drop caused by long coaxial cables;
   e) be reliable;
   f) provide overload (better if dynamic) and thermal protection with diagnostic;
   g) avoid every type of trimming;
   h) provide the possibility to be driven by a microcontroller or a simple digital logic to implement all these functions;
   i) Finally, it must be cheap and get a small area in the board.

All these functions are hard to be implemented with discrete components, but are greatly made easier by using an integrated device, like LNBP, that has been specially designed for this purpose.

3. FUNCTIONAL BLOCKS.

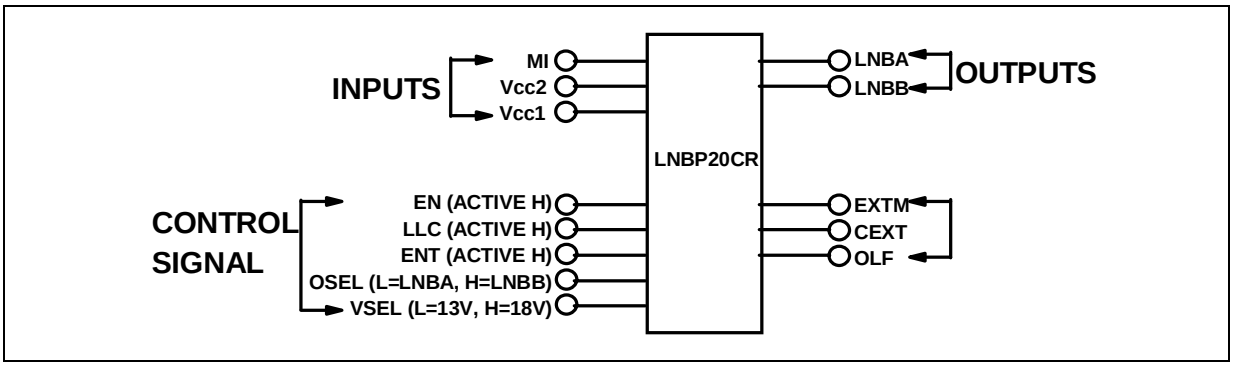
LNBP comprises the following operative blocks (see figure 2):

Figure 2: Internal Block Diagram



1. The **oscillator** is activated by putting the ENT pin (Enable Tone) = H and is factory trimmed at 22KHz ± 2KHz, avoiding the need to use external trimming. The rise and fall edges are controlled to be in the 5 to 15µs range, 10µs typ., to avoid RF pollution towards the receiver. The Duty Cycle is 50% typ. It modulates the DC output with a ± 0.3V amplitude and 0V average. The presence of this signal usually gives the LNB information about the band to be received.
2. The **OSEL (OUTPUT PORT SELECTION)** selects the two outputs of the LNB (LNBA and LNBB), in order to drive a dual-dish system, depending on its present state. When OSEL is L, the LNBA port is selected. When OSEL is H, the LNBB port is selected. The LNBA and LNBB outputs supply either 13V or 18V. If VSEL is low (VSEL = L) 13V is selected, otherwise, if VSEL is high (VSEL = H) 18V is selected. This kind of feature changes the LNBP polarization type. The LNB switches horizontal or vertical polarization depending on the supply voltage it gets from the receiver.
3. In order to keep the power dissipation of the device low, the **input selector** automatically selects Vcc1, that is the lowest input voltage, when 13 V out is selected (i.e. VSEL is L). If 18V out is selected (i.e. VSEL is H), Vcc2 input is selected. So power dissipation at Iout=500mA is: Pd=(22-18)*0.5=2W (with Vcc2=22V and Vout=18V) or (15-13)*0.5=1W (with Vcc1=15V and Vout=13V). Without input selection we should have Pd=(22-13)*0.5=4.5W, which is much higher. Moreover, an internal switch selects the **MI (MASTER INPUT)** to be transferred to the LNBA when the EN pin is low. This case occurs when two receivers are connected in series and the slave receiver (the nearest to the antenna) is disabled. The master receiver supplies the LNB by means of the MI input of the slave receiver.
4. The **line length compensation** function is useful when the antenna is connected to the receiver by a long coaxial cable that adds a considerable DC voltage drop. When the LCC pin is H, the output voltage selected is increased by about 1V.
5. The **reference** drives all the internal blocks that require a high precision thermal compensated voltage source.
6. The LNBP has two different **protection** features, and both turn off the outputs. The first one acts in overload conditions (i.e. for output current ≥ 500mA), and the second for overheating (i.e. for Tamb ≥ 150°C).
   a) The overload protection case occurs when output current request is ≥ 500mA. In this condition the device limits the output current at 500mA for a time Ton depending on the Cext value. When Ton has elapsed, output goes low for a time of Toff=15*Ton. This keeps the power dissipated by the device low in overload conditions, and avoids to oversize the heatsink in such a condition.
   b) In the thermal protection case the output is disabled until the chip temperature has fallen. After that the LNBP restarts working properly. The LNBA bypass switch is not protected, so the MI input must be driven by a current limited voltage source.

Figure 3: LNBP Pin Grouping



In figure 3 the LNBP pins are grouped by functions. The 5 control signals are logic inputs that control the IC function, and it is recommended that the VIH not exceed 7V.

Cext controls the restore timing of the overload protection. If an overload protection is present, output goes low for a time imposed by the Cext value. At the same time the OLF pin, an open collector output, goes low.

In figure 4 and figure 5 the behavior of Ton and Toff times vs. Cext is respectively shown. When Toff has elapsed, the output returns active for a time Ton=Toff/15. Then, OLF returns a high impedance output. If the overload is still present the cycle is repeated. This behavior greatly reduces the dissipation in the device. In fact, in short circuit conditions with Vcc2=25 V, considering Iout internally limited at 650mA and Toff=15*Ton we obtain: Pd average=Vin*Iout*Ton/(Ton+Toff)=25*0.65*1/(1+15)=1.02W, that is lower than the power dissipated in normal conditions.

Figure 4: Overload Protection On Time versus C_{ext}

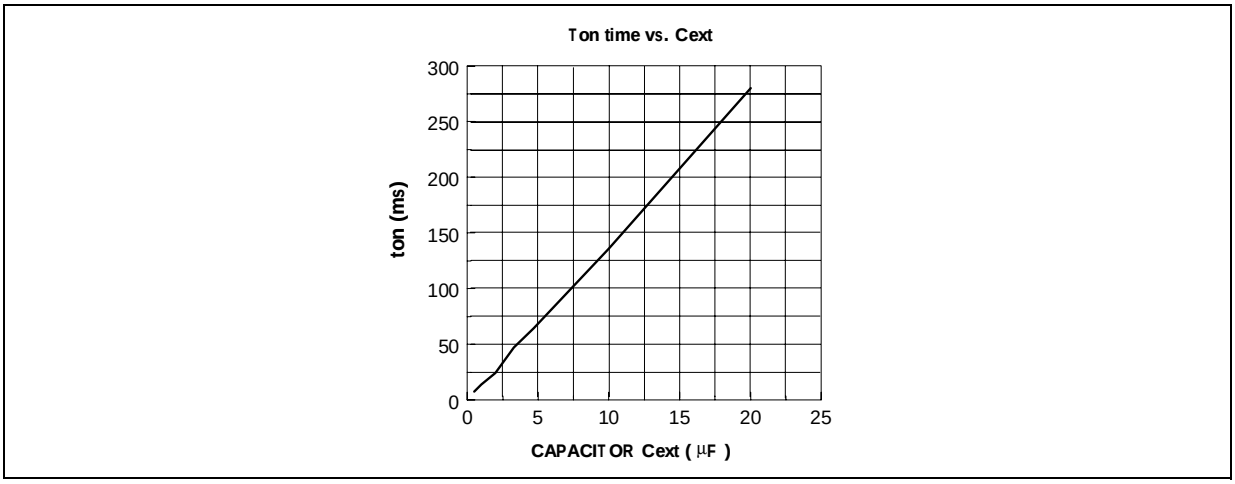
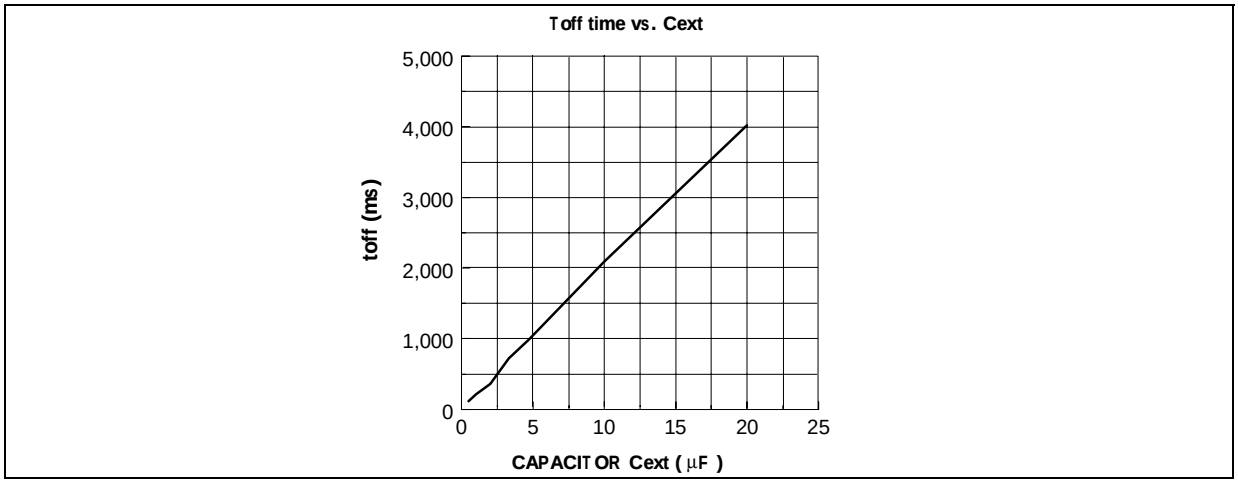


Figure 5: Overload Protection Off Time versus C_{ext}



The Cext must be properly chosen. It is related to the Iout and Cout (total capacitor connected to the LNBA or LNBB output) values. Large Cout values at start-up give high current peak for a long time, and consequently, an overload condition for a time that could be greater than the Ton imposed by Cext. So the output will be forced low, completely discharge and will not start. For proper use it is necessary that

Cout/Cext ≤ 20. The OLF also gives information about the thermal protection status. If the thermal protection is triggered, the output is disabled and the OLF goes low. When the chip temperature has fallen, the output returns active and the OLF returns to its 3-state condition.

By sensing the ON/OFF ratio of the OLF signal, a microcontroller can discriminate if an overload or a thermal protection is present.

EXTM modulates the Vout by a capacitor connected in series (see figure 6). In this case:
Vout a.c.=Vin a.c.*Vout d.c./3 where, respectively, Vout a.c. and Vin a.c. are alternate components of Vout and Vin, and Vout d.c. is the direct component of Vout. For example, if an a.c. signal of 600mV p.p. must be imposed to the 13V d.c. out, the formula is as follows:
Vin a.c.= 3*Vout a.c./Vout d.c.=3*600/13 ª140 mV p.p. If we dispose a 0-5V square wave signal to modulate output voltage, it is necessary to lower this signal amplitude. In accordance to figure 7 we have:
R1=R2*(V1/Vin-1).

Figure 6: How to Use EXTM Input

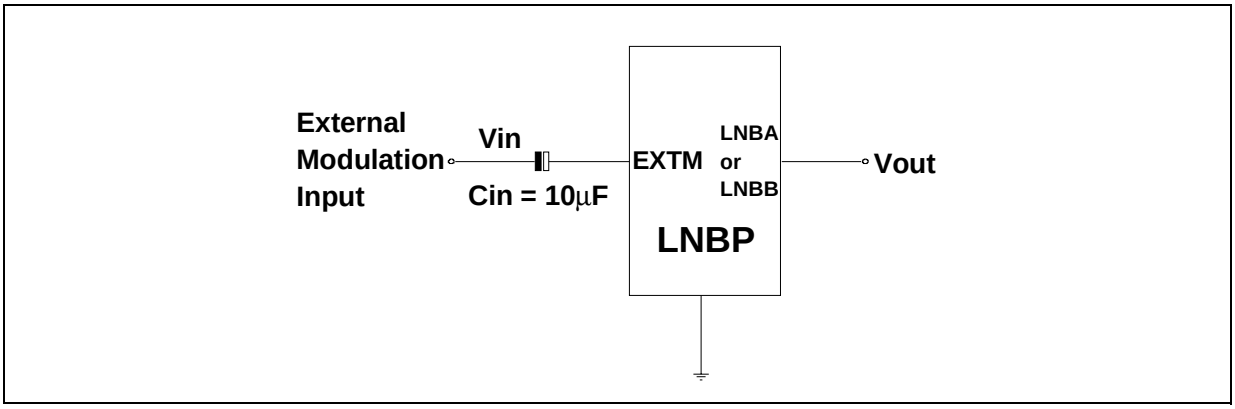
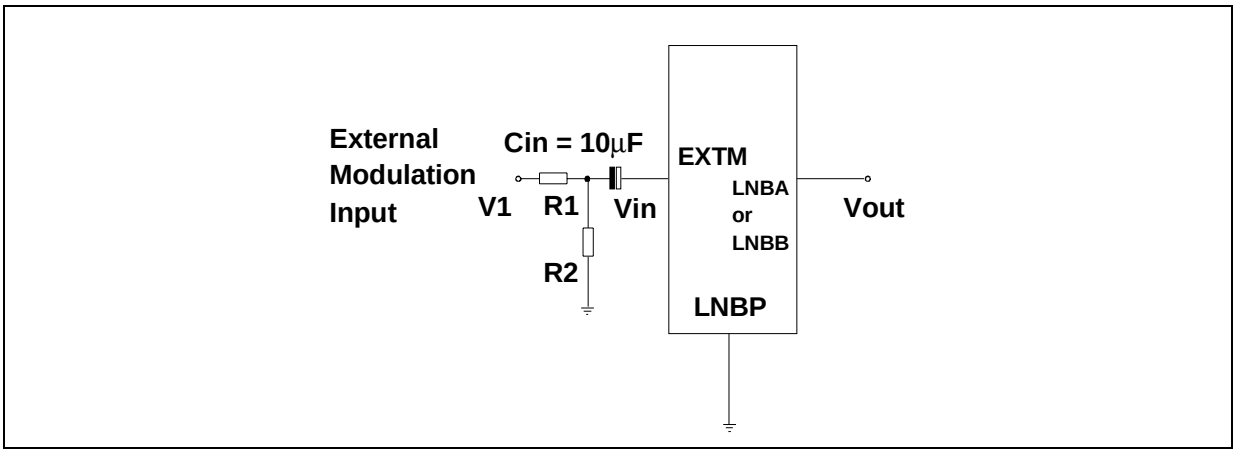


Figure 7: How to Adjust the External Modulation Level



R2 must be in the 50Ohm range to minimize the effects of the EXTM input resistance variations. In our example we obtain:
R1=50*(5/0.14-1)=1.7kOhm.
As a side effect, the EXTM modifies the Vout by a resistor connected between this input and the GND. Figure 8 and 9 report the Vout value vs. R.

Figure 8: Vout Value vs. Resistance on the EXTM pin at VSEL = L

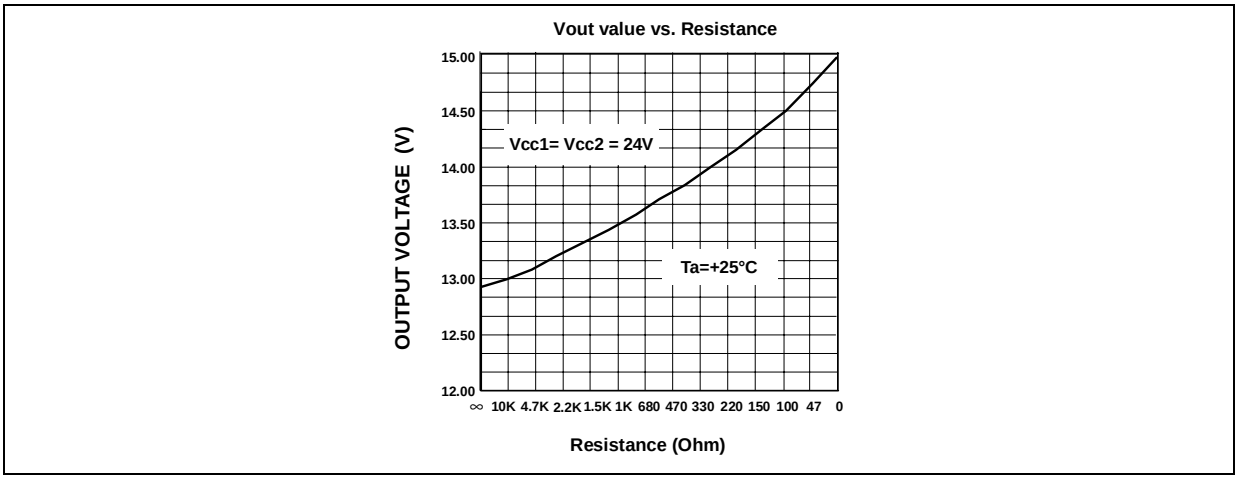


Figure 9: Vout Value vs. Resistance on the EXTM pin at VSEL = H

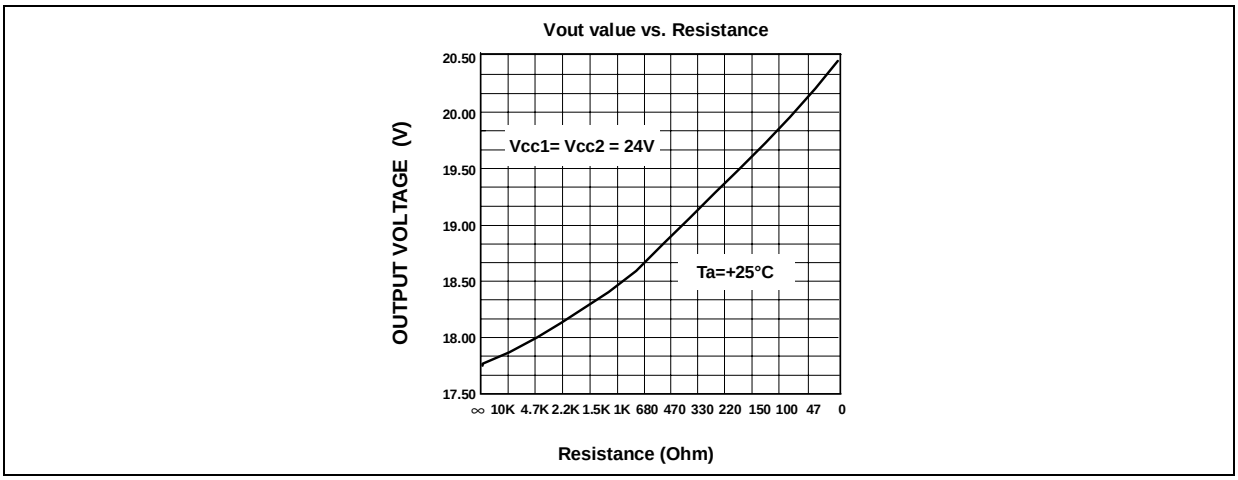
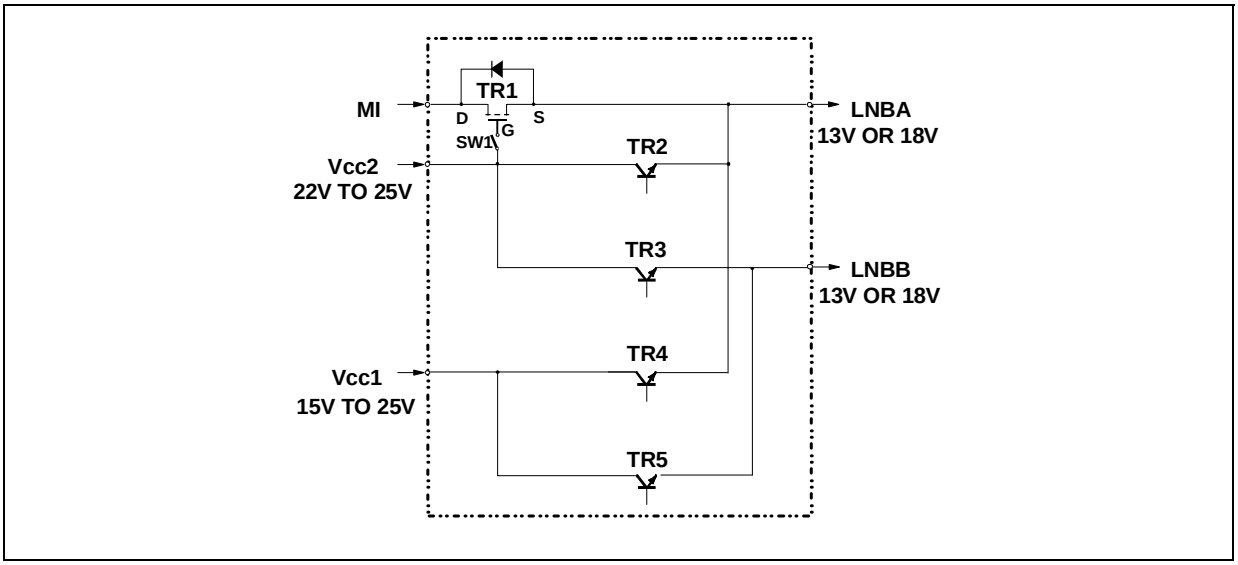


Figure 10: LNBP Output Stages



4. OPERATING MODE.

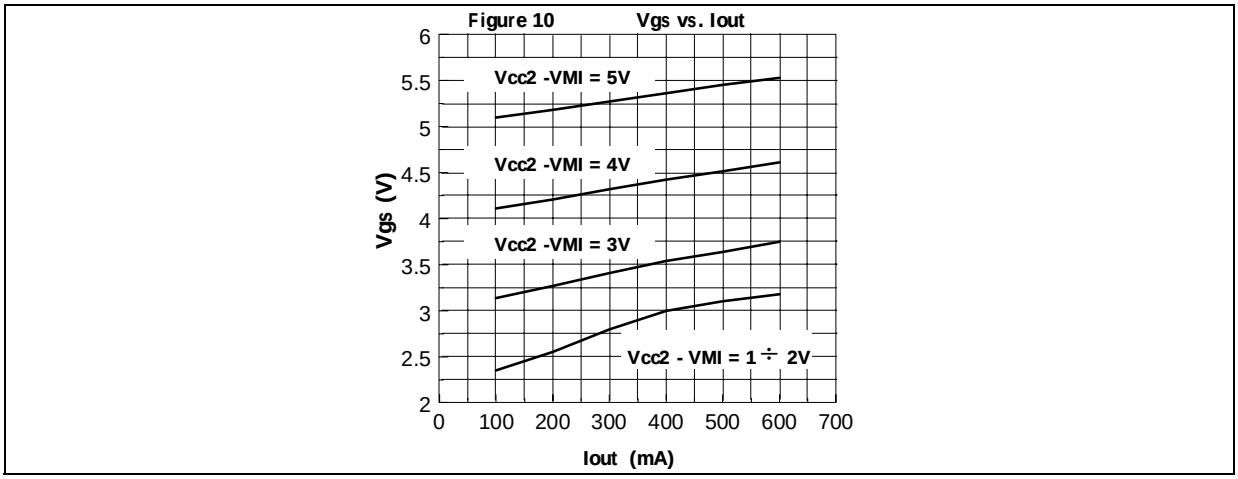
LNBP has 3 power inputs (Vcc1, Vcc2 and MI) and two outputs (LNBA, LNBB) internally connected in accordance to the scheme reported in figure 10. By analyzing this scheme we can make out the following results:

1. TR1 is an N-channel Power MOSFET with its source connected to the LNBA. It is driven by SW1, that joins the gate to Vcc2. The drop between MI and LNBA is due to the Ron of TR1, but in some conditions it is increased by inadequate driving. In fact we have:
   Vdrop=Vdrain-Vsource=VMI-(Vcc2-Vgs)=Vgs-(Vcc2-VMI).

   We can see that the drop can be minimized increasing the (Vcc2-VMI) value. For example, if Vcc2 increases, the effect of inadequate driving is cancelled.
   Vgs depends on the TR1 and Iout characteristics. Figure 11 gives the Vgs vs. Iout plot, with Vcc2-VMI as the parameter. Therefore, given Iout,Vcc2 and VMI we can calculate the Vdrop. If Vcc2=22V, MI=21V and Iout=500mA the formula is as follows: Vdrop=Vgs-1V. In figure 11 it results that Vgs=3.1V at ILOAD=500mA and Vcc2-VMI=1V and in such conditions Vdrop=3.1V-1V=2.1V.

If we increase Vcc2 at 26V we obtain: Vdrop=5.65V-5V=0.65V, which is much lower.

Figure 11: Loop-Through Switch Gate Voltage



2. In some cases it happens that two or more receivers share the same coaxial cable making their output hard paralleled, so the same voltage is present at the outputs of the receivers. If a receiver is not disconnected at the mains, it will flow a current from the LNBA to the MI by means of the parasitic D-S TR1 diode. Moreover, the TR2 (or TR4) $B_{Vb\text{-}e}$ could be exceeded, so a reverse current could flow from the LNBA to Vcc2 (or Vcc1) or from the LNBB to Vcc2 (or Vcc1), with possible destruction of the relative transistor. To overcome this drawback it is enough to add one or two diodes, depending on how many outputs are used, in series at the LNBA or LNBB pins (see figure 12). In this case we have to consider the voltage drop across the diode that is load and temperature dependent. These effects can be minimized by using Schottky diodes and activating the LLC function.

In alternative we can add one, two or three diodes - it depends if one, two or three inputs are used - in series at input oins M1, Vcc1 and Vcc2 (see figure 13). In this case diodes do not causea change at Vout, but only a worsening of voltage drop, that can be minimized by using Shottky diodes. Diodes used in figures 12 and 13 must withstand a continuous current of almost 1A and a breakdown voltage of 30V (suggested type is BYV10-30).

Figure 12: Reverse Current Protection Using Diodes on the Outputs

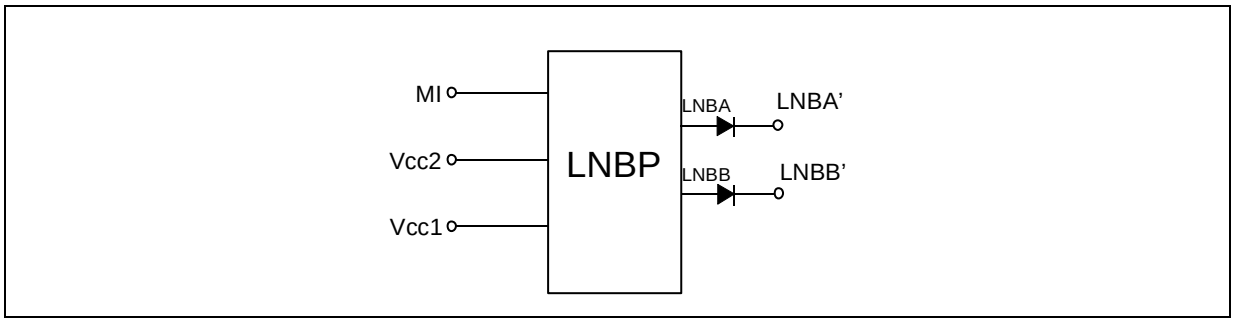
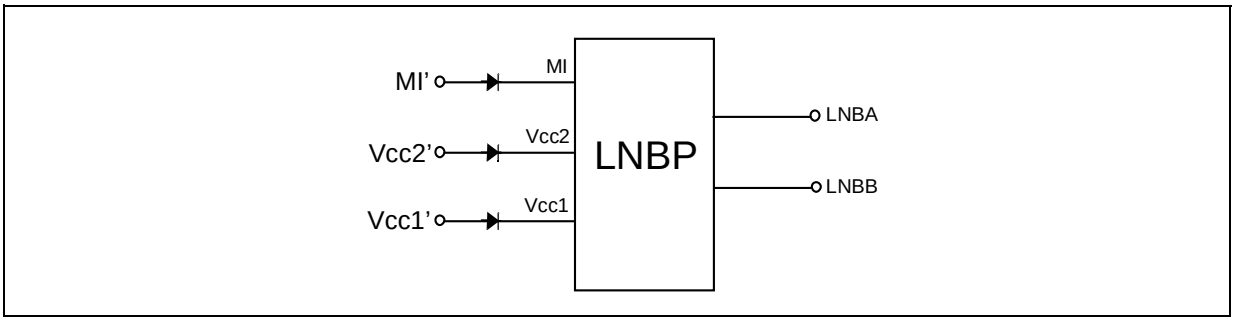


Figure 13: Reverse Current Protection Using Diodes on the Inputs



3. In alternative we can add one, two or three diodes, depending on how many inputs are used, in series at the MI, Vcc1 and Vcc2 input pins (see figure 13). In this case diodes do not cause a change at Vout, but only worsen the voltage drop, which can be minimized by using Schottky diodes. Diodes used in figures 12 and 13 must withstand a continuos current of almost 1A and a breakdown voltage of 30V (suggested type is BYV10-30).

5. APPLICATION HINTS.

1. LNBP has an LLC pin to compensate the voltage drop across the cable. This pin adds a discrete 1V value at the selected output voltage when it is active. It is also possible to obtain a continuous variation of the LNBA or LNBB voltage by using EXTM input.
2. If only a single 22V source is suitable, at the cost of higher power losses in the device and higher heatsink surface, it is possible to power the Vcc1 and Vcc2 pins by the same 22V source without affecting any other circuit performance. In order to reduce power dissipation in the device, it can be useful to insert an adequate resistor in series to the Vcc1 pin (see figure14). This resistor must be dimensioned considering that the minimum voltage on the Vcc1 pin must be ≥ 16 V, with a supply current I_{SUPPLY} = 500 mA.
   This means: R ≤ (22-16) / 500 *10 -3 ≅ 12 Ohm.
   Power dissipated in this resistor is:
   Pd = R*Iout^2 = 12* (500*10 -3)^2 = 3W.
   It is recommended to bypass the Vcc1 and Vcc2 pins by 2.2µF electrolytic capacitors.

   3W is the power dissipated saved by the device.
3. If Vcc2 is not inserted (i.e. the receiver is not connected to the mains) the TR1 can not bypass MI to the LNBA, because the gate is not driven (see figure 10). It is possible to overcome this drawback by using the scheme reported in figure 15.

Figure 14: How to Get Vcc1 Using a Drop Resistor

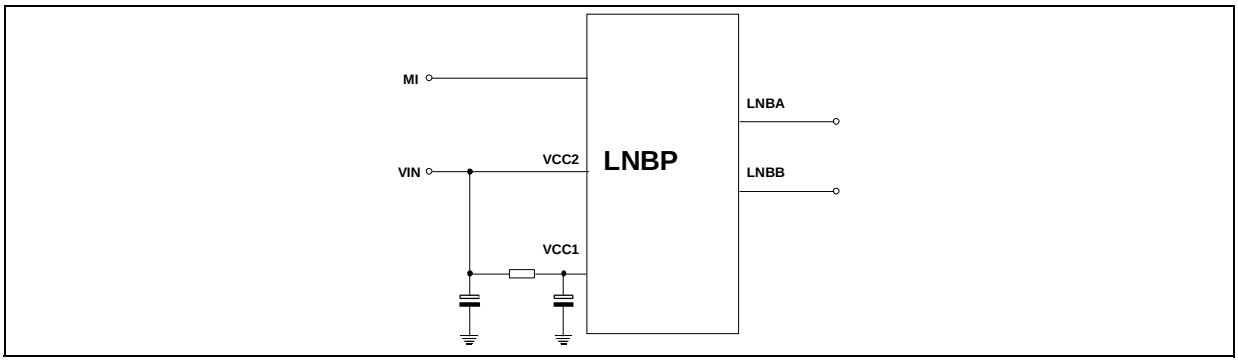
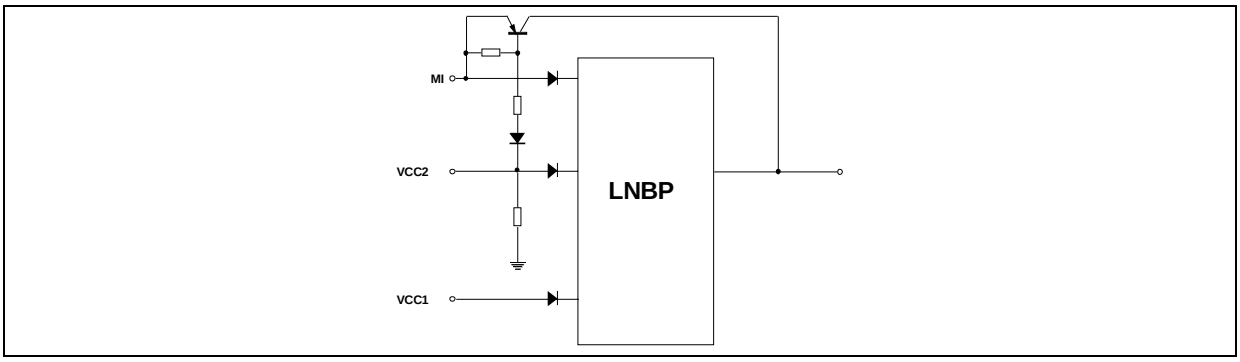


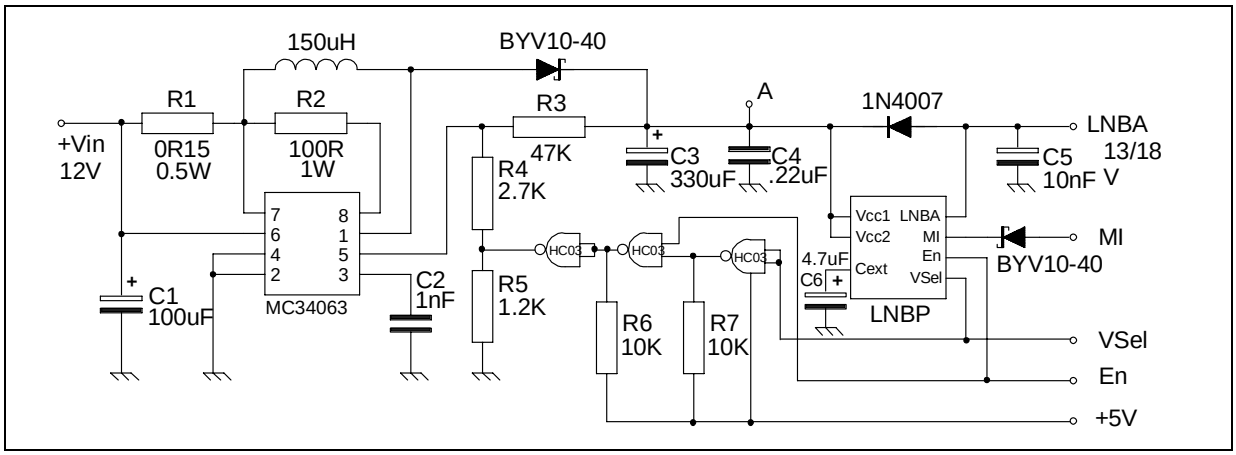
Figure 15: A Loop-Through Switch That Works Without Vcc2



6. SINGLE SUPPLY APPLICATION.

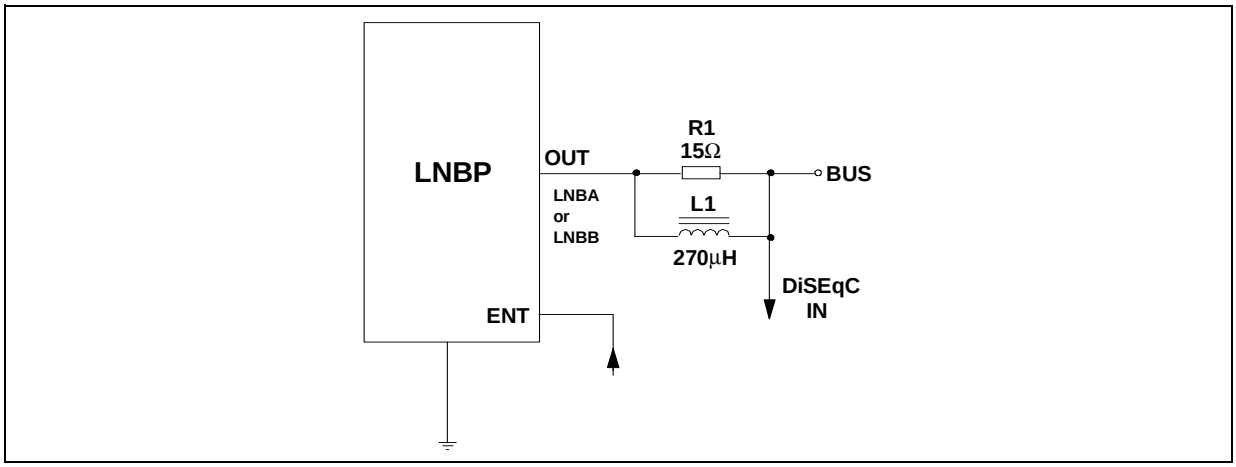
In some applications (TV receivers, PC cards, etc.) a 12V power supply is available. It is possible to use this voltage to supply the LNBP. Figure 16 reports the schematic of the application proposed. It uses an MC34063 to step-up the 12V input at a value of 16V or 23V, depending on the Vsel status. If Vsel is H (i.e. the LNBP gives 18V at out LNBA), a 23V voltage is available at point A. If Vsel is L (i.e. the LNBP gives 13V at out LNBA), a 16V voltage is available at point A. This keeps the power dissipated by LNBP low and gives good efficiency because the LNBP is supplied with a minimum drop. Diode D2 protects the LNBP by reverse current. If the LNBP is disabled (i.e. En is L), the 23V voltage is selected at point A, regardless of the Vsel status. The changing voltage at point A is actuated by HC03, which is an open-drain quad 2-input nand gate.

Figure 16: Single Supply Application Using MC34063A Plus LNBPxx



7. DiSEqC* SPECIFICATION.

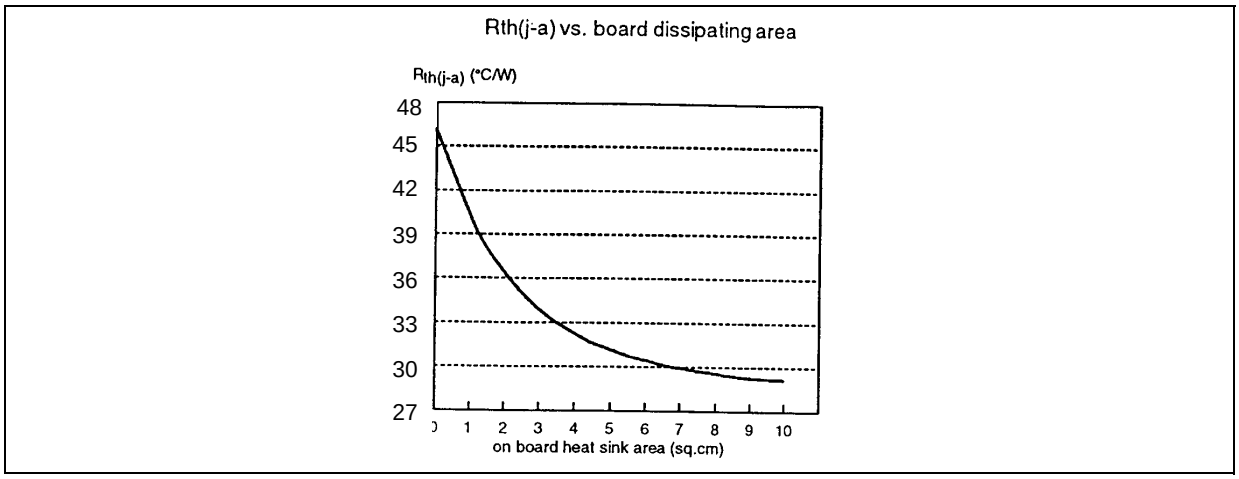
Figure 17: Impedance Matching for DiSEqC



The DiSEqC standard was born to implement the most complex system required, for example, by multiple-satellite installations, where multiple LNB placed in the parabola must communicate with the receiver in a two-way mode. This standard is compatible with 13/18V and 22kHz tone and is easily implemented by a microcontroller. It requires hardware specifications that are faithfully satisfied by LNBP. In particular, the bus impedance can be matched using the scheme reported in figure 17.

8. THERMAL MANAGEMENT.

Figure 18: Thermal Resistance versus On-Board Copper Heatsink Area



LNBP has a built-in dynamic protection system that considerably lowers the power dissipation in short or overload conditions. Therefore, the operative condition is the worst condition for power dissipation. LNBP is available in 3 packages: PowerSO-10, PowerSO-20 and MULTIWATT15. The last package can be assembled on a heatsink with:

Rth heatsink ≤ (Tj-Tamb)/Pd -R Thjc -R Thcs, where:

Tj=junction temperature (can be fixed at 150°C max);

Pd=dissipated power=Σ (Vin-Vout)*Iout;

R Thjc = junction-case thermal resistance ~2°C/W;

R Thcs =case-heatsink thermal resistance ~1÷1.5°C/W.

For SMD packages we must obtain the right R Thtot. This can be achieved soldering the metallic case of the package on an adequate copper surface that acts like a heatsink. In the figure 18 the typical R Thtot = R Th heatsink + R Thjc + R Thcs vs. copper surface is shown, for a board with 1 or 2 layers. In the 2 layers case, a convenient number of ways (~9/cmsq) must be provided. For best results these ways must be inserted below the device and near it. Doubling the surface we obtain a 3°C/W of R reduction.

Figure 19: Electrical Schematic Board of PowerSO-20™

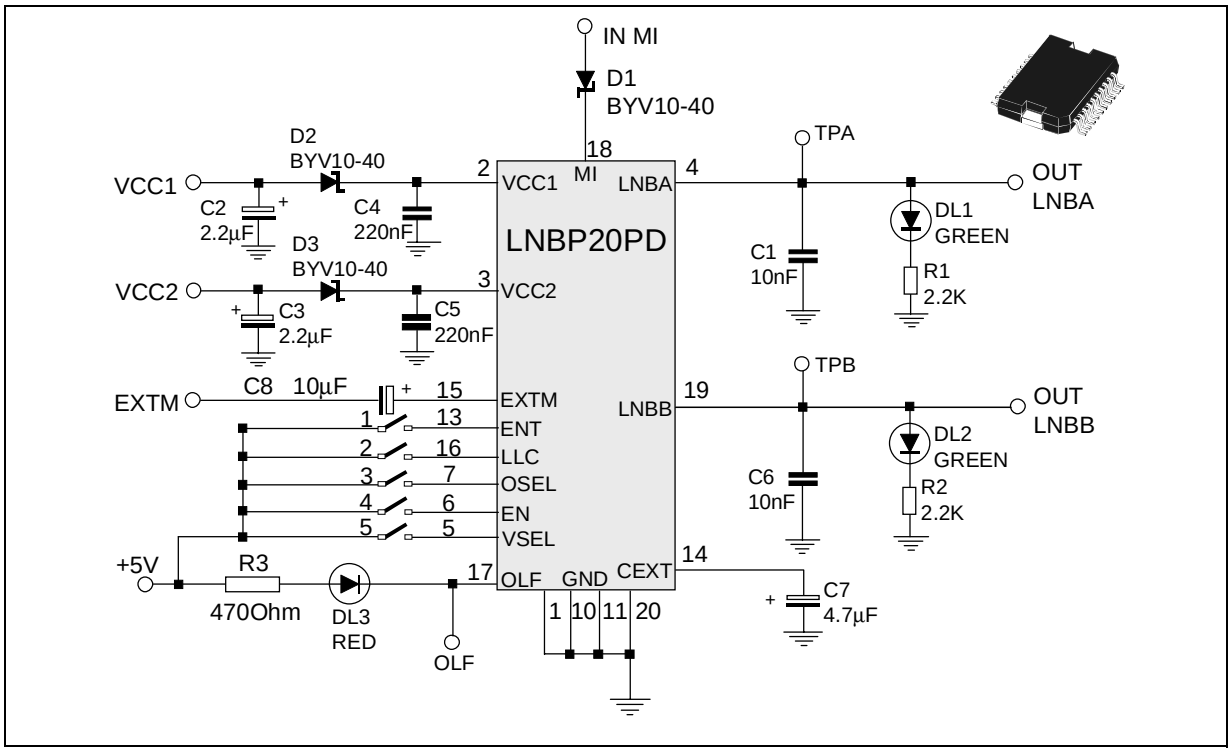


Figure 20: Electrical Schematic Demoboard of MULTIWATT15™

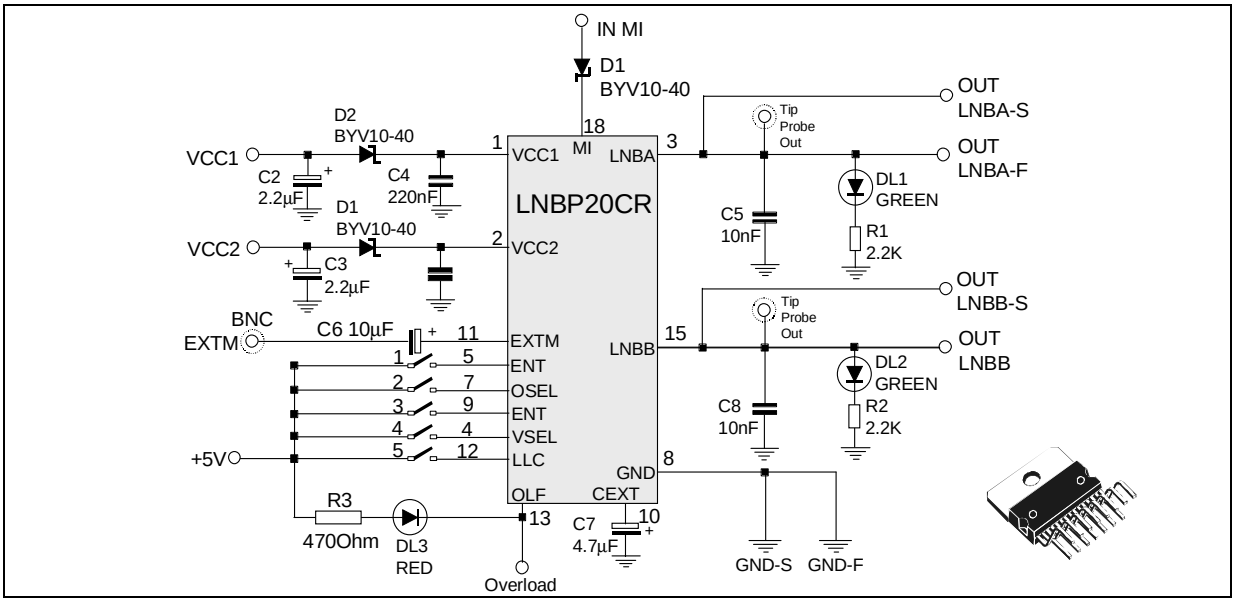


Figure 21: PowerSO-20 Demoboard

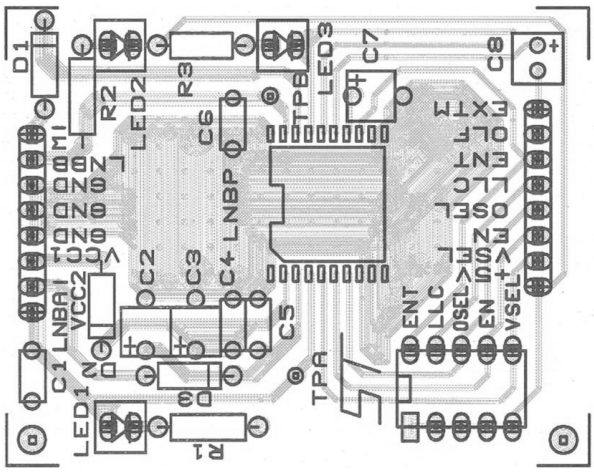
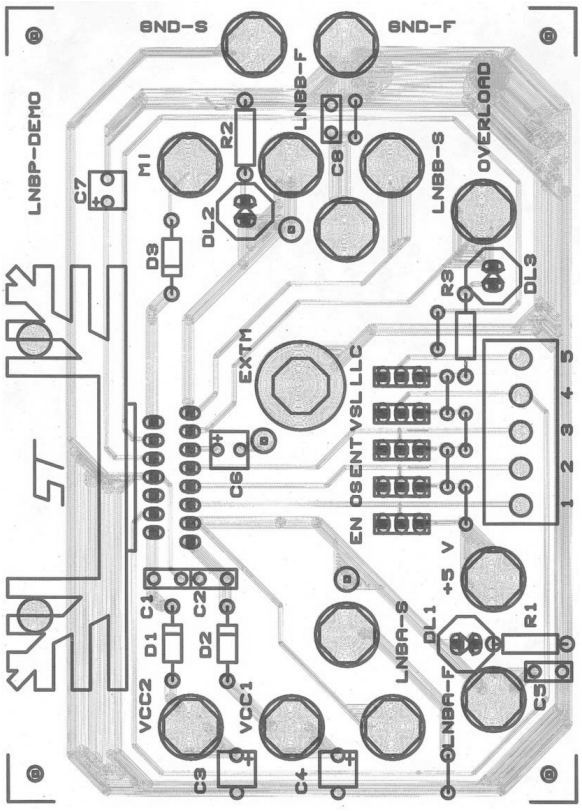


Figure 22: MULTIWATT15 Demoboard



The two demoboards of the LNBP of the PowerSO-20 and MULTIWATT packages are shown below. The different layer drawings are shown in figure 19 and 20. The first one is based on the PowerSO-20 package and the second on the MULTIWATT packages.

10. SCHEMATIC CIRCUIT DESCRIPTION.

10.1 POWER SO-20™ Package.

Two comb connectors (8 pins each) are used for the input and output voltage and for all control signals (Vsel, EN, Osel, LLC, ENT). It is possible to force at high levels all the control signals through a 5 pin dip-switch. If the control signals come from outside the board, the dip-switches must be in the OFF position. An oscilloscope probe can be connected to the TPA and TPB test points to monitor the 22KHz signal.

10.2 MULTIWATT™ Package.

The MULTIWATT electric schematics is shown in figure 20. In the board some plugs are provided for the input of the following signals: Vcc1,Vcc2, MI, +5V and GND (force and sense). Also, LNBA and LNBB (force and sense) are connected by plugs. The load is connected between the output connector LNBA-F (or LNBB-F) and GND-F. Between the LNBA-S (or LNBB-S) and GND-S two voltmeters can be connected to monitor the output voltage. Besides, two plugs connected with the two outputs permit the

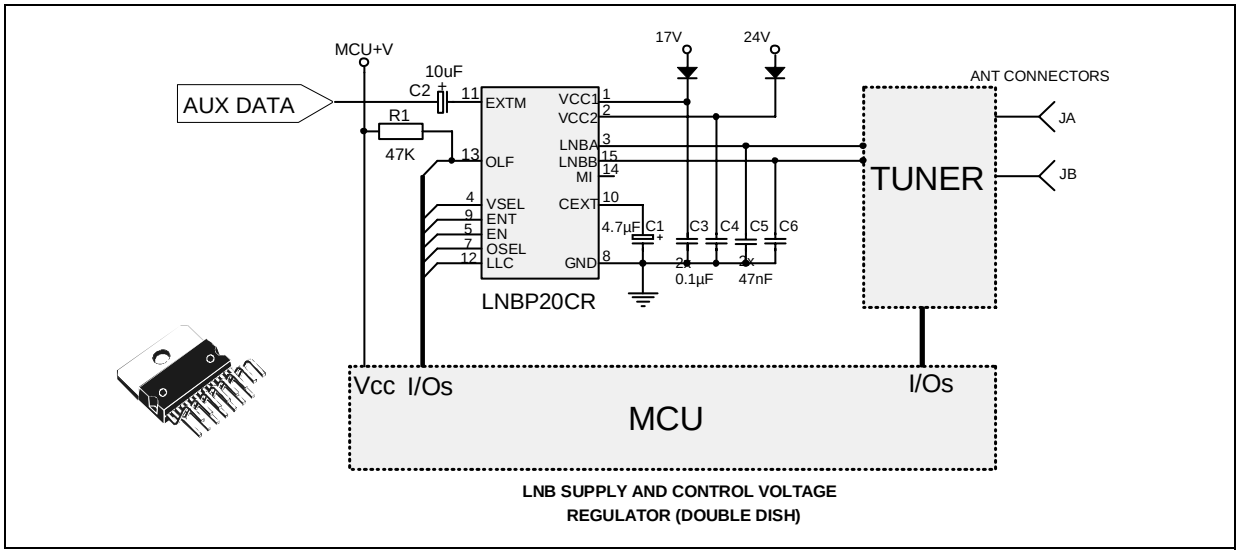
insertion of the oscilloscope probes to monitor the 22kHz tone. The EXTM input can be connected to the relative BNC connector. It is, moreover, possible to force at high level the following inputs: *EN, Osel, ENT, Vsel*, and *LLC* by five switches. It is moreover possible to force such inputs even through the five poles connector. In this case all the switches must be in off position.

11. CONCLUSION

This paper gives practical information to develop numerous applications using this solution for supplying satellite LNB. The use of the existing LNBP Demoboard allows the development of the final product. On the next pages there are numerous examples of typical application schematics based on LNBP.

Typical Application Schematics are shown below.

Figure 23: Two Antenna Ports Receiver



LNB SUPPLY AND CONTROL VOLTAGE REGULATOR (DOUBLE DISH)

Figure 24: Single Antenna Receiver with Master Receiver Port

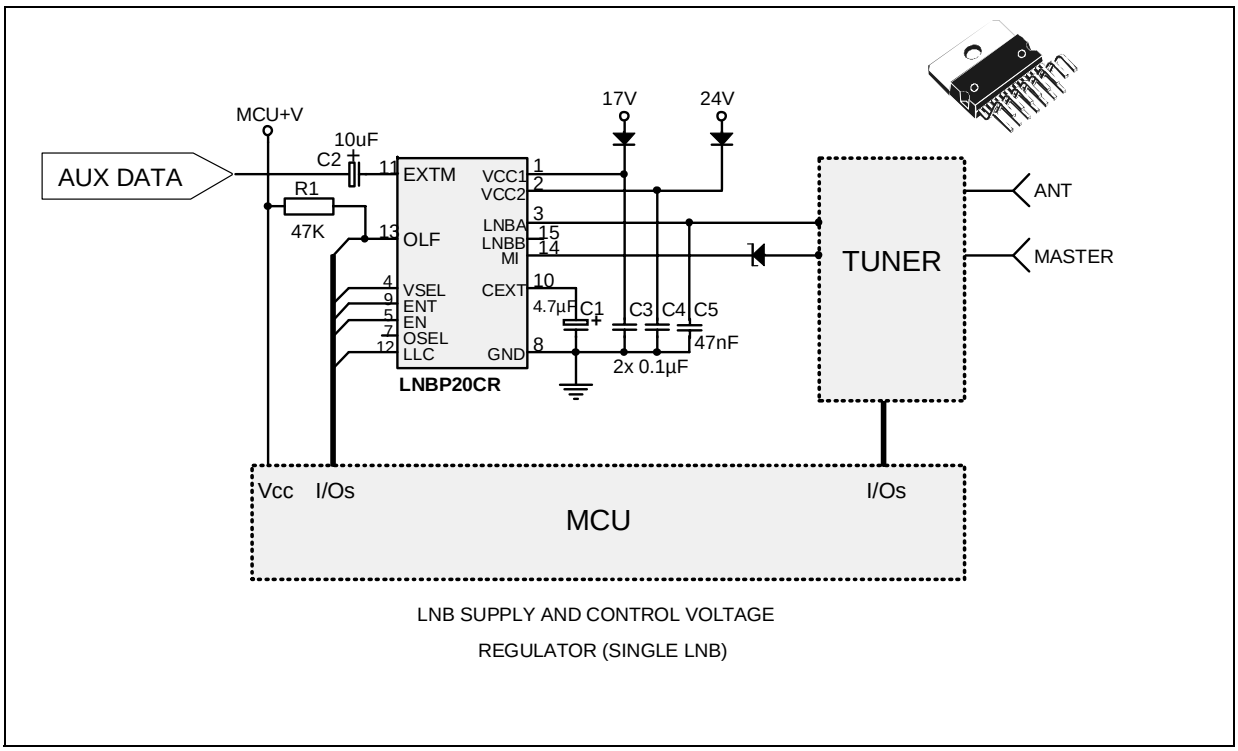
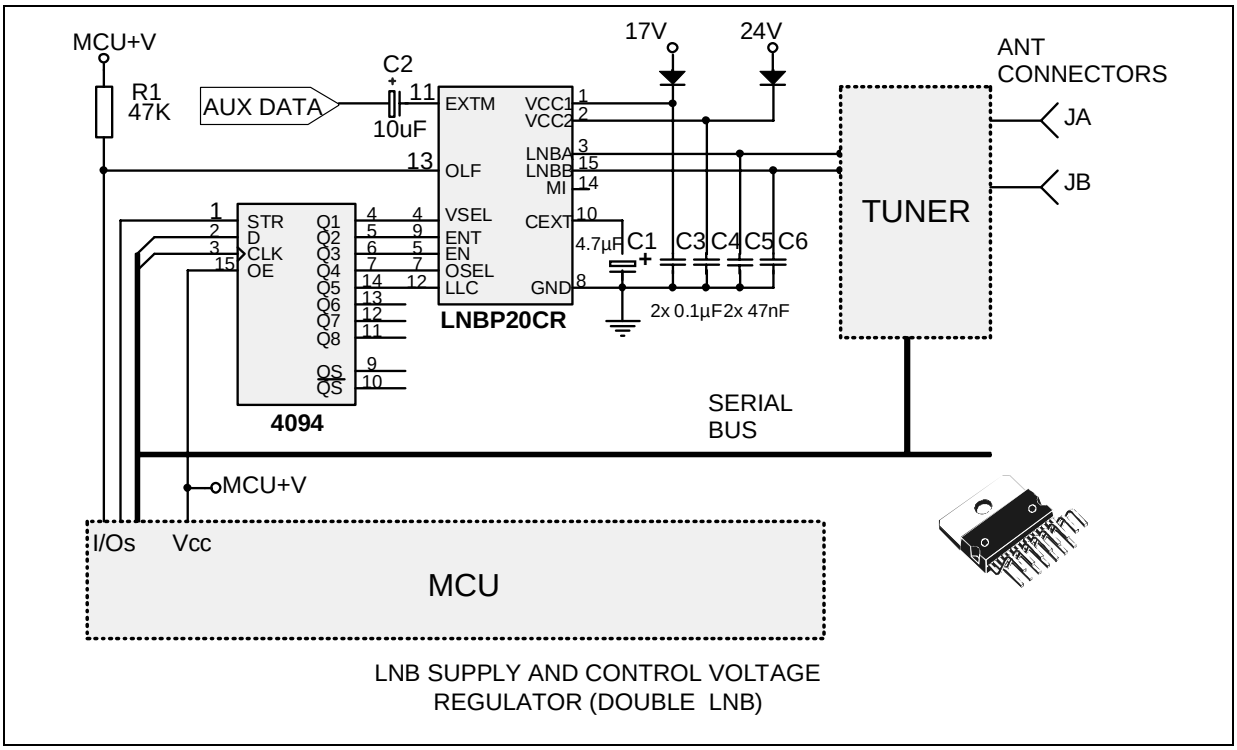


Figure 25: Using Serial Bus to Save MPU I/Os



Typical Schematics cont'd

Figure 26: Two Antenna Ports Receiver

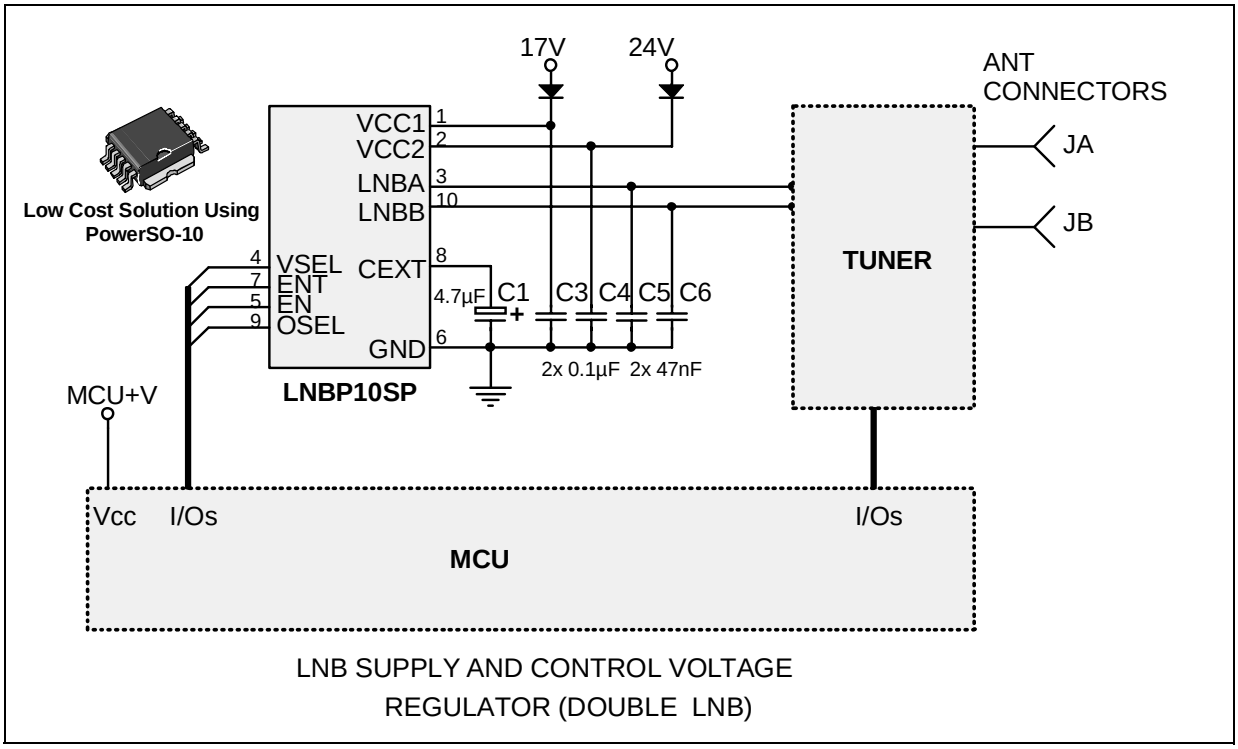


Figure 27: Connecting Together Vcc1 and Vcc2

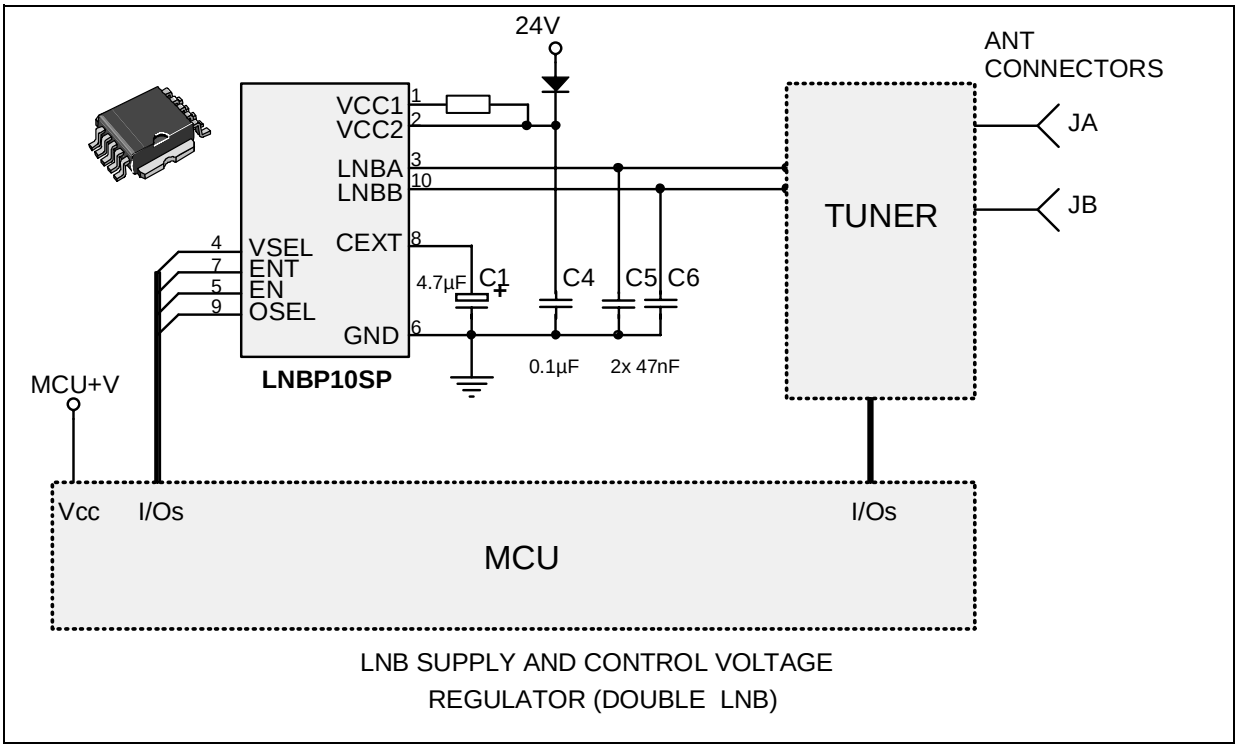
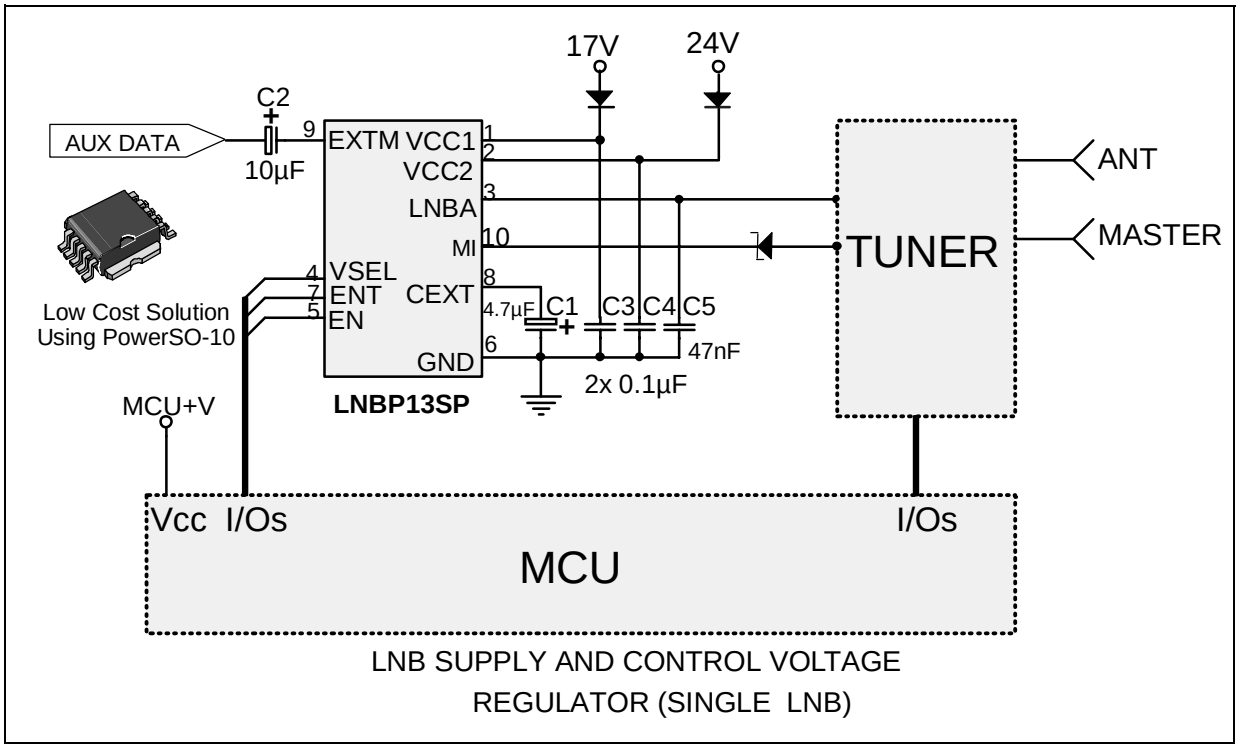
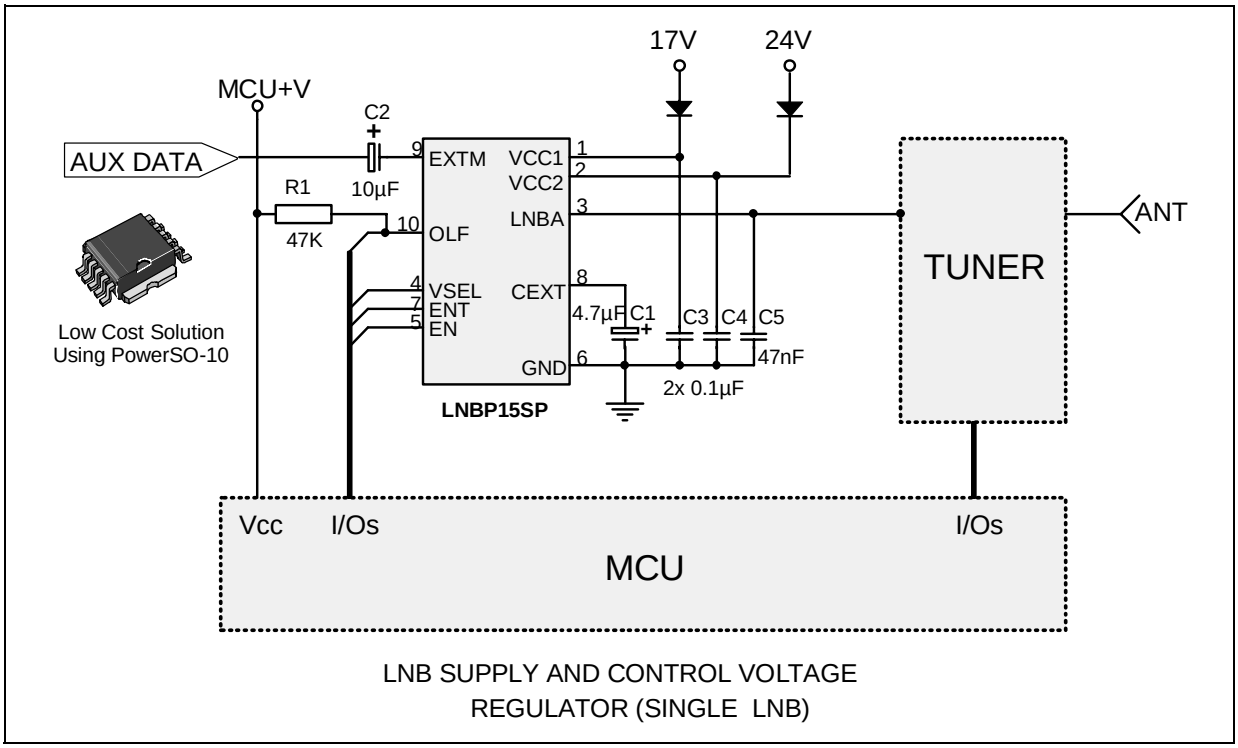


Figure 28: Single Antenna Receiver with Master Port



LNB SUPPLY AND CONTROL VOLTAGE
REGULATOR (SINGLE LNB)

Figure 29: Single Antenna Receiver Overload Diagnostic



LNB SUPPLY AND CONTROL VOLTAGE
REGULATOR (SINGLE LNB)