AN1550
APPLICATION NOTE

LNBP21: A DiSEqC™ 2.0 COMPLIANT SINGLE SUPPLY SOLUTION FOR LNB POWER AND LOGIC CONTROL

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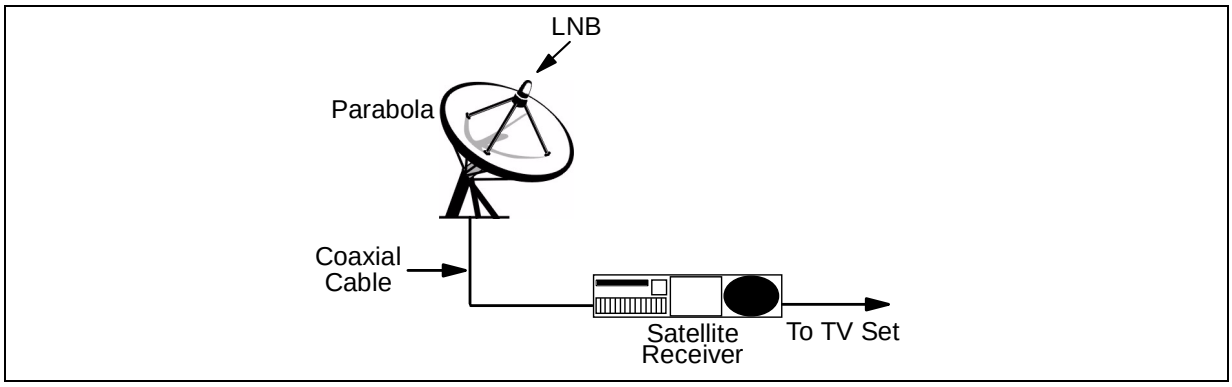
1. INTRODUCTION.

A typical satellite receiver system is formed by the blocks reported in figure 1:
- The **parabola** is the antenna of the system and focuses the satellite signal to the LNB;
- The **LNB (low noise block)** is placed on the focus of the parabola and converts the incoming signal in the 10GHz range to a lower frequency signal (in the 1-2GHz range) called "first conversion signal".

Figure 1: Basic Satellite TV Installation



This allows the signal to be carried by an inexpensive coaxial cable towards the receiver. Additionally it improves the first conversion signal level by a built-in low noise amplifier. A universal LNB can change polarization type (Horizontal or Vertical) or operative band by command signals sent by the receiver.

- The **coaxial cable** joins the LNB to the receiver and carries out 3 functions:
a) to transfer the first conversion signal from the LNB to the receiver;
b) to transfer command signals from the receiver to the LNB to change polarization or signal band;
c) to carry the DC voltage to supply the LNB.

- The **receiver** converts the first conversion signal in control signals for the TV system.

The **supply/interface block** is placed inside the receiver, which provides for two important features:
- to supply the LNB block
- to generate all the signals/voltages that LNB needs to operate correctly.

The supply/interface block must perform the following functions:
- be ready to accept future digital standards with an external modulation input and fast oscillator start-up;
- implement the loop-through function in slave condition for single dish, multiple receiver system;

- accept the paralleling of 2 or more receivers and in this condition avoid the flow of reverse current from the output to GND;
- give accurate, thermal compensated outputs with the possibility to compensate the DC voltage drop caused by long coaxial cables;
- be reliable;
- provide overload (better if a dynamic one) and thermal protection with diagnostic;
- avoid every type of trimming;
- provide the possibility to be driven by a microcontroller or a simple digital logic to implement all these functions;
- it must be cheap and get a small area on the board.

All these functions are hard to be implemented with discrete components, but are greatly made easier by using an integrated device as like LNBP21 that has been specially designed for the purpose.

1.2. LNBP21.

LNBP21 is the integrated solution for supplying/interfacing satellite LNB modules. It gives good performance in a simple and economical way, with minimum use of external components. It comprises a lot of functions that allow to realize LNB supplying/interfacing in accordance to the international standards. Besides, it includes an I^2C™(*) bus interface and, thanks to an integrated step-up DC/DC controller, it works with a single input voltage supply.

2. BLOCK DIAGRAM GENERAL DESCRIPTION.

Here below a description of the LNBP21 internal blocks.

2.1. Step-up Controller.

The LNBP21 has a built in step-up DC/DC converter controller that, from a single supply source ranging from 8V to 15V, generates the voltages that let the linear post-regulator work at a minimum power dissipation. The DC/DC converter external components will be connected to the Gate, Sense and VUP pins.

2.2. Preregulator + U. V. Lockout + P. On Reset.

This block includes a 5V voltage reference connected to the Byp pin, an **Undervoltage Lockout** circuit, intended to disable the whole circuit when the supplied Vcc drops below a fixed threshold (6.7V typ.), and a Power On Reset that sets all the I^2C registers to zero when the Vcc is turned on and rises from zero above the on threshold (7.3V typ).

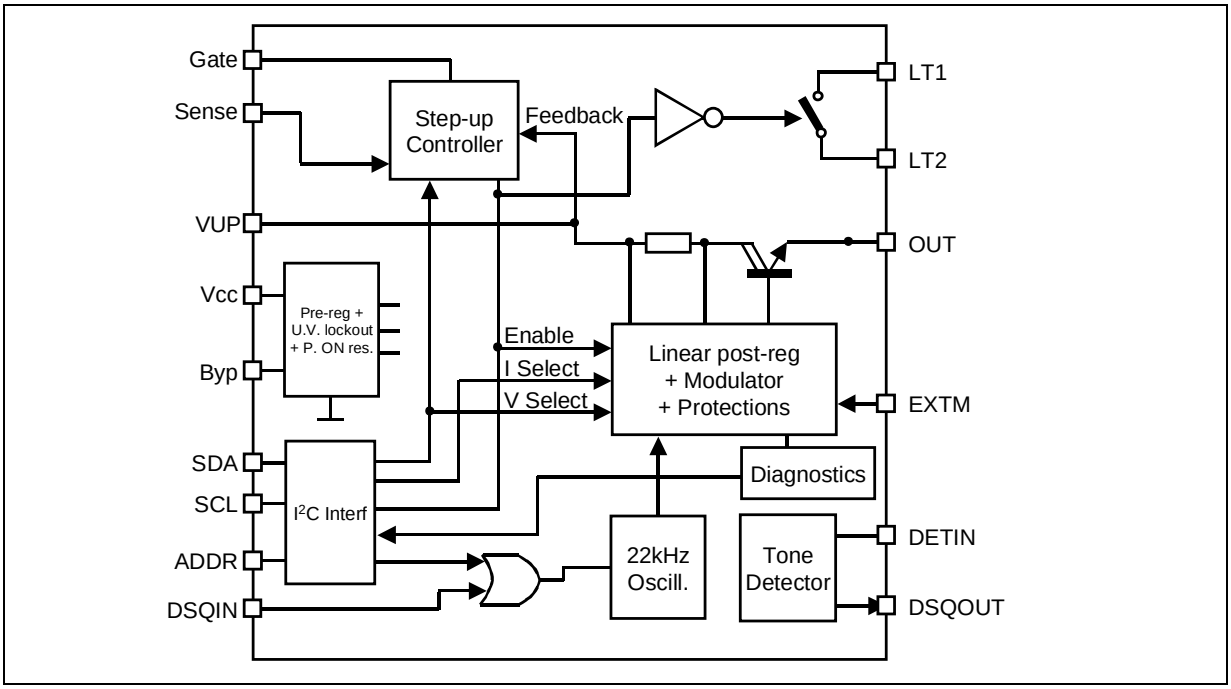
2.3. I^2C Interface.

All the functions of this IC, except for the DETIN/ DSQOUT, are controlled via I^2C bus by writing 6 bits on the System Register (SR, 8 bits). The same register can be read back, and two bits will report the **diagnostic** status. The LNBP21 I^2C interface Address can be selected among four different addresses by setting the voltage level of the dedicated ADDR pin.

2.4. 22kHz Oscillator.

The internal 22kHz tone generator is factory trimmed in accordance to the standards, and can be controlled either by the I^2C interface or by a dedicated pin (see DSQIN in figure 2) that allows immediate DiSEqC™(**) data encoding. The rise and fall edges are controlled to be in the 5µs to 15µs range, 8µs typ., to avoid RF pollution towards the receiver. The Duty cycle is 50% typ. It modulates the DC output with a ± 0.35V amplitude and 0V average.

Figure 2: Block Diagram



2.5. Tone Detector.

This block provide a complete circuit to decode the 22kHz burst code present on the DETIN pin in a digital signal by the DSQOUT pin where an open drain MOSFET is connected.

2.6. Loop-Through Switch (LT1-LT2).

An internal switch, connected to the LT1 and LT2 pins, allows the MASTER INPUT function needed to transfer the output of a Master unit connected to the LT1 pin when the device is set in shut-down by setting the I^2C EN bit low. This case occurs when two receivers are connected in series and the slave receiver (the nearest to the antenna) is disabled. The master receiver can supply the LNB via the LT1 input of the slave one.

2.7. Linear Post-reg + Modul. + Protection.

The output voltage selection, the 22kHz tone and the current selection commands join this block that manages all the LNB output function. This block gives feedback to the I^2C interface, by the **Diagnostics** block regarding the status of the Thermal Protection, Over Current Protection and OUT port settings.

The **EXTM** pin connected to this block can be used to provide an external Tone generator (up to 50kHz)

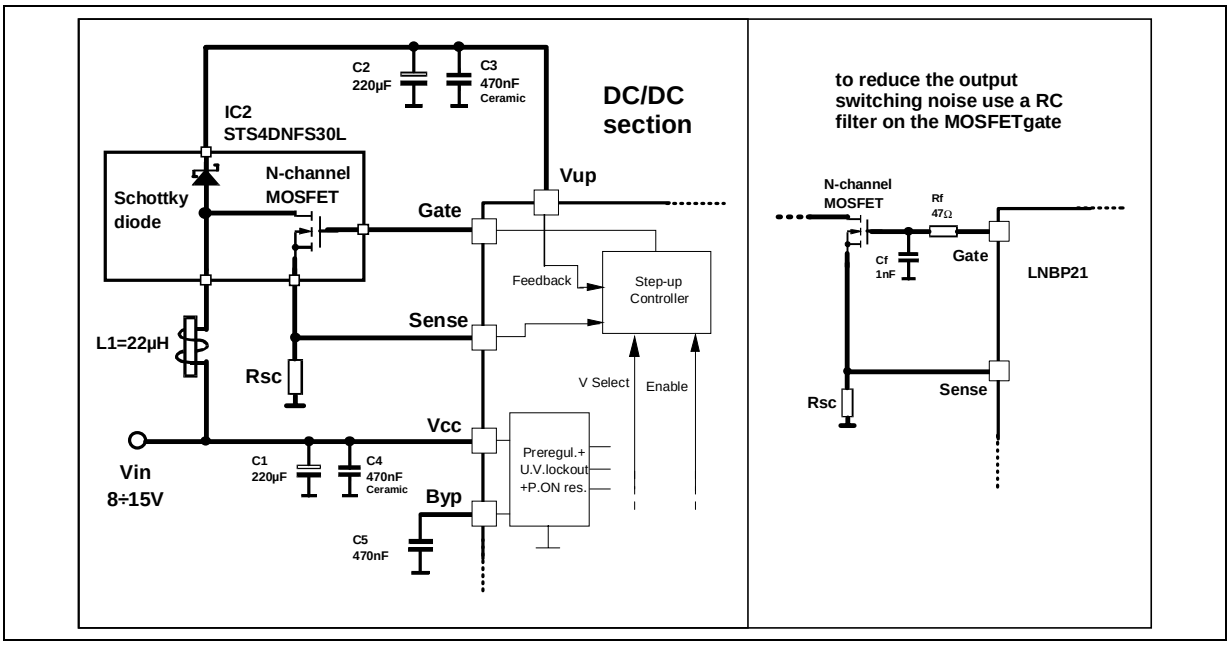
that will be amplified (gain is typ. 5) and superimposed to the output voltage when the LNB output is enabled. Moreover, the EXTM pin can be used to slightly increase or decrease the LNB output voltage by connecting an external resistor respectively between this pin and ground or between this pin and the OUT port.

3. EXTERNAL COMPONENT SELECTION.

3.1. DC/DC Converter.

The DC/DC converter controlled by the integrated step-up circuitry supplies the linear post-regulator and is connected to its input by the VUP pin. The step-up controller keeps the drop voltage across the linear post-regulator at 3.5V typ. at all the LNBP21 output condition (13V, 14V, 18V or 19V). Figure 3 shows the schematic related to the DC/DC converter section.

Figure 3: Step-up External Components



3.2. Inductor.

The LNBP21 operate with a standard 22µH inductor for the entire range of supply voltages and load current. The Inductor saturation current rating (where inductance is approximately 70% of zero current inductance) must be greater than the switch peak current (Ipeak) calculated at:
-maximum load (IOUT max);
-minimum Input Voltage (VIN min);
-maximum DC/DC output voltage (VUP max =VOUT max +3.5V typ.).

At this condition the switch peak current is given by the following formula:

$$I_{peak} = \frac{VUP_{max} \cdot IOUT_{max}}{Eff \cdot VIN_{min}} + \frac{VIN_{min}}{2LF}\left(1 - \frac{VIN_{min}}{VUP_{max}}\right) \qquad (1)$$

where: Eff. is the efficiency of the DC/DC converter (90% typ. at highest load), L is the inductance (22µH typ.), and F is the PWM frequency (220kHz typ.).

Table 1: Recommended Inductors

Vendor	Part Number	Isat (A)	DRC (mOhm)	Mounting Type
Sumida (www.sumida.com)	CD104-220MC RHC110-220M	1.6 2.4	67 88	SMD T.H.
Toko (www.tokoam.com)	822LY-220K 824LY-220K A671HN-220L A814LY-220M	1.3 1.72 2.44 2.0	70 76 21 75	T.H. T.H. T.H. SMD
Panasonic (www.panasonic.com)	ELC08D220E ELC10D220E	1.8 3.2	51 40	T.H. T.H.
Coilcraft (www.coilcraft.com)	DC1012-223 PVC-0-223-03 DO3316P-223	2.5 3 2.6	46 35 85	T.H. T.H. SMD

Several inductors that work well with the LNBP21 are listed in the table 1, although there are many other manufacturers and devices that can be used. Consult each manufacturer for more detailed information and for their entire selection of related parts, since many different shapes and sizes are available. Ferrite core inductors should be used to obtain the best efficiency. Choose an inductor that can handle at least the Ipeak current without saturating, and ensure that the inductor has a low DCR (copper wire resistance) to minimize I^2R power losses and, consequently, to maximize the total Efficiency.

3.3. Sense Resistor (R_{SC}).

As well as the Inductor saturation current, also the sense resistor value must be set taking in consideration the switch peak current calculated by the Equation 1. Being the DC/DC switch current feedback achieved by the drop voltage on this external resistor connected on the Sense pin, the peak current rating is set by the Rsc value calculated from Equation 2:

$$R_{SC} < \frac{V_{sense}}{I_{peak}} \qquad (2)$$

where Vsense is 200mV typ. (see datasheet on page 10) and Ipeak is calculated from Equation 1. Make sure the R_{SC} value is always lower than the Vsense / Ipeak ratio.
In the typical application condition (Vcc=12V, IOUT(max)=500mA) a 100mOhm Rsc is a good choice.
If VIN<10.5V the inductor peak current can be close to 2A, than, it is necessary to decrease the R_{SC} value. In the worst case with: VIN=8V, and IOUT=500mA, taking in account the internal comparator tolerance, we suggest to use an RSC of 0.05W.
Low cost axial through-hole resistors could also be used but of course these are usually bigger and need a larger area on the PCB.
See table 2 for some suggested SMD resistor part numbers.

Table 2: Sense Resistor Suppliers

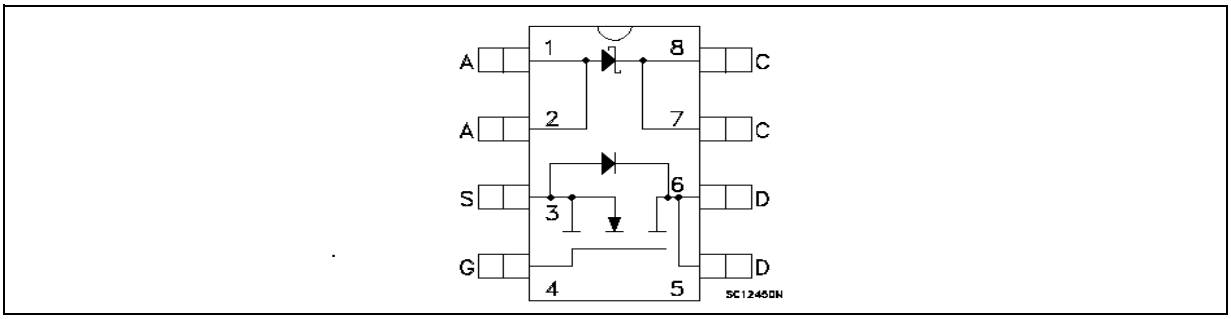
Series	Manufacturer	Web Site
RL73	MEGGITT	www.meggittelectronics.com
ML2512	RCD Components	www.rcd-comp.com
RL2512	PACCOM Electronics	www.paccom.com
RL2512	COOLTRON	www.cooltron.com
RMC1	SEI Electronics	www.seielect.com

3.4. Power Transistor & Schottky Diode.

It is profitable to use a FETTKY like **STS4DNFS30L** (see IC2 in figure 3) that is an integrated solution including a 30V 4A N-Channel MOSFET and a 3A Schottky diode suitable for all the LNBP21 and LNBS21 DC/DC converter application conditions. Compared to discrete solution the STS4DNFS30L is cost effective and helps to reduce the layout area. Figure 4 shows the STS4DNFS30L SO-8 package pin configuration.

Nevertheless, it is possible to use two separate devices; in this case, we suggest the n-channel MOSFET STN4NF03L (or similar) in SOT-89 package, and a 2A schottky diode like STPS2L30A for the LNBP21, while, we suggest the 3A schottky diode STPS3L40S (or similar) for the LNBS21 application.

Figure 4: STS4DNFS30L's SO-8 Pin Configuration



3.4. Output Capacitors.

Two capacitors are needed on the DC/DC converter output stage (C2 and C3 in figure 3): a ceramic capacitor essential to reduce the high frequency switching noise, and a electrolytic one to filter the output voltage. The switching noise is due to the voltage spikes of the fast switching action of the output switch, and to the parasitic inductance of the output capacitors. To minimize these voltage spikes, special low inductance capacitors can be used, and their lead lengths must be kept short and as close as possible to IC pins.

The most important parameter for the output capacitors is low effective series resistance (ESR). The product of the peak inductor current and the output filter electrolytic capacitor's ESR determines the amplitude of the ripple seen on the output voltage. A 220µF output filter capacitor with ESR lower than 100mOhm in parallel with a 470nF ceramic capacitor is a good choice in most application conditions. Higher value and lower ESR will strongly reduce the output ripple voltage and output switching noise. Smaller value and/or higher ESR capacitors are acceptable for light loads. Since the output filter capacitor's ESR affects efficiency, use low ESR capacitors for best performance.

The capacitor's voltage rating should be at least 35V but higher voltage electrolytic capacitors generally have lower ESR numbers, and for this reason, to select a capacitor rate for a higher voltage, would

normally improve the DC/DC performances in terms of output ripple and efficiency. See Table 3 for component selection.

Table 3: Capacitor Suppliers

Vendor	Series	Mounting Type
Sanyo (www.sanyo.com)	OS-CON Electrolytic	Through hole
Nichicon (www.nichican.com)	PL Electrolytic	Through hole
Panasonic (www.panasonic.com)	HFQ electrolytic	Through hole
Sprague Phone (603) 224-1961	594D electrolytic	SMD
Taiyo-Yuden (www.t-yuden.com)	Ceramic	SMD
AVX (www.avxcorp.com)	Ceramic	SMD
Murata (www.murata.com)	Ceramic	SMD

3.4. Input Capacitors.

An electrolytic bypass capacitor (C1 in figure 3) between 100µF and 470µF located close to the LNBP21 is needed for stable operation. Besides, a ceramic capacitor (C4 in figure 3) between 220nF and 470nF is recommended to reduce the switching noise at the input voltage pin.

3.6. Layout Guidelines.

Due to high current levels and fast switching waveforms, which radiate noise, a proper PC board layout is essential. Protect sensitive analog grounds by using a star ground configuration.

Also, minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. Minimize ground noise by connecting GND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Place input bypass capacitors (C1, C4) as close as possible to Vcc and GND and the DC/DC output capacitors (C2, C3) as close as possible to VUP. Excessive noise at the Vcc input may falsely trigger the Under Voltage circuitry, resetting the I^2C internal registers. If this occurs it will set all the registers to zero setting the LNBP21 in shutdown mode.

In order to reduce the switching noise it is possible to add an R-C filter on the MOSFET gate as shown in figure 3.

4. DiSEqC IMPLEMENTATION.

The LNBP21 has a built-in 22kHz tone generator that can be controlled either by the I^2C interface or by a dedicated pin (see DSQIN in figure 2) that allows immediate DiSEqC data encoding for the DiSEqC compliance. When the I^2C tone enable bit (TEN) is set to HIGH, a continuous 22kHz tone is generated regardless of the DSQIN pin logic status. The TEN bit must be set LOW when the DSQIN pin is used for DiSEqC encoding.

4.1. DiSEqC 2.x.

Besides the unidirectional DiSEqC 1.x compliance, the LNBP21 is also compliant to the bi-directional DiSEqC 2.x specification thanks to its built-in 22kHz Tone-Detector that allows a fully bi-directional DiSEqC interfacing. The tone detector input pin (see DETIN in figure 5) must be AC coupled to the DiSEqC bus, and the extracted PWK data are available on the DSQOUT pin. The DSQOUT pin is internally connected to an open-drain MOSFET at which must be connected an external pull-up resistor as shown in figure 4. By using the circuit in figure 4, when a 22kHz tone is detected on the DETIN, the MOSFET is set on, otherwise the MOSFET is open. The PWK data is decoded as (see figure 6):
0> Logic Level Low = if a 22kHz tone is present on the DETIN pin;
1> Logic Level High = when the DETIN do not detect any 22kHz tone presence.

The PWK data is exchanged between the LNBP21 and the main µP using logic levels that are compatible with both 3.3V and 5V microcontrollers. This data exchange, made through two dedicated pins, DSQIN and DSQOUT, maintain a very accurate timing relationship between the PWK data and the PWK modulation.

Figure 5: DETIN/DSQOUT Circuit

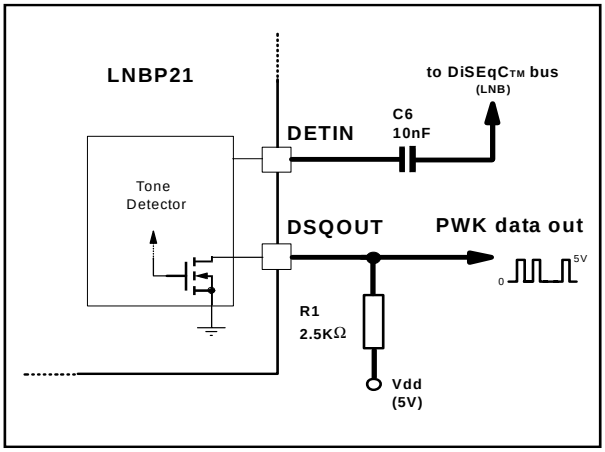
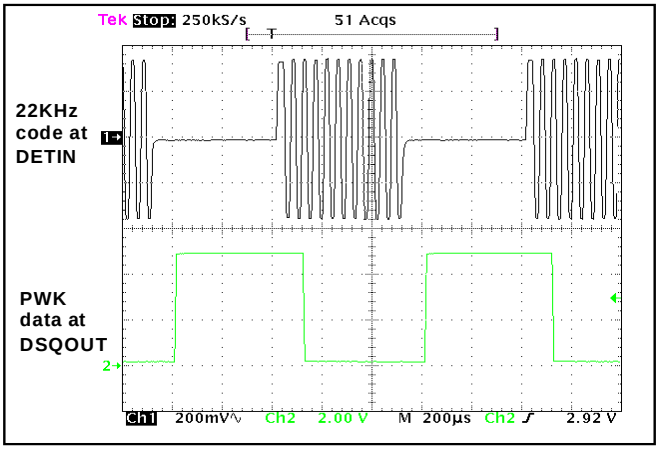


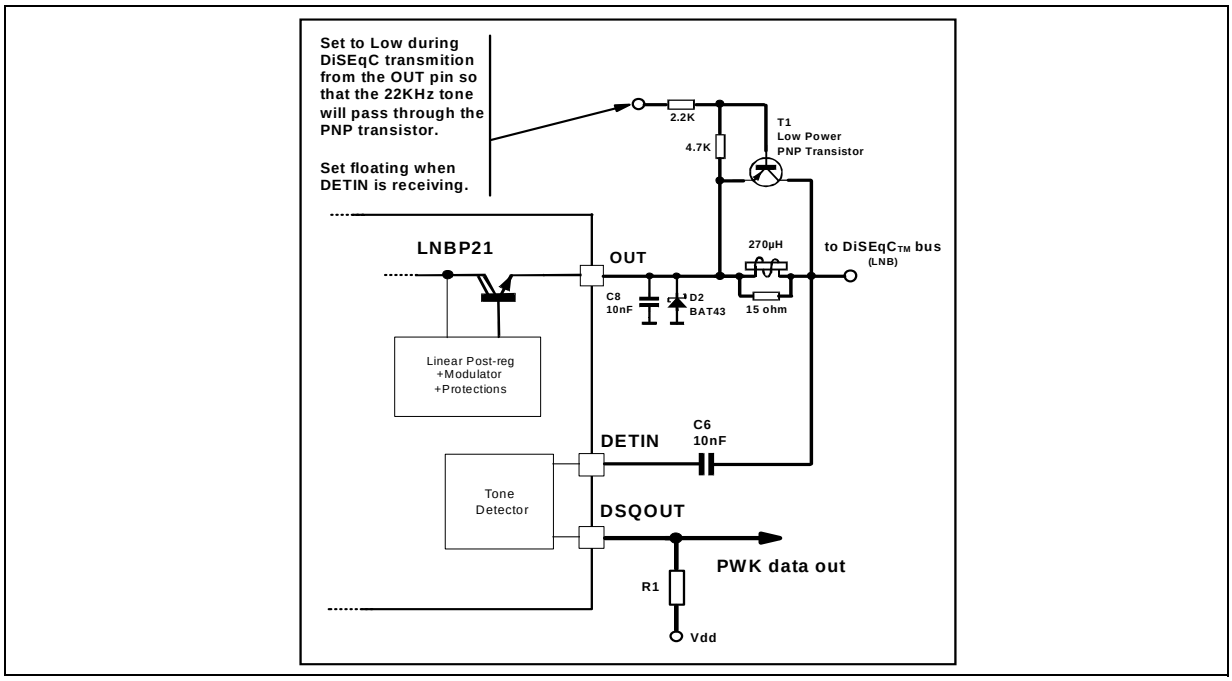
Figure 6: DETIN / DSQOUT Waveform



The DSQIN and DSQOUT pins should be directly connected to two I/O pins of the µP, thus leaving the resident firmware the task of encoding and decoding the PWK data in accordance to the DiSEqC™ protocol. Full compliance of the system to the specification is thus not implied by the bare use of the LNBP21.

The system designer should also take in consideration the bus hardware requirements that include the source impedance of the Master Transmitter measured at 22kHz. To limit the attenuation at carrier frequency, this impedance has to be 15ohm at 22kHz, dropping to zero ohm at DC to allow the power flow towards the peripherals. This can be simply accomplished by the LR termination put on the OUT pin of the LNBP, as shown in figure 7.

Figure 7: DiSEqC 2.x Implementation



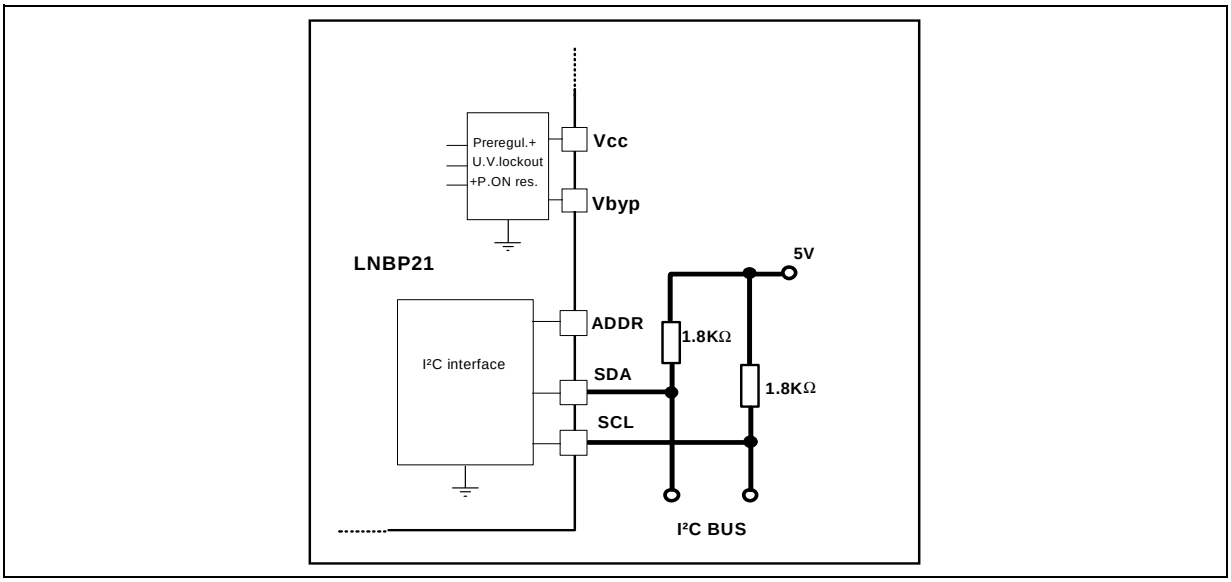
In some cases the output LR filter may cause some distortion of the 22kHz tone coming from the LNBP21 OUT pin (especially with high DiSEqC bus capacitance and light load). It is possible to solve this problem by connecting a simple PNP transistor (500mA, 45V, general purpose transistor) as shown in figure 6. The input pin of this additional circuit (base of PNP through the 2.2KOhm resistor) must be set to a low level voltage during DiSEqC transmission from the LNBP21 OUT pin, so that the 22kHz tone will pass through the PNP transistor without any distortion, while it can be left floating when the DETIN is receiving the 22kHz code from the DiSEqC bus.

Unidirectional (1.x) DiSEqC and non-DiSEqC systems normally do not need this termination, and the OUT pin can be directly connected to the LNB supply port of the Tuner. There is also no need of Tone Decoding, thus DETIN and DSQOUT pins can be left unconnected (in this case connecting the DETIN pin to ground to avoid any switching noise into the tone detector circuit is suggested).

5. I²C BUS INTERFACE.

Thanks to the integrated I²C interface, Data transmission from main µP to the LNBP21 and vice versa takes place through the 2 wires I²C bus interface, consisting of the two lines SDA and SCL. Pull-up resistors to positive supply voltage must be externally connected only if not already present on the I²C bus lines. Two 1.8kOhm resistors are a good choice (see figure 8).

Figure 8: I²C Bus Push-pull Resistors



5.1. Clock Frequency.

The I²C interface is compatible with the I²C fast mode specification that allows a bit rate up to 400Kbit/s.

5.2. System Register Reset.

Because the LNBP21 has an integrated under-voltage lockout circuit, particular attention must be kept to the input voltage level (Vcc). In fact if the input voltage drops below a fixed threshold (6.7V typically with about 500mV of hysteresis), the I²C system registers is reset to zero and the whole LNBP21 is set in stand-by condition thus keeping the power blocks disabled. Once the Vcc rises above 7.3V, the I²C interface becomes operative and the SR can be configured by the main µP. This is due to about 500mV of hysteresis provided in the UVL threshold to avoid false retriggering of the Power-On reset circuit.

5.3. I²C Interface Address.

The LNBP21 integrated I²C interface has 4 different addresses selectable by simply setting the ADDR pin between one of the 4 different voltage ranges as shown on table 4. Figure 9 shows how it is possible to select the I²C interface address by using the LNBP21 bypass voltage pin. Of course, by selecting the I²C interface address it is possible to set the ADDR pin by using any other supply voltage source in the range from 0V to 5V.

Figure 9: Address Pin Voltage Setting

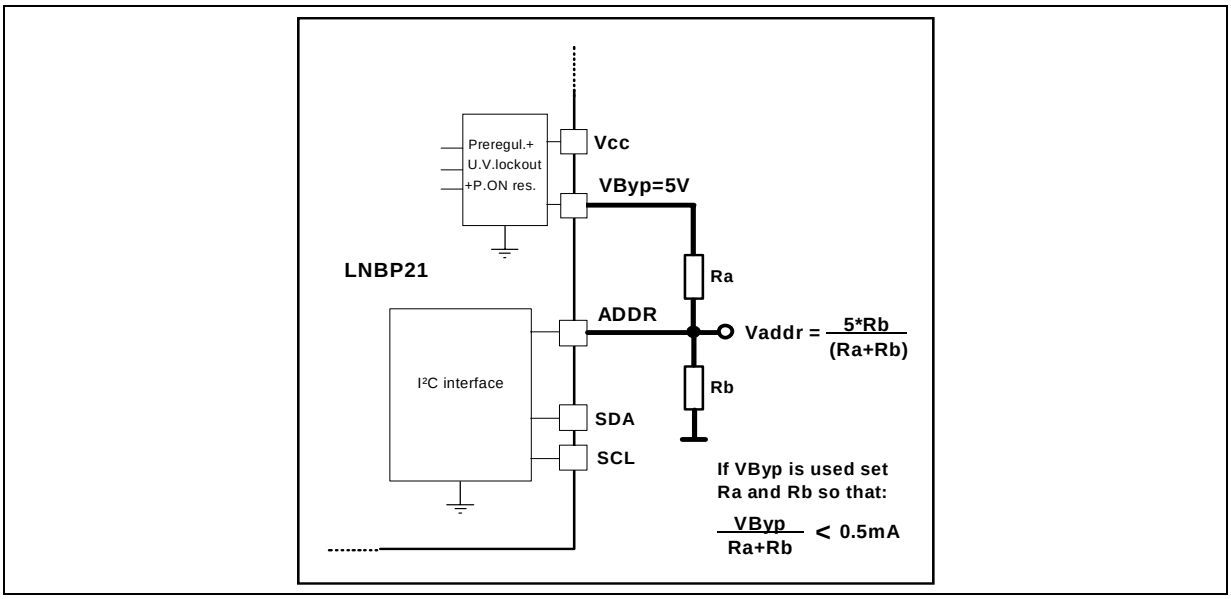


Table 4: Address Pin Voltage Range

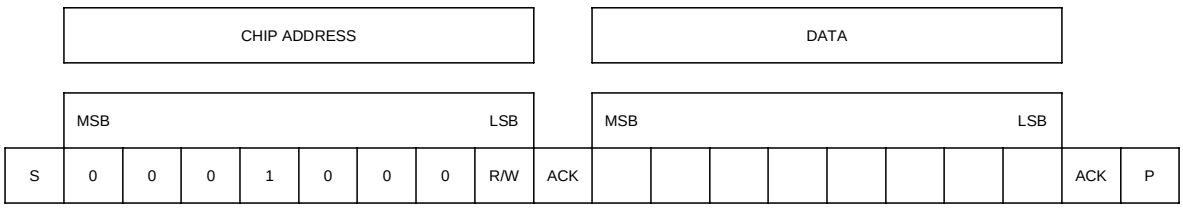
I²C™ Interface Address	MIN (V)	TYP (V)	Max (V)
0001000	0	-	0.7
0001001	1.3	1.5	1.7
0001010	2.3	2.5	2.7
0001011	3.3	3.5	5

6. LNBP21 SOFTWARE DESCRIPTION.

6.1. Interface Protocol.

The interface protocol comprises:

- A start condition (S)
- A chip address byte = hex 10 / 11 (the LSB bit determines read(=1)/write(=0) transmission)
- A sequence of data (1 byte + acknowledge)
- A stop condition (P)



ACK=Acknowledge
S=Start
P=Stop
R/W=Read/Write

6.2. System Register (SR, 1 Byte).

MSB							LSB
R, W	R, W	R, W	R, W	R, W	R, W	R	R
PCL	ISEL	TEN	LLC	VSEL	EN	OTF	OLF

R, W=Read and Write bit
R=Read-only bit
All bits reset to 0 at Power-On

6.3. Transmitted Data (I^2C™ Bus WRITE MODE).

When the R/W bit in the chip address is set to 0, the main µP can write on the System Register (SR) of the LNBP21 via I^2C bus. Only 6 bits out of the 8 available can be written by the µP, since the remaining 2 are left to the diagnostic flags, and are read-only.

PCL	ISEL	TEN	LLC	VSEL	EN	OTF	OLF	FUNCTION
			0	0	1	X	X	VOUT=13V, VUP=16V, Loop-through switch open
			0	1	1	X	X	VOUT=18V, VUP=21V, Loop-through switch open
			1	10	1	X	X	VOUT=14V, VUP=17V, Loop-through switch open
			1	1	1	X	X	VOUT=19V, VUPVUP=22V, Loop-through switch open
		0			1	X	X	22kHz tone is controlled by DSQIN pin
		1			1	X	X	22kHz tone is ON, DSQIN pin disabled
	0				1	X	X	IOUT(min)=500mA, IOUT(max)=650mA, Isc=300mA
	1				1	X	X	IOUT(min)=400mA, IOUT(max)=550mA, Isc=200mA
0					1	X	X	Pulsed (dynamic) current limiting is selected
1					1	X	X	Static current limiting is selected
X	X	X	X	X	0	X	X	Power blocks disabled, Loop-through switch closed

X = do not care
Values are typical unless otherwise specified

6.4. Received Data (I^2C bus READ MODE).

The LNBP21 can provide to the Master a copy of the SYSTEM REGISTER information via I^2C bus in read mode. The read mode is Master activated by sending the chip address with R/W bit set to 1. At the following master generated clock bits, the LNBP21 issues a byte on the SDA data bus line (MSB transmitted first).

At the ninth clock bit the MCU master can:
- acknowledge the reception, starting in this way the transmission of another byte from the LNBP21;
- not acknowledge, stopping the read mode communication.

While the whole register is read back by the µP, only the two read-only bits OLF and OTF convey diagnostic informations about the LNBP21.

7. OUTPUT VOLTAGE TRIMMING.

7.1. VOUT Trimmings (DirecTV 2.2 Compliance).

The purpose of this section is to show how it is possible to slightly increase the VOUT value with the use of one external resistor on the EXTM pin in order to meet the DirecTV specification which requires that the VOUT values be higher than the ones guaranteed by the LNBP21 specification.

Figure 12 shows the internal EXTM block diagram. The inserted resistor (Rext), being in parallel with R3, modifies the output voltage divider (in this case reducing one of the resistors that compose it). Adding the Rext the VOUT will be:

$$VOUT = \frac{V_{ref}}{R_2 + (R_3 \parallel R_{ext})} \cdot [R_1 + R_2 + (R_3 \parallel R_{ext})] \qquad (3)$$

Please refer to figures 10 and 11 for the typical VOUT value vs Rext.

Figure 10: VOUT vs Rext

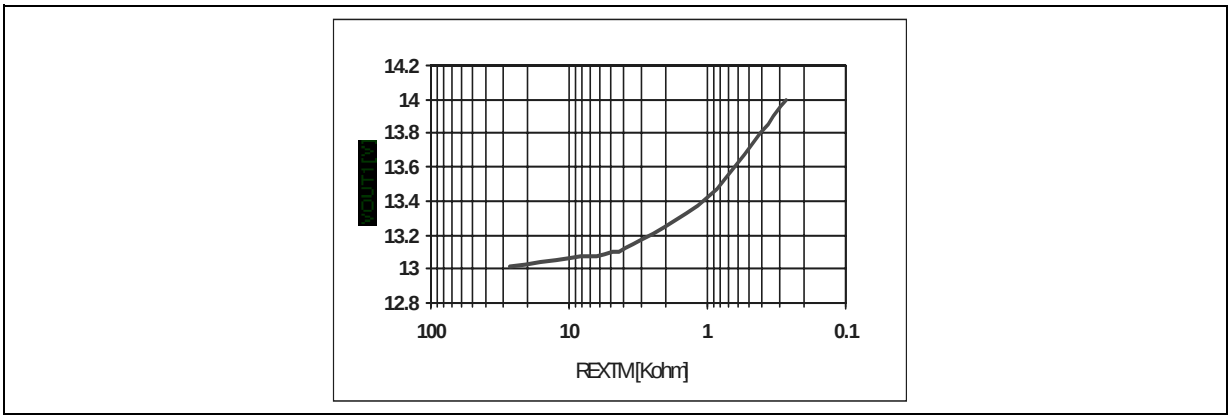


Figure 11: VOUT vs Rext

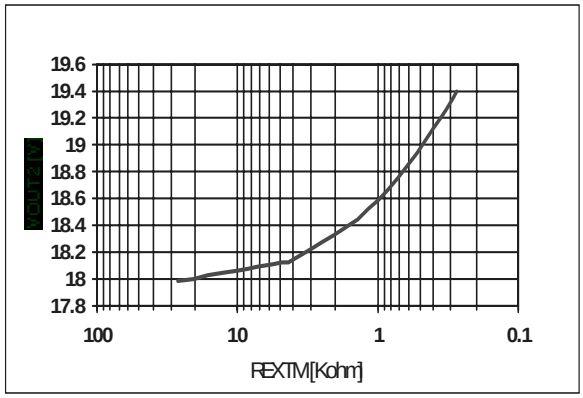
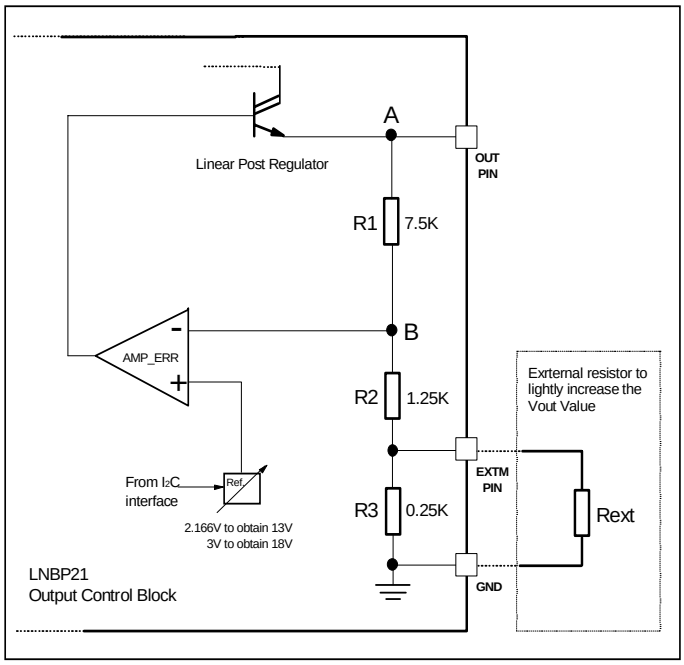


Figure 12: EXTM Resistor For VOUT Increase



7.2. Resistors Tolerance.

Feedback resistors are body resistors. Body resistors have a guaranteed maximum tolerance of ±20%; this is due to process spread. The resistors ratio is kept within the ±2% tolerance range with a proper resistors matching.

Natural reference tolerance is ±3%.

7.2. Example: DirecTV Recommendations.

DirecTV recommended VOUT ranges are:
- from 17.75V to 21.0V for the (VOUT)LOW;
- from 12.75V to 14V for the (VOUT)HIGH.

Instead the LNBP21 specified range is:
- from 17.30V to 18.70V when the high voltage is selected (Vsel pin HIGH);
- from 12.50V to 13.50V when the low voltage is selected (Vsel pin LOW).

In order to meet the DirecTV requirement, VOUT typical values must be modified with the use of an external resistor. The best resistor value to be chosen, in this case, is 1kohm. This value will allow designers to meet min/max values specified in the DirecTV 2.2 spec, also taking into account the internal voltage reference tolerance and the internal resistor bridge tolerance. The tolerance of the external resistor has very little impact on VOUT variation. For example, if a 1% tolerance is chosen for the external resistor, VOUT will vary by less than 0.1%.

8. PROTECTIONS.

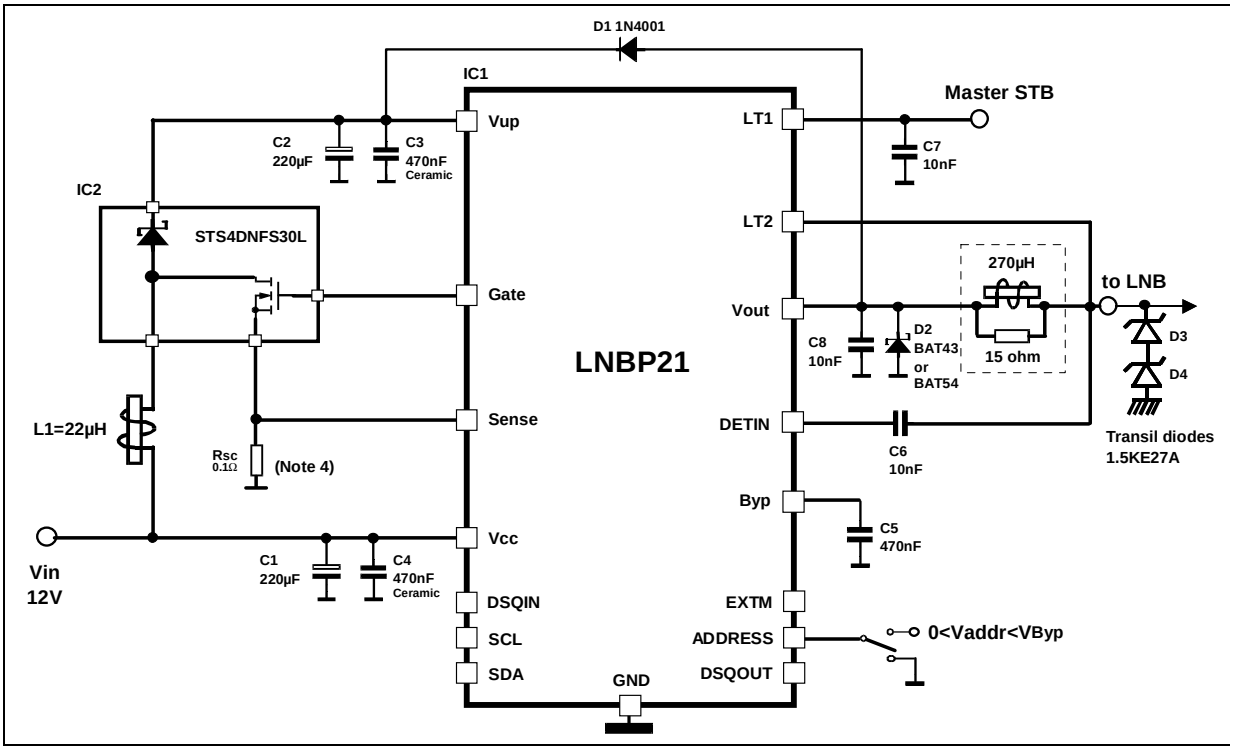
8.1. Output Pin Protection.

Because the output pins are directly connected to the coaxial cable and then to the dish, it is very important to protect the application from any external voltage overstress coming from the coaxial cable connectors (such as: ESD, lightning surge, erroneous plug connections, etc.). The LNBP21 output pins are guaranteed up to 4kV with the HBM model HBM-11C and Zap Method MIL-STD 883D-3015.7.

As shown in the typical application circuit in figure 13, we suggest to use some diodes:
- D1, a simple IN4001, or similar, to protect the device from any reverse current;
- D2, a low power and low cost Schottky diode (BAT43 and BAT54 are ST parts), to protect the device from any negative voltage stress higher than -0.3V.

Finally, in order to protect the device from lightning surges we strongly suggest to add on the output pins two transil diodes in series. This solution has no problem with VBR matching; the 2 TVs breakover at the same time and dissipate the same energy.

Figure 13: Typical Application Circuit



As shown in figure 13, we suggest to use two 1.5KE15A (ST part number); with this devices each 1.5KE15A can dissipate 368A–8/20us with a total of 736A–8/20µs (i.e. 11kW – 8/20µs). Moreover two 1.5KE15A in series have:

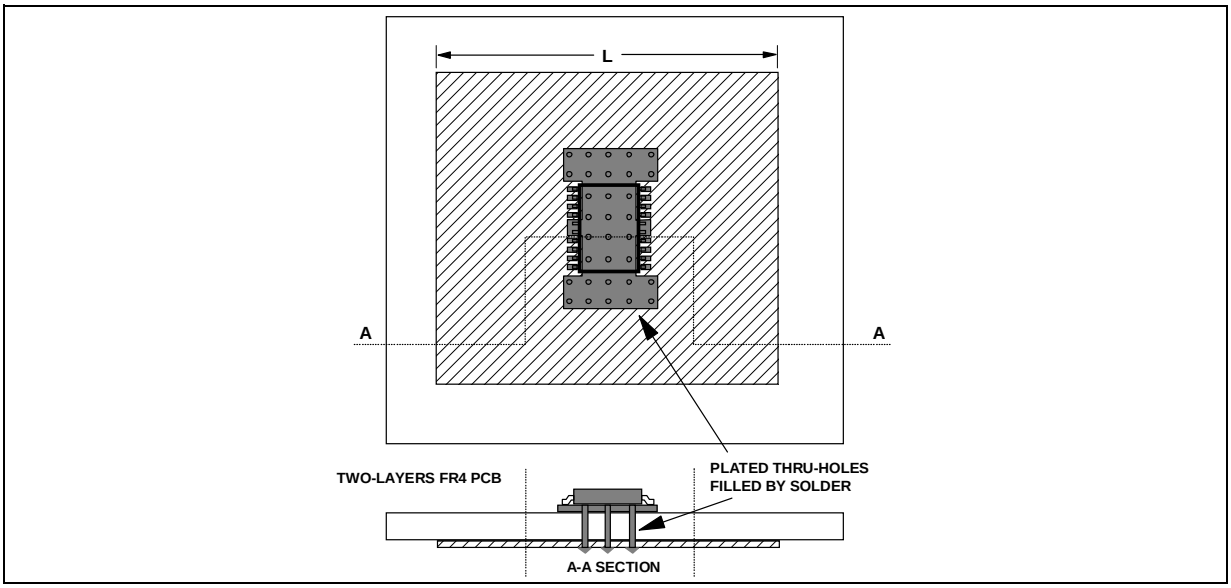
- Stand-off voltage VRM=25.6V @1uA;
- Clamping VBRmin=28.6V@1mA.

9. THERMAL DESIGN NOTES.

During normal operation, the device dissipates some power. At maximum rated output current (500mA), the voltage drop on the linear regulator leads to a total dissipated power that is 1.75W typ. The heat generated requires a suitable heatsink to keep the junction temperature below the overtemperature protection threshold. Assuming a 40°C temperature inside the Set-Top-Box case, the total Rthj-amb has to be less than 50°C/W. While this can be easily achieved using a through-hole power package that can be attached to a small heatsink or to the metallic frame of the receiver, a surface mount power package must rely on PCB solution whose thermal efficiency is often limited. The simplest solution is to use a large, continuous copper area of the GND layer to dissipate the heat coming from the IC body.

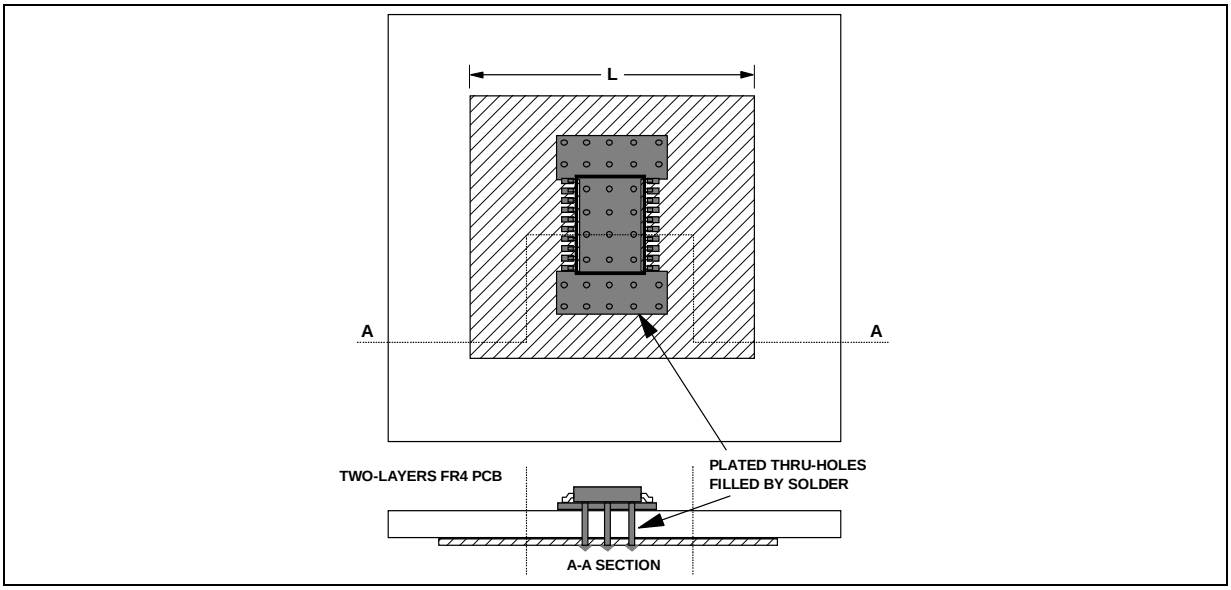
The SO-20 package of this IC has 4 GND pins that are not just intended for electrical GND connection, but also to provide a low thermal resistance path between the silicon chip and the PCB heatsink. Given an Rthj-c equal to 15°C/W, a maximum of 35°C/W are left to the PCB heatsink. This figure is achieved if a minimum of 25cm^2 copper area is placed just below the IC body. This area can be the inner GND layer of a multi-layer PCB or in a dual layer PCB, an unbroken GND area even on the opposite side where the IC is placed. In both cases, the thermal path between the IC GND pins and the dissipating copper area must exhibit a low thermal resistance.

Figure 14: SO-20 Suggested PCB Heatsink Layout



In figure 14, a suggested layout for the **SO-20** package with a dual layer PCB is shown, where the IC Ground pins and the square dissipating area are thermally connected through 32 via holes, filled by solder. This arrangement, when L=50mm, achieves an Rthc-a of about 25°C/W. Different layouts are possible too. Basic principles, however, suggest to keep the IC and its ground pins approximately in the middle of the dissipating area; to provide as many vias as possible; to design a dissipating area having a shape as square as possible and not interrupted by other copper traces.

Figure 15: PowerSO-20™ Suggested PCB Heatsink Layout



Due to the presence of an exposed pad connected to GND below the IC body, the **PowerSO-20™** package has an Rthj-c much lower than the SO-20, only 2°C/W. As a result, a much lower copper area must be provided to dissipate the same power and minimum of 12cm^2 copper area is enough, see figure 15.

10. DEMOBOARDS.

Figure 16: Demoboard Schematics

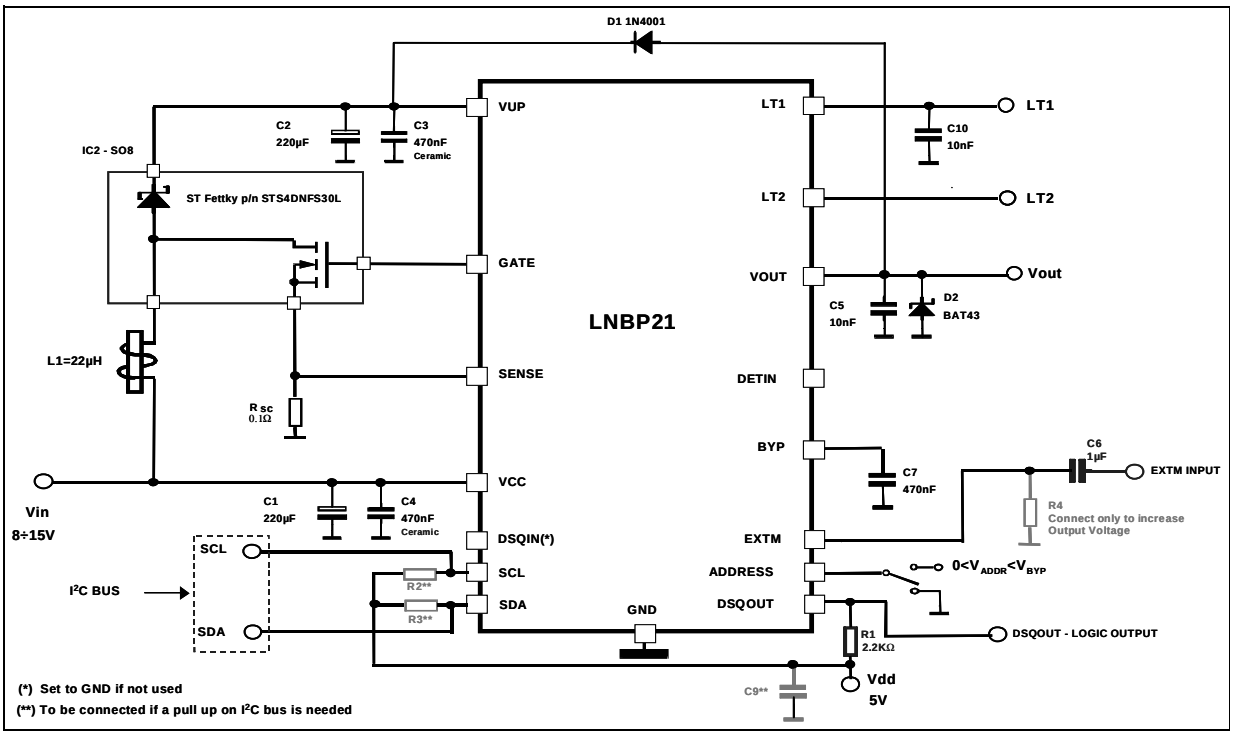
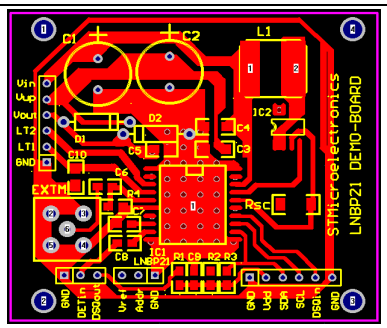
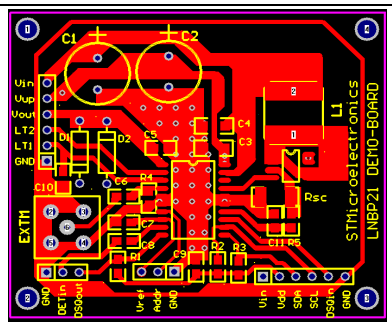


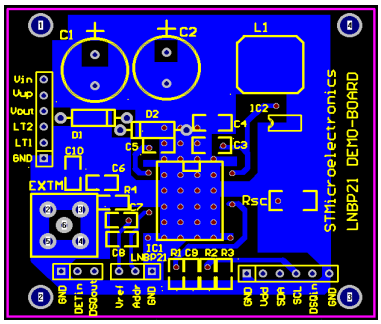
Figure 17: LNBP21 Demoboard PCB Layout



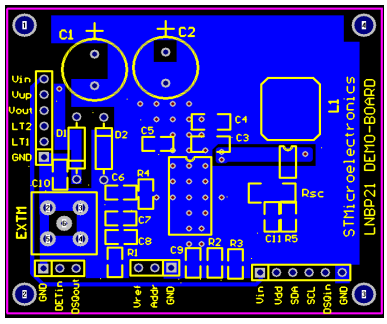
PSO20: Top Layer



SO20: Top Layer



PSO20: Bottom Layer



SO20: Bottom Layer