AN1624
APPLICATION NOTE

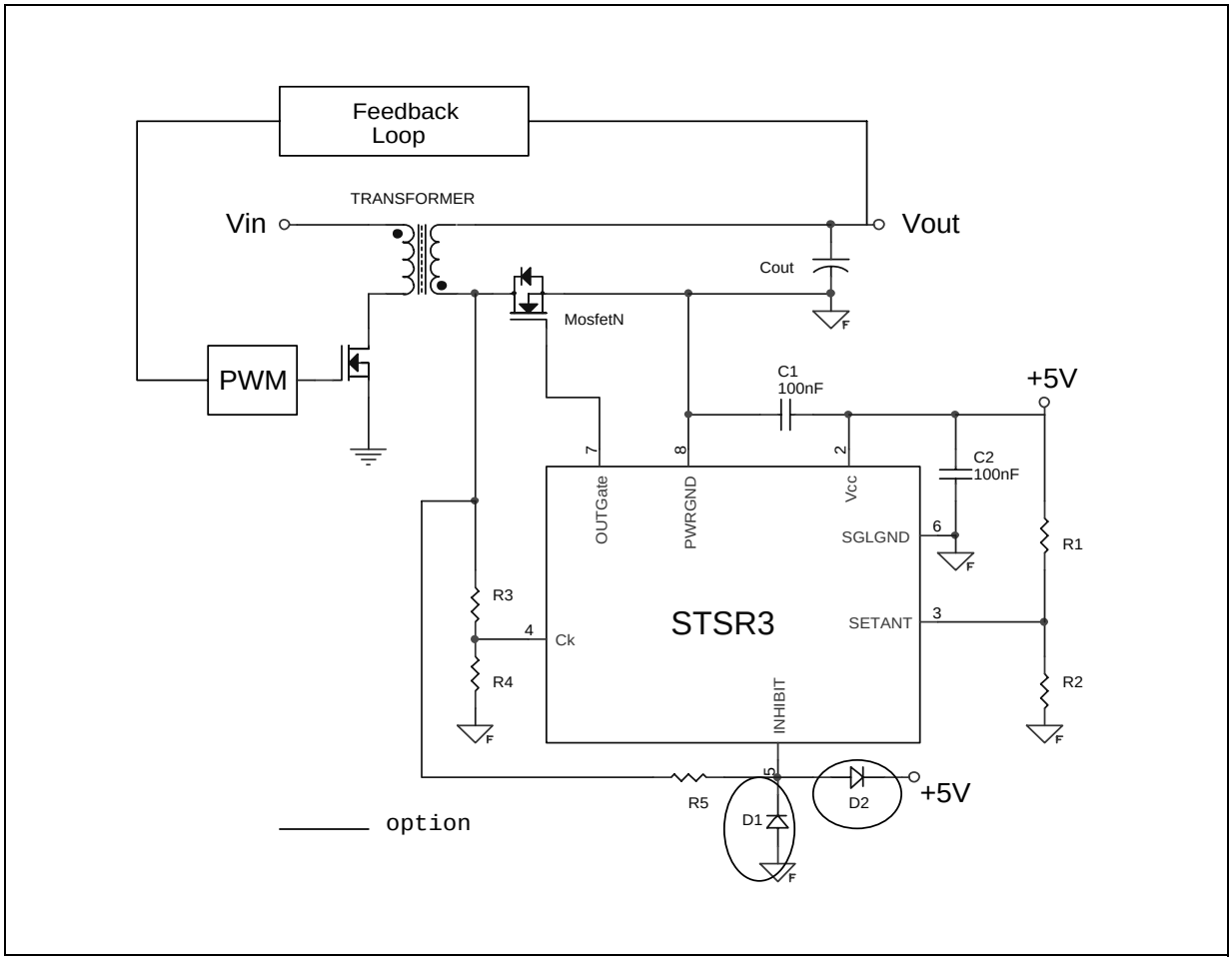
STSR3 SIMPLIFIES IMPLEMENTATION OF SYNCHRONOUS RECTIFIER IN FLYBACK CONVERTER

F. Librizzi - F. Lentini

1. ABSTRACT

This paper describes the functionality and the operation of the STSR3 device used as the secondary synchronous rectifier driver in Flyback topology switched mode power supplies. A Schematic and layout description of a demo board able to replace diode rectification with synchronous rectification in Flyback converters is shown below.

Figure 1: Typical Application Schematic



2. GENERAL DEVICE DESCRIPTION

The STSR3 Smart Driver IC provides a high current output to properly drive secondary Power Mosfets used as Synchronous Rectifiers in high output current, high efficiency Flyback Converters. From a synchronizing clock input, withdrawn on the secondary side of the isolation transformer, the IC generates a driving signal with set dead times with respect to the primary side PWM signal.

The IC operation prevents secondary side shoot-through conditions at turn-on of the primary switch providing anticipation in turn-off of the output. This smart function is implemented by a fast cycle-after-cycle logic control mechanism, based on a high frequency oscillator synchronized by the clock signal. This anticipation is externally set through external components.

A special Inhibit function allows shut-off of the drive output by sensing the Synchronous Rectifier source-drain voltage and consequently turning it off when necessary. This feature makes a discontinuous conduction mode possible and avoids reverse conduction of the synchronous rectifier in parallel operation of the converter.

The STSR3 allows implementing Synchronous Rectification in Discontinuous Mode PWM, Continuous Mode PWM and Quasi Resonant Flyback Converters.

3. PIN CONNECTIONS AND DESCRIPTIONS

The STSR3 is housed in an SO-8 package for SMD assembly. Device pin out is shown in figure 2 and table 1 briefly summarizes the device pin functionality.

Figure 2: Pin Configuration

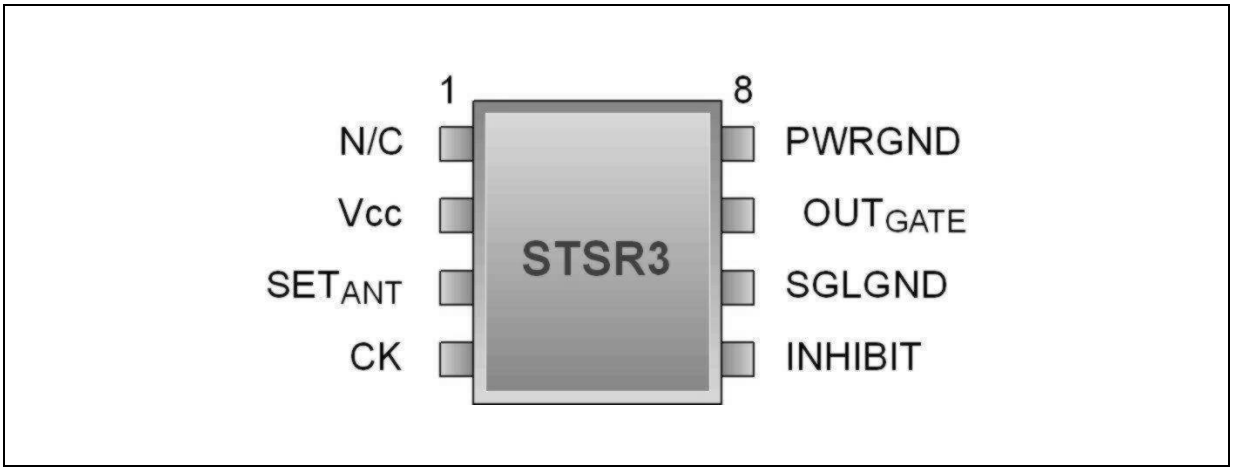
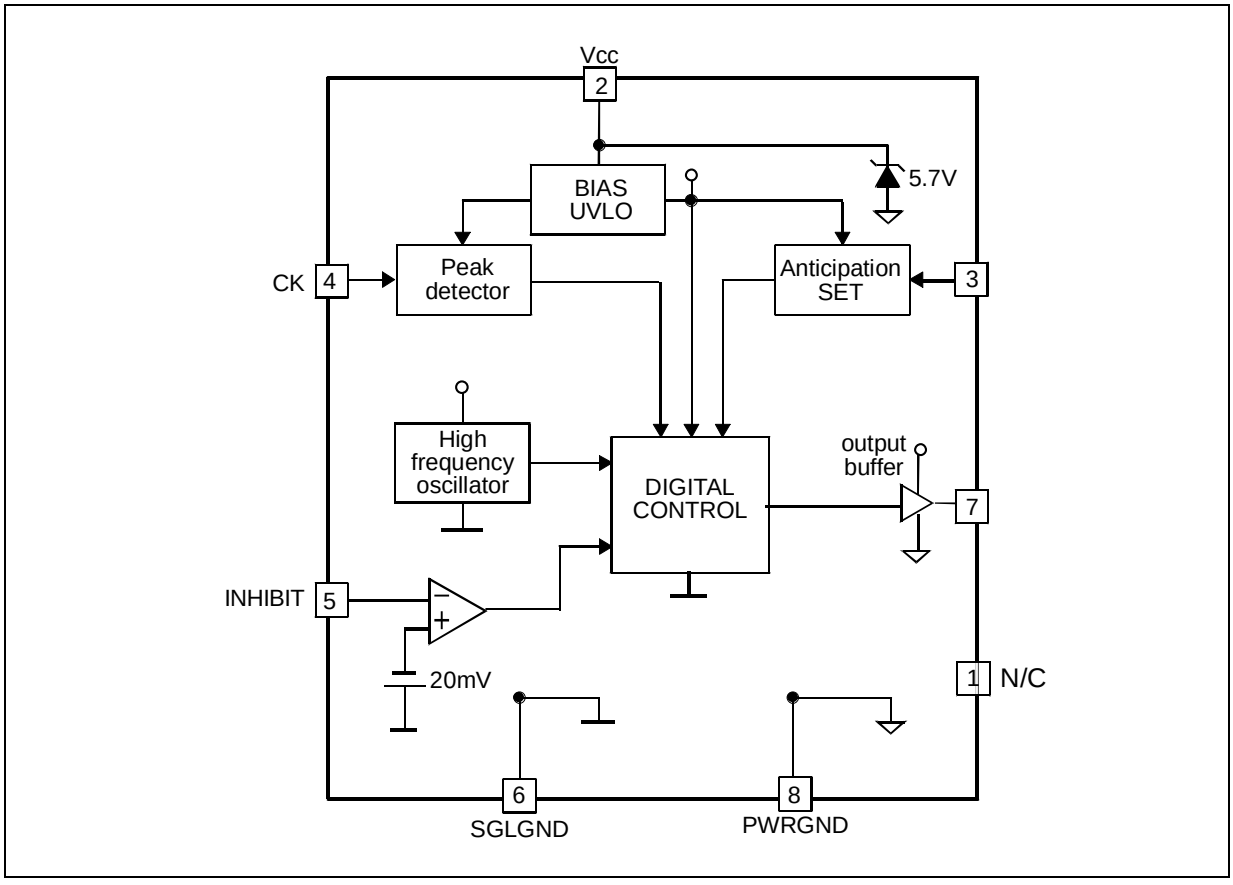


Table 1: Pin Description

Pin Number	Pin Name	Pin Function
1	N/C	Not internally connected
2	Vcc	Supply input from 4V to 5.5V
3	SETANT	Sets the anticipation in turning-off the OUT_{GATE}
4	CK	Synchronization for IC's operation
5	INHIBIT	Discontinuous Mode Detector
6	SGLGND	Reference for all the control logic signals
7	OUTGate	Output for MOSFET Gate Drive
8	PWRGND	Reference for power signals

Figure 3: Block Schematic



4. SUPPLY VOLTAGE AND UNDER VOLTAGE LOCK-OUT

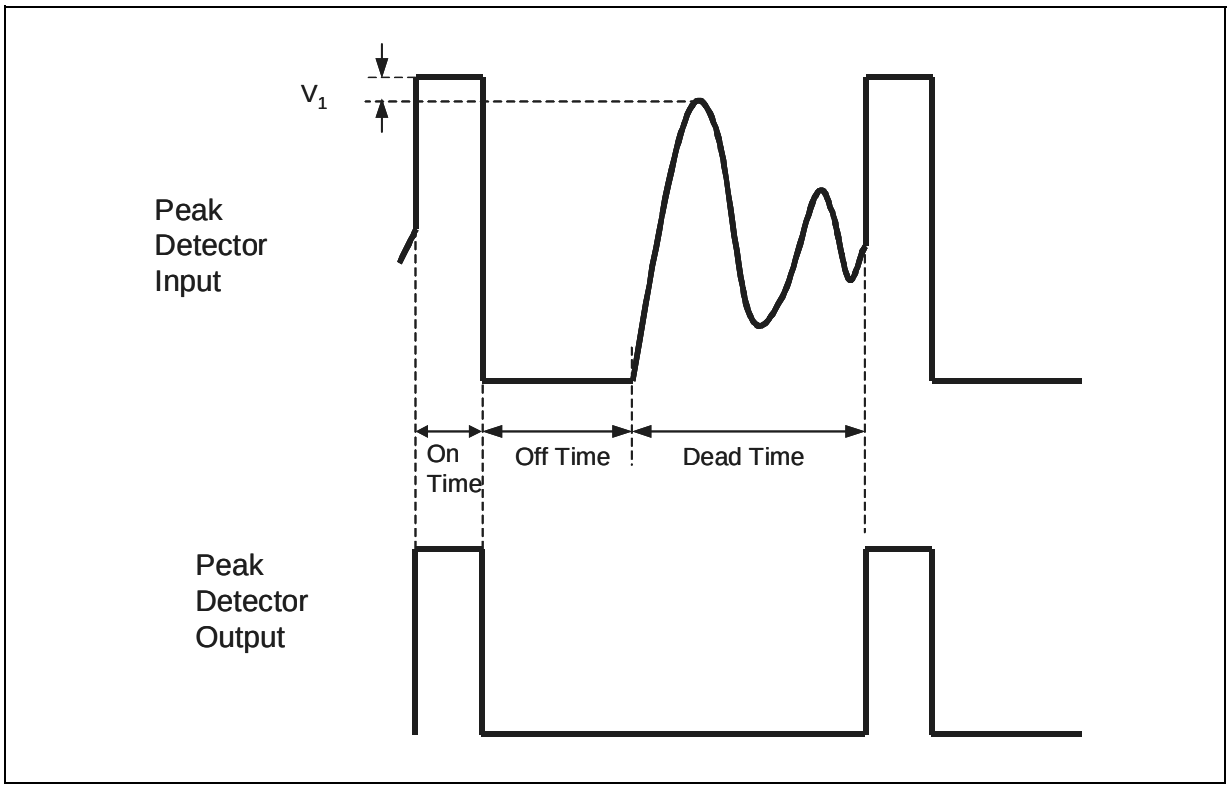
The supply input range is from 4V to 5.5V. An internal zener diode limits the maximum voltage to 5.8V. A 100nF ceramic capacitor must be connected between Vcc and SGLGND pin in order to assure a stable supply voltage. This capacitor must be placed very close to the device. Another 100nF capacitor must be connected between Vcc and PWRGND.

Under Voltage Lock Out feature guarantees proper start-up while it avoids undesirable driving during eventual dropping of the supply voltage.
As shown in the Block Diagram, the Vcc voltage also supplies also the output driver, consequently the maximum driving voltage is 5.5V, so the use of logic gate threshold mosfets is recommended.

5. SYNCHRONIZATION

An innovative feature of the STSR3 is the capability to operate in the secondary side without any synchronization signal coming from the primary side. The STSR3 synchronization is obtained directly from the secondary side using the voltage across the Synchronous mosfet as the information for the switching transitions. The Ck pin is the input for the synchronization signal; the internal threshold is set at 2.6V. As can be seen in figure 3, a Peak Detector is present at the input of the Ck pin. This block is able to distinguish between the primary mosfet switching transitions and the eventual sinusoidal waveform caused by discontinuous mode operation or resonant reset configurations (see figure 4). A wrong synchronization causes wrong driving of the synchronous rectifier.

Figure 4: DCM waveform



5.1 Continuous Conduction Mode

When the Flyback converter is working in continuous mode the voltage across the source and drain of the synchronous mosfet has a square shape. This voltage can be applied to the Ck pin using two different configurations: with a resistor divider (figure 6) or with a diode and pull-up resistor (figure 7). In most cases a spike is present during turn-off of the synchronous mosfet; this spike must be eliminated at the Ck pin in order to avoid false synchronization.

Using the resistor divider, the spike is eliminated by adding a small capacitor (C1) as shown in figure 6.

Figure 5: CCM waveform and Ck circuit

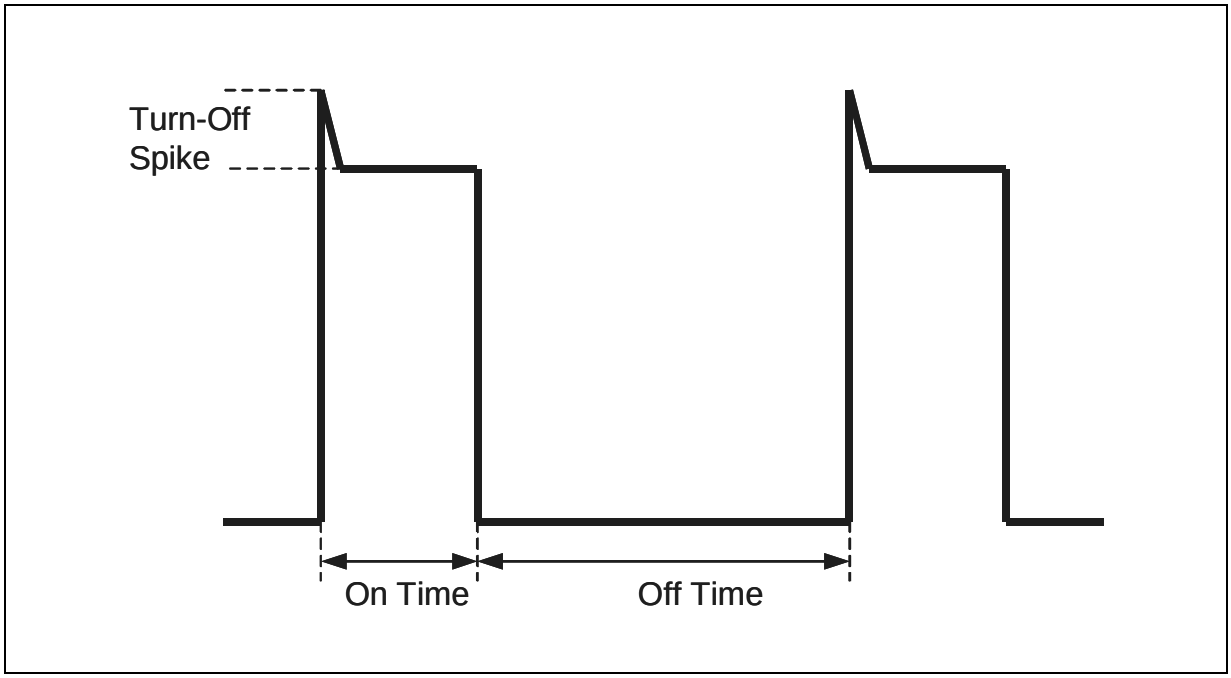
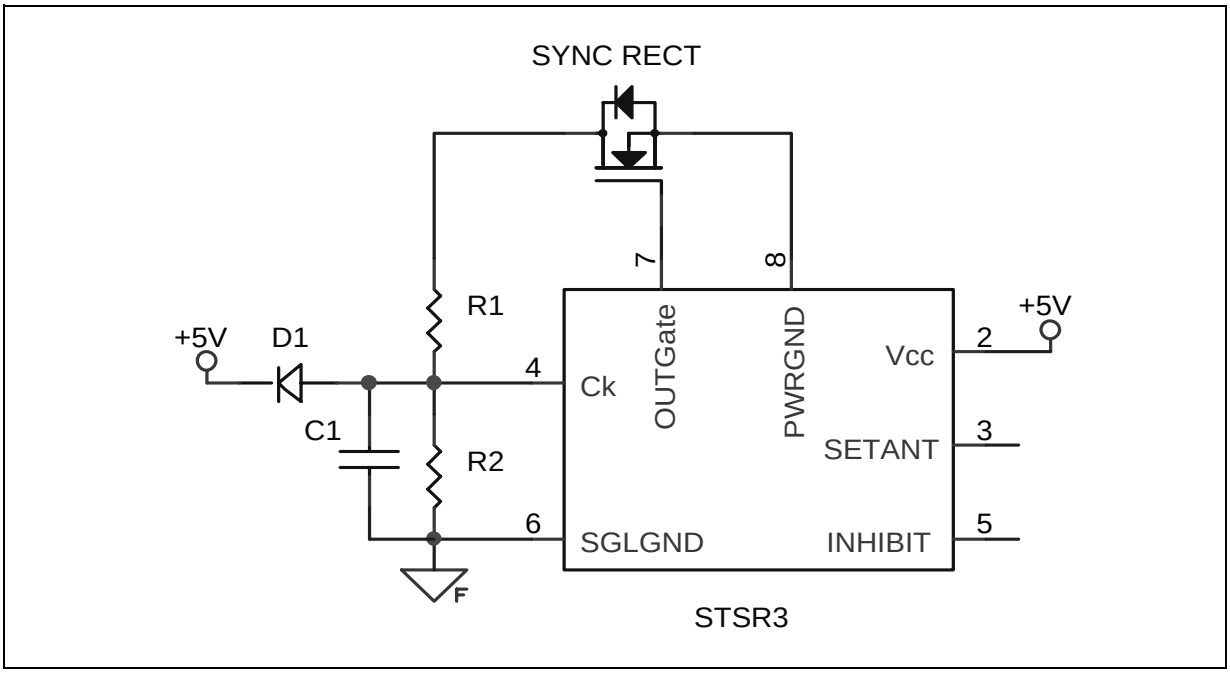


Figure 6: Synchronization with a resistor divider



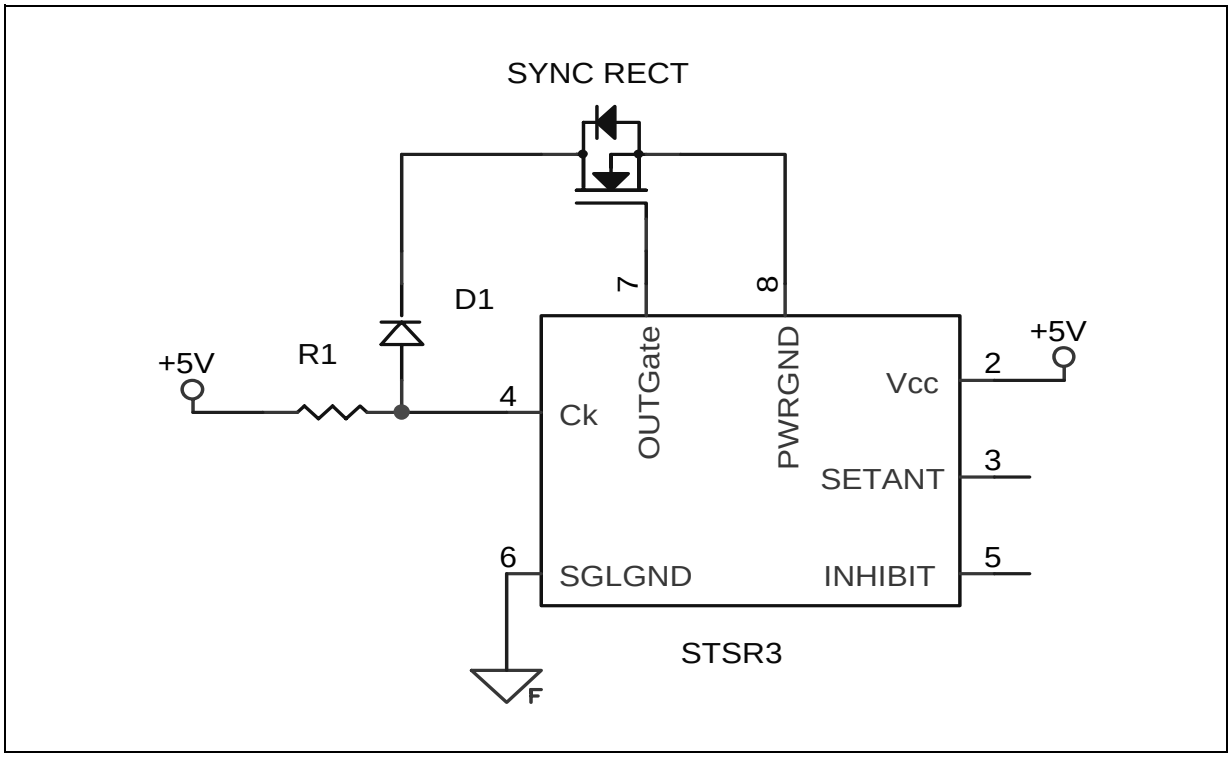
As an example, in a Flyback converter for telecom application, the DC input voltage has a 1:2 variability range (typically 36V-72V). Consequently, the secondary winding voltage also has 1:2 variability. The resistor divider can be calculated in order to have about 2.8V at the Ck pin at 36V input; at 72V input, the

Ck pin reaches 5.6V. Even if this value is higher than the maximum voltage on the CK pin it can be accepted, limiting the current flowing into the pin to 10mA.
The value of capacitor C1 is dependent on the amount of synchronous mosfet turn-off spike and on the value of R1. In order to reduce the delay introduced by R1 and C1 together, the minimum capacitor value should be used.

In the case of an Adaptor Flyback converter, working with 85VAC to 270VAC input, the variability range is 1:3. At the minimum input voltage, 2.8V must be guaranteed at the Ck pin, consequently at maximum input voltage, the voltage at the Ck pin will be 8.9V or higher. This voltage exceeds the absolute maximum ratings of the device. If R1 limits the current flowing into the Ck pin to a value below the maximum Ck current value indicated in the datasheet, the device can still working properly; otherwise diode D1 must be added to protect the device.

Figure 7 shows the synchronization circuit with diode and pull-up resistor. In this case there is no problem with the turn-off spike and maximum CK pin voltage. This circuit cannot work properly in Discontinuous Mode due to the ringing present in the voltage drain of the synchronous rectifier.

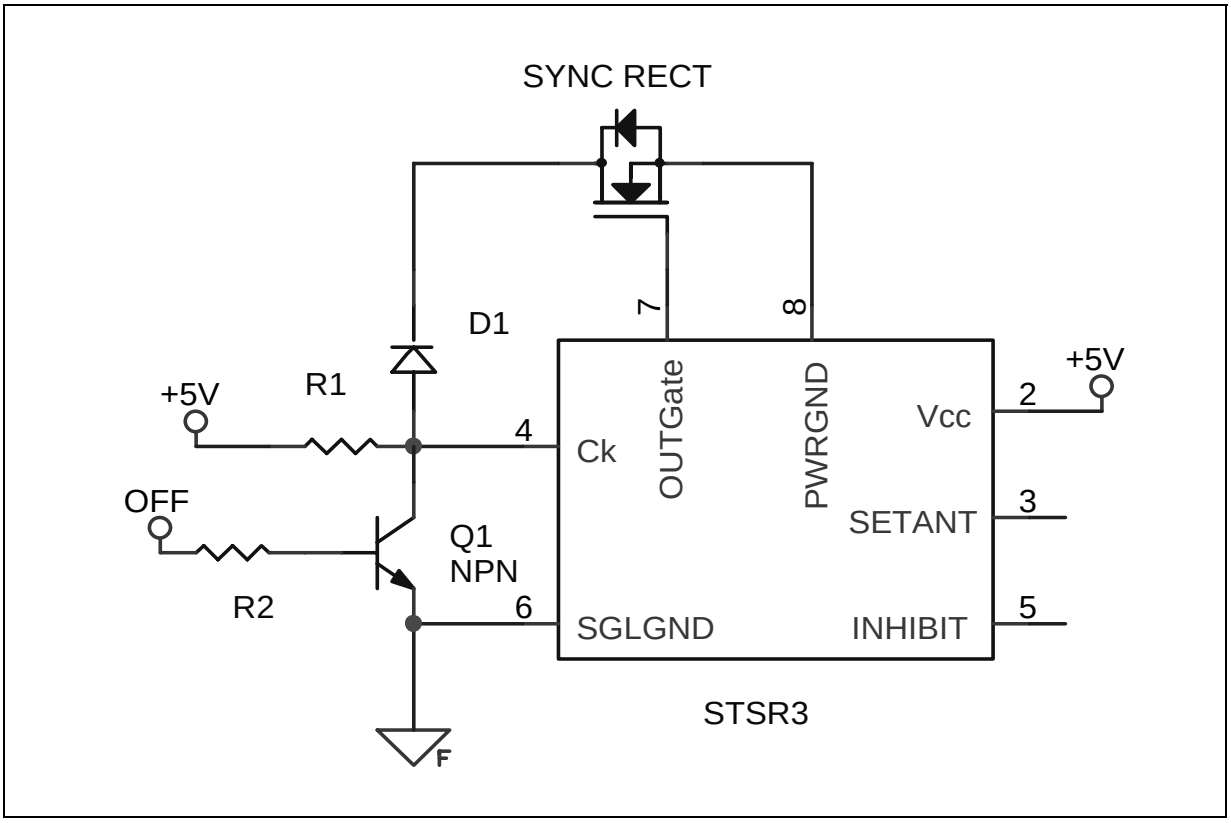
Figure 7: Synchronization with a diode and pull-up resistor



The STSR3 can be turned off easily adding a NPN transistor between Ck and SGLGND. This transistor forces the CK pin to GND when the signal OFF is high. In this condition the OUTGate will be in a low state turning off the Synchronous Mosfet.

Figure 8 shows the turn-off circuit when using a diode and pull-up resistor to synchronize the STSR3, the same configuration of Q1 and R2 can be used with a resistor divider circuit.

Figure 8: Shut down circuit

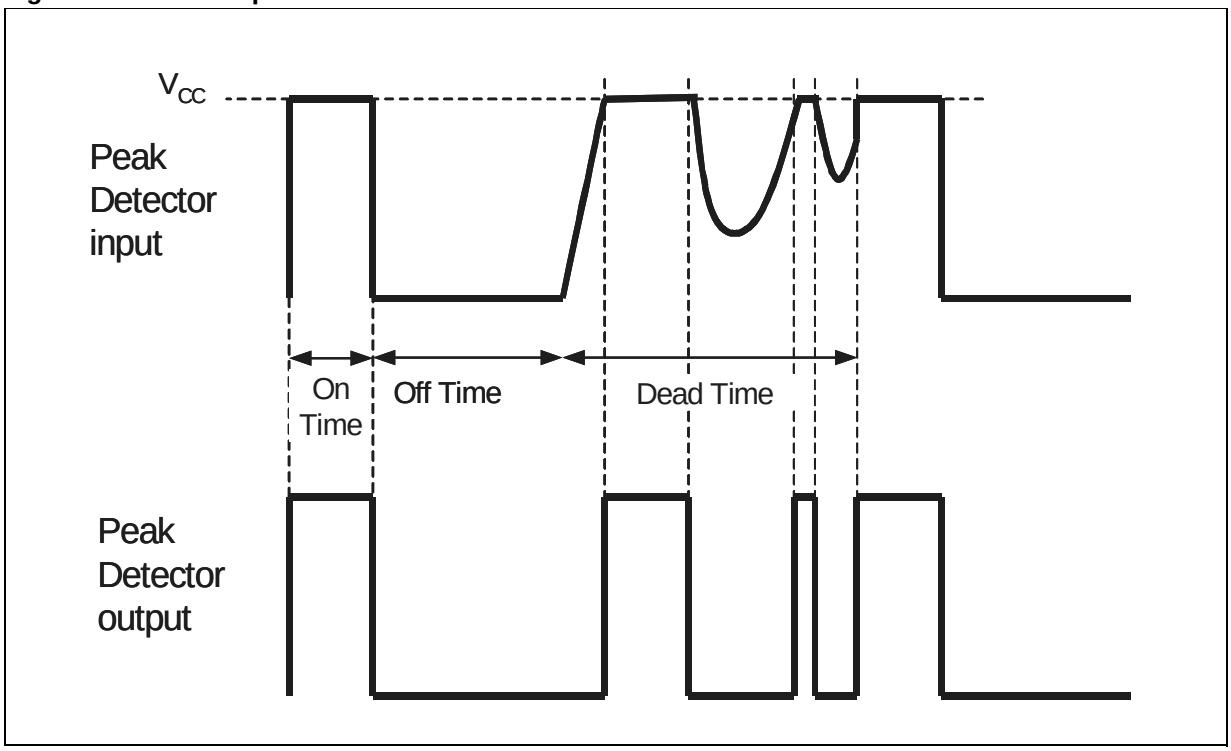


5.2 Discontinuous Conduction Mode

As shown in figure 4, in discontinuous mode operation there can be some problems in detecting the primary switching transitions. The internal peak detector is only able to determine the peak value reached by the signal at the Ck pin, neglecting all signals that have a lower value. Referring to figure 4, a minimum voltage difference V_1 =400mV between the switching transition waveform and the sinusoidal waveform must be assured in order to allow the Peak Detector to work properly.

As mentioned in the previous paragraph, if the input voltage variability range is higher than 1:2, diode D1 must be added to clamp the voltage on the Ck pin. In these conditions, both switching transition waveform and the sinusoidal waveform are clamped, and the peak detector is unable to operate correctly causing false triggering of the STSR3 (see figure 9). In this case, using an external peak detector, like the one shown in the next paragraph, solves the problem.This allows correct operation of the device both in continuous and discontinuous mode.

Figure 9: DCM clamped



6. EXTERNAL CLOCK DETECTOR

The external clock detector is a circuit to be used when the input voltage variability is higher than 1:2. This circuit substitutes the circuit of figure 5-6 and assures correct operation of the STSR3 both in discontinuous and continuous conduction mode, providing a pure square waveform to CK.

R20 is a pull up resistor, when the SR mosfet is on or its body diode is conducting, the voltage V1 is low. When the mosfet is Off (at the time of the primary switch), the voltage V1 is at 5V. R22 and C10 form a low pass filter, which allows provision of a correct synchronized signal even when the ringing is almost zero (see Figure 11). But R22 and C10 also cause an undesired delay, so the R21 and C9 group reduce this delay during fast switching transitions. The ST logic port 741T70 eliminates the noise, which could false trigger the internal peak detector of the STSR3.
In paragraph 11 suggested values for this circuit are given.

Figure 10: External Clock Detector Circuit

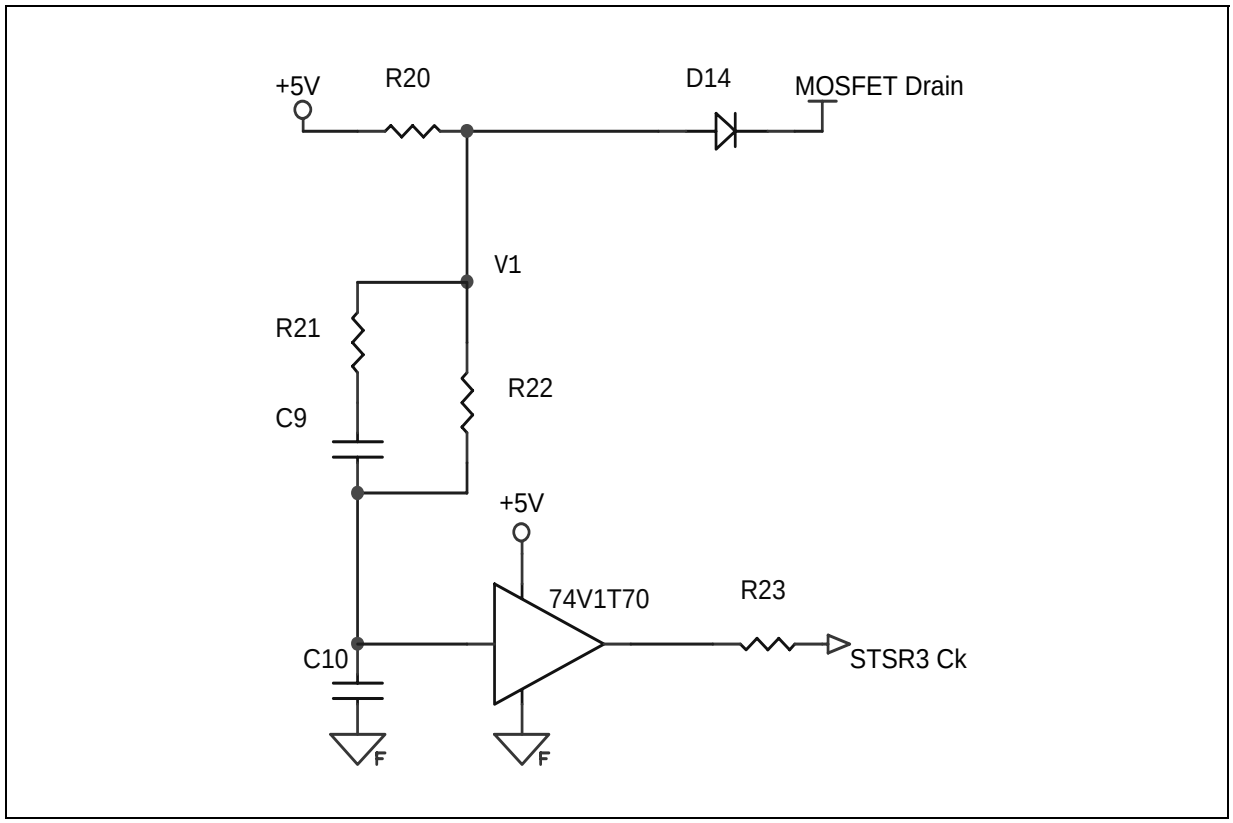
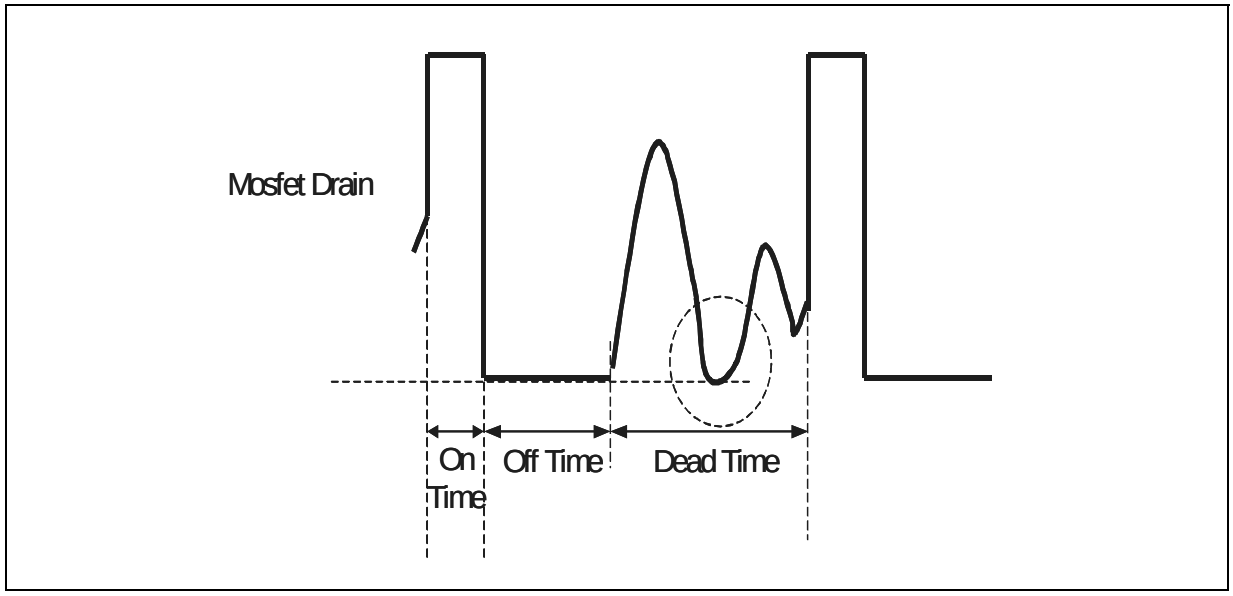


Figure 11: The ringing voltage near to zero can cause false trigger of the IC



7. INHIBIT OPERATION

One of the differences between diode rectification and synchronous rectification is the possibility for Mosfets to conduct the current in both directions while diodes conduct just in one direction. In discontinuous mode with diode rectification, when the inductor current reaches zero it cannot reverse

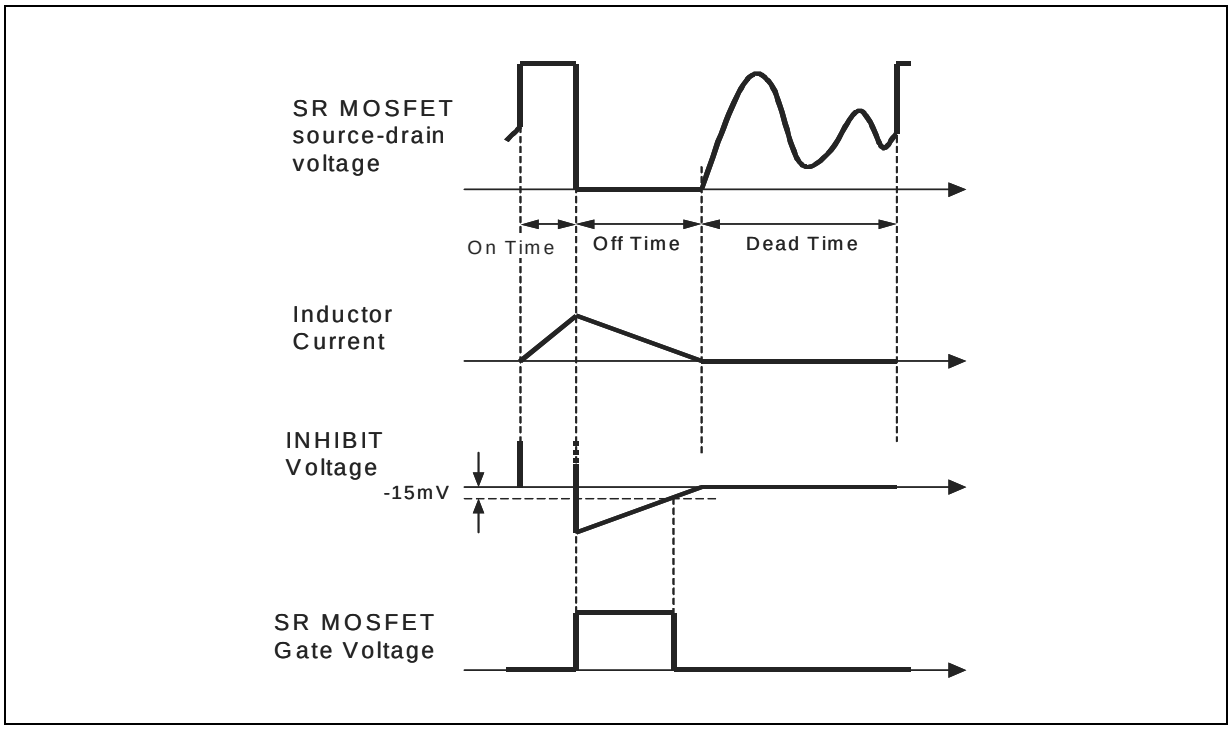
because the diode does not allow current flowing from cathode to anode. Using mosfets as rectifiers, when the inductor current reaches zero, it continues to decrease becoming negative and flowing from drain to source of the synchronous mosfet. In this condition the converter works as if it was in continuous mode.

If discontinuous mode operation is required, the synchronous mosfet must be turned off when the current is zero, consequently the body diode operates as a common rectifier, avoiding reversal of the inductor current.

The INHIBIT pin is able to turn off the synchronous mosfet when its current is approaching zero allowing discontinuous mode operation of the converter.
On the INHIBIT pin, there is an internal comparator with a -25mV threshold. This pin is connected through a resistor to the drain of the synchronous mosfet. At the beginning of the off time (when Ck goes to low level), OUTGate goes high. The INHIBIT voltage is monitored for 250ns: if the voltage on INHIBIT is higher than -25mV, OUTGate becomes low; if the voltage on INHIBIT is lower than -25mV OUTGate is kept high until the voltage reaches -25mV. This is because when the synchronous mosfet is conducting, the voltage on its drain is: Vds= -Rds(on)*Idrain. If Vds is higher than -25mV, it means that the current is decreasing and discontinuous mode is approaching, so OUTGate is turned-off allowing operation of the body diode of the mosfet (see figure 12). When the converter is in continuous mode the INHIBIT voltage is always lower than -25mV and OUTGate is kept high.
During transition in which the primary mosfet is turned off, the INHIBIT voltage must fall from high value to -25mV in less than 250ns. The resistor value R26 must be chosen in order to fit this specification.

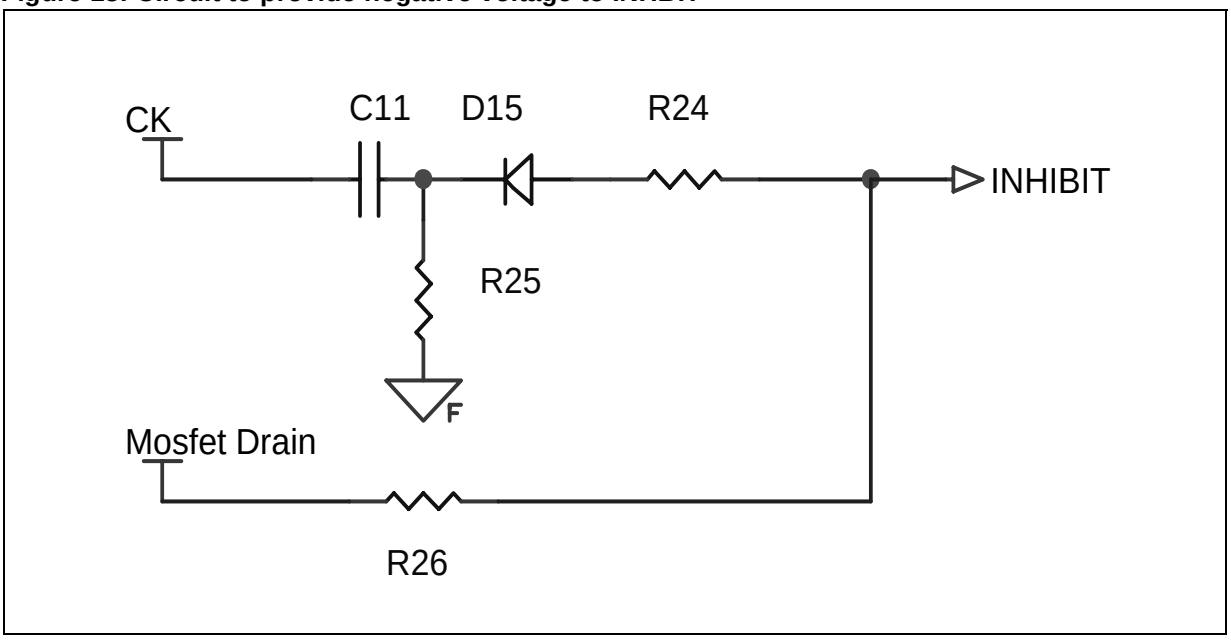
When the converter operates in parallel with other power supplies, the INHIBIT pin, detecting the voltage across the synchronous mosfet, also avoids the converter to sink current from the output.

Figure 12: INHIBIT waveforms



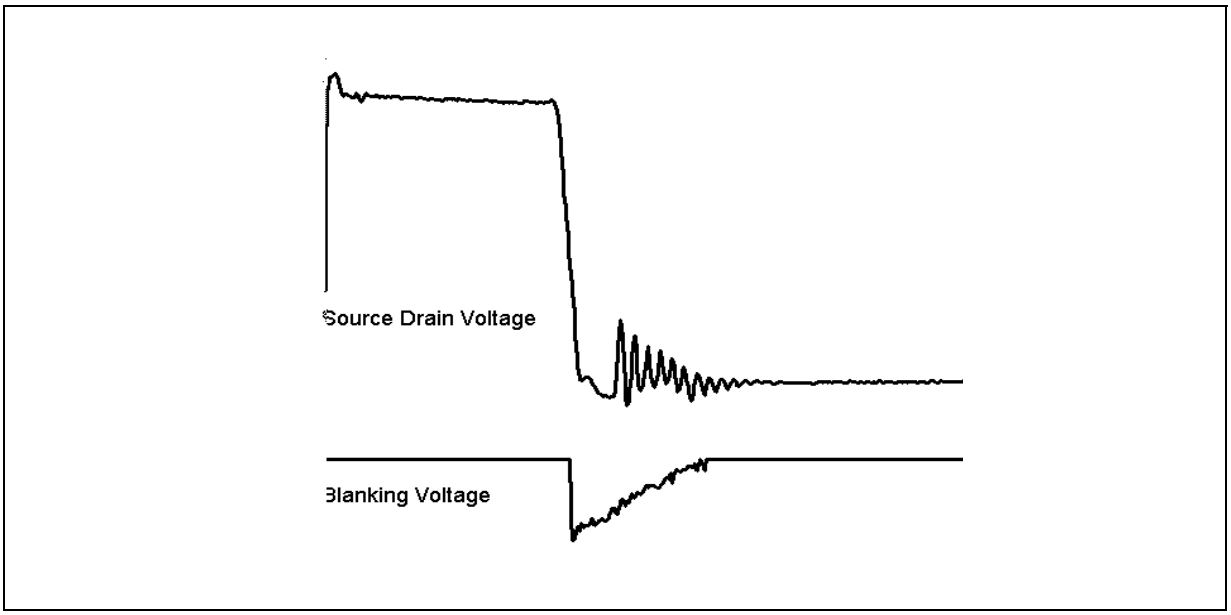
Although the INHBIT pin allows operation in Discontinuous Mode, the -25mV threshold could be sensitive to the ringing present at the SR Mosfet drain during turn off of the primary switch, causing incomplete turn on of OUTGate. This inconvenience can be avoided using the clock signal to provide a negative voltage to the INHIBIT pin acting as a blanking time. This negative voltage can be easily generated with some discrete components as shown in figure 13.

Figure 13: Circuit to provide negative voltage to INHBIT



The blanking time value is determined by C11 and R25. This time has to last the necessary time to cover the ringing caused by the primary switch turn off (see Figure 14).

Figure 14: Ringing during turn off of the primary switch



8. ANTICIPATION

One of the major problems of synchronous rectification is the generation of proper driving signals to avoid cross conduction between the Synchronous rectifier and the primary switch.

Referring to figure 15, when the primary Mosfet is turned-on, the voltage Vs tends to go negative. If the synchronous mosfet is turned off with some delay, a short circuit loop between primary side and secondary sides occurs. In order to avoid this undesired condition, the synchronous mosfet must be turned off before the primary mosfet is turned on; this means that a certain amount of 'anticipation' is needed.

Figure 16 shows the detailed timing of Ck and OUTGate signals in normal operation. Time interval t_{ant} provides the required anticipation to avoid any short circuit condition. For t_{ant} it is possible to choose between three different values using the SETAnt pin according to table 2:

Figure 15: Short circuit in the secondary side

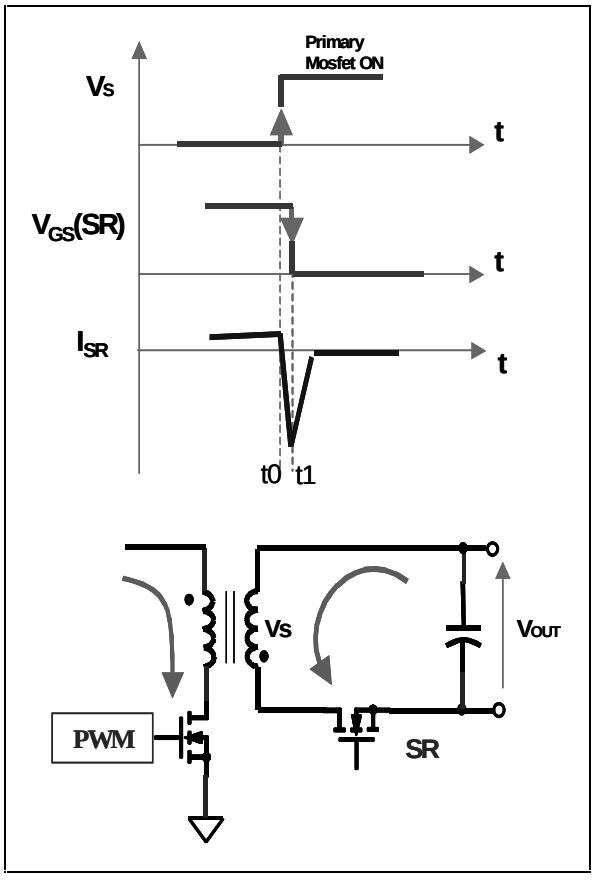


Table 2: Anticipation values

Parameter	Condition	Value	Unit
tant	$0<SETAnt<\frac{1}{3}Vcc$	75	ns
	$\frac{1}{3}Vcc<SETAnt<\frac{2}{3}Vcc$	150	ns
	$\frac{2}{3}Vcc<SETAnt<Vcc$	225	ns

The voltage on the SETAnt pin can be obtained using a resistor divider of the supply voltage (see Table 2).

The Digital Control Block generates these anticipations by counting the number of high frequency pulses included within the switching period. Due to the digital nature of this system, some bits can be lost during the counting, causing a jitter in the output driving signal. The value in the table is an average value, which takes into account this jitter. Figure 17 shows the jitter during turn off of OUTGate.

Figure 16: STSR3 Timing

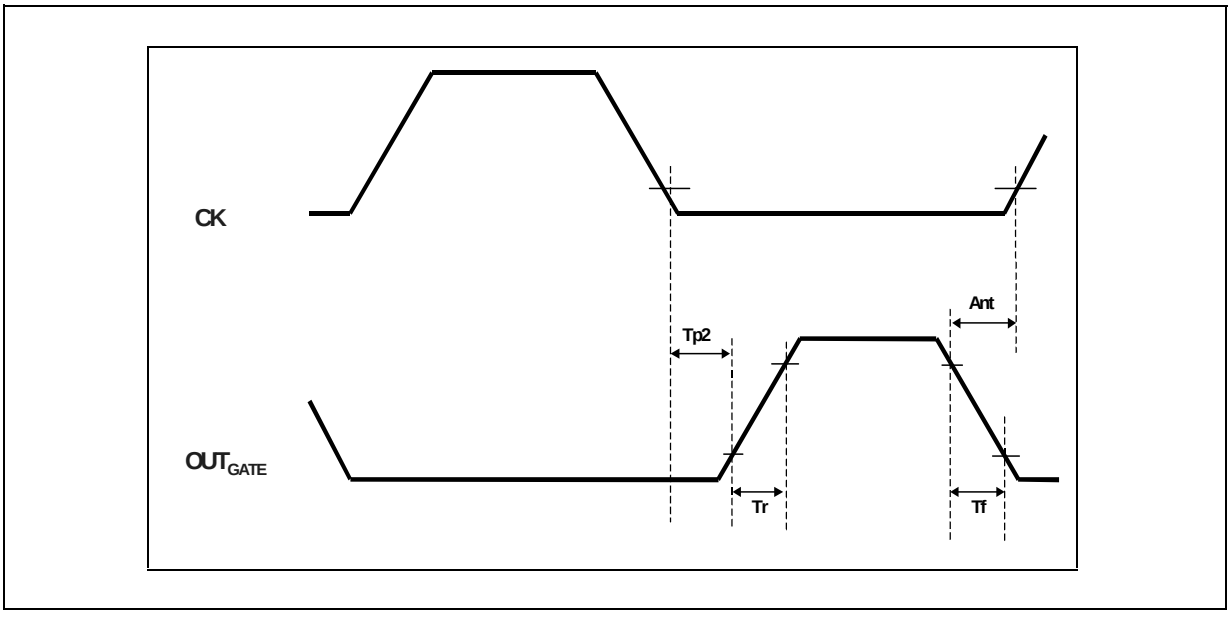
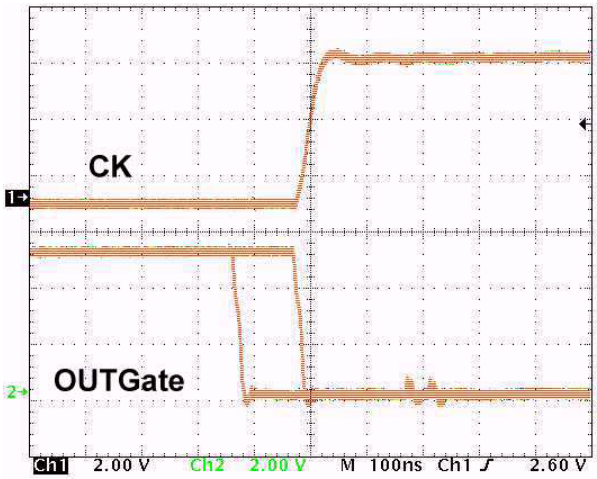


Figure 17: OUTGate turn off Jitter



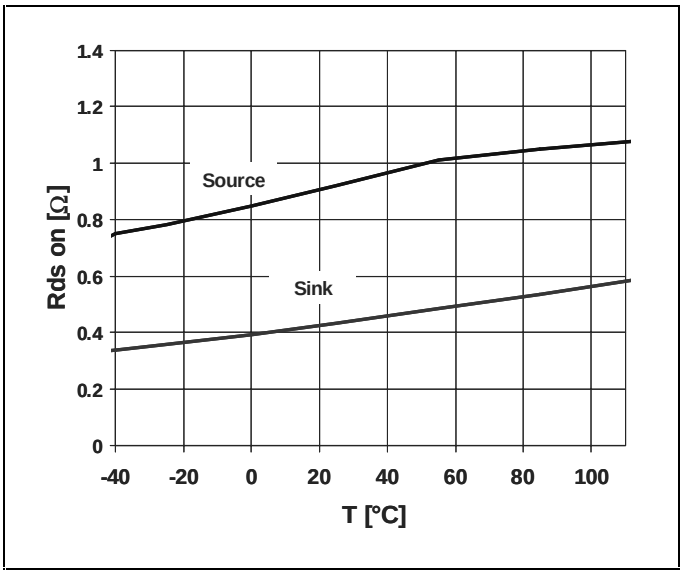
9. NO LOAD AND LIGHT LOAD OPERATION

When the duty-cycle is lower than 14%, an internal feature of the STSR3 allows a total shutdown of OUTGate and of most internal parts of the device, causing a reduction in power consumption. In these conditions the low output current of the converter is carried by the body diode of the mosfet. The IC starts to operate again when the duty-cycle is higher than 18%, therefore having a 4% of hysteresis. This feature allows correct operation when primary the PWM controller imposes burst mode due to the very light output load.

10. OUTPUT DRIVERS

The output driver has a high current capability, being able to source up to 2A and to sink up to 3.5A peak current. Consequently, the synchronous mosfet is switched very quickly, allowing paralleling of several mosfets to reduce conduction losses. The high level driving voltage is equal to Vcc voltage; therefore the device drives only mosfets with logic level gate thresholds.

Figure 18: Rds(on) source/sink vs Temp



11. TRANSIENT BEHAVIOR

During very heavy load changes, the duty cycle can vary very fast from a low value to high value and vice versa in a few switching periods.
Being the anticipation time for OUTGate based on the calculation of the switching period (frequency) and not on duty cycle, even during fast duty cycle changes the anticipation time is provided correctly, always providing correct driving for the Synchronous Mosfet.

Figure 19a: Duty Cycle very fast variation

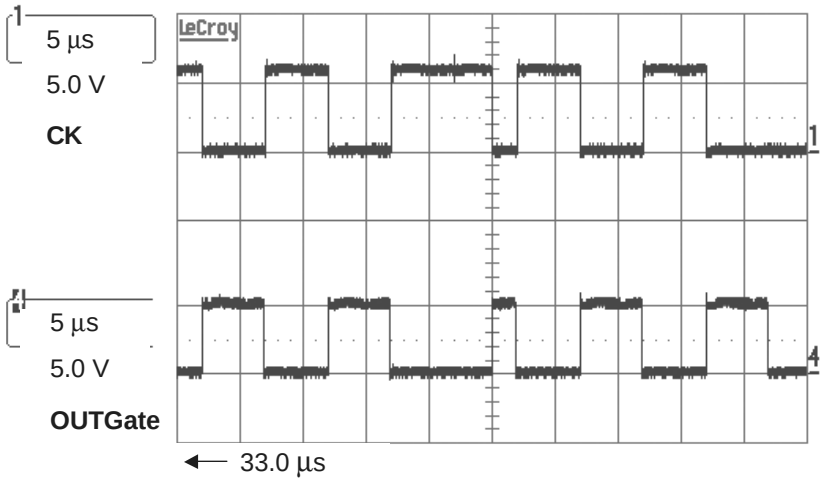


Figure 19b: Duty Cycle very fast variation

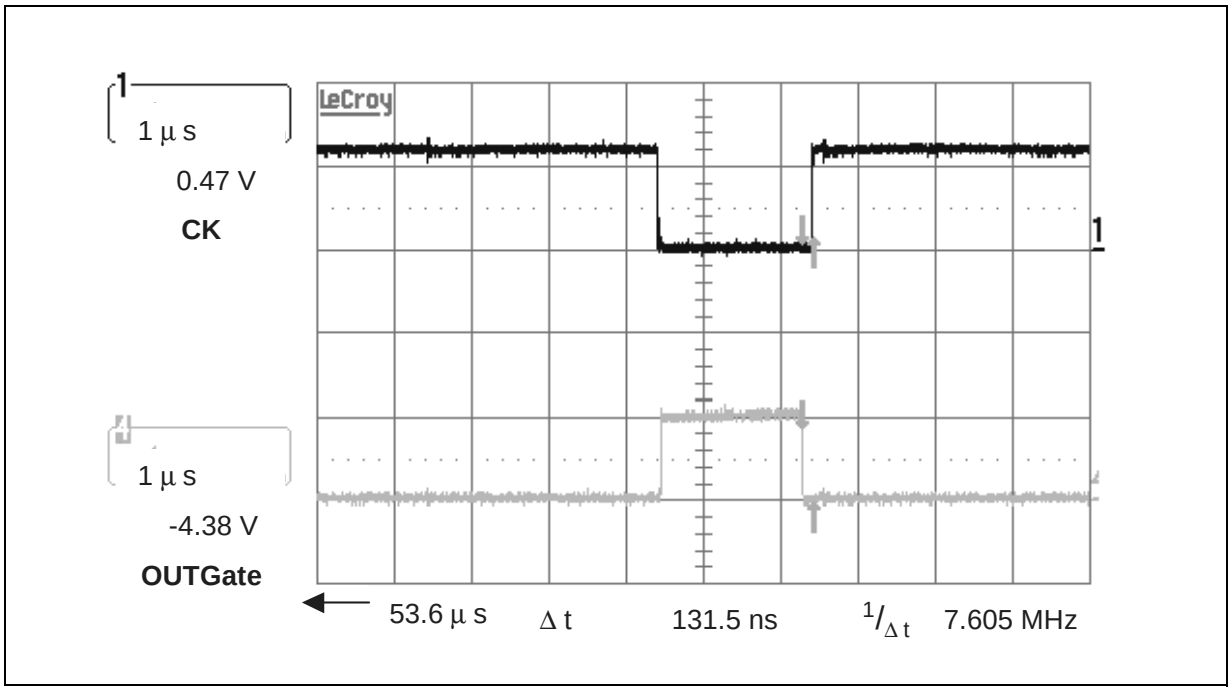


Figure 19a shows the condition in which the duty cycle passes from 50% to 80% in one cycle and back to 50%. OUTGate is provided correctly, and in figure 19b the anticipation time of 131ns is shown.

12. DEMOBOARD DESCRIPTION

The schematic of figure 20 presents a test board for the STSR3. This board replaces the diode in a Flyback converter and includes all the components needed by the STSR3 to operate, plus the synchronous mosfet. Synchronization is obtained with the external clock detector making the board usable in every kind of Flyback converter, both AC/DC and DC/DC. Some parts of the circuit shown in fig.20 might not be necessary depending on the kind of the application. For example if there is no ringing at turn-off of the primary switch, the components R24, D15, R25 and C11 can be omitted.
A Synchronous Mosfet in the TO220 package can be mounted on board. ST provides suitable Synchronous Mosfets for this application:

P/N	VD_{SS} (V)	$RDS_{(on)}$ @ 5V (mΩ)	$I_{D(cont)}$ (A)
STP100NF03L-03	30	4.5	100
STP80NF03L-04	30	5	80
STP90NF03L	30	12	90
STP85NF3LL	30	9	85
STP70NF3LL	30	12	70
STP100NF04L	40	5	100
STP80NF55L-06	55	8	80
STP60NF06L	60	16	60
STP80NF75L	75	13	80
STP40NF10L	100	36	40

The board allows us to easily pass from diode rectification to synchronous rectification in Flyback converter applications. Table 3 shows detailed components selection.

Figure 20: Demo board Schematic

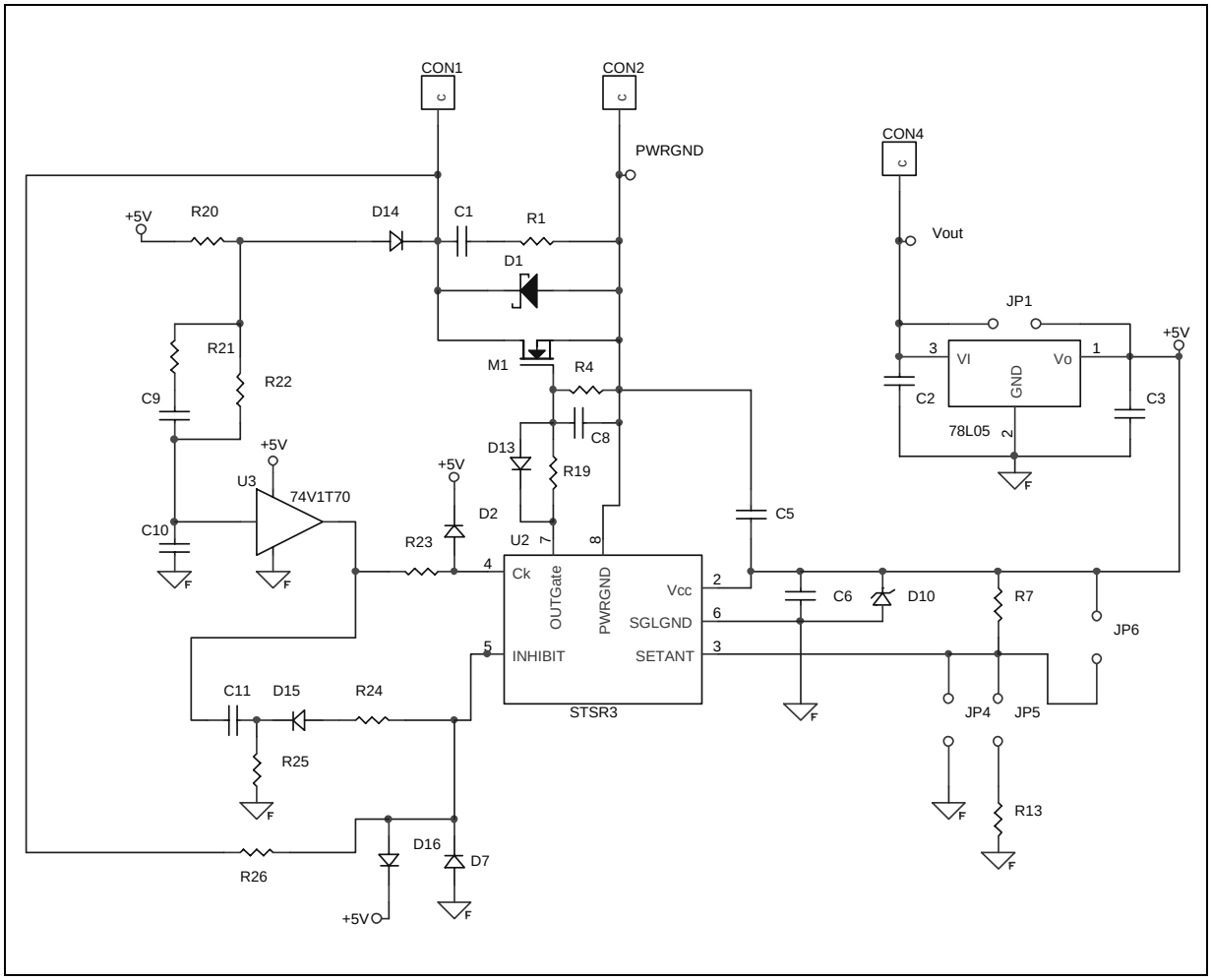


Table 3: Demo Board Components

Component	Notes
Supply	
C5, C6	Vcc bypass capacitors 100nF ceramic
U1	Standard voltage regulator to provide 5V supply voltage (SOT89). Omit this component and close jumper JP1 if 5V is already present on the board L78L05ACU
C2	78L05 input capacitor (330nF ceramic)
C3	78L05 output capacitor (150nF ceramic)
D10	Protects Vcc from voltages higher than 5.6V
JP1	Close this jumper if a 5V is already available on the board
Synchronization	
D2	Protects Ck pin from voltages higher than Vcc (not necessary if U3 is used)
D14	Blocks the high voltage coming from the SR Drain
R20	Pull–up resistor (3.3kΩ)
R21	Speed up resistor (10kΩ)
R22	Low pass filter resistor (10kΩ)
R23	Ck series resistor (1kΩ)
C9	Speed up capacitor (22pF)
C10	Low pass filter capacitor (10pF)
U3	Non Inverting Buffer ST 74V1T70
INHIBIT	
R26	Limits the current to diode D16 when SR Drain voltage is higher than Vcc
D16	Protects INHIBIT pin from voltages higher than Vcc. Not necessary if the current flowing into INHIBIT pin is less than 10mA.
D7	Protects INHIBIT pin from negative voltages.
D15	Prevents C11 to be discharged
R24	Blanking circuit summing resistor
R25	Blanking Time resistor
C11	Blanking Time capacitor
Anticipation	
R7, R13	Resistor divider which provides voltage level to set Anticipation time R7=R13=10kΩ
JP6	Sets the maximum anticipation time
JP5	Sets the medium anticipation time
JP4	Sets the minimum anticipation time
Power	
M1	Synchronous Mosfet TO220
R4	Gate pull down resistor
R19	Gate series resistor (Typically 0Ω)
C8	Gate capacitor to avoid dv/dt turn-on of the SR Mosfet (Not necessary in common application))
D13	Speed up turn-off of SR Mosfet if R19 is used.
D1	A Schottky Rectifier in parallel to synchronous mosfet can increase converter efficiency due to low drop voltages during Gate drive dead time
C1, R1	A small snubber reduces synchronous Mosfet turn-off spike

13. PCB LAYOUT

Any Switch Mode Power Supply requires a good PCB (Printed Circuit Board) design layout in order to achieve maximum performance in terms of system functionality and emitted radiations. Component placing, traces routing and width are the major issues. Some fundamental rules will be given so that the PCB designer can produce a good layout for the STSR3

All traces carrying current should be drawn on the PCB as short and thick as possible. This should be done to minimize resistive and inductive parasitic effects, gaining in system efficiency and radiated emissions. Current return routing is another crucial issue. Signal ground (SGLGND) and power ground (PWRGND) must be routed separately and connected to a single ground point.

The INHIBIT pin, due to the -25mV comparator could be sensitive to layout, so make the INHIBIT connection as short as possible.

As a rule of thumb, traces carrying signal currents should be placed far from traces carrying pulsed currents or quickly swinging voltages avoiding any coupling effect between them.

Figure 21a: Board Layout - Components (two times actual size)

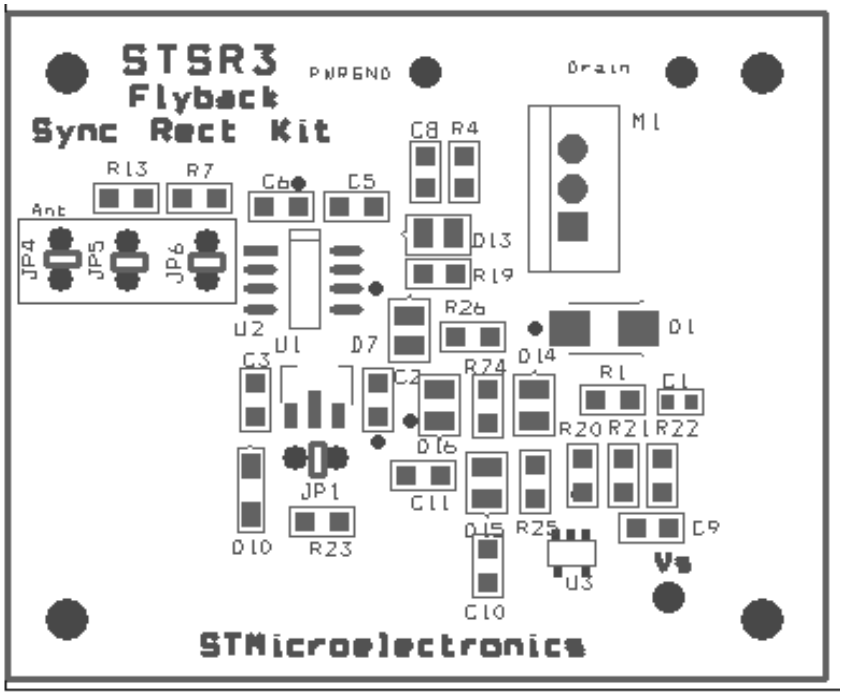


Figure 21b: Board Layout - Top Side (two times actual size)

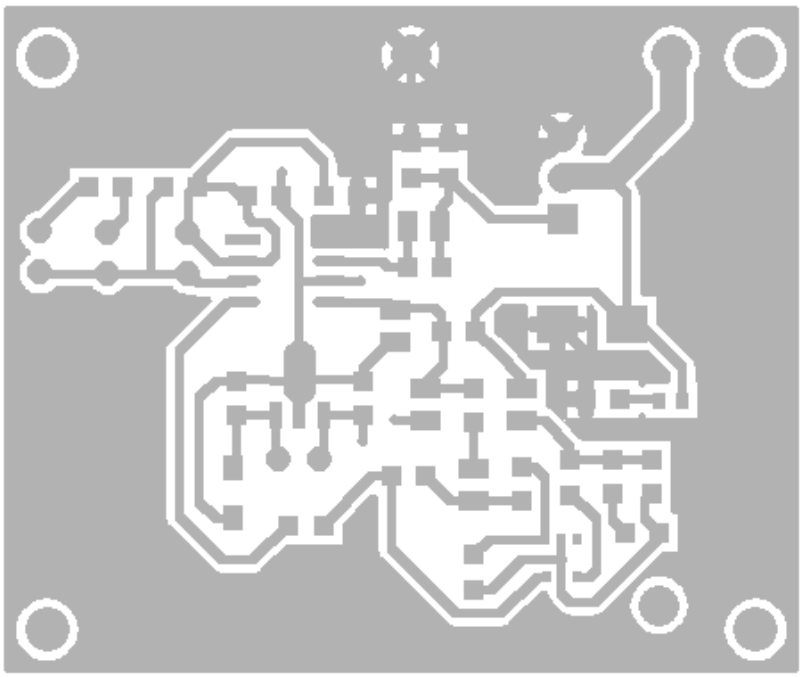
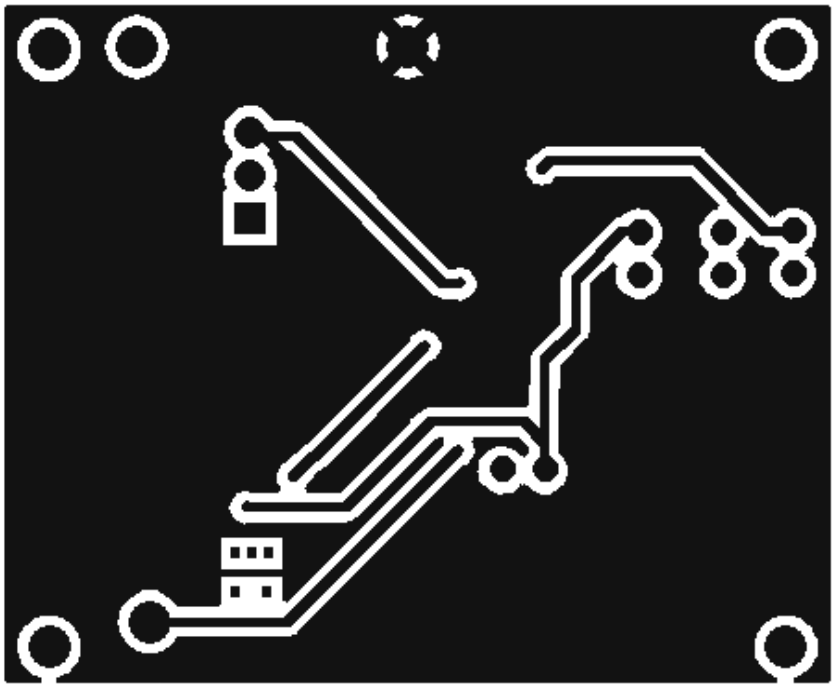


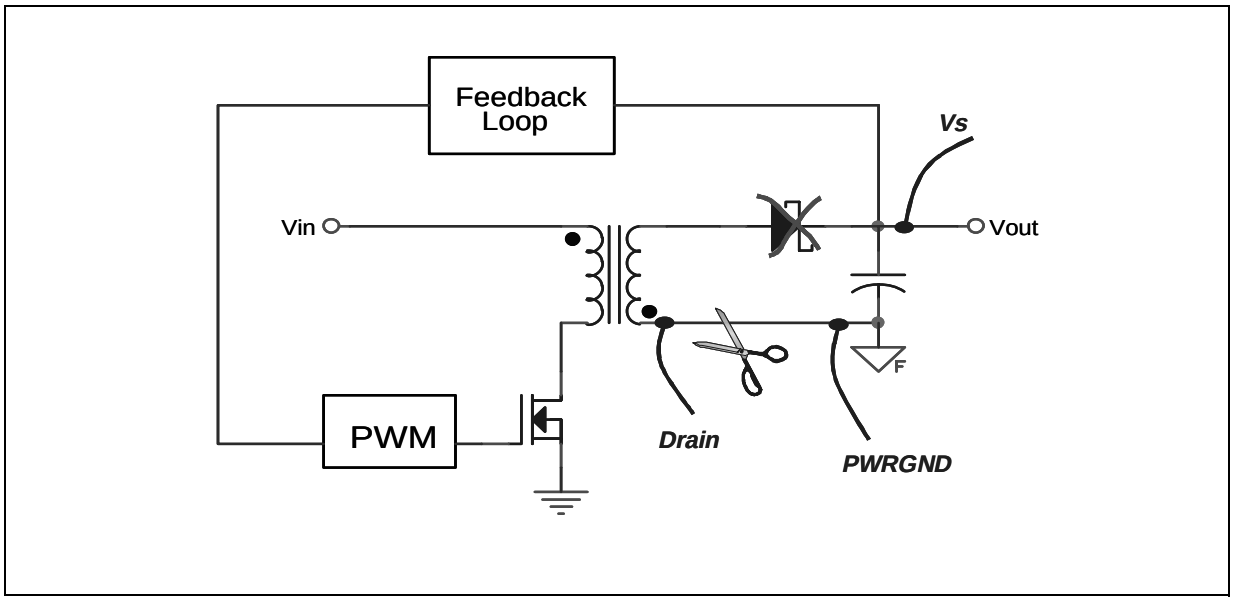
Figure 21c: Board Layout - Bottom Side (two times actual size)



14. HOW TO USE THE BOARD

The demo board is meant to implement synchronous rectification in a Flyback converter. If the diode is mounted on the board, it must be removed. Connect the Demo Board as depicted in figure 22. If Vout is equal or higher than 5V connect Vs to Vout (as in the figure 22). If Vout is lower than 5V, connect Vs together with FW Drain.

Figure 22: Connecting the Demo Board



15. CONCLUSION

A new device for controlling synchronous rectifiers in high efficiency AC/DC and DC/DC Flyback Converters is presented. The device is completely transparent to the primary PWM controller, and it works in the secondary side requiring no interaction with the primary side. The device is able to operate with any kind of topological configuration providing the correct driving signal for the synchronous MOSFET.
The presented board allows implementation of synchronous rectification in any existing Flyback converter in an easy and effective way.