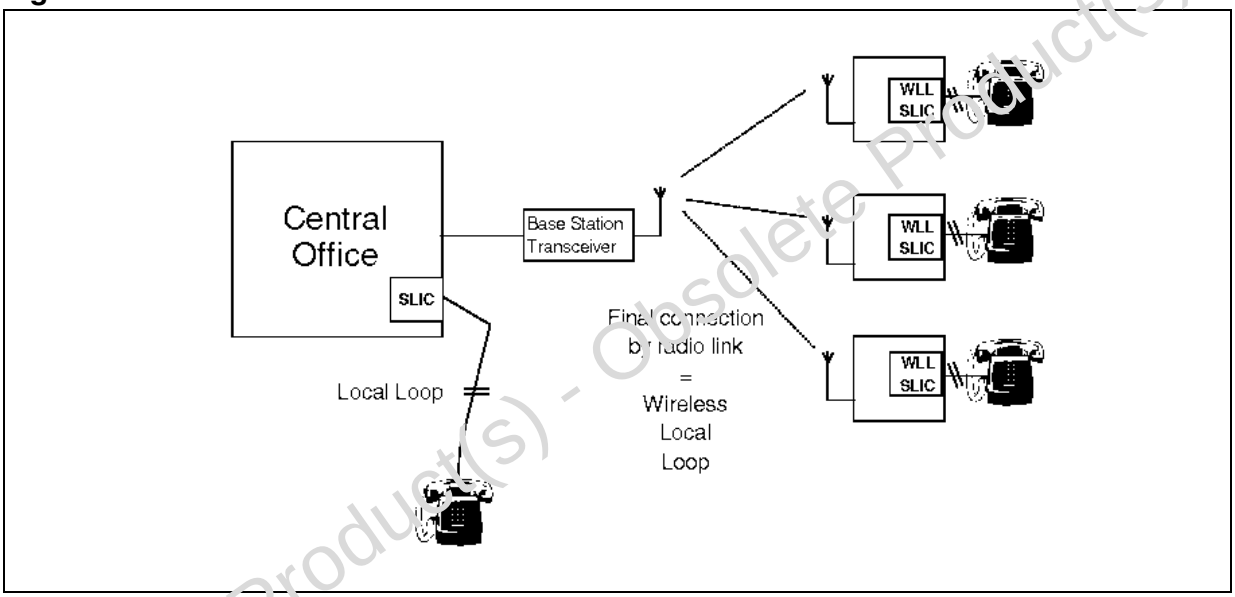
AN2117
APPLICATION NOTE

STLC3055N SINGLE SUPPLY SLIC FOR WLL APPLICATION

The STLC3055N is a slic device specially designed for WLL (Wireless Local Loop) and ISDN Terminal Adapters. It is a feature optimization of the first STLC3055Q generation

1 WIRELESS LOCAL LOOP SYSTEM

Figure 1.



The main characteristics of this device consist in the possibility to :

– operate with a single supply voltage in a range from + 5.5V to +12V
– generate the negative battery
– generate a ring signal (trapezoidal wave form)

In the following paragraphs a detailed description about device functionalities, as well as application hints, can be found. Having at hand a copy of the device Data Sheet is essential for quicker and easier understanding of the content of this Application Note.

2 PACKAGE

STLC3055N is housed in standard TQFP package plastic with copper leadframe. No copper slug surfaces out of the plastic body. STLC3055N uses the package option “standard”.
The thermal resistances, shown in Table 1 and Figure 2, are considered between the junction and the ambient, in still air, and are calculated or measured in °C/W.

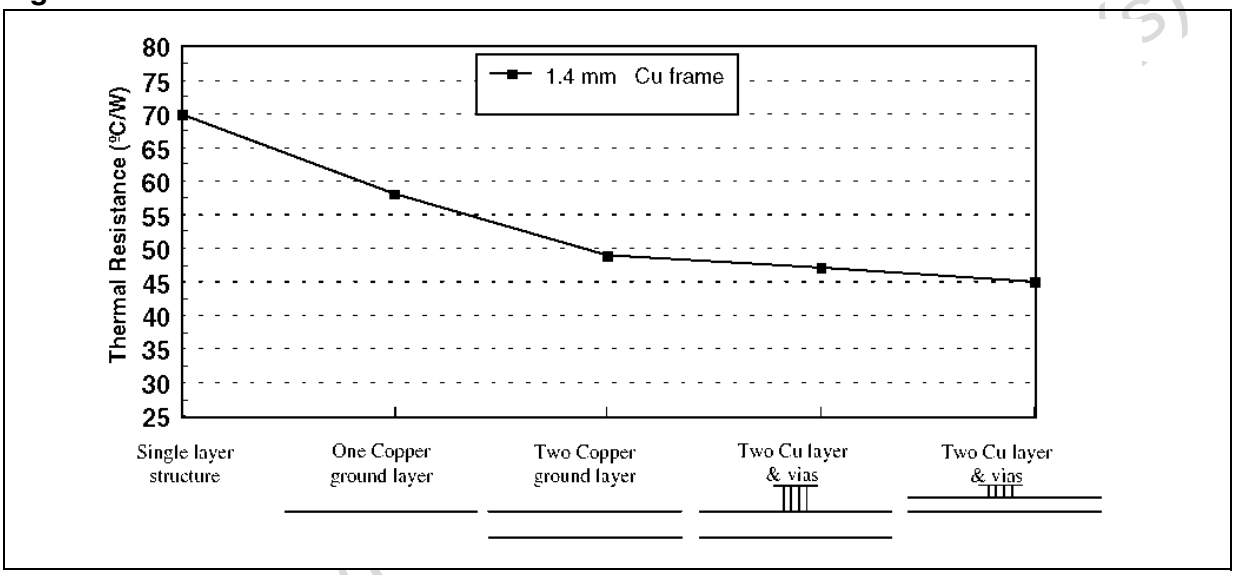
Table 1. Thermal Resistance versus Package Size

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient (Full plastic TQFP on single layer board)	70	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient (Full plastic TQFP on four layer board)	45	°C/W

2.1 TQFP 10 x 10 x1.4

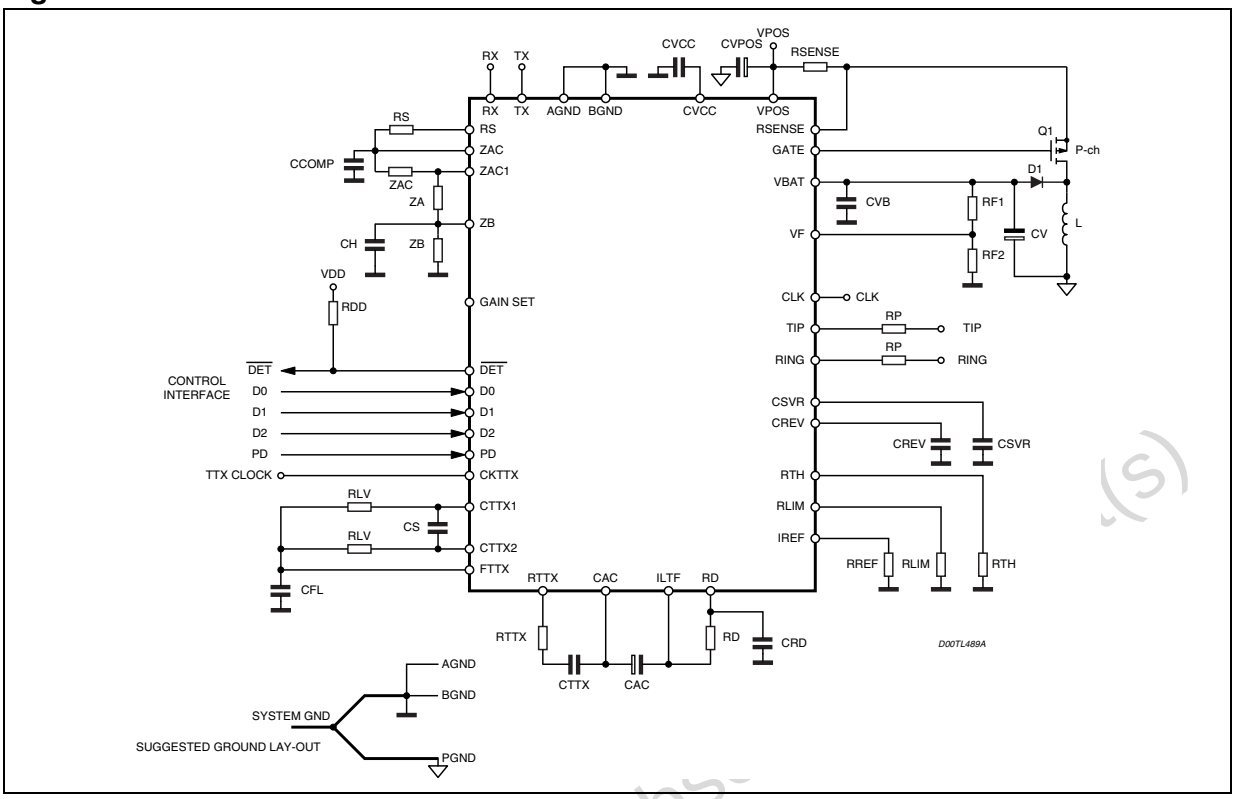
Theta (j-a) on boards - STILL AIR

Figure 2. Thermal Resistance versus Board Structure.



3 TYPICAL APPLICATION SCHEMATIC

Figure 3.



3.1 VBAT VOLTAGE GENERATION

The slic, when operated with a positive supply voltage V_{POS} and a proper clock signal (typ 125KHz), is able to generate a V_{BAT} voltage for the Active and Ring operation.

The V_{BAT} voltage level, with a 10% of spead, is defined by the voltage divider RF1, RF2 and can be set choosing a proper value of RF1 among a recommended set of values

Table 2.

RF1 (KΩ)	V_{BAT} (Active mode)	V_{BAT} (Ring mode)
270	-45.8V	-64.0V
285	-48.2V	-67,4V
300	-51.2V	-71.8V
315	-54.0V	-75.3V
330	-56.0V	-78.2V

These values are referred to the device in Active mode, On-Hook condition (I_L = 0mA) and in Ring mode without load.

Of course the V_{BAT} value has to be choosen taking into account the Absolute Max. Ratings (V_{Btot}) of the device, therefore, $V_{Btot} = (V_{BAT} + V_{POS})$ = 90V mustn't be overcome.

By an internal circuit this V_{BAT} voltage (in active mode I_L = 0) will be increased to a predetermined value generating the V_{BAT} for the R_{ING} status, whenever the Ring mode is selected

through the control interface.
These two voltage levels (i.e. V_{BAT} Active, V_{BAT} ring) are hence correlated, fixing one (Ring or Active), the other will be fixed at the same time.

3.2 OPERATION IN OFF-HOOK CONDITION

Main feature of this device is that changing from On-Hook to Off-Hook condition, I_L >0mA, the V_{BAT} voltage will be automatically adjusted depending of the loop resistance and by the current limitation value programmed (I_{LIM}).
It should be noted that the device is optimised to operate on short loop applications (R_{loop} ≤500Ω) in order to obtain a correct ring-trip detection.
In these conditions and for a line current reaching the programmed constant current feed value (I_{LIM}), the STLC3055N works like a current generator with a fixed DC current.
A fixed voltage drop, 4V on TIP/gnd and about 6V on RING/Vbat, assures the DC functionality and the proper swing for the AC signal.
Therefore, once the line is set in Off-Hook, the STLC3055N automatically adjust the self generated battery voltage (V_{BAT}) to feed the line with a fixed DC current (programmable via R_{LIM}), OPTIMISING IN THIS WAY THE POWER DISSIPATION.
Therefore, considering max. and min. R_{loop} values ranging from, 500, 100Ω, with a fixed parameters, I_{LIM} = 25mA, and 2Rp = 100Ω, the battery voltage (V_{BAT}) will be almost equal to :

- 1) V_{BAT} = 25mA x (500+100) + 10V = - 25V
- 2) V_{BAT} = 25mA x (100+100) + 10V = - 15V

A proper current threshold (typ.9mA), programmable by external resistor RTH, allows the correct on/off hook transition function.
During the off-hook dynamic transition the CAC capacitor is charged and the line current regulator system, sensing the current flowing into RD, reduces the Iloop current to the programmed I_{LIM} value, set by R_{LIM}.
The settling time of the I_{LIM} current is about 150ms and it is function of the CAC splitter capacitor (min. value allowed is 22μF).

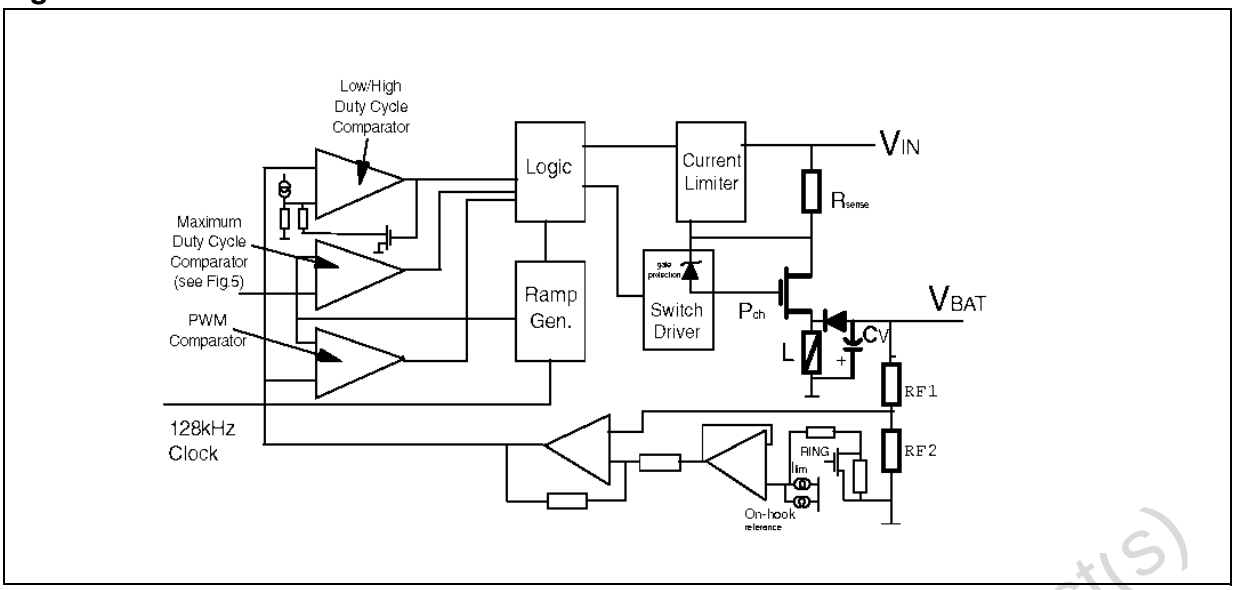
3.3 VPOS CHARACTERISTICS

The input voltage V_{POS} can change slowly, within the data sheet range value (5.5V-12V), without effect on the V_{BAT} voltage.
The STLC3055N can operate correctly when the V_{POS} voltage goes below the 5.5V (only instantaneous value, no steady-state), the only limitation is the minimum voltage required on the external PMOS to keep it in a proper linear area.
Fast transients, ripple and spikes, on the supply voltage V_{POS}, will appear on TIP/RING, with a reduced amplitude, according to the voltage supply rejection of the device.
Bench measurements on SVRR give -35dB @ f = 50Hz, -47dB @ f = 4KHz using the test circuit configuration with the device in Active mode loaded with R_{loop} of 500Ω and I_{LIM} = 25mA.

3.4 START-UP AND DC-DC CONVERTER

In order to prevent problem during start-up, an internal circuit turns-on the gate of the Mosfet only when V_{POS} reaches 4V and turns it off for V_{POS} lower than 3V.
For V_{POS} voltage higher than 4V the dc/dc converter power-on is controlled by a soft start circuit embedded on the devices.

Figure 4. DC-DC Converter Circuit



The dc\dc converter works in Buck-Boost configuration and its operation can be described as a two step process.

Mosfet in turn-on condition :

energy from Vpos is stored in the inductor, diode reverse biased, load on V_{BAT} powered by the energy stored in the output capacitors CV.

Mosfet in turn-off condition :

energy stored in the inductor is delivered to the output capacitor and hence on the load, by the diode forward biased.

An internal circuit controls the duty-cycle of the gate signal so that the output current of dc\dc converter can be proportional to the load. When, for a short time, an higher power is required, an enbedded circuit fix the max duty-cycle to about 95%.

The Rsense, in this case, guarantees the maximum value of the limited current.

3.5 INPUT CURRENT LIMITATION

The power supply, in the WLL applications, usually hasn't got high power current capability so that, when a ring trip occurs, the status of the slic changes from Ring mode to off-hook condition and since the loop current control is not immediately working, the line current reaches the output stages current limitation value that is about 80mA.

As a consequence, an high peak current is sunk from V_{POS} that could be higher of its maximum current capability. In this case, if no limiting current circuit is used, (Rsense = 0), the V_{POS} voltage would drop down.

To prevent this type of problem, the STLC3055N incorporates a circuit on the V_{POS} input limiting the peak current, that is sunk from V_{POS}, to a value defined by the formula:

$$I_{peack} = \frac{100mV}{R_{sense}}$$

This input current limitation circuit will be working, avoiding the overload problem on V_{POS}, during all the transient caused by changes of the line current conditions.

3.6 VPOS CURRENT CAPABILITY

In the table below are summarized the value of the current drawn from V_{POS} supply vs R_{EN} @ 20Hz condition (For REN definition see section 3.9 below)

Table 3.

	1REN (EUROP.)	3REN (EUROP.)	5REN (USA)
Vpos (V)	Ivpos (mA Tot)	Ivpos (mA Tot)	Ivpos (mA Tot)
5.5	130	420	590
6.0	120	280	520
9.0	90	180	360
12.0	60	140	270

Of course when the power supply-voltage cannot feed the max. current, i.e. it hasn't got enough current capability, the V_{POS} voltage will be affected.

3.7 RSense SETTING

The RSENSE resistor set the input peak current value.

Of course, the input peak current value selected have to be lower than the power supply current capability limit.

In typical application the input peak current is fixed to 900mApK (100mV / 110mΩ) in order to guarantee a proper performances in the total range of the current loop (20-40mA) and the Vpos supply (5.5-12V), driving up to 3REN of load.

If the device have to drive up to 5REN the value of R_{SENSE}, have to be reduced up to 100 - 90 mΩ in order to increase the input peak current to 1 - 1.1Apk just to guarantee the correct operation at low Vpos voltage condition (5.5V - 6V) using ringing frequency 20-25Hz .

If the device have to work with a limited input peak current of about 0.6Apk, setting the R_{SENSE} resistor value in a range from 170-180mΩ, it is mandatory to use a Vpos voltage of 12V.

3.8 TRAPEZOIDAL RINGING SIGNAL

In the application domain targeted by our product (Integrated Access Device, Set Top Box, Small Office Home Office etc...) not sinusoidal ring waveform are accepted, for this reason, the STLC3055N generates ringing signal with a trapezoidal waveform.

This type of waveform is very similar to a sinewave wose distortion can be kept lower than 5% and Crest Factors value of 1.2, just properly selecting the external C_{REV} capacitor.

Because the value of C_{REV} is function of the ringing frequency, this value have to be adapted to the ringing frequency used.

A C_{REV}=18/22nF gives a proper trapezoidal ringing signal and a proper shaping with 20/25Hz of ringing frequency, increasing this one to 68Hz, the value of C_{REV} should be choosen in a range 6.8nF/8.2nF

3.9 RINGER LOAD

In the typical application the STLC3055N can drive up to 3REN European standard (1REN = 1800Ω + 1μF), @ f = 20Hz, Crest Factor (VppK/Vrms) = 1.22 the level measured at Ringer terminal are summarized in the following tables

Table 4. (V_{POS} = 6V)

CREV	CREST FACTOR	1 REN Vppk	1 REN Vrms	3 REN Vppk	3 REN Vrms
22nF	1.22	62.5V	51.2V	61.8V	50.2V

Table 5. (V_{POS}=12V)

CREV	CREST FACTOR	1 REN Vppk	1 REN Vrms	3 REN Vppk	3 REN Vrms
22nF	1.22	63.2V	51.8V	62.8V	50.8V

If the device have to drive up to 5REN as requested by USA specs (1REN = 8µF + 6930Ω) it is necessary to modify same external components as follows:
R_{SENSE} = 90mΩ to increase the current capability in order to guarantee this performance @ V_{POS} = 5.5V
R_D = 2.2 KΩ in order to avoid a false Off-Hook detection (I_{RTH} =100/RD)
The following tables summarized the results @ 20Hz of ringing frequency :

Table 6. (V_{POS} = 6V)

CREV	CREST FACTOR	1 REN Vppk	1 REN Vrms	3 REN Vppk	3 REN Vrms	5 REN Vppk	5 REN Vrms
22nF	1.22	62.0V	50.6V	59.6V	48.7V	57.8V	47.0V

Table 7. (V_{POS}=12V)

CREV	CREST FACTOR	1 REN Vppk	1 REN Vrms	3 REN Vppk	3 REN Vrms	5 REN Vppk	5 REN Vrms
22nF	1.22	63.0V	51.3V	60.8V	49.3V	58.6V	47.5V

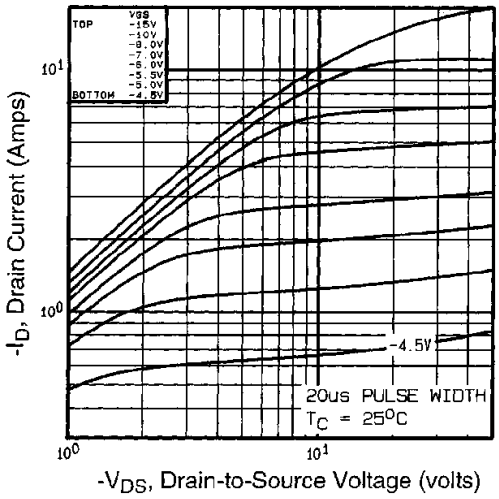
3.10 FUNCTIONING AT LOW VPOS (5.5V)

When the device is working to V_{POS} = 5.5V, a good efficiency can be reached if the P-MOS:

- works in the linear region with a series resistance equal to Ron
- gives a proper ID current with the Vgs (about V_{POS}) generated by the driver

The IRF9510S assures the correct operation in a linear region starting from a minimum V_{POS} voltage of 5.5V.
From fig.1 of appears that the mosfet with a V_{thmax} = 4V, in the condition of V_{gs} = 5V and V_{ds} = 1V is able to guarantee a minimum current value of 700mA.
In the application $V_{gs} = V_{pos}$, considering negligible the R_{sense} drop, the value of V_{gs}-V_{th} = 1.5V allows to the mosfet to work in a linear region.
Linear region is obtained for Vds < Vgs-Vth

Figure 5. Typical Output Characteristics T_{case} = 25°C



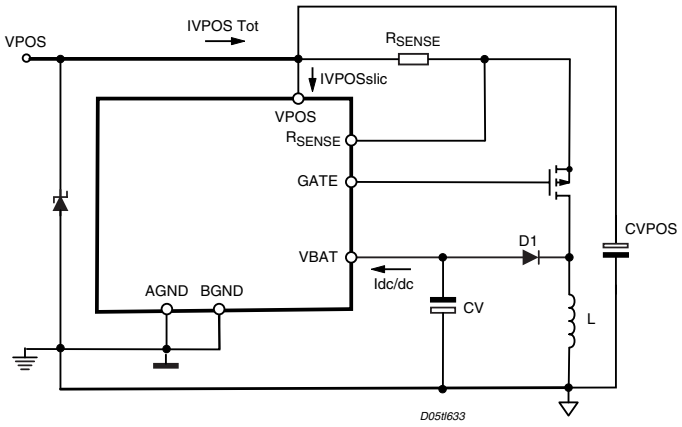
3.11 EFFICENCY AND POWER DISSIPATION

The best efficiency of the DC/DC converter, at the fixed CLK frequency, can be obtained with:

- a good compromise between Rds-on and the parasitic input/output capacitances value of the PchMosfet, for this reason the IRF9510/20 (V_{DSS} = -100V; $R_{DS(ON)}$ =1.2Ω; I_D = -4.0A) has been chosen.
- a coil inductor for dc/dc applications like SMD coil made by Sumida type CDRH125, 100uH,
- an high efficiency fast recovery diode like the SMBYW01-200 showing a Trr Max=35ns @ V_F = 1A
- of course η is also influenced by the V_{pos} choice

In the following tables, the results of the measurements, made on ST board, of the DC/DC converter efficiency are summarized.

Figure 6.



The efficiency parameter is calculated with the following formula:

$$\eta = \frac{\frac{I_{dc}}{dc} \cdot V_{BAT}}{IV_{POStot} - IV_{POSslic}} \cdot V_{POS}$$

Measurements condition:

- external switch PchMOS IRF9510
- slic status considered: High Impedance; Active with Iloop=25 mA, R_{loop} = 500 ohm.
- SMD power inductor, SUMIDA, type CDRH125 typical value 100µH, Rs = 2.5Ω , permissible DC current 1.3A .

Table 8. H.I . Feeding @ Open circuit

Vpos (V)	Ivpos (mA Tot)	Ivpos (mA pin25)	Idc/dc (mA)	Vbat (V)	Pvpos (mW)	Pvbat (mW)
6	13.15	3.75	0.17	-50.80	56.40	**8.6**
12	17.70	4.40	0.20	-51.20	160.00	**10.25**

Table 9. Active mode @ R_{loop} = 500Ω

Vpos (V)	Ivpos (mA Tot)	Ivpos (mA pin25)	Idc/dc (mA)	Vbat (V)	Pvpos (mW)	Pvbat (mW)	Eff (%) η
5.5	177	7.0	29.5	24.8	935.00	731.60	78%
6	160	7.2	29.5	24.8	916.80	731.60	80%
9	111	8.0	29.8	24.8	927.00	739.04	80%
12	86	8.3	29.8	24.8	932.40	739.04	79%

Of course, for a given value of supply voltage V_{pos}, the current consumption, from V_{pos} supply, will be influenced by the electrical characteristics of the selected coil

Just to put in evidence the advantage, in term of power consumption, of the STLC3055N, versus the first generation product STLC3055Q here below are reported the measures referred to the above mentioned device in H.I . Feeding @ Open circuit.

Table 10. STLC3055Q

Vpos (V)	Ivpos (mA Tot)	Ivpos (mA pin25)	Idc/dc (mA)	Vbat (V)	Pvpos (mW)	Pvbat (mW)
6	32	4.6	2.3	-52.2	164.4	120.0
12	22	4.6	2.5	-52.7	208.8	131.7

3.12 MICRO INTERFACE

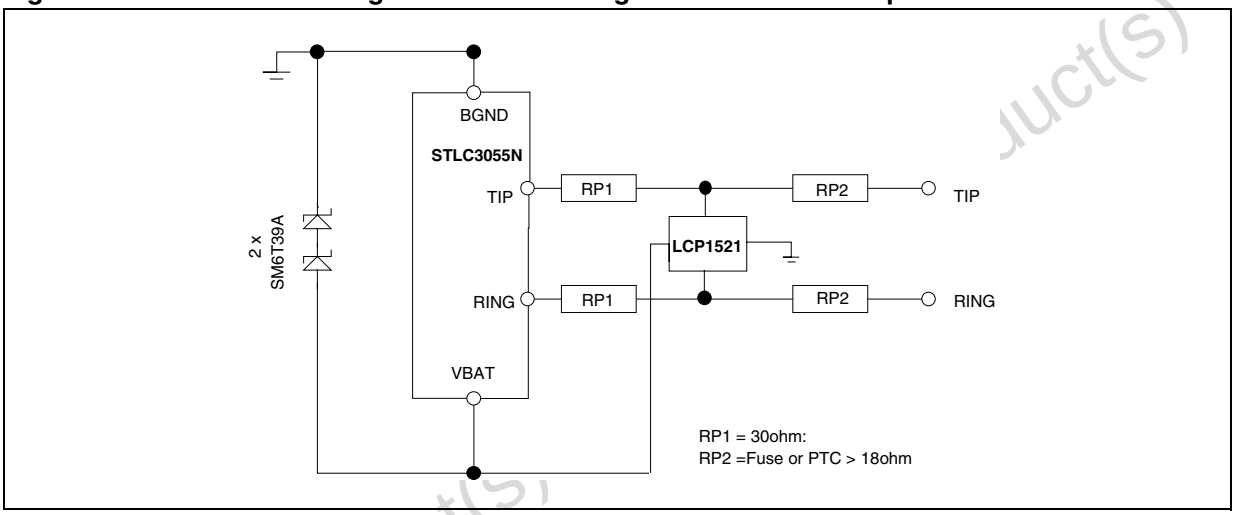
The input levels are interpreted as TTL levels: therefore both 3.3 or 5V CMOS input signals can be accepted by the STLC3055N.

Output DET signal is an open drain (need external pull-up resistor to V_{CC}), therefore also in this case depending on V_{CC} value both 3.3V and 5V logic levels can be generated.

3.13 PROTECTION

Different circuit configuration can be used to protect the device from overvoltages.
The proper solution depends on specified overvoltage and in particular whether the environment, where the STLC3055N has to work, is defined by the K20 requirements or not.
If K20 is requested, a solution, that includes a transient voltage suppressor LCP1521
PTC resistors and two transils has to be used.
Two diodes inside the LCP1521 will clamp to ground the positive lightnings, power cross and voltage overstress.
On the negative ones, the device will fire because of the gate triggered on the voltage V_{BAT}.
A series of two transils (2xSM6T39A), to best fit the voltage clamp (typ.78V), avoid to exceed the total voltage (V_{btot}) applied to the device supply pins $V_{bot} = V_{pos}+V_{BAT} = 90V$ according to the Absolute Max. Rating of the STLC3055N.
PTC resistors like Raychem TR250/80T series will prevent damaging during power cross conditions.

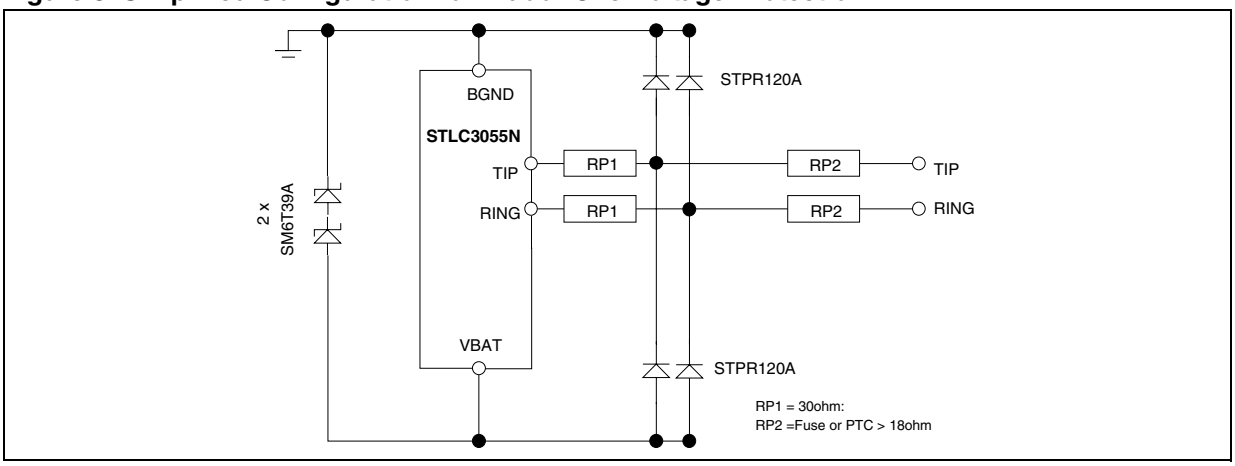
Figure 7. Standard Overvoltage Protection Configuration for K20 Compliance



RP1 = 30Ω and RP2 = ≥18Ω

When K20 requirements are not to be met, a simpler solution consists in the adoption of diodes, between VBAT/TIP,RING, TIP,RING/GND, like :
BYT 11-600 or BYW 100-200 for through hole assembly,
STTB 106U or STPR 120A for SMD assembly.
Also in this case a 2xSM6T39A transils must be used (see fig 8).

Figure 8. Simplified Configuration for Indoor Overvoltage Protection



RP1 = 30Ω and RP2 = ≥18Ω

3.14 RING TRIP

In this slic, the Ring Trip detection is performed sensing the average current (an image of the line current), rectified by a proper circuit, injected in RD resistor.

It is then filtered by CAC capacitor and compared to the Ring Trip Threshold (I_{RTH}), internally programmed, by RD resistor itself (please do not confuse with the resistor RTH setting the Off-Hook threshold for Active and H.Z. modes).

If the average of the trapezoidal AC current changes by the transition from higher ring impedance (on-hook condition) to low impedance (Off-Hook condition), the voltage on RD resistor increases.

As soon as this voltage overcomes the programmed threshold (I_{RTH}) the Ring Trip will be detected.

(In Ring mode there isn't any DC current into RD resistor but only the rectified average current). It is clear that the above described Ring Trip method is obtimised to operate in a short loop (<500ohm) applications and not in presence of very long line.

The ring-trip detection threshold is programmed by the formula : $I_{RTH} = 100/RD$

With 20Hz of ring frequency, CAC=22µF, RD=4KΩ the pin DET goes low about 100ms after the off-hook transition.

When the slic is in Ring mode the average current reaches a level that depends of the REN load, this value, for a correct functionality, have to be lower than I_{RTH} threshold.

Typical application can guarantee up to 3REN of load.

Increasing the REN number up to 5REN, the AC load will increase, the average current I becomes higher than I_{RTH} and, in this case, a ring trip will be detected.

Reducing properly the value of RD it is possible to riadjust the situation.

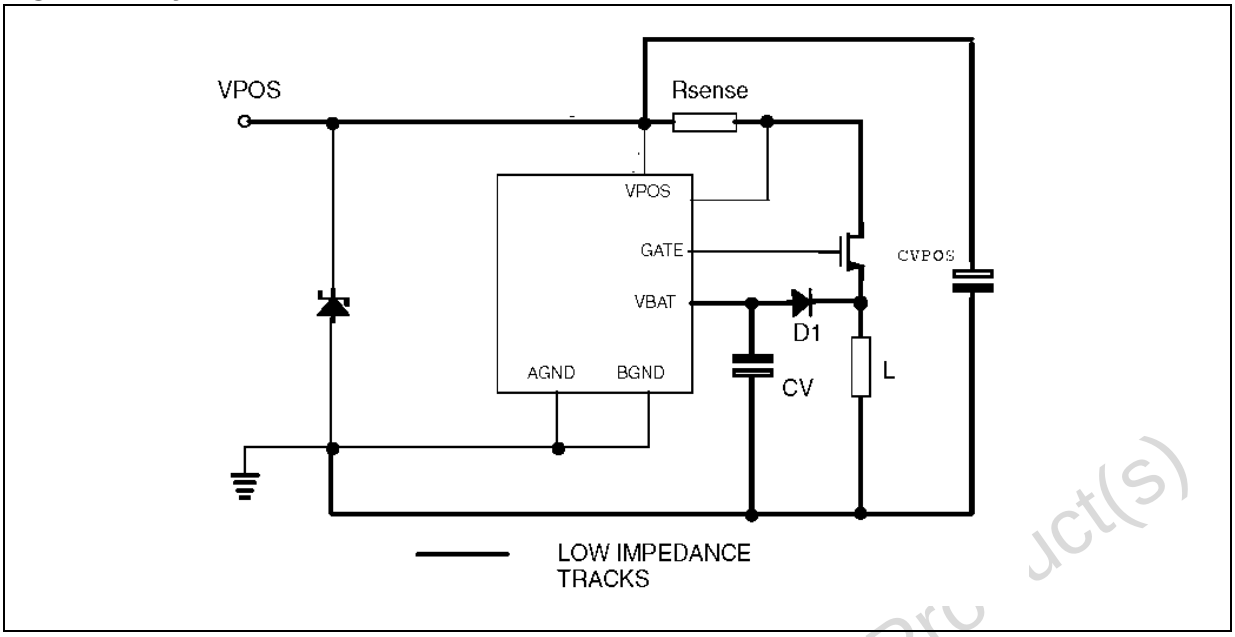
Of course, at the same condition, increasing I_{RTH} threshold, will also increase the Ring trip time.

At the end it is possible to say that the Ring Trip function is function of:

- load (REN number)
- value of the Ring Trip rectified average threshold current "I_{RTH}"
- value of the max peak current sunk from V_{POS} "Ipk", higher the REN number lower the value of R_{SENSE}

3.15 PCB PRECAUTIONS

Figure 9. Layout Reference

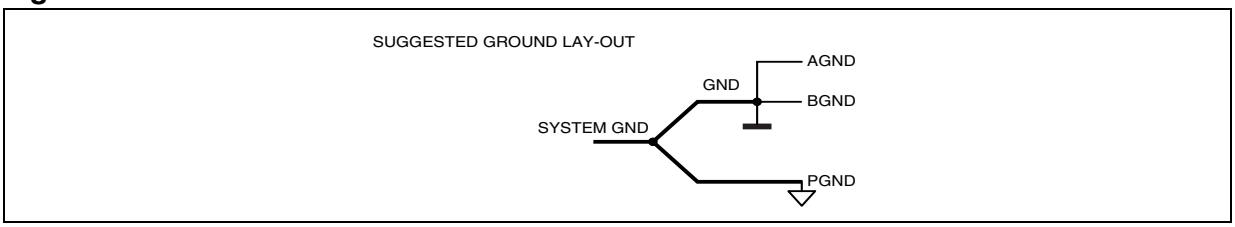


A good PCB layout is a basic aspect to avoid noise problem, that in some cases can even bring the device into a wrong operating condition.
In practice, such noise can be injected by Ground, Supply, parasitic coupling between PCB tracks and by high impedance points.
The layout should prevent any coupling between the DC/DC converter components and analog pins that are referred to AGND (ex: RD, I_{REF}, R_{TH}, R_{LIM}, V_F).
As a first reccomendation the components CV, L1, PMOS, D1, CVPOS, R_{SENSE} should be kept as close as possible to each other and isolated from the other components.
Noise could be produced by the ripple on CVBAT capacitor and in particular across its equivalent series resistor value (ESR). The lower this value, the lower the ripple that can be present on V_{BAT}. A particular care has to be taken for the tracks used for connection between VPOS and dc/dc converter that must be low impedance ones. This is due to the high current flowing in this tracks.
You can prevent noise also connecting R_{REF} (26K1) as close as possible to the I_{REF} pin.

3.16 GROUND CONFIGURATION

Another important point is the ground connection: a star configuration is suggested (see Fig. 3, Application Diagram).

Figure 10.



In fact it's very important to create, on the layout, a proper P-GND area and connecting at this point the gnd of the CV electrolitic capacitor, the gnd of the CVPOS electrolytic capacitor, and the gnd of the inductor .
This P-GND area has to be connected, by a proper track, on the center of the star.
In this way all the perturbation produced by the peack current produced by the switching transistor will be cooled by the center of the gnd star (system GND) without any perturbation on the other AGND/BGND.
All the other components have to be connected on the GND (AGND/BGND) area.

3.17 CAPACITOR

CVB and C14, ceramic capacitors may be used to filter the high frequency ripple and noise that respectively CV and CVPOS, electrolytic capacitors, are not able to reject.
Good choice is to connect also a 100nF from VPOS and GND in order to cancel high frequency noise on the VPOS pin. Above capacitor may be or may not be used depending on the high frequency sensitivity of the apparatus that includes our device.
CRD avoid the noise coupling on RD pin that is an high impedance input.

3.18 ON-HOOK TRANSMISSION

Voice transmission performances are guaranteed in the complete range of loop current down to 0mA setting the slic in Active mode, receiving data on RX, pin during ringing pause.
The max output voltage is correlated to the 2Wire Overload Voltage parameter (see d.s.)

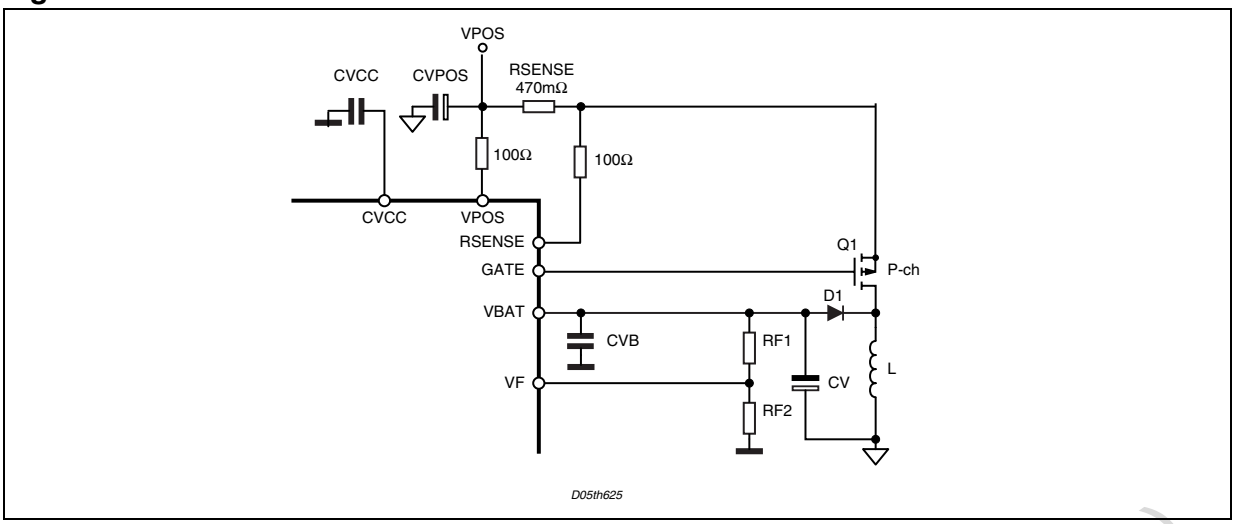
3.19 PHONE DETECTION

The pin DET can also be used to detect the load status of the line.
In fact, with the loop in OH-HOOK condition, setting the slic in Active Reverse polarity and then changing its status to H.I. Feeding when a typ telephone is connected, pin DET will go to low level for a time of about 1.5ms, if the line is open this time becomes about 2µs.

3.20 ESD IMMUNITY

The ESD protection, in this device, withstand a discharge of 2KV with the Human Body Model. If the STLC3055N has to work in sensitive apparatus where equipement tests against ESD immunity are required (4KV, 8KV) some precautions have be taken.
Because the device, during these tests, is usually supplied, the ESD transient can puts in on condition the internal ESD protection diodes connected on VPOS and R_{SENSE} pins.
When the transient disappear and VPOS supplied is higher than 9V, the internal ESD diodes are not able to recover back in off condition.
Using VPOS supply up to 9V the recovery of the ESD diodes is guaranteed and the equipment will be able to pass the ESD immunity tests. When it is not possible to use a reduced VPOS voltage a solution can be found using the schematic configuration below shown.

Figure 11.



Since this solution have an inpact on the threshold of the input limitation circuit it is necessary to increase the RSENSE resistor up to 470 mΩ to restore the previous situation.

3.21 SETTING RESISTOR

The current flowing into the resistor of the STLC3055N application:

IRLIM, IRTH, IRREF = 1.3V/R

IRD = Iline/100

IRSENSE = 100mV/RSENSE

IRF1, IRF2 can be considered about 300μA

Into RS, ZAC, ZA, ZB, RLV, RTTX no dc current flow.

3.22 LONGITUDINAL BALANCE

To avoid degradetion on this parameter, it is very important to use 1% of tolerance of Rp resistors and 1% matching on PTC resistors (if they are used).
In fact low Longitudnal Balance rejection, caused by the mismatching of the resistors or PTC, is able to generate noise problems.
For example in a WLL GSM based, noise can be generated by the 25Hz produced by the 4ms burst of the antenna transmission.

3.23 TTX FILTER

A proper metering pulse (12KHz 16KHz) cancelling low pass filter, with 3rd order, can be obtained choosing those values for the external components:
RLV=16K2//16K2 =8.1K, CFL=1.5nF, R1=1.3 MΩ, R2=180K, C1=47pF, C2=6.8pF.
If the TTX is not requested the components RLV, CS, CFL, RTTX, CTTX can be removed, the pins CKTTX, CTTX1, CTTX2, FTTX have to be connected to GND and, the pin RTTX open.

3.24 GAIN SETTING

In order to adapt the slic also versus the 3.3V, low supply voltage CODEC, the device has the possibility to change TX and RX gains by the Gain Set control pin.

Table 11.

Gain Set	RX Gain	TX Gain	Impedance Syntesys Scale Factor
0	0dB	- 6dB	X 50
1	+ 6 dB	- 12dB	X 25

3.25 COMPLEX IMPEDANCE

Most Countries (Administration) adopt complex impedance for both the “Exchange Impedance” (Zexch) and the “Balance impedance” instead of the 600ohm, purely resistive impedance. As a consequence, the AC input impedance that the slic plus protection resistor shows at its line terminals, (Zs), have to be calculated in order to match properly the Zexch to obtain good performances on the Return Loss parameter.
When Zexch is a complex impedance, the synthesised impedance Zs will be calculate as :

$$Zs = \frac{ZAC}{50} + 2R_p \ , \qquad \text{where 50 is a fixed scale factor .}$$

(For ZAC definition see datasheet)
For Gain Set = 1 the scale factor is 25
Considering, for example, the ETSI 2 complex impedance Zexch = 270 + (750//150nF)
An AC input impedance has to be synthesized on Pins Tip /Ring of the slic (ZAC), to do so, the proper Zs, considering the line terminal, have to be calculated as :
ZAC=(Zs-2Rp)*50 because 2Rp = 100ohm
ZAC= (270-100)*50 + [(750*50)//(150nF/50)]=
ZAC = 8.5K + (37.5K//3nF)
In this way the slic will synthesize Zs impedance matching properly the Zexch.
Also for the 2 to 4 wire conversion, the administration defines an AC terminal Balance impedance Zb properly used to obtain the THL performance.
Good Trans-Hybrid Loss performance and since a proper echo cancellation can be obtained matching properly the two external impedance, ZA and ZB, that can also be complex impedance.
ZA = 50 x Zexch
ZB = 50 x Zb
For Gain Set = 1 the scale factor is 25
In case of Zb=Zexch, the impedances ZA and ZB can be replaced by two resistors calculating their value as:
ZA=ZB= 50 x |Zexch| For Gain Set = 1 the scale factor is 25
Were |Zexch| is the modules @ 1KHz .
For ETSI 2 the value |Zexch| = 842ohm
ZA=ZB= 50 x 842ohm = 42.1Kohm
A typ value of 120pF (with Gain Set = 0) for the capacitors CComp and CH guarantee the first loop stability and the second good THL performances.
For Gain Set = 1 the capacitor value duplicate.

4 REVISION HISTORY

Table 12.

Date	Revision	Description of Changes
May 2005	1	First Issue
October 2005	2	Modified fig11.

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