AN2760
Application note

Using clock distribution circuits in smart phone system design

Introduction

As smart phones become more and more popular in the market, additional features such as A-GPS, Bluetooth, WLAN and DVB-H are now included in the cell phone design. In all of these application modules, there is a common need for a master clock which is typically an external crystal oscillator. With the master clock the data transmitted or received is modulated to the proper frequency. In this application note, conventional clock trees which use discrete crystals for different modules or discrete buffer solutions are compared to the clock solution using the integrated STCD1020/1030/1040 series circuits from STMicroelectronics (referenced as STCD10x0 throughout this application note, please refer to the STCD1020, STCD1030, STCD1040 datasheet). The benefits of using STCD10x0 are illustrated and technical hints are given to help cell phone system designers use the STCD10x0 clock distribution solution.

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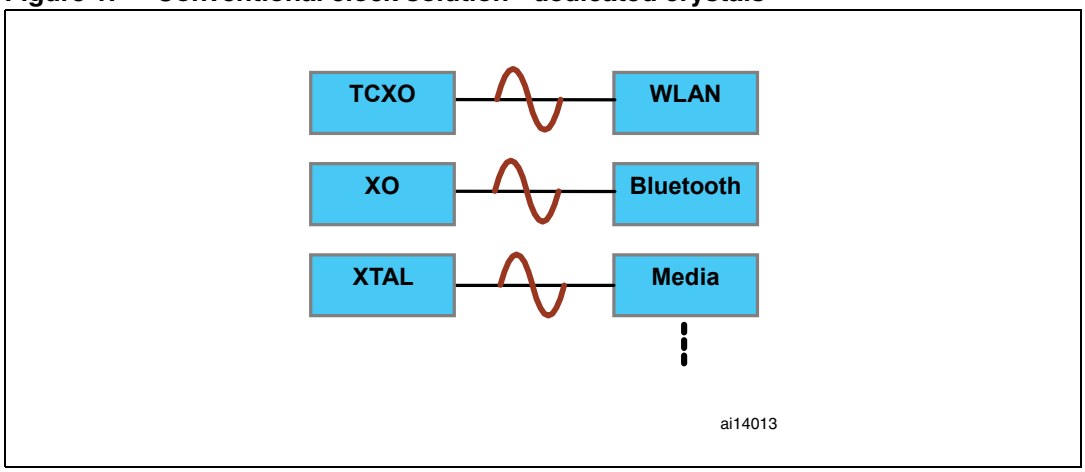
1 Conventional cell phone clock solutions compared to the STCD10x0 integrated solution

1.1 Conventional clock solution - dedicated crystals for dedicated modules

The easiest design of the clock tree in smart phones is to use dedicated crystals for different application modules. This is illustrated in *Figure 1*.

Figure 1. Conventional clock solution - dedicated crystals



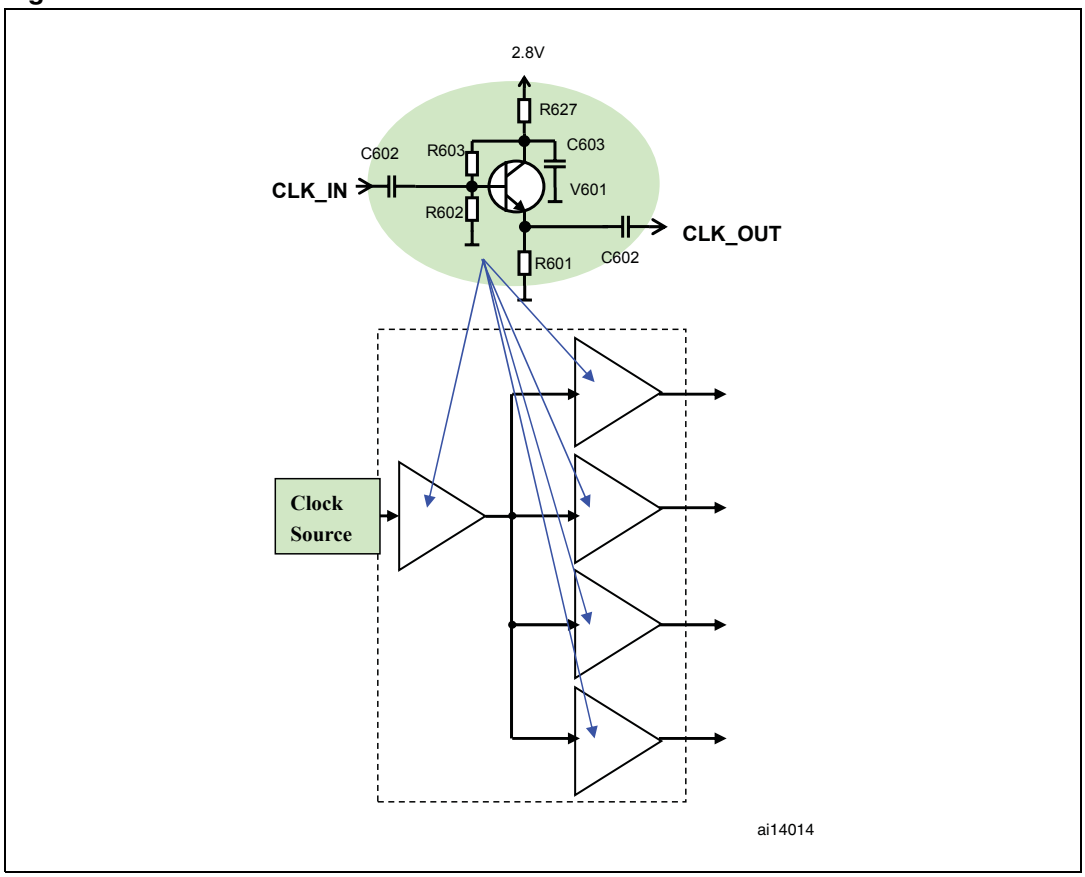
Although the solution in *Figure 1* is simple, an obvious drawback is the cost. Normally WLAN and Bluetooth can accept the master clock in several different frequencies. For example, 13, 16, 16.8, 19.2, 26, 3.6, 38.4 and 52 MHz are all accepted by WLAN, Bluetooth, and FM radio. Different modules recommend different master clock frequencies and those recommended values are not always the same. For example, 19.2 MHz is recommended for Bluetooth by some chip vendors while 26 MHz is recommended for WLAN. Due to the design risk and time-to-market, cell phone vendors are not willing to use the same crystal to serve all application modules although this is possible.

A typical external clock source (typically 10 pF load capability) is always short of fan out capability if several application modules are directly connected to its output.

1.2 Conventional clock solution - discrete buffer solution

Since the cost of a TCXO (temperature compensated crystal oscillator) is extremely high and some of the common frequencies can be used for different applications, cell phone designers have tried to use a discrete buffer solution (with emitter followers) to solve the insufficient fan out issue. A two-stage discrete buffer is used as shown in *Figure 2*. The first stage could solve the problem of the fan out of the clock source (normally TCXO) and also provide a good isolation of input channel to output channels. The second stage distributes the master clock to different application modules and also provides good isolation between different output channels.

Figure 2. Conventional clock solution - discrete buffer solution

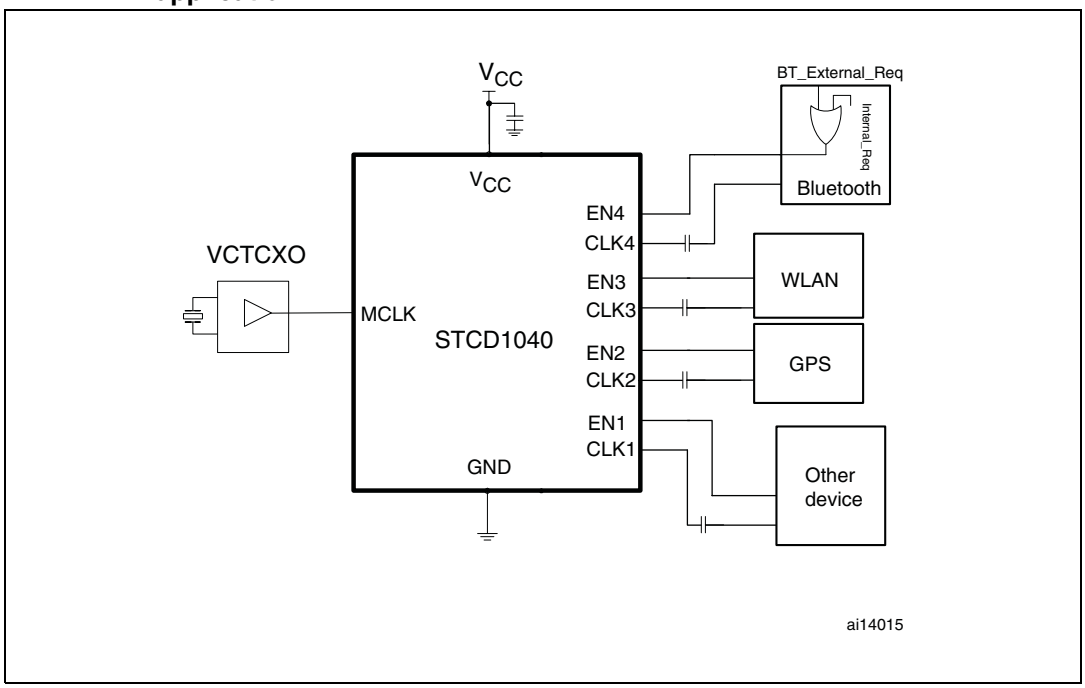


In *Figure 2* only one clock source (TCXO) is used in order to greatly reduce the cost, but there are several drawbacks. The most important issue is the PCB area. This solution includes 5 discrete buffers and each buffer consists of many discrete components such as a bipolar transistor, resistors and capacitors. The large PCB area and the difficulty in routing always become problematic for the system designers. The second issue is the large quiescent current (the static current consumed by the buffer itself) and the inability of the output buffers to be shut down (constantly conduct quiescent current) to save current even when the connected application module does not require the clock.

1.3 Integrated clock solution - STCD10x0

In order to resolve the drawbacks of conventional clock solutions and facilitate cell phone system design, STMicroelectronics has introduced an integrated clock solution with STCD10x0 series clock distribution circuits. A typical application is given in *Figure 3*. The user should note that both sine wave and square wave clock source can be used and the STCD10x0 can distribute to the outputs with unity gain clocks.

Figure 3. Typical application circuit using STCD1040 in mobile phone or MID application



Note: The output DC cut capacitors should only be used on the sine wave clock transmission (not necessary for square wave clock source).

An external clock source (VCTCXO: voltage controlled TCXO) can be connected to the STCD10x0 directly since a DC-CUT capacitor has been integrated into the STCD10x0. Each of the output channels can be enabled/disabled individually so that there is no extra current consumption when there is no clock request for this channel. In order to match different application requirements, two voltage versions (1.8 V and 2.8 V) can be selected by the users. Four-channel outputs with 10 pF capacitive loads for each output consume only 2.8 mA quiescent current. A comparison of the STCD1040 and a discrete buffer solution is given in *Table 1*.

Table 1. Conventional discrete buffer and integrated STCD10x0 clock solution

Parameter	Conventional discrete buffer	STCD10x0
PCB area/cost	Large	Small (up to 60% less PCB area)
Quiescent current	High	Low (at least 30% less current)
Output enable	Always on	Can be disabled individually
Input DC-CUT cap	Required	Not required
System cost	High	Low

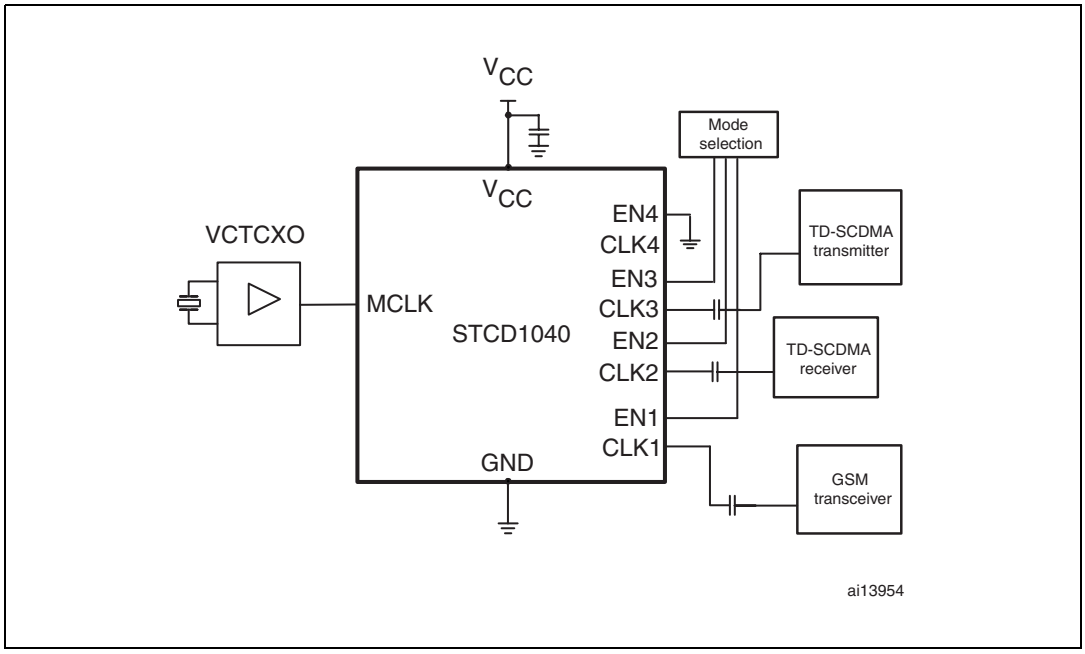
1.4 Integrated STCD10x0 clock solution in MID application

Mobile Internet Device (MID) represents a new category of small and truly mobile devices which integrate the advantages of both UMPC (Ultra-Mobile PC) and mobile phones. This application has recently gained much attention and the trend to incorporate many types of wireless connection technologies such as WLAN, BT and GPS into MIDs. The STCD10x0 solution provides significant benefit to the MID clock solution, not only in system cost but also in PCB area. The connection of the STCD10x0 clock solution in MIDs is also illustrated in *Figure 3*.

1.5 Integrated STCD10x0 clock solution in multimode RF front-end

In multimode mobile RF front-end, multiple reference clocks are typically used for the transceivers. *Figure 4* gives an example of TD-SCDMA/GSM dual-mode mobile RF front-end clock application. Alternatively, the clock from VCTCXO could be distributed by STCD10x0 to the TD-SCDMA transmitter and receiver and GSM transceiver separately.

Figure 4. Typical application circuit using STCD1040 in dual-mode mobile RF front-end



2 Cell phone system design with STCD10x0 clock solution

2.1 Preparation to use STCD10x0

2.1.1 Setting a common clock frequency for each application

In each of the applications (WLAN, GPS, BT, FM radios etc.), the default reference clock frequencies are not the same. The user should configure the internal register or external pins of each application module to make sure they accept the same clock frequency. Once this is done, the common clock source signal can be distributed by the STCD10x0.

Table 2 gives the user an example of different methods to configure each application module to accept the same common reference clock frequency. CS-101560 is the GPS chip from CSR, GSC3KT is the Bluetooth chip from Sirf, STLC4550 and STLC9000 are WLAN chips from STMicroelectronics. Normally, 19.2 MHz, 26 MHz and 38.4 MHz are commonly accepted and the user can configure the internal registers, or external pins, or just directly connect to ensure they run at the same common frequency.

Table 2. Configuring common reference clocks for GPS, BT or WLAM

Part	Common ref. freq.	Ref. clock setting method	How to configure
CS-101560 (CSR)	19.2 MHz	Internal register	Set registers "PSKEY_ANA_FREQ (0x1fe)" and "PSKEY PLLX_FREQ_REF (0xabc)" value to "19200".
	26 MHz		Set register "PSKEY_ANA_FREQ (0x1fe)" value to "26000".
	38.4 MHz		Set registers "PSKEY_ANA_FREQ (0x1fe)" and "PSKEY PLLX_FREQ_REF (0xabc)" value to "38400".
GSC3KT (Sirf)	19.2 MHz	Pin configure	Set pins "ED[7]:JTCK:JTDI" to be "010".
	26 MHz		Set pins "ED[7]:JTCK:JTDI" to be "110".
	38.4 MHz		Set pins "ED[7]:JTCK:JTDI" to be "000".
STLC4550 (ST)	19.2 MHz	Pin configure	Set pins "MODE(4:0)" to be "00100".
	26 MHz		Set pins "MODE(4:0)" to be "11100".
	38.4 MHz		Set pins "MODE(4:0)" to be "11010".
STLC9000 (ST)	19.2 MHz	Automatic detection	An integrated automatic detection algorithm detects the system clock frequencies
	26 MHz		
	38.4 MHz		

2.1.2 Choosing the right clock source

Phase noise is a critical specification in reference clocks. The total phase noise of the clock tree should be obtained by summing the additive phase noise of the STCD10x0 and the phase noise of the clock source (TCXO) in terms of power as illustrated in *Equation 1:*

Equation 1

$$PN_T = 10^{\frac{PN_C}{10}} + 10^{\frac{PN_X}{10}} < PN_A$$

where:

PN_T is the total phase noise in dBc/Hz

PN_C is the additive phase noise of STCD10x0 and

PN_X is the phase noise of clock source

Make sure the total phase noise is kept within the phase noise requirement of each application PN_A. The user should choose the right TCXO with proper phase noise to meet the requirement.

2.2 Power supply V_{CC} of STCD10x0 and decoupling

The STCD10x0 is designed with ultra-low added phase noise so that the device can also be used for master clocks in RF front-end transmitters and receivers for cell phones. A very clean power supply (as specified 30 µVrms supply noise from 300 Hz to 50 kHz in the datasheet) is needed. Normally a TCXO (or VCTCXO) is used as the master clock source. It is strongly recommended to share the same power supply for STCD10x0 with the TCXO since the supply for the TCXO is always an ultra-low noise, high PSRR, LDO. The LDO can be shut down when the TCXO (also STCD10x0) is not needed.

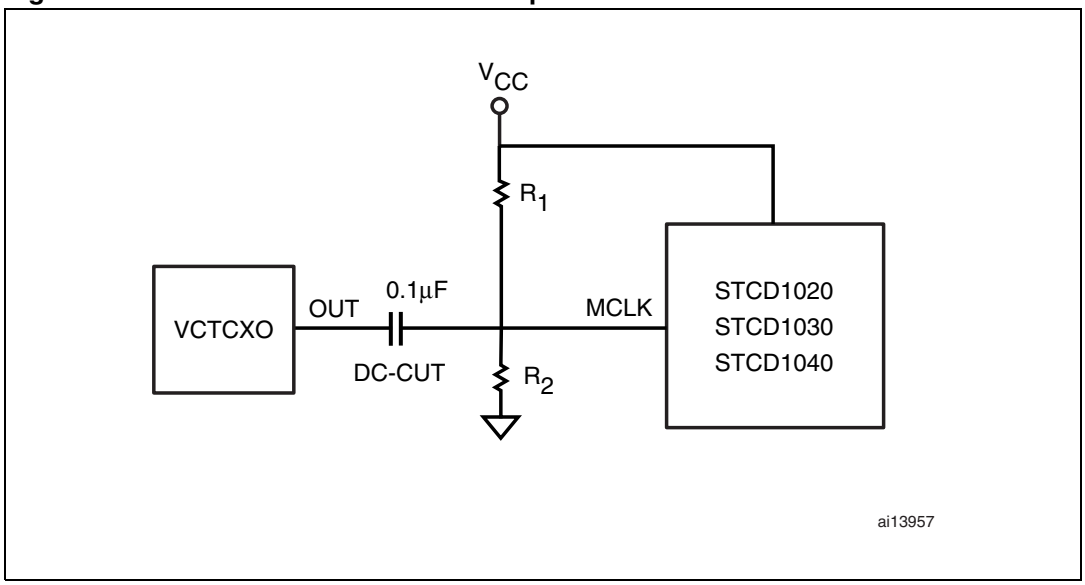
A 1 µF capacitor is highly recommended to be placed as close as possible to the V_{CC} pin of the STCD10x0 on the PC board to minimize the noise of the V_{CC} and guarantee the performance of the phase noise.

2.3 Connection of the MCLK pin to external clock source

If the output of the clock source voltage level is within the supply rails of the STCD10x0, the output of the source clock should be connected directly to the MCLK of the STCD10x0. The direct connection of the source clock is the most common case, allowing a DC-CUT capacitor to be saved on the PCB.

The input clock voltage level of the STCD10x0 cannot exceed the supply rails when it is directly connected to the source clock. If it is necessary to connect a source clock with a voltage level exceeding the supply rails of the clock distribution circuits in the application, the user needs to connect a DC-CUT capacitor serially as shown in *Figure 5*. A voltage divider formed by a resistor string is also needed to set a proper DC bias for the clock input which can keep the clock voltage within the supply rails of STCD10x0. The proper DC voltage is around half of the supply.

Figure 5. Connection of the DC-CUT capacitor and bias



2.4 Connecting STCD10x0 outputs to application modules

The output channels of the STCD10x0 are biased at half of V_{CC} internally by design. 1µF DC-CUT capacitors are required at each of the outputs in most applications.

2.5 Power-down sequence

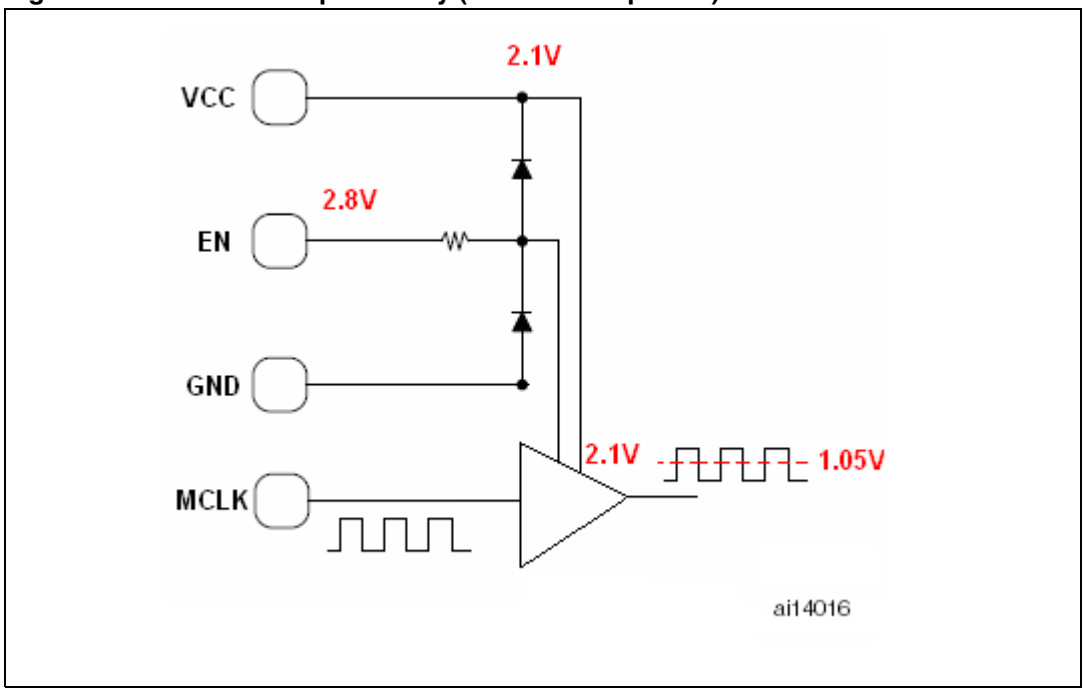
If the STCD10x0 shares the same power supply with TCXO (clock source), it is suggested to power up the TCXO before enabling each of the clock outputs since normally it will take several milliseconds for the TCXO to stabilize its output.

If the STCD10x0 uses different power supplies with TCXO, it is not recommended to power down V_{CC} of STCD10x0 since it only consumes standby current which is no more than 1µA (when no clock output is enabled, the STCD10x0 enters standby mode). If shutdown of the STCD10x0 is preferred, the following power-down steps must be followed:

1. Shut down clock source TCXO output
2. Disable EN pins, pull low
3. Shut down STCD10x0 power V_{CC}

If the power-down sequence is not strictly followed as above, the user may find the clock output waveform viewed at the condition of TCXO active with output, V_{CC} of STCD10x0 shutdown, and EN pins active. This possibility is illustrated in *Figure 6*.

Figure 6. Power-down possibility (incorrect sequence)



In the STCD10x0 chip design, there are ESD diodes for the EN pins to connect to V_{CC} and GND for ESD protection. If V_{CC} is powered down (disconnect to supply) and an active high signal is present on the EN pin (for example, 2.8 V), the ESD diode which connects the EN pin to V_{CC} will conduct and pull V_{CC} up to 2.1V. When the external TCXO is active and sends a clock output to MCLK of STCD10x0, a clock waveform should be viewed at the output as illustrated in *Figure 6* which could cause a problem to the application.

3 Conclusion

As smart phones become more and more powerful with versatile application features, more and more clocks are needed in the cell phone system design. Conventional clock solutions with dedicated crystals or discrete buffers cannot meet the requirement of the design. Using the STCD10x0 in cell phone system design is a very cost-effective, easy solution and shortens the design and layout cycle which allows for faster time-to-market.

4 Revision history

Table 3. Document revision history

Date	Revision	Changes
31-Jul-2008	1	Initial release.