AN3159
Application note

STEVAL-ILH005V2: 150 W HID electronic ballast

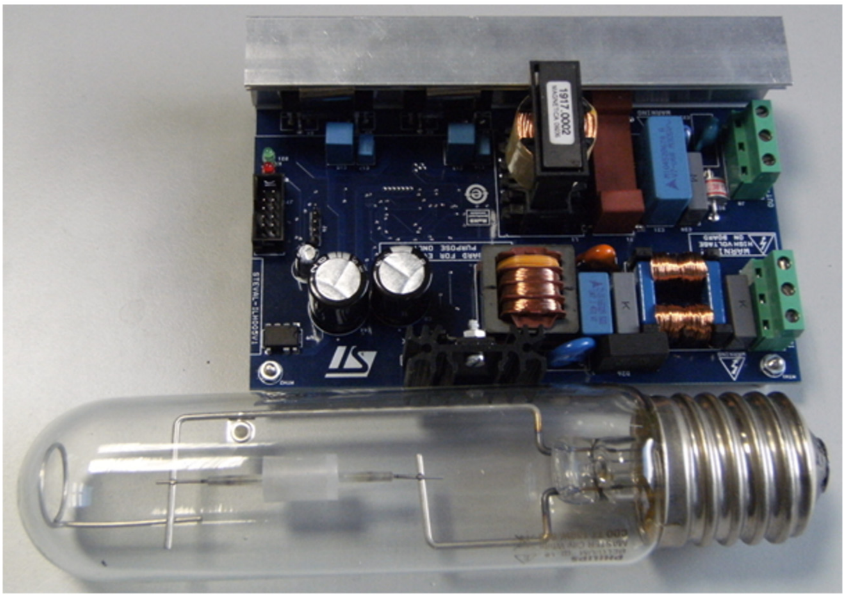
Introduction

This application note describes a two-stage electronic ballast for 150 W HID metal halide lamps. The ballast is made up of a boost converter (power factor controller - PFC) working in transition mode and an inverter made up of a full bridge that drives the lamp at low frequency square wave.

The ballast was developed for 185÷265 V_{AC} 50/60 Hz input mains and is able to drive 150 W metal halide and high pressure sodium lamps.

All lamp phases have been analyzed and some design criteria are given with the test results.

Figure 1. STEVAL-ILH005V2 image



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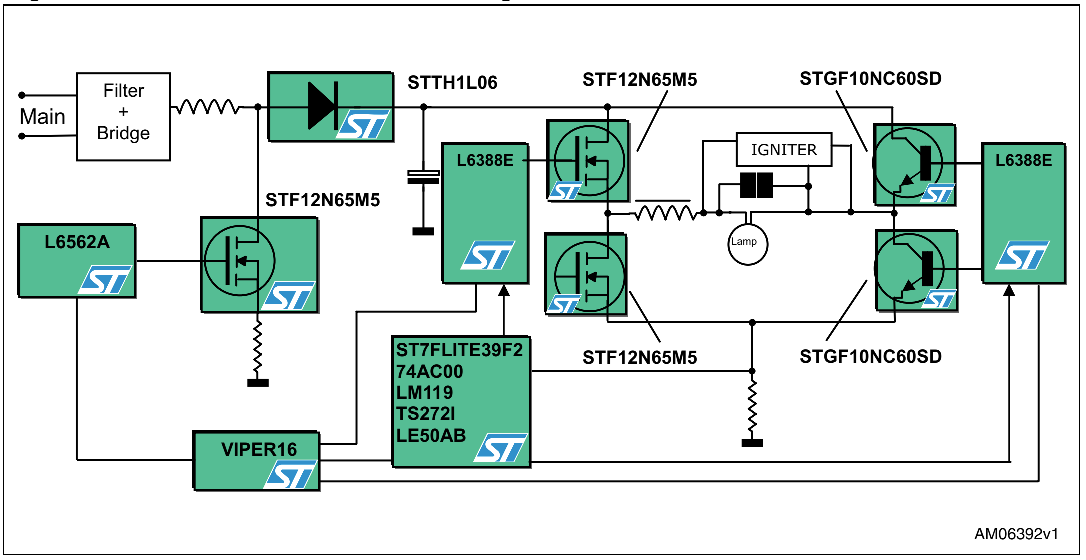
1 General circuit description

The block diagram of the ballast is shown in *Figure 2*. The complete circuit is made up of two stages:

- The boost converter which regulates the DC bus voltage and corrects the power factor
- The inverter stage made up of a full bridge that converts the DC current coming from the PFC stage into an AC current for the lamp.

The operation mode of the full bridge realizes a buck converter. The full bridge also supplies the igniter block to generate the high-voltage pulses.

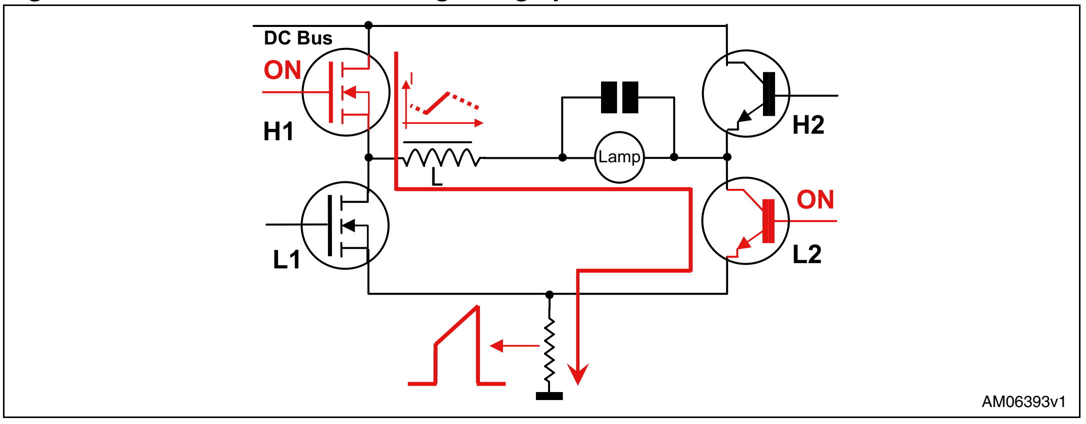
Figure 2. 150 W HID ballast block diagram



To generate a square wave current in the lamp, the circuit is driven in the following way (see *Figure 3*):

1. When low side device L2 is switched ON, the high side power MOSFET H1 operates with a high-frequency pulse width modulation (PWM). The duty cycle D is established by a constant-current control circuit.

Figure 3. Inductor current during charge phase



In this condition the inductor current increases linearly and the voltage across the inductor L is:

Equation 1

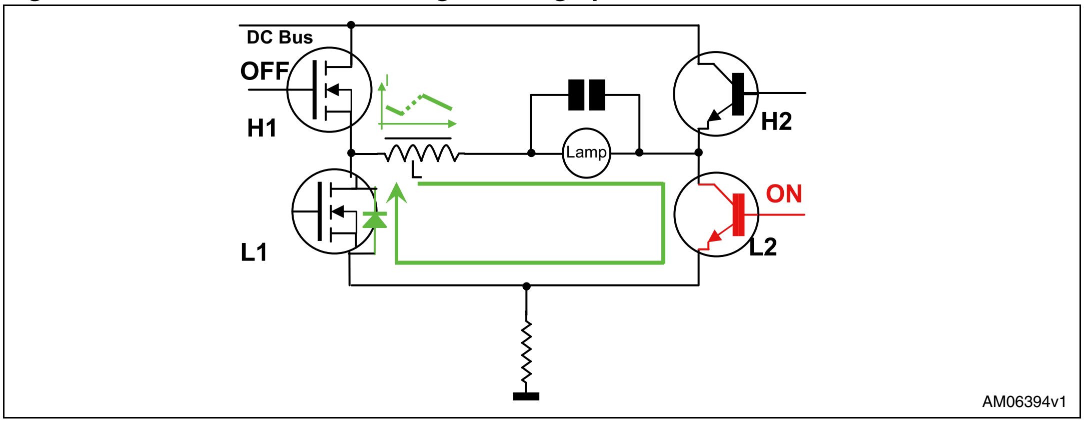
$$V_L = V_{dc} - V_{LAMP}$$

where:

- V_L= lamp voltage
- V_{DC} = DC bus voltage
- V_{LAMP} = lamp voltage

2. When the high side device H1 is switched OFF, the current flows in the low side devices (see *Figure 4* below).

Figure 4. Inductor current during discharge phase



The voltage across the inductor L is:

Equation 2

$$V_L = -V_{LAMP}$$

The current through L decreases linearly. In this way the circuit works as a rectifier buck converter.

The circuit operates in mode A and B complementary in low frequency supplying the lamp with low frequency square wave alternate current.

2 Lamp power calculation

The lamp power is obtained by multiplying the lamp voltage signal for the lamp current.

The lamp voltage is sensed directly across the lamp. The lamp current is obtained by means of the relations reported below.

In continuous mode the lamp current is coincident with average inductor current. Starting from peak inductor current the average value is:

Equation 3

$$I_{LAMP} = I_{AV} = I_{peak} - \frac{\Delta I}{2}$$

where:

- I_{LAMP} = lamp current
- I_{AV} = inductor average current
- I_{peak} = inductor peak current
- ΔI = inductor current ripple

The ripple current in a buck converter in continuous mode is expressed as:

Equation 4

$$\Delta I = \frac{V_{bus}}{f \cdot L} \times \delta \times (1 - \delta)$$

where:

- V_{bus} = DC bus voltage
- L = inductance value
- f = switching frequency
- δ = duty cycle

For the buck converter in continuous mode the duty cycle relation is:

Equation 5

$$\delta = \frac{V_{LAMP}}{V_{BUS}}$$

In the relation (*Equation 4*) substituting (*Equation 5*) it is possible to obtain:

Equation 6

$$\frac{\Delta I}{2} = \frac{1}{2 \cdot f \cdot L \cdot V_{BUS}} \times V_{LAMP} \times (V_{BUS} - V_{LAMP})$$

Assuming V_{BUS} and f are constant it is possible to write:

Equation 7

$$K = \frac{1}{2 \cdot f \cdot L \cdot V_{bus}}$$

The equation (*Equation 3*) can be written as:

Equation 8

$$I_{LAMP} = I_{peak} - K \times V_{LAMP} \times (V_{BUS} - V_{LAMP})$$

This relation is valid because the average current is equal to the lamp current.

This formula is implemented in the ST7 microcontroller in order to calculate the lamp current and regulate the lamp power.

3 Board description

Detailed electrical schematics are given below.

3.1 Electrical schematics

Figure 5. PFC and auxiliary power supply electrical schematic

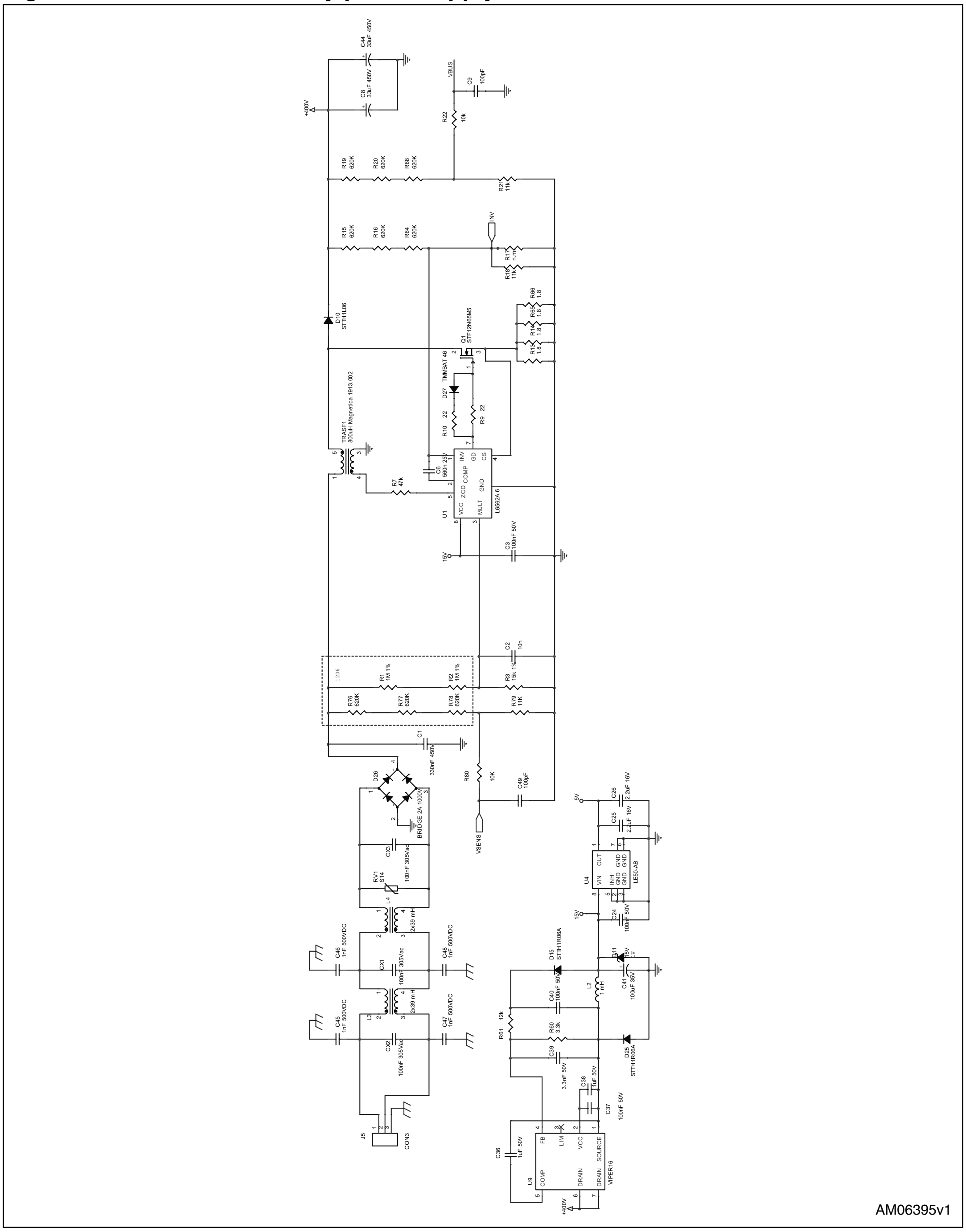


Figure 6. Full bridge electrical schematic

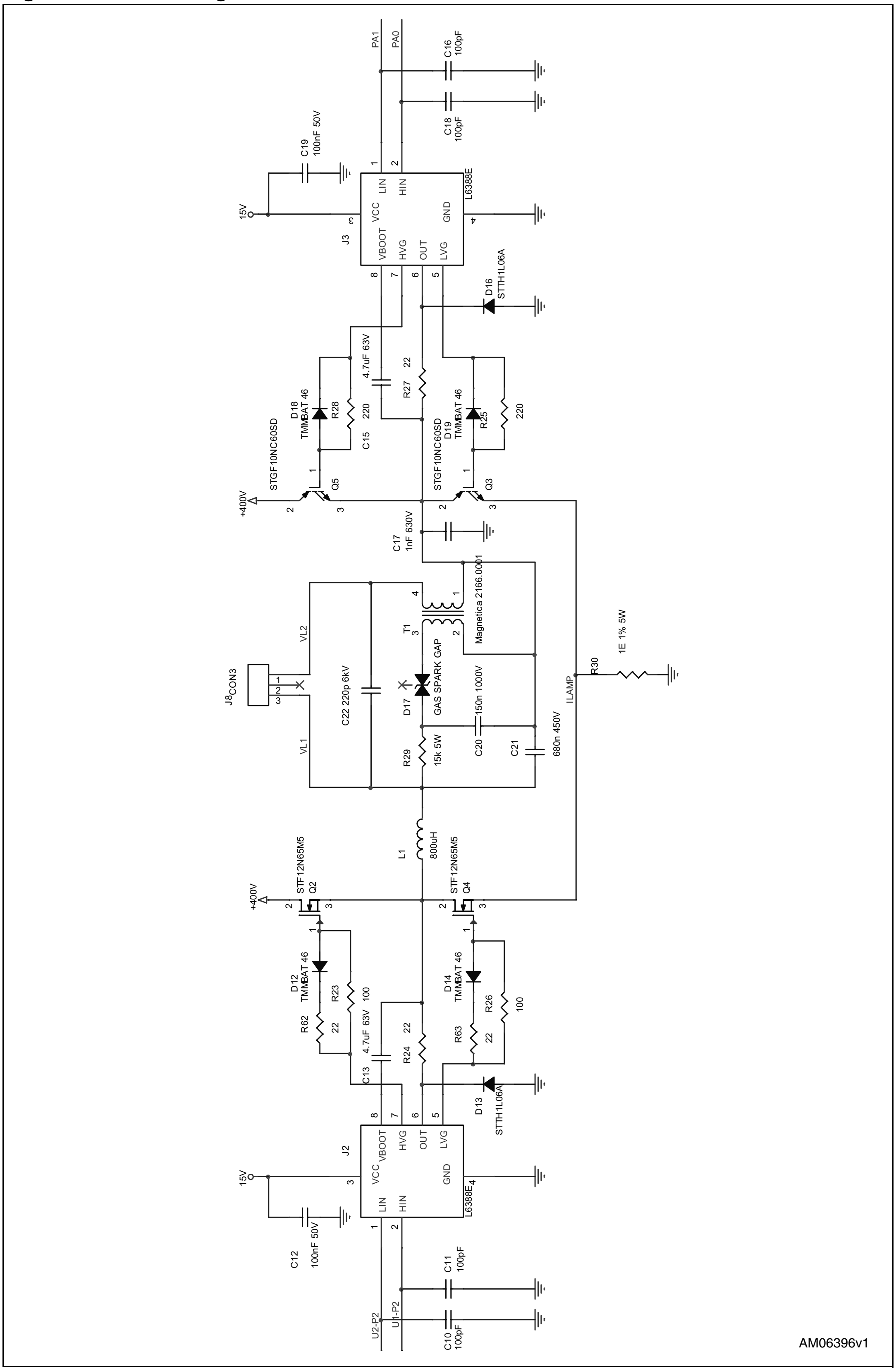
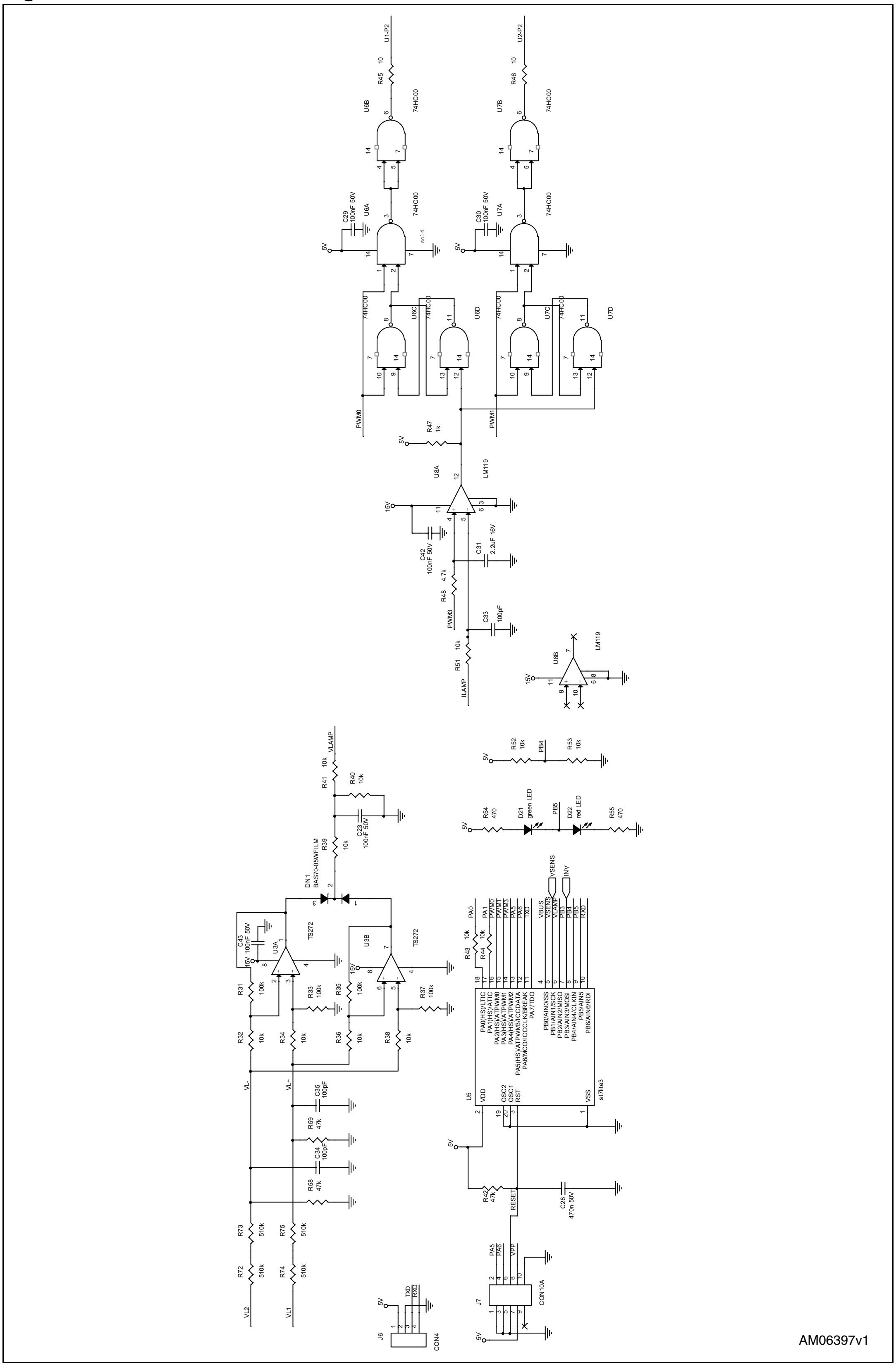


Figure 7. STEVAL-ILH005V1: control section electrical schematic



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3.2 Board layouts

Figure 8. Board layout: top view (not to scale)

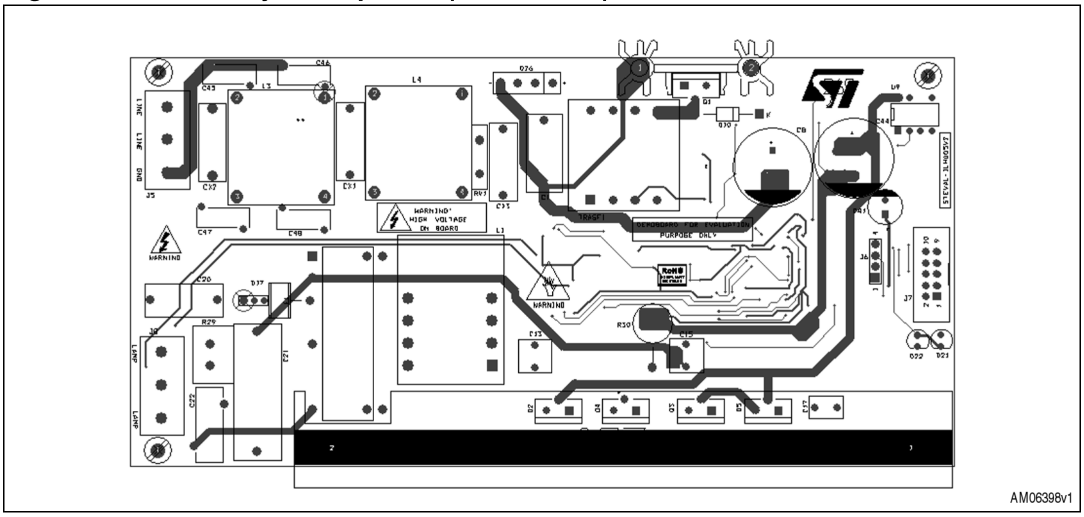
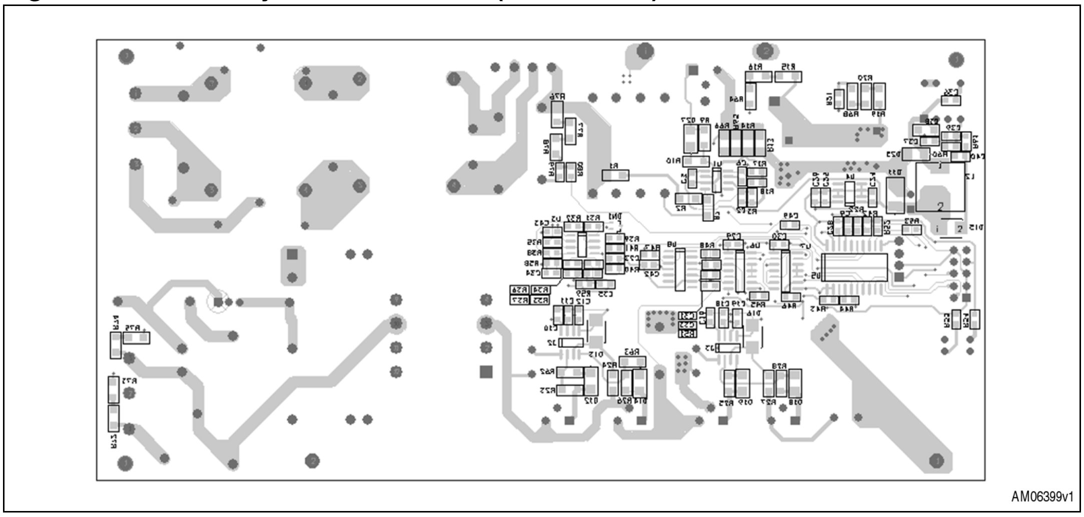


Figure 9. Board layout: bottom view (not to scale)



3.3 Bill of material

Table 1. Bill of material

Reference	Value	Rated	Type	Manufacturer
CX1,CX2,CX3	100 nF, 10%	305 V_{AC}	Polypropylene film capacitor X2	TDK-EPC B32922C3104K000
C45,C46,C47,C48	1 nF, 20%	500 V_{AC}	Y1 suppression ceramic capacitor	
C1	330 nF, 10%	450 V_{DC}	Polypropylene film capacitor (MKT)	TDK-EPC B32672Z4334K000
C2	10 nF, 10%	50 V	X7R ceramic capacitor	
C3,C12,C19,C23, C24,C29,C30,C37,C40, C42,C43	100 nF, 10%	50 V	X7R ceramic capacitor	
C6	560 nF, 10%	25 V	X7R ceramic capacitor	
C8,C44	33 µF, 20%	450 V	Electrolytic capacitor	TDK-EPC B43851F5336MK000
C9, C10,C11,C16,C18, C33,C34,C35,C49	100 pF, 5%	50 V	COG ceramic capacitor	
C13,C15	4.7 µF, 20%	63 V	Polyester film capacitor	TDK-EPC B32529D0475M000
C17	1 nF, 5%	630 V	Polypropylene film capacitor	
C20	150 nF, 101	1000 V	Polypropylene film capacitor	TDK-EPC B32652A0154K000
C21	680 nF, 10%	305 V_{AC}	Polypropylene film capacitor	TDK-EPC B32924C3684K000
C12	220 pF, 10%	6 kV/ 6.3 kV	High-voltage ceramic capacitor	
C25,C26,C31	2.2 µF, 10%	16 V	X7R ceramic capacitor	
C28	470 nF, 10%	50 V	X7R ceramic capacitor	
C36,C38	1 µF, 20%	50 V	X7R ceramic capacitor	
C39	3.3 nF, 10%	50 V	X7R ceramic capacitor	
C41	100 µF, 20%	35 V	Low ESR electrolytic aluminium capacitor	
DN1	BAS70-05WFILM	70 mA/70 V	Schottky diodes	STMicroelectronics BAS70-05WFILM

Table 1. Bill of material (continued)

Reference	Value	Rated	Type	Manufacturer
D10	STTH1L06	1 A/600 V	Ultrafast high-voltage rectifier	STMicroelectronics STTH1L06
D11	15 V	15 V	Zener diode	
D12,D14,D18,D19,D27	TMMBAT 46	100 V/150 mA	Small signal Schottky diode	STMicroelectronics TMMBAT 46
D13,D16	STTH1L06A	1 A/600 V	Ultrafast high-voltage rectifier	STMicroelectronics STTH1L06A
D17	Gas spark gap	350 V/300 A	GAS spark gap	TDK-EPC B88069X0220T502
D21	Green LED	2 mA	High efficiency green diffused LED 2 mA 3 mm	
D22	Red LED	2 mA	High efficiency red diffused LED 2 mA 3 mm	
D15,D25	STTH1R06A	1 A/600 V	Turbo 2 ultrafast high-voltage rectifier	STMicroelectronics STTH1R06A
D26	Bridge 2 A 1000 V	2 A/1000 V	Bridge rectifier	
J2,J3	L6388ED	600 V	High-voltage high and low side driver	STMicroelectronics L6388ED
J5,J8	CON3		Screw terminal 7.5 mm pitch	
J6	CON4		4-pin stripline connector 2.54 mm pitch	
J7	CON10A		10-way 2-row vertical boxed connector	
L1	800 µH	2.5 A	Bridge inductor	MAGNETICA 1917.0002
L2	1 mH	350 mA	Power inductor	TDK-EPC B82464Z4105M000
L3,L4	2x39 mH	1.2 A	Power line choke	EPCOS B82733F2122B001
Q1,Q2,Q4	STF10NM60N	600 V /0.53 Ω	Power MOSFET	STMicroelectronics STF10NM60N

Table 1. Bill of material (continued)

Reference	Value	Rated	Type	Manufacturer
Q3,Q5	STGF10NC60SD	600 V/10 A	PowerMESH™ IGBT	STMicroelectronics STGF10NC60SD
RV1	S14	275 V_{AC}	Varistor	TDK-EPC B72214S0271K101
R1,R2	1 MΩ, 1%		Metal film resistor	
R3	15 kΩ, 1%		Metal film resistor	
R7,R42,R58,R59	47 kΩ, 1%		Metal film resistor	
R9, R10,R24,R27,R62,R63	22 Ω, 1%		Metal film resistor	
R13,R14,R65,R66	1.8 Ω, 1%		Metal film resistor	
R15,R16,R19,R20,R64,R68, R76,R77,R78	620 kΩ, 1%		Metal film resistor	
R17	0	Not mounted	Metal film resistor	
R18,R21,R79	11 kΩ, 1%		Metal film resistor	
R22,R32,R34,R36,R38,R39, R40,R41,R43,R44,R51,R52, R53,R80	10 kΩ, 1%		Metal film resistor	
R23,R26	100 Ω, 1%		Metal film resistor	
R25, R28	220 Ω, 1%		Metal film resistor	
R29	15 kΩ, 5%		Ceramic resistor	
R30	1 Ω, 1%		Metal film resistor	
R31,R33,R35,R37	100 kΩ, 1%		Metal film resistor	
R45,R46	10 Ω, 1%		Metal film resistor	
R47	1 kΩ, 1%		Metal film resistor	
R48	4.7 kΩ, 1%		Metal film resistor	
R54,R55	470 Ω, 1%		Metal film resistor	
R60	3.3 kΩ, 1%		Metal film resistor	
R61	12 kΩ, 1%		Metal film resistor	

Table 1. Bill of material (continued)

Reference	Value	Rated	Type	Manufacturer
R72,R73,R74,R75	510 kΩ, 1%		Metal film resistor	
TRASF1	800 µH E25 n1/n2=10	1 A	PFC inductor	MAGNETICA 1913.0002
T1			Igniter	Vogt / MAGNETICA SL0607111102 / 2166.0001
U1	L6562A		Transition-mode PFC controller	STMicroelectronics L6562AD
U3	TS272		Dual operational amplifiers	STMicroelectronics TS272AID
U4	LE50-AB		Low drop voltage regulators	STMicroelectronics LE50AB
U5	st7lite3		Microcontroller	ST ST7FLITE39F2M6
U6,U7	74HC00		QUAD 2-input NAND GATE	STMicroelectronics M74HC00M1R
U8	LM119		High speed dual comparators	STMicroelectronics LM119D
U9	VIPer16		VIPer	STMicroelectronics VIPER16LN
Heatsink 1				
Heatsink 2				
MTH1, MTH2	Mounting hole		Mount M3x10 mm spacer	

4 PFC section

The front-end stage of conventional offline converters, typically consisting of a full-wave rectifier bridge with a capacitor filter, has an unregulated DC bus from the AC mains. The filter capacitor must be large enough to have a relatively low ripple superimposed on the DC level. The current from the mains is a series of narrow pulses with very high amplitude. A consequence of this condition is the distortion of the AC line voltage, and poor utilization of the power system's energy capability. This can be measured considering two parameters:

- total harmonic distortion (THD)
- power factor (PF)

A traditional input stage with capacitive filter has a low PF (0.5-0.7) and a high THD. By using switching techniques, a power factor corrector (PFC) preregulator, the PF is very close to 1 and THD falls to very low values (<10%) drawing a quasi-sinusoidal current from the mains, in phase with the line voltage.

Theoretically, any switching topology can be used to achieve a high PF but, practically, the boost topology has become the most popular thanks to the advantages it offers (low-cost solution, low noise on input section, and easy to drive switch).

Two methods of controlling a PFC preregulator are currently widely used:

- fixed frequency average current mode PWM (FF PWM)
- transition mode (TM) PWM (fixed ON time, variable frequency).

In this application the PFC section is realized with a boost converter working in transition mode, the PFC stage and design criteria are explained.

4.1 Input specifications

- Minimum mains voltage (rms value): $V_{ACmin} = 185$ V
- Maximum mains voltage (rms value): $V_{ACmin} = 265$ V
- Minimum main frequency: $f_{min} = 47$ Hz
- Rated out power: $Pout = \frac{P_{LAMP}}{\eta_{bridge}}$
- Output current: $I_{out} = \frac{P_{out}}{V_{out}} = 0.38A$
- Rated lamp power: $P_{LAMP} = 150$ W
- Expected bridge efficiency: ηbridge = 95%
- Regulated DC output voltage (DC value): Vout = 420 V
- Maximum output overvoltage (DC value): ΔOVP = 50 V
- Maximum output low-frequency ripple: ΔVoutx = 20 V
- PFC minimum switching frequency: $f_{min} = 28$ kHz
- Expected PFC efficiency: η_{PFC} 96%
- Expected input section efficiency: η_{in} 99%
- Expected power factor: 0.99.

4.2 Operating conditions

- Expected input power:

Equation 9

$$P_{in} = \frac{P_{LAMP}}{\eta_{Bridge} \cdot \eta_{PFC} \cdot \eta_{in}} = \frac{150}{0.95 \cdot 0.96 \cdot 0.99} = 166W$$

- Maximum rms input current:

Equation 10

$$I_{in} = \frac{P_{in}}{V_{ac\,min} \cdot PF} = \frac{168}{185 \cdot 0.99} = 0.92A$$

- Maximum peak inductor current:

Equation 11

$$I_{LPK} = 2 \cdot \sqrt{2} \cdot I_{in} = 2 \cdot \sqrt{2} \cdot 0.92 = 2.6A$$

- Maximum rms inductor current:

Equation 12

$$I_{L1} = \frac{2}{\sqrt{3}} \cdot I_{in} = \frac{2}{\sqrt{3}} \cdot 0.92 = 1.06A$$

- Maximum rms diode current:

Equation 13

$$I_{D10} = I_{L1pk} \sqrt{\frac{4 \cdot \sqrt{2}}{9 \cdot \pi} \cdot \frac{V_{ac\,min}}{V_{out}}} = 0.77A$$

4.3 Power components

Input capacitor

To calculate the input capacitor the following relationship can be used:

Equation 14

$$C_{in} = \frac{I_{in}}{2 \cdot \pi \cdot f_{sw\,min} \cdot r \cdot V_{ac\,min}} = \frac{0.92}{2 \cdot \pi \cdot 30k \cdot 0.1 \cdot 185} = 262nF$$

A commercial value of 220 nF was selected. A bigger capacitor improves the EMI behavior but worsens the THD.

Output capacitor

The output bulk capacitor selection depends on the DC output voltage and the converter output power.

Equation 15

$$C_o = \frac{P_{out}}{4 \cdot \pi \cdot f_{min} \cdot V_{out} \cdot \Delta V_{out}} = \frac{150}{4 \cdot \pi \cdot 47 \cdot 420 \cdot 20} = 31.9\mu F$$

Considering the tolerance of the electrolytic capacitors, two capacitors of 22 µF, in parallel, were selected.

Boost inductor

The boost inductor must be calculated at minimum and maximum V_{AC}. The minimum inductance value must be selected.

Equation 16

$$L1 = \frac{V_{ac}^2 \cdot (V_{out} - \sqrt{2} \cdot V_{ac})}{2 \cdot f_{sw\,min} \cdot Pin \cdot V_{out}}$$

Equation 17

$$L_{1max} = \frac{185^2 \cdot (420 - \sqrt{2} \cdot 185)}{2 \cdot 28k \cdot 166 \cdot 420} = 1.39\,mH$$

Equation 18

$$L_{1min} = \frac{265^2 \cdot (420 - \sqrt{2} \cdot 265)}{2 \cdot 28k \cdot 166 \cdot 420} = 0.81\,mH$$

For this application, boost inductance of 0.8 mH has been chosen.

Power MOSFET selection

For power MOSFET selection, the following parameters must be considered:

1. Breakdown voltage. This depends on the output voltage, the admitted overvoltage, and the external conditions (minimum temperature for example)
2. $R_{DS(on)}$. This depends on the output power

The MOSFET used in this section is the STF12N65M5 which guarantees high breakdown voltage and low $R_{DS(on)}$. Thermal measurements have confirmed this to be the right choice of device.

Boost diode selection

The PFC section is realized with a boost converter working in transition mode. The STTHxL06 family, which is using ST Turbo2 600 V technology, is specially suited as the boost diode in discontinuous or transition mode power factor corrections.

The selection criteria it is based on breakdown voltage and current. A rough selection can be performed adopting the following criterion:

- The breakdown voltage must be higher than (Vout + Vop) +margin
- The diode current must be higher than 3 times the average current Iout

In this case STTH1L06 has been chosen. The rms diode current is:

Equation 19

$$I_{D10} = I_{L1pk}\sqrt{\frac{4\cdot\sqrt{2}}{9\cdot\pi}\cdot\frac{V_{ac\,min}}{V_{out}}} = 0.77A$$

To evaluate the conduction losses use the following equation:

Equation 20

$$P_{D10} = 0.89\cdot I_{out} + 0.165\cdot I_{D10}^2 = 0.43W$$

Considering T_{jmax} = 150 °C and the maximum ambient temperature T_{ambmax} = 50 °C, it is possible to calculate the $R_{THJ\text{-}amb}$ as follows:

Equation 21

$$R_{THJ\text{-}amb} = \frac{T_{jmax} - T_{ambmax}}{P_{diode}} = \frac{150-50}{0.43} = 231°C/W$$

The calculated R_{th} is higher than the STTH1L06 thermal resistance junction-ambient, so no heat sink is needed.

In any case, thermal measurements confirmed the real device temperature.

4.4 L6562A biasing circuitry

- Pin 1 (INV): a resistive divider is connected between the boost regulated output voltage and this pin. The internal reference on the non-inverting input of the E/A is 2.5 V (typ.), while the DIS intervention threshold is 27 µA (typ.). The divider resistor is selected using the following equations:

Equation 22

$$\frac{R_{outH}}{R_{outL}} = \frac{V_{out}}{2,5} - 1$$

Equation 23

$$R_{outH} = \frac{\Delta V_{OVP}}{27\mu A}$$

where R_{outH} is the upper resistor, R_{outL} is the lower one, and ΔV_{OVP} is the overvoltage threshold.

Fixing the V_{OVP} value at 55 V Vout = 420 V obtains:

Equation 24

$$R_{outH} = 1.851M\Omega$$

Equation 25

$$\frac{R_{outH}}{R_{outL}} = 167$$

Equation 26

$$R_{outL} = \frac{R_{outH}}{167} = 11k\Omega$$

Using SMD resistor 1206 size, the R_{outH} value is obtained connecting in series 3 resistors of 620 kΩ. A commercial value of 11 kΩ for R_{outL} is selected.

This pin can also be used as an ON/OFF control input if shorted to GND.

- Pin 2 (COMP): this pin is the output of the E/A that is fed to one of the two inputs of the multiplier. A feedback compensation network is placed between this pin and the INV pin. The compensation network can be just a capacitor which can be dimensioned using the formula reported below and setting the bandwidth (BW) from 20 to 30 Hz.

Equation 27

$$C_{comp} = \frac{1}{2 \cdot \pi \cdot (R_{outH} // R_{outL}) \cdot BW}$$

where the symbol $R_{outH}//R_{outL}$ is the equivalent value of the parallel between R_{outH} and R_{outL}.

In this design, choosing a bandwidth of 25 Hz, a capacitor C= 560 nF has been used.

- Pin 3 (MULT): this pin is the second multiplier input and is connected through a resistive divider to rectified mains to get a sinusoidal voltage reference. The procedure to properly set the operating point of the multiplier is:

1. Select the max. value of Vmult. The maximum peak value occurs at maximum mains voltage.

Equation 28

$$Vmult_{max} = \frac{ILpk \cdot R_s}{1.1} \cdot \frac{V_{acmax}}{V_{acmin}} = \frac{2.59 \cdot 0.375}{1.1} \cdot \frac{265}{185} = 1.27$$

where 1.1 V/V is the multiplier maximum slope reported in the datasheet.

2. Calculate the maximum divider ratio.

Equation 29

$$K_p = \frac{Vmult_{max}}{\sqrt{2} \cdot Vac_{max}} = \frac{1.27}{\sqrt{2} \cdot 265} = 3.38 \cdot 10^{-3}$$

3. Calculate the lower resistor supposing a 0.2 mA current flowing into the multiplier divider.

Equation 30

$$R_{multL} = \frac{Vmult_{max}}{Imult} = \frac{1.27}{0.2 \cdot 10^{-3}} = 6.35k\Omega$$

4. Calculate the upper resistor using the following formula:

Equation 31

$$R_{multH} = \frac{1-K_p}{K_p} \cdot R_{multL} = \frac{1-0.555}{1-0.555} \cdot 6.35k\Omega = 1865.15k\Omega$$

The commercial values for R_{multL}= 6.8 kΩ have been selected. Two resistors of 910 kΩ have been connected in series for R_{multH}= 1820 kΩ. Adopting these values $V_{multmin}$= 0.97 V and $V_{multmax}$= 1.39 V.

- Pin 4 (CS): this pin is the inverting input of the current sense comparator. The sense resistor value (R_s) can be calculated as follows:

Equation 32

$$R_s < \frac{V_{csmin}}{IL_{pk}} = \frac{1}{2.59} = 0.386$$

where:

– ILpk = is the maximum peak current

– V_{csmin} = 1 V (see the L6562A datasheet)

To obtain this value four resistor values of 1.5 Ω in parallel have been connected obtaining 0.375.

- Pin 5 (ZCD): this is the input of the zero current detector circuit. To calculate the right turn ratio between main and auxiliary winding, the maximum turn ratio must be calculated as:

Equation 33

$$n_{max} = \frac{n_{primary}}{n_{auxiliary}} = \frac{V_{out} - \sqrt{2} \cdot Vac_{max}}{\text{Arming voltage} \cdot \text{margin}} = \frac{420 - \sqrt{2} \cdot 265}{1.4 \cdot 1.15} = 28$$

The turn ratio must be lower than this value. For this application a turn ratio =10 was selected.

The limiting resistor can be calculated considering the maximum voltage on the auxiliary winding with the selected turn ratio and assuming 0.8 mA current through the pin. The resistor value can be obtained using the formula:

Equation 34

$$Rmin = \frac{\frac{Vout}{n_{aux}} - VzcdH}{I_{max}} = \frac{\frac{420}{10} - 5.7}{0.8} = 45{,}4k\Omega$$

Equation 35

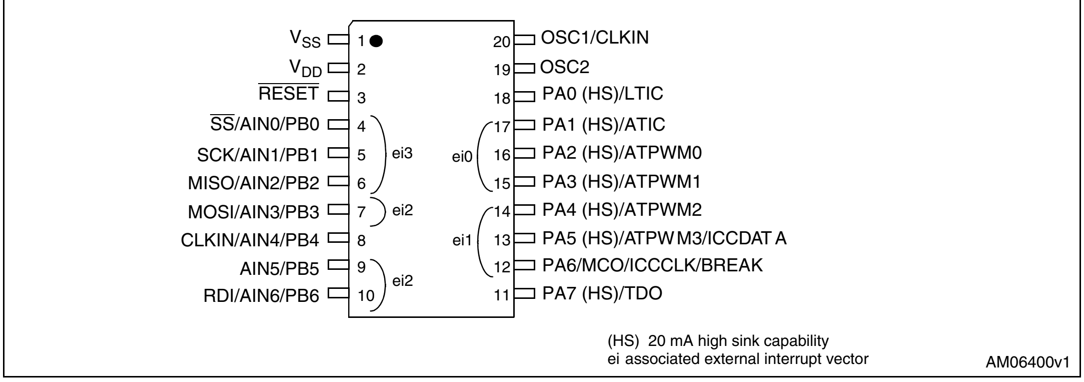
$$Rmax = \frac{\frac{Vout}{n_{aux}} - VzcdL}{I_{max}} = \frac{\frac{420}{10} - 0}{0.8} = 52{,}5k\Omega$$

V_{ZCDH} and V_{ZCDL} are the upper and lower ZCD clamp voltages of the L6562A. The higher value must be chosen. The commercial value of 56 k was selected.

- Pin 6 (GND)
- Pin 7 (GD): gate driver
- Pin 8 (Vcc): supply of the device.

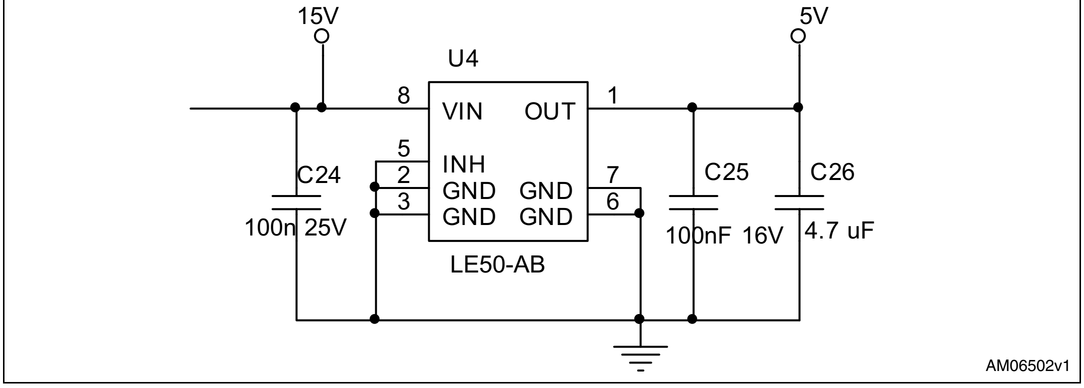
5 ST7 microcontroller application pins utilization

Figure 10. ST7FLITE39F2 pinout



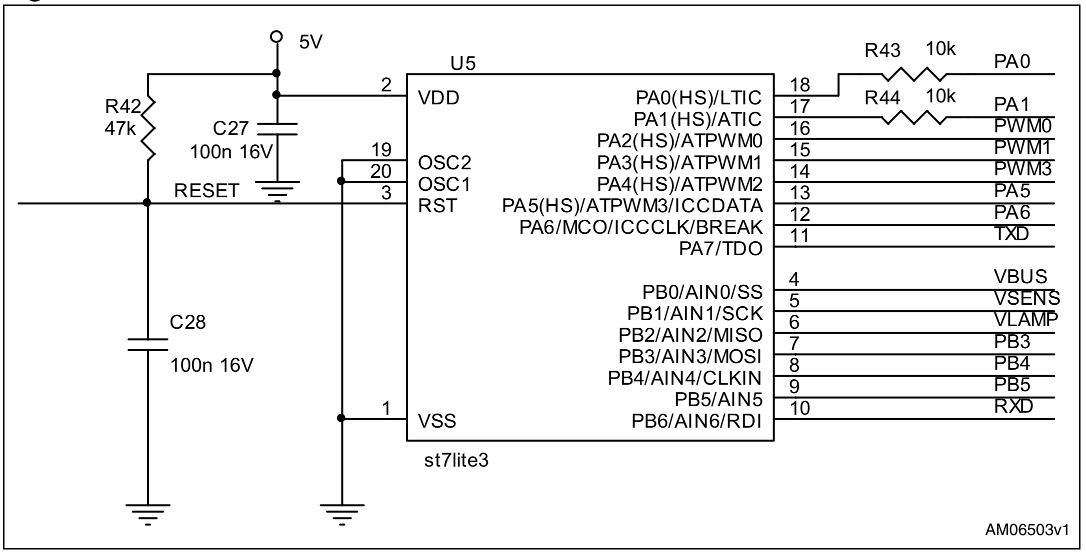
- Pin 1: GND
- Pin 2: VDD, main supply voltage. The power is realized using an STMicroelectronics LE50. It is able to supply 5 V with ± 1% of tolerance. In *Figure 11* the adopted circuit is shown.

Figure 11. MCU reference voltage circuit



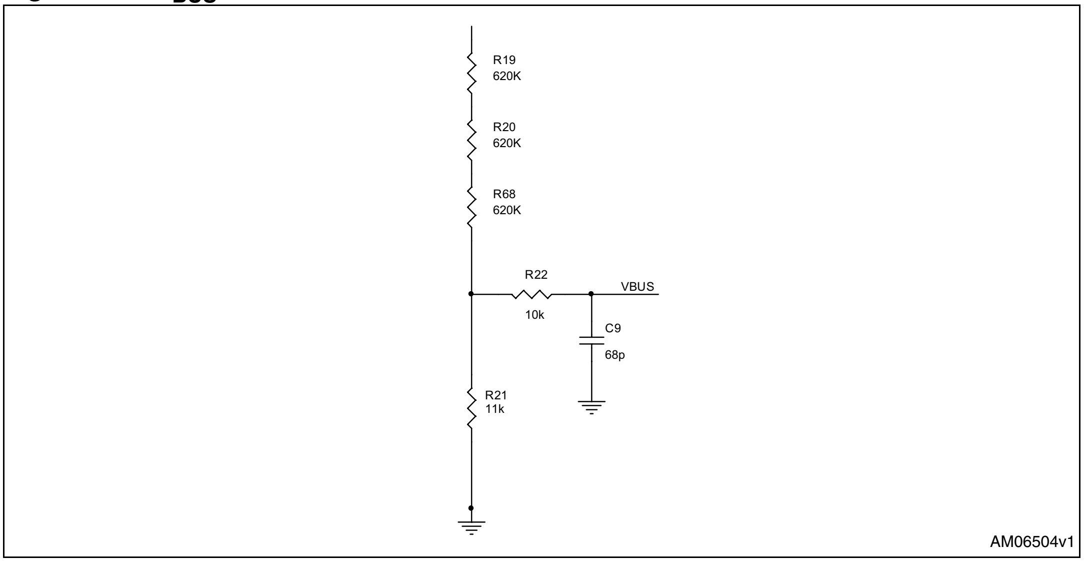
- Pin 3: reset non-maskable interrupt (active low). R2 and C6 are used to detect if the reference voltage has reached 5 V. The MCU gives a reset if the +5 V level voltage is not reached.

Figure 12. Pin utilization and reset circuit



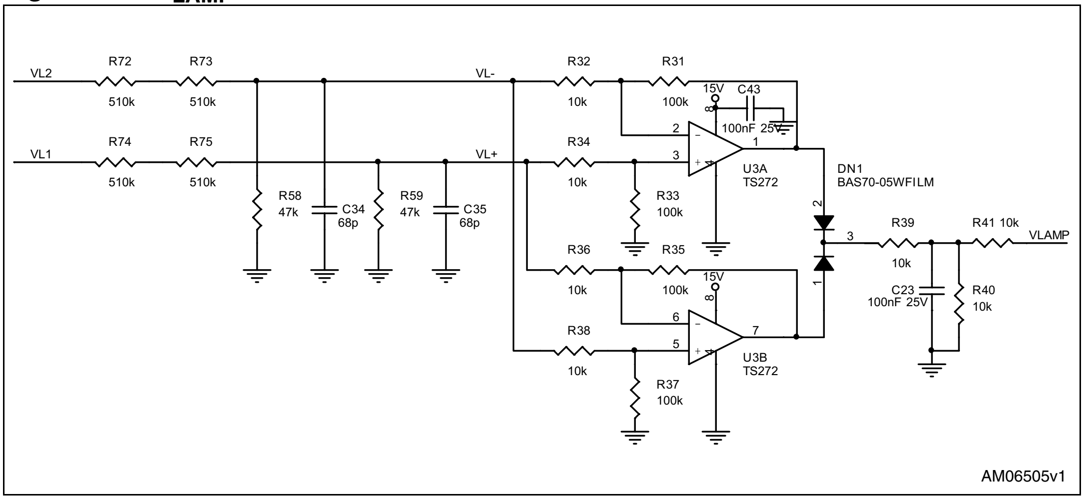
- Pin 4: ADC channel 0 analog input, to provide the V_{BUS} measurement. A resistor partition is used to obtain a maximum of 5 V, starting from a +400 V of bus, compatible with the MCU voltage input.

Figure 13. V_{BUS} measurement circuit



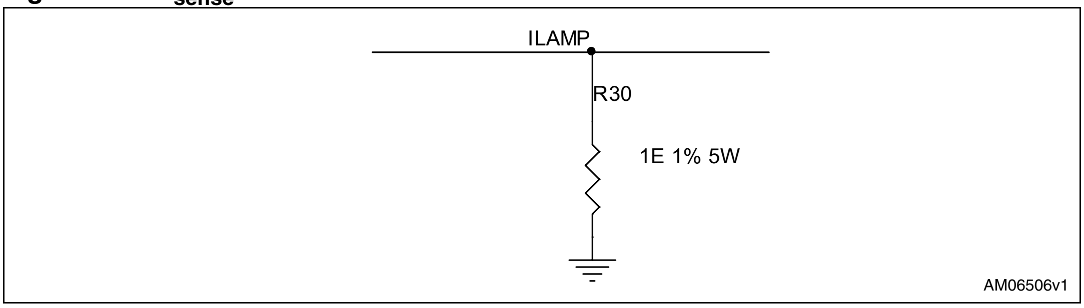
- Pin 5: ADC analog input 1 - not used
- Pin 6: ADC analog input 2. Used to measure the lamp voltage. In *Figure 14* the circuit to measure the lamp voltage is shown. The voltage across the capacitor C23 is used as the input of U4a to obtain a signal compatible with the MCU input.

Figure 14. V_{LAMP} measurement circuit



- Pin 7: PB3 digital floating input with interrupt. Used for maximum current protection
- Pin 8: PB4 digital floating input. Used for MCU Vref calibration
- Pin 9: push-pull output. Used to drive two status LEDs. The green LED indicates the normal status. The red LED indicates a fault condition (for example overcurrent protection).
- Pin 10: SCI RXD. Used for external communication, power line modem or PC
- Pin 11: SCI TXD. Used for external communication, power line modem or PC
- Pin 12-13: PA6-PA5. Not used
- Pin 14: PA4 output PWM3. Used to generate a reference voltage for the constant-current control.

Figure 15. R_{sense} circuit



The current signal is obtained through the sense resistors R30, R49, and R50 connected in parallel (I_{LAMP} signal *Figure 15*) and is compared with the reference voltage coming from the MCU.

When the I_{LAMP} signal exceeds the threshold, the comparator output follows down giving the reset signal at the drivers.

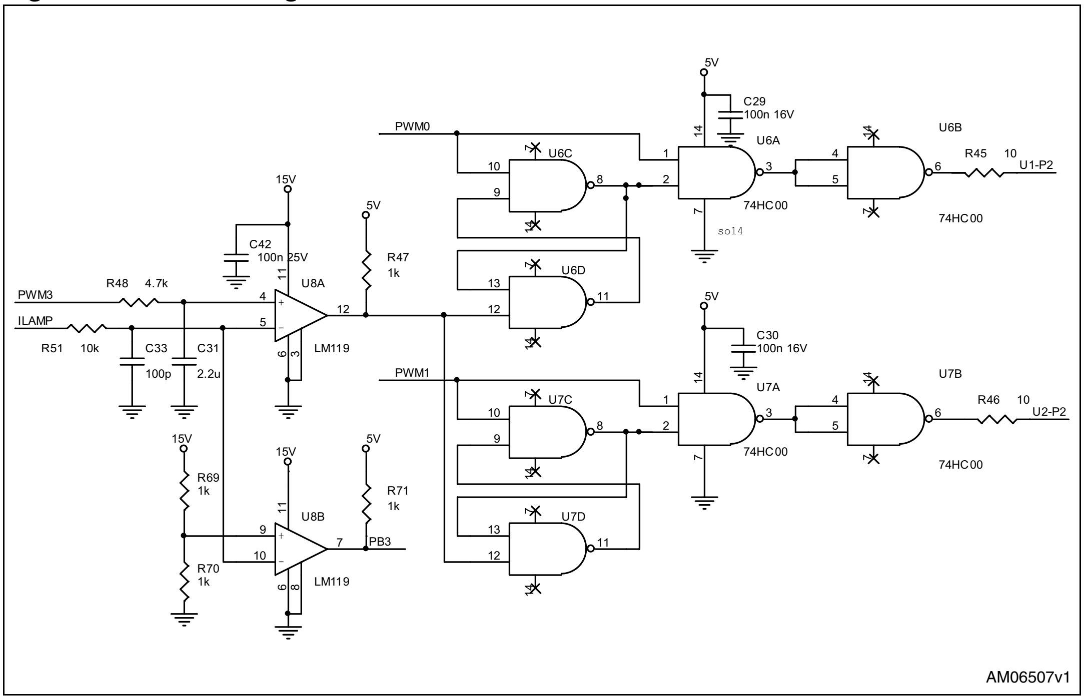
- Pin 15-16: PA3-PA2 output PWM1 and PWM0. These signals are connected to two flip-flops realized using U6 and U7 STMicroelectronics Nand logics 74AC00.

  (See *Figure 16*)

The set signal is obtained by PWM rising edge, directly from micro PWM1 and PWM0. This signal is generated at 40 kHz fixed frequency.

The reset signal is obtained by the output comparator U8A. In this way it is possible to generate a PWM signal for drivers with fixed frequency and controlled duty cycle. Since the system works in continuous conduction mode, to avoid instability in the current control circuit, the maximum duty cycle is limited to 50%.

Figure 16. Current regulation circuit



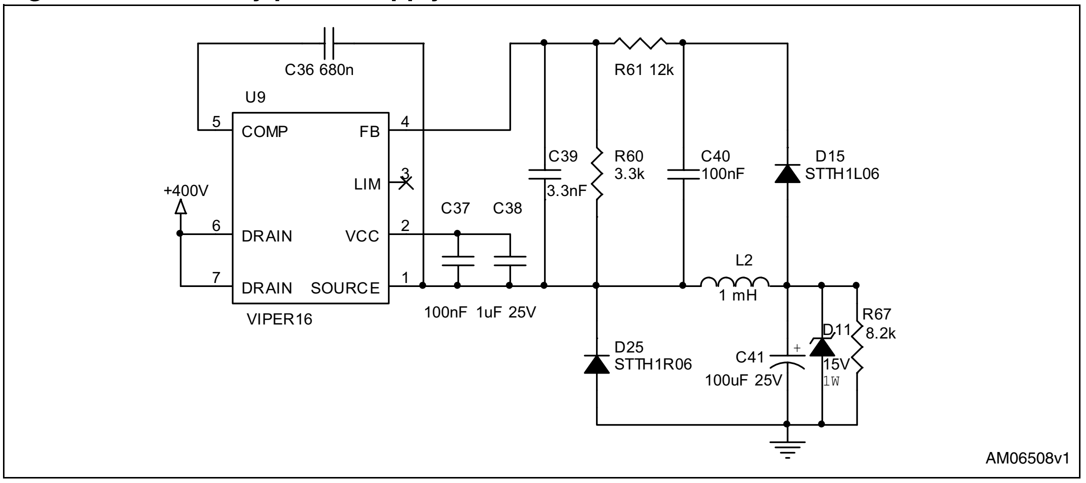
- Pin 17-18: PA1-PA0 push-pull outputs, They generate the signals for the low side driver and are connected to the L6385 Low_Side_Input pins by means of simple resistors
- Pin 19-20: OSC2-OSC1 external quartz input - not used.

6 Auxiliary power supply

The proposed power supply can be successfully applied in applications requiring 15 V for the power switch gate driver. This circuit assures good performance in terms of size and performance at very low cost.

It is based on the VIPer16 in non-isolated buck configuration. The schematic is shown in *Figure 17* below.

Figure 17. Auxiliary power supply



7 Lamp data

The lamp data are reported below. Each lamp data is valid for the corresponding operating phase.

Ignition phase

The ignition voltage, in the case of a cold lamp, is about 3-5 kV and increases with increasing lamp temperature. It can reach 25 kV in the case of a hot re-strike.

The circuit is not designed to supply this high-voltage pulse.

Warm-up phase

During this phase a high warm-up current must be supplied (about 30% higher than nominal current) to prevent the lamp extinguishing. The lamp voltage increases gradually starting from a quarter of nominal lamp voltage up to the nominal value. For 150 W metal halide lamps a current of 2 Arms was applied.

Burn phase

The lamp is designed to be driven with a low frequency square wave AC current to avoid acoustic resonance of the electric arc.

To avoid the risk of acoustic resonance, in this application the commutating frequency of the full bridge has been chosen at 160 Hz. This frequency was chosen in order to avoid a flickering effect.

The nominal lamp voltage is approximately 95 V and the nominal lamp power is 150 W.

The differential resistance of the lamp is small and negative. To obtain a stable operating point, impedance in series with the lamp is needed.

8 Experimental results

These results have been obtained for the input section and output stage.

For the PFC stage the power factor and the THD have been measured in the whole input voltage range.

Moreover, thermal measurements have been conduced.

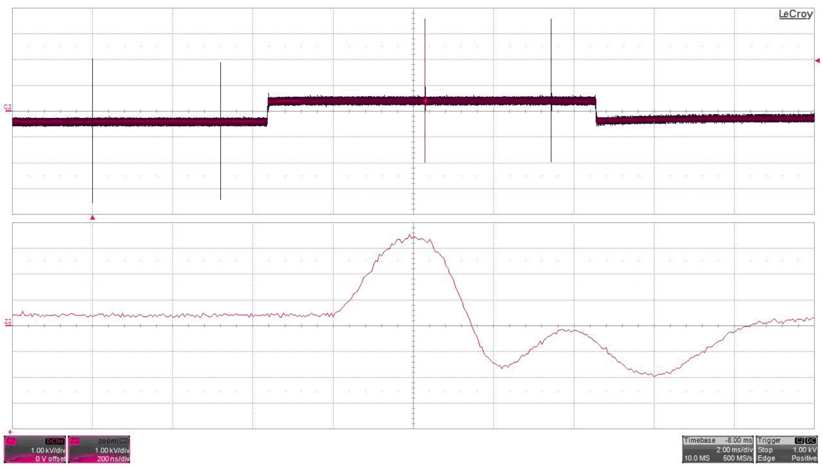
In the full bridge section the following phases have been analyzed:

- Ignition
- Warm-up
- Steady-state

8.1 Lamp ignition phase

The high-voltage transformer generates a proper ignition voltage to ignite the lamp. The voltage across the lamp is shown below. As can be seen, the peak voltage is higher than 3.5 kV having a frequency of 300 Hz.

Figure 18. Lamp ignition voltage



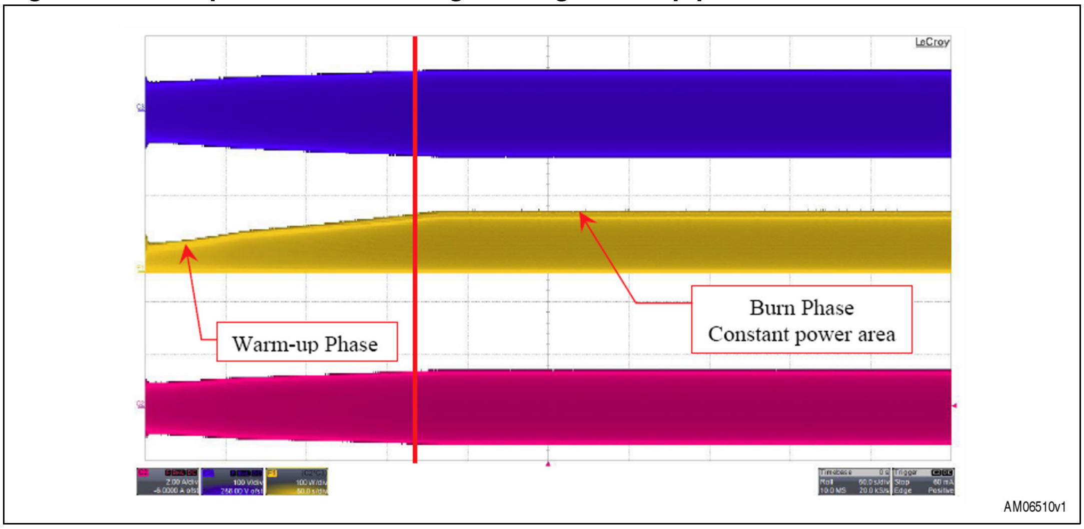
C2 = ignition voltage (1 kV/div).

8.2 Warm-up phase

During this phase the lamp current is limited, the lamp voltage increases and the lamp power also increases until the nominal lamp power. After that, the microcontroller maintains constant the power.

In *Figure 19* the whole warm-up phase is shown. As can be seen, the duration of this phase is about 3 minutes.

Figure 19. Lamp current and voltage during warm-up phase

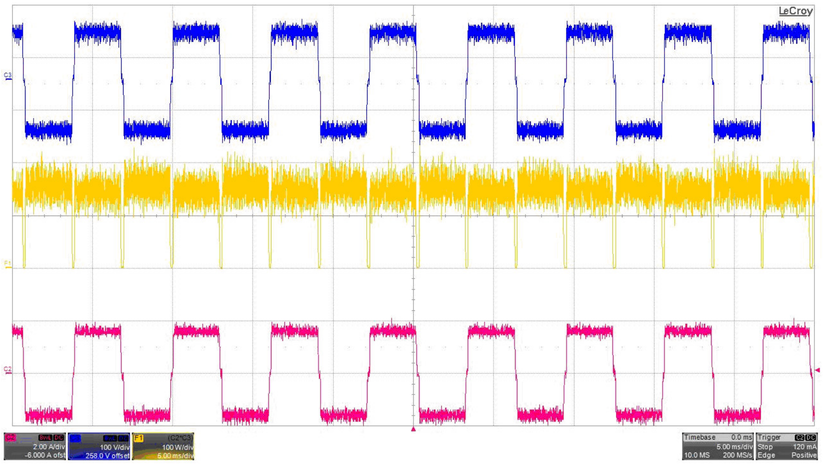


- C2 = lamp current (red waveform)
- C3 = lamp voltage (blue waveform)
- F1 = lamp power (yellow waveform)

8.3 Burn phase

During this phase the lamp is supplied with low frequency square wave current and the lamp power is maintained constant. In *Figure 20* some waveforms are shown.

Figure 20. Steady-state phase: lamp current, voltage, and lamp power



- C2 = lamp current (red waveform)
- C3 = lamp voltage (blue waveform)
- F1 = lamp power (yellow waveform)

8.4 PFC section measurements

In burn phase, the power factor, and the input current THD have been measured. Results are given below.

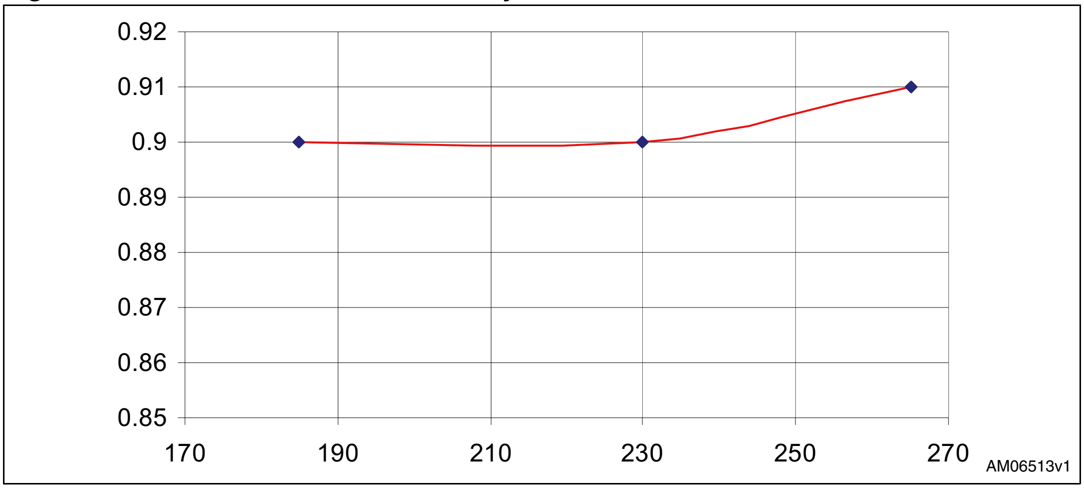
Table 2. STEVAL-ILH005V1: power factor and THD

Vinput	PF	THD %
185	0.999	2.7
230	0.997	2.8
265	0.997	3

8.5 Ballast efficiency

Figure 21 shows a diagram of total ballast efficiency versus input voltage. The system efficiency is obtained as the ratio of lamp power and input power.

Figure 21. STEVAL-ILH005V1 efficiency



8.6 Thermal measurements

These measurements were performed at ambient temperature of 25 °C and at minimum input voltage (185 V, worst case for PFC section).

Thermal measurements on the power device have been performed on the board using an infrared thermo-camera.

For the PFC section the temperature was measured on the power MOSFET and on the diode.

On the power MOSFET, mounting a heatsink with a thermal resistance of R_{th} = 11.40 °C/W, the temperature on the top of the package was 55 °C. On the top of the boost diode the temperature was 70 °C.

In the output stage on the bridge devices a heatsink, with a thermal resistance of R_{th} = 6.23 °C/W, was mounted. The temperature on these switches was 60 °C.

8.7 Conducted emission pre-compliant tests

Tests have been performed in order to evaluate the electromagnetic compatibility and disturbance of the STEVAL-ILH005V2. The measurements have been performed in neutral and line wires, using a peak detector and considering average and quasi-peak limits based on EN 55015 standards. The tests have been performed at 230 V_{AC} input voltage. Results show that emission levels are below the limits.

Figure 22. Peak measurement: line wire

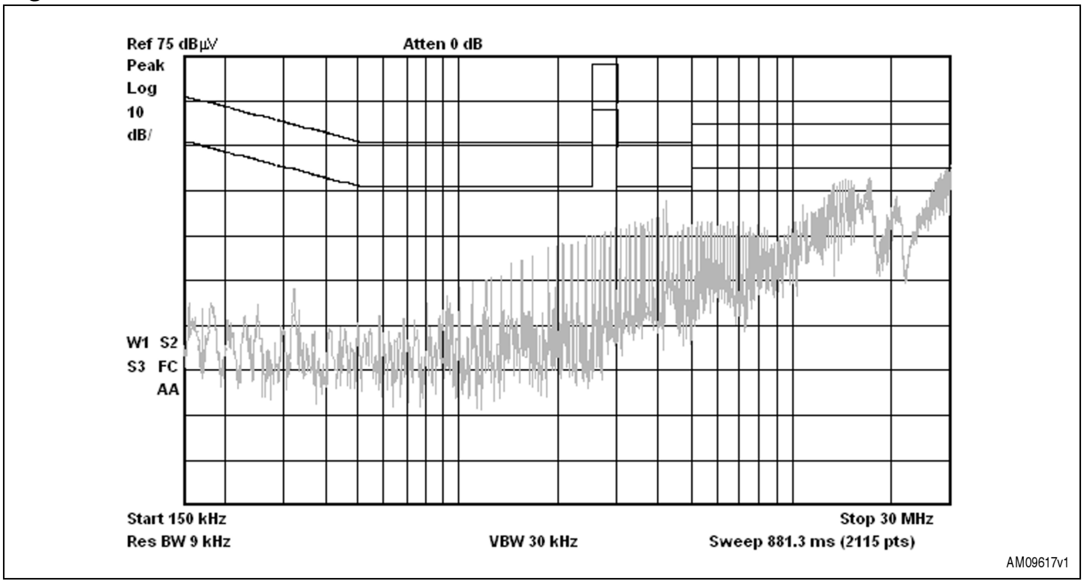
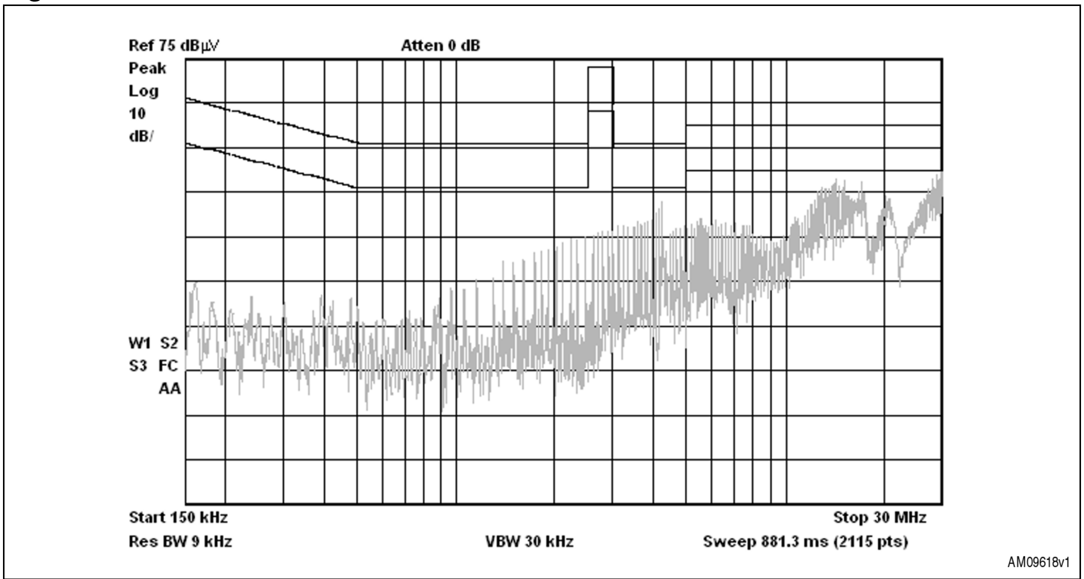


Figure 23. Peak measurement: neutral wire



9 References

1. AN2747 application note
2. AN2761 application note

10 Revision history

Table 3. Document revision history

Date	Revision	Changes
06-Apr-2011	1	Initial release.

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