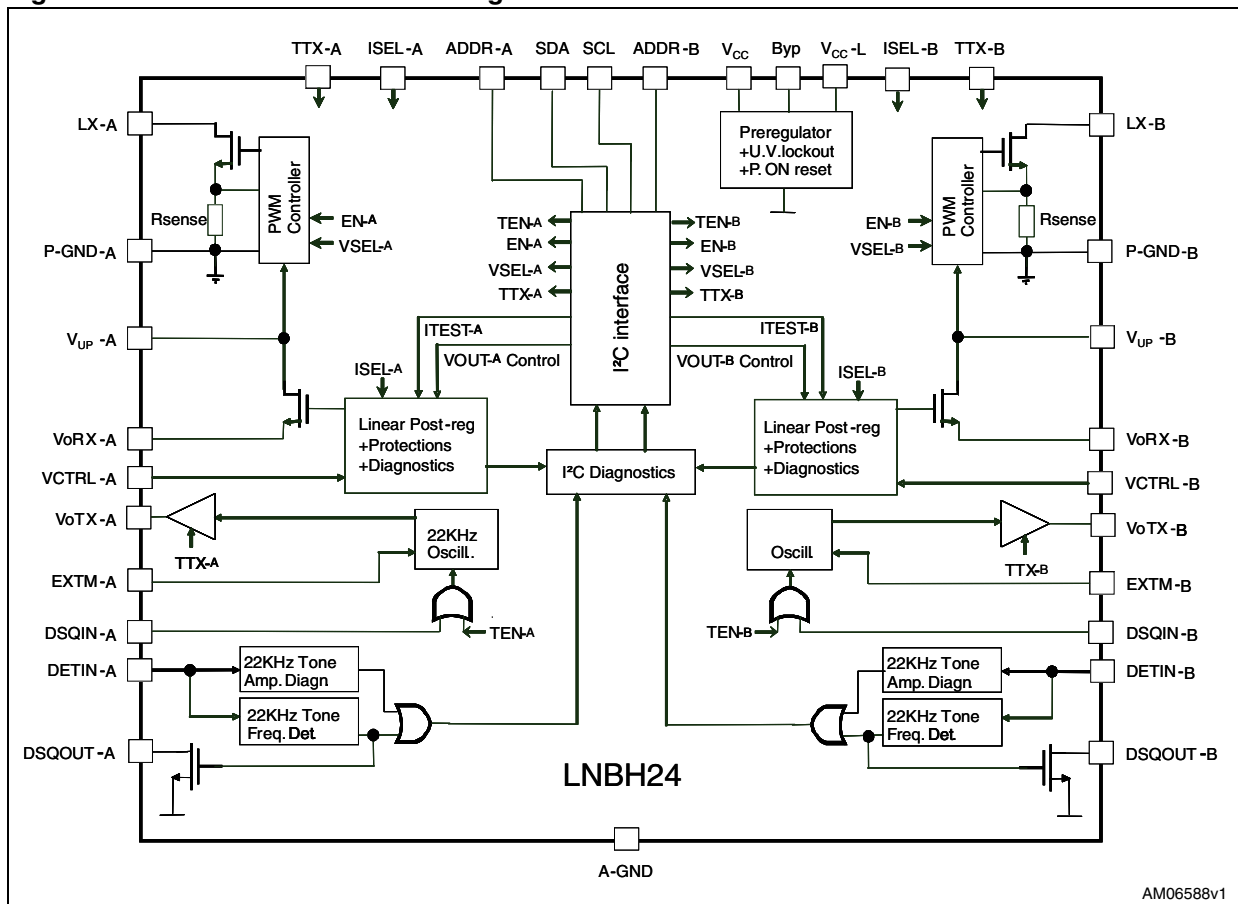## LNBH24: dual supply and control IC with step-up and I^{2}C interface

Introduction

This application note is intended to provide additional information and suggestions for the correct use of the LNBH24 device. All waveforms shown are based on the STEVAL-CBL004V1 and STEVAL-CBL006V1 demonstration boards described in *Section 5*.

The LNBH24 is an integrated solution for supplying/interfacing two independent LNB down-converters in the antenna dishes. It gives good performance in a simple and cheap way, minimum external components are required. It comprises all the functions that allow the realization of a dual tuner STB with supplying/interfacing functions in accordance with international standards. Moreover, it includes an I^{2}C bus interface and, thanks to a fully integrated step-up DC-DC converter, it works with a single input voltage supply for a reasonable range.

Figure 1.   LNBH24 internal block diagram

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Contents

List of figures

1 Block diagram description

Below is a description of the LNBH24 internal blocks that includes two completely independent sections. Except for the Vcc and I^{2}C inputs, each circuit can be separately controlled and have their own independent external components. All the specifications below must be considered equal for both sections (A/B).

1.1 Step-up controller

The LNBH24 has a built-in step-up DC-DC converter that, from a single supply source ranging from 8 V to 15 V, generates the voltages that let the linear post-regulator work at a minimum power dissipation. The DC-DC converter external components are connected to the Lx and Vup pins (see *Figure 5*). No external Power MOSFET is needed.

1.2 Pre-regulator block

This block includes a voltage reference connected to the BYP pin, an undervoltage lockout circuit, intended to disable the whole circuit when the supplied Vcc drops below a fixed threshold (6.7 V typ.), and a power-on reset that sets all the I^{2}C registers to zero when the Vcc is turned on and rises from zero above the ON threshold (7.3 V typ.).

1.3 I^{2}C interface and diagnostic

The main functions of the device are controlled via the I^{2}C bus by writing 8 bits on the system register (SR bits in write mode). On the same register, there are 5 bits that can be read back (SR bits in read mode) and which provide 5 diagnostic functions.

Five bits report the diagnostic status of five internal monitoring functions:

● VMON: output voltage diagnostic. If the output voltage level is below the guaranteed limits (refer to the datasheet) the VMON I^{2}C bit is set to "1"

● TMON: 22 kHz tone diagnostic. If the 22 kHz tone amplitude and/or the tone frequency is out of the guaranteed limits (refer to the datasheet.), the TMON I^{2}C bit is set to "1"

● IMON: minimum output current diagnostic to detect if no LNBs are connected on the bus or cable not connected to the IRD, the LNBH24 is provided with a minimum output current flag by the IMON I^{2}C bit in Read mode, which is set to "1" if the output current is lower than 12 mA, typically, with ITEST=1 and 6 mA with ITEST=0

● OTF: overtemperature flag. If an overheating occurs (junction temperature exceeds 150 °C), the OTF I^{2}C bit is set to "1"

● OLF: overload flag. If the output current required exceeds the current limit threshold or a short-circuit occurs, the OLF I^{2}C bit is set to "1".

Moreover, three bits report the last output voltage register status (EN, Vsel, LLC) received by the IC. Each section (A/B) has two selectable I^{2}C addresses, respectively, by the ADDR-A and ADDR-B pins (see *Table 1*).

1.4 22 kHz oscillator

The internal 22 kHz tone generator is factory trimmed in accordance to the standards, and can be controlled by the DSQIN pin (TTL compatible) that allows immediate DiSEqC™ data encoding tone frequency. The rising and falling edges are controlled to be in the 5 µs to 15 µs range, 8µs typ. for 22 kHz. The duty cycle is 50% typ., it modulates the DC output with a 0.650 Vpp (typ.) amplitude as well as the DSQIN pin.

The EXTM is a logic input to allow the activation of the 22 kHz tone output, on the VoTX pin, by using the IC integrated tone generator. If the EXTM pin is used, the internal 22 kHz generator must be kept ON (TTX pin or TTX bit set HIGH). When a TTL compatible 22 kHz signal is applied (for example, a 22 kHz square wave from the demodulator), the EXTM internal circuit detects the 22 kHz TTL signal code and activates the internal 22 kHz tone on the VoTX output. The 22 kHz tone on the output is activated after some delay from the TTL signal presence on the EXTM pin. Tone output starts with about 1.5T delay after the 1st cycle of the TTL signal and stops after about 2T delay after the TTL signal on the EXTM has expired (see the diagram below). Tone output can also be activated by the DSQIN pin. Starting with 1.5T ±25 µs maximum delay and stopping after 2T ±25 µs maximum delay with 20~24 kHz tolerance for the EXTM input pin.

**Figure 2.   EXTM timing control**
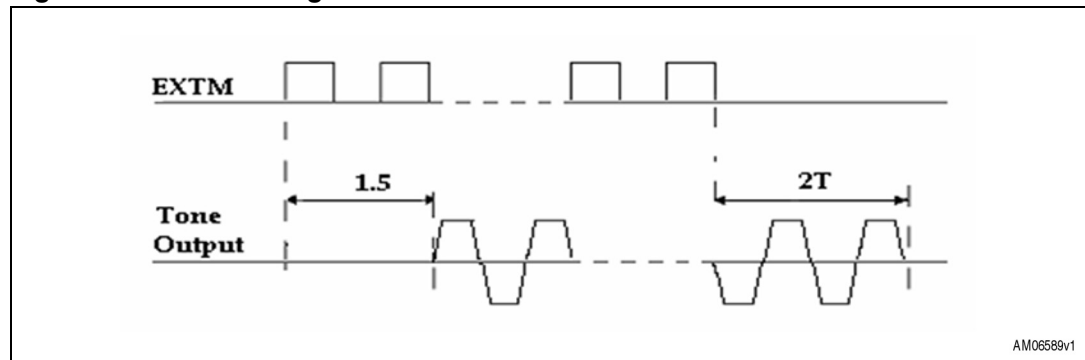
1.5 Tone detector

This block provides a complete circuit to decode the 22 kHz burst code present on the DETIN pin in a digital signal by the DSQOUT pin where an open drain MOSFET is connected. Tone is also monitored and a dedicated bit (TMON) provides the diagnostic function described in *Section 1.3*.

1.6 DiSEqC communication

The following steps must be taken to ensure the correct implementation of the DiSEqC 2.0 communication:

Figure 3. DiSEqC timing control

AM06590v1
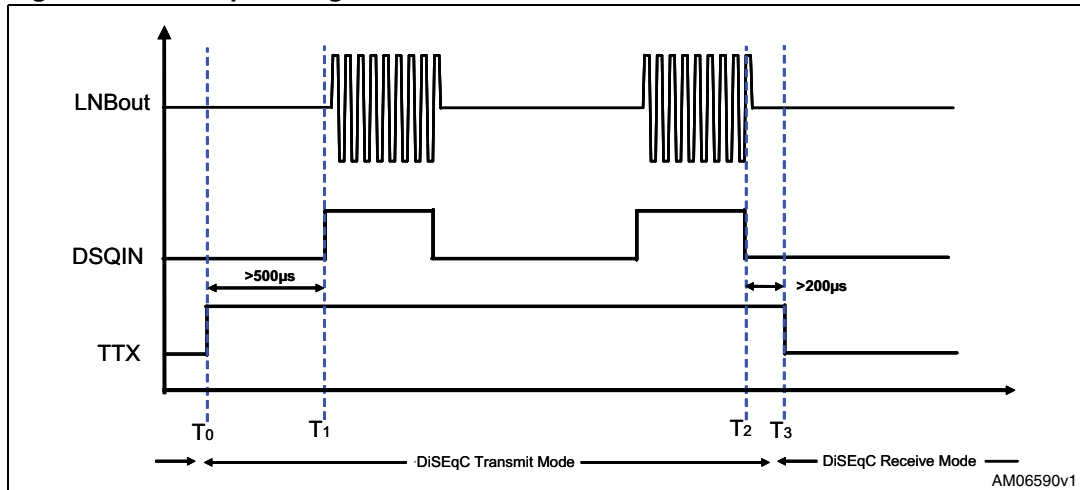
- T0: before starting the DiSEqC transmission, the TTX function is to be activated (through the TTX pin or TTX I^2C bit)

- T1: after 500 µsec (min.), the IC is ready to receive the DiSEqC code through the DSQIN pin (or, alternatively, the TEN I^2C bit) can be set HIGH to activate the 22 kHz burst

- T2: when the transmission has elapsed, the TTX function is to be set LOW (through the TTX pin or TTX I^2C bit) not earlier than 200 µsec after the last falling edge of the DiSEqC code.

1.7 Linear post-regulator, modulator and protection

The output voltage selection and the current selection commands join this block that manages all the LNB output functions. This block gives feedback to the I^2C interface, through the diagnostic block, regarding the status of the thermal protection, overcurrent protection, and OUTPUT settings.

2 Pin description

The LNBH24 package is the PWSSO-36 ePad for SMD assembly. *Figure 4* shows the device pinout and *Table 1* briefly summarizes the device pin functionality.

Figure 4. LNBH24 pin configuration
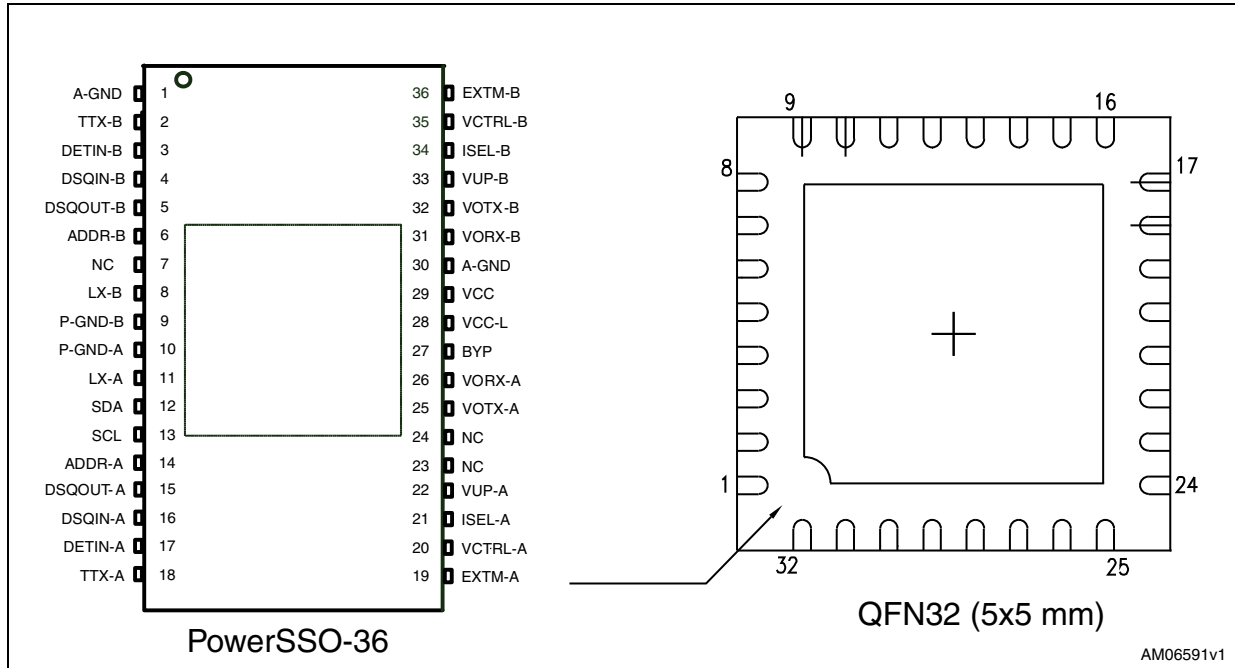
Table 1.   BOM

| Reference	Value / generic part number	Package	Manufacturer	Manufacturer's ordering code / orderable part number	Supplier	Supplier's ordering code
R1	100 Ω	1206				
Rsel A, Rsel B	11 kΩ	1206				
R3A, R3B	10 kΩ	1206				
R4A, R4B	15 Ω	1206				
C12A, C12B	10 nF	1206				
C2, C7	0.1 µF	1206				
C8, C10A, C10B, C11	0.22 µF	1206				
C4A, C4B, C6A, C6B	0.47 µF	1206				
C9A, C9B	10 µf 35 V	El.Al. radial				
C1, C3A, C3B, C5A, C5B	100 µF 35 V ESR=150 mΩ÷350 mΩ	El.Al. radial				
L1A, L1B	22 µH	Radial	Panasonic	ELC08D220E	RS-component	233-5140
L3A, L3B	220 µH	Radial	Panasonic	ELC08D221E	RS-component	233-5235
L2A, L2B	Ferrite bead	AXIAL-0.4	Panasonic	EXCEL A35	RS-component	226-8185
D1A, D2B	STPS2L30A	SMB	STMicroelectronics			
D2A, D2B, D4A, DAB	BAT-43	DO-35	STMicroelectronics			
D3A, D3B	1N5819	DIODE-0.4	STMicroelectronics			
TVSA, TVSB	LNBTVS4-220	SMB	STMicroelectronics			
LNBH24	LNBH24	PowerSSO-36, QFN-32	STMicroelectronics			
CN1	Strip 2p M	HDR1X2				

Table 1.   BOM (continued)

Reference	Value / generic part number	Package	Manufacturer	Manufacturer's ordering code / orderable part number	Supplier	Supplier's ordering code
CN3, CN4	Strip 8p M	HDR1X8				
CN2	Strip 4p M	HDR1X4				

3 Component selection guidelines

The LNBH24 application schematic shows the typical configuration for a dual LNB power supply.

Figure 5. LNBH24 demonstration board schematic
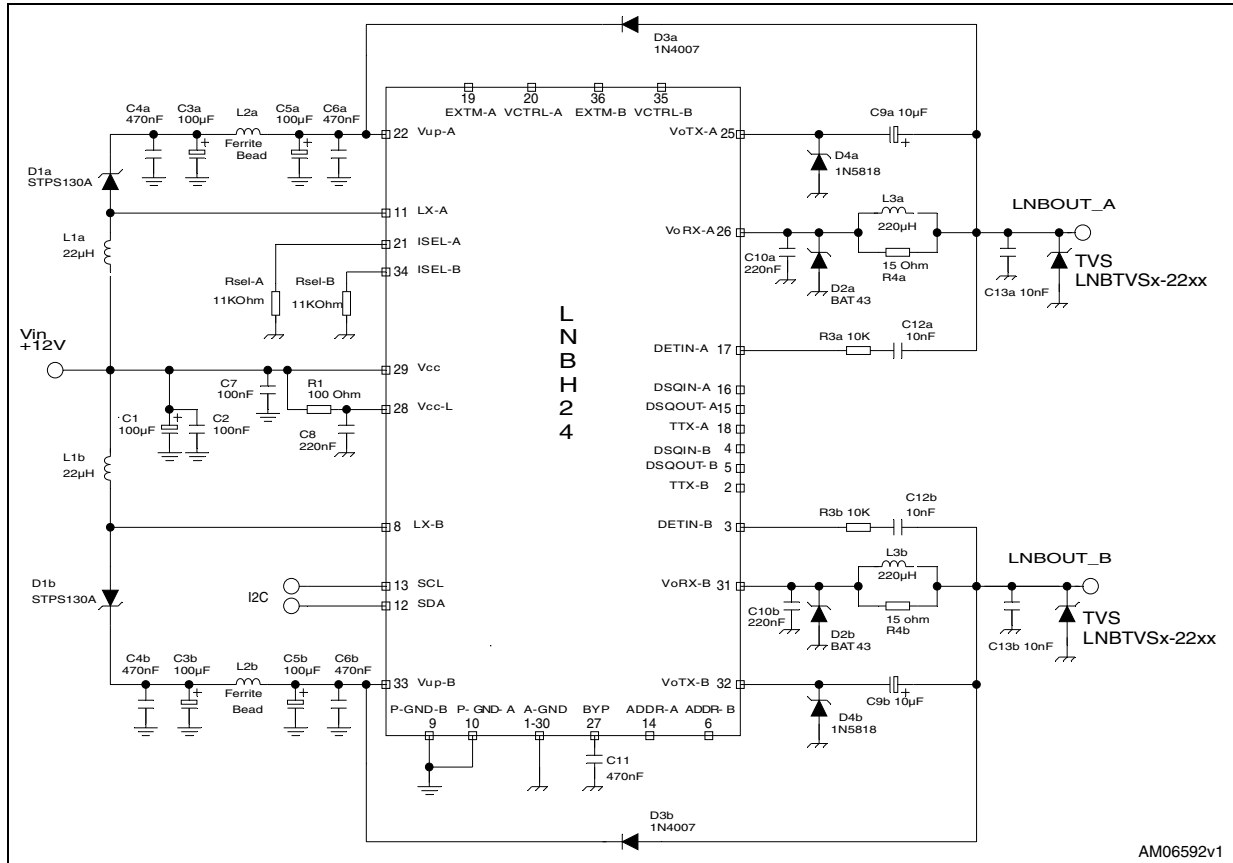
Note: *The TVS diode is to be used if surge protection is required (see Section 3.4).*

For pin configuration of the QFN32 package see Figure 4.

3.1 Inductor

The LNBH24 operates with a standard 22 µH inductor for the entire range of supply voltages and load current. The inductor saturation current rating (where inductance is approximately 70% of zero current inductance) must be greater than the switch peak current (Ipeak) calculated at:

● Maximum load ($IOUT_{max}$)
● Minimum input voltage (VIN_{min})
● Maximum DC-DC output voltage ($VUP_{max} = VOUT_{max} + 0.75$ V).

In this condition the switch peak current is given by the following formula:

Equation 1

$$Ipeak = \frac{VUP_{max} \cdot IOUT_{max}}{Eff \cdot VIN_{min}} + \frac{VIN_{min}}{2LF}\left(1 - \frac{VIN_{min}}{VUP_{max}}\right)$$

where:

- Eff. is the efficiency of the DC-DC converter (93% typ. at highest load)
- L is the inductance (22 µH typ.)
- F is the PWM frequency (220 kHz typ.).

Example:

- Application conditions
- $VOUT_{max}$= 19.2 V (supposing EN=Vsel=1, LLC=0)
- VIN_{min}= 11 V
- VUP_{max}=$VOUT_{max}$+Vdrop= 19.2 V+0.75 V= 19.95 V
- $IOUT_{max}$= 500 mA
- Eff=90%.

By using *Equation 1*, Ipeak is:

Equation 2

$$Ipeak = \frac{19.95 * 0.5}{0.9 * 11} + \frac{11}{2 * 22 * 10^{-6} * 220 * 10^{3}}\left(1 - \frac{11}{19.95}\right) = 1.52A$$

Table 2.   **Recommended inductors**

Vendor	Part number	Isat(A)	DRC (mΩ)	Mounting type
Sumida	CD104-220MC	1.6	67	S.M.D
	RHC110-220M	2.4	88	T.H.
Toko	822LY-220K	1.3	70	T.H.
	824LY-220K	1.72	76	T.H.
	A671HN-220L	2.44	21	T.H.
	A814LY-220M	2.0	75	SMD
Panasonic	ELC08D220E	1.8	51	T.H.
	ELC10D220E	3.2	40	T.H.
Coilcraft	DC1012-223	2.5	46	T.H.
	PVC-0-223-03	3	35	T.H.
	DO3316P-223	2.6	85	SMD

Several inductors that work well with the LNBH24 are listed in *Table 2*, although there are many other manufacturers and devices that can be used. Consult each manufacturer for more detailed information and for their entire selection of related parts, as many different shapes and sizes are available. Ferrite core inductors should be used to obtain the best efficiency. Choose an inductor that can handle at least the Ipeak current without saturating, and ensure that the inductor has a low DCR (copper wire resistance) to minimize power losses and, consequently, to maximize the total efficiency.

Table 3.   Recommended inductors for output R-L filter

Vendor	Part number	Isat(A)	DRC(mΩ)	Mounting type
Sumida	CD104-221MC	1.6	67	S.M.D
	RHC110-221M	2.4	88	T.H.
Toko	822LY-221K	1.3	70	T.H.
	824LY-221K	1.72	76	T.H.
	A671HN-221L	2.44	21	T.H.
	A814LY-221M	2.0	75	SMD
Panasonic	ELC08D221E	1.8	51	T.H.
	ELC10D221E	3.2	40	T.H.
Coilcraft	DC1012-223	2.5	46	T.H.
	PVC-0-223-03	3	35	T.H.
	DO3316P-223	2.6	85	SMD

3.2   Output current limit selection

The linear regulator current limit threshold can be set by an external resistor connected to the ISEL pin. The resistor value defines the output current limit by the equation:

Equation 3

$$Imax(A) = \frac{10000}{Rsel}$$

where Rsel is the resistor connected between ISEL and GND. The highest selectable current limit threshold is 1.0 A typ. with Rsel=10 kΩ The above equation defines the typical threshold value for each output. However, it is advisable to not exceed, for a long period, a total amount of current of 1 A from both sections (Iout_A+Iout_B<1A) in order to avoid the overtemperature protection triggering.

3.3   Schottky diode

In typical application conditions it is recommended to use a 1 A Schottky diode suitable for the LNBH24 DC-DC converter. Take into consideration that the DC-DC converter Schottky diode must be selected depending on the application conditions (V$_{RRM}$ >25 V). We suggest an N-channel Schottky diode such as the STPS130A. In worst-case conditions, low input voltage and higher output current, select the Schottky diode which is able to support the Ipeak whose value is calculated according to *Equation 1*.

Note: *The average current flowing through the Schottky diode is lower than Ipeak and can be calculated by Equation 4.*

Equation 4

$$Id = Iout \times \frac{VOUT}{VIN}$$

Table 4.   Recommended Schottky diode

Vendor	Part number	I_F(av)	V_F(max.)
STMicroelectronics	1N5818	1 A	0.50 V
	1N5819	1 A	0.55 V
	STPS130A	1 A	0.46 V
	STPS1L30A	1 A	0.30 V
	STPS2L30A	2 A	0.45 V
	1N5822	3 A	0.52 V
	STPS340	3 A	0.63 V
	STPS3L40A	3 A	0.5 V

3.4   TVS diode

The LNBH24 device is directly connected to the antenna cable in a set-top box. Atmospheric phenomenon can cause high voltage discharges on the antenna cable causing damage to the attached devices. Surge pulses occur due to direct or indirect lightning strikes to an external (outdoor) circuit. This leads to currents or electromagnetic fields causing high voltage or current transients. LNBH24 devices are not able to "survive" such a high energy discharge. Transient voltage suppressor (TVS) devices are used to protect the LNBH24 and the other devices electrically connected to the antenna cable.

The LNBTVS, developed by STMicroelectronics is a dedicated lightning and electrical overstress surge protection for LNB voltage regulators. This protection is designed to comply with the stringent IEC61000-4-5 standard with surges up to 500 A with a whole range of products for cost/performance optimization.

The correct choice of the TVS diode must be made according to the maximum peak power dissipation that the diode supports.

Table 5.   Recommended LNBTVS

Vendor	Part number	VBR_{TYP}(V)	Ppp (W) 10/100 µs
STMicroelectronics	LNBTVS4-220	23.1	1800
	LNBTVS4-221	23.1	2000
	LNBTVS4-222S	23.1	2000
	LNBTVS6-221S	21.3	3000

Select the TVS diode which is able to support the Ppp(W) whose value is indicated in *Table 5*.

4 Output capacitors

Two electrolytic low cost capacitors are needed on the DC-DC converter output stage (C3 and C5 in *Figure 1*). Moreover, two ceramic capacitors are recommended in order to reduce the high frequency switching noise. The switching noise is due to the voltage spikes of the fast switching action of the output switch, and to the parasitic inductance of the output capacitors. To minimize these voltage spikes, special low inductance ceramic capacitors can be used, and their lead lengths must be kept short and as close as possible to the IC pins (C4 and C6 in *Figure 1*). In order to further reduce the switching noise, a ferrite bead is suggested between C3 and C5 (see *Section 4.1*).

The most important parameter for the output capacitors is the effective series resistance (ESR). The DC-DC converter control loop circuit has been designed to properly work with low cost electrolytic capacitors which have ESR in the range of 200 mΩ A 100 µF output filter capacitor with ESR between 150 mΩ and 350 mΩ is a good choice in most application conditions. It is also possible to use electrolytic capacitors up to 220 µF with ESR between 100 mΩ and 300 mΩ The capacitor voltage rating should be at least 25 V, but if the highest voltage selection condition is used (AUX=1), 35 V or higher voltage capacitors are advised.

4.1 Ferrite bead

The most important parameter when selecting the ferrite bead is the rated current. Be sure that the ferrite has a current rating of at least 2 A and impedance higher than 60 Ω at 100 MHz.

4.2 Input capacitors

An electrolytic bypass capacitor (C1 in *Figure 1*) between 100 µF and 470 µF, located close to the LNBH24, is needed for stable operation. Moreover, a ceramic capacitor between 100 nF and 470 nF is recommended to reduce the switching noise at the input voltage pin.

5 PCB layout

Any switch-mode power supply requires a good PCB layout in order to achieve maximum performance. Component placement and GND trace routing and width, are the major issues. Basic rules commonly used for DC-DC converters for good PCB layout should be followed. All traces carrying current should be drawn on the PCB as short and as thick as possible. This should be done to minimize resistive and inductive parasitic effects, and increase system efficiency. White arrows indicate the suggested PCB (ring) ground plane to avoid spikes on the output voltage (this is related to the switching side of the LNBH24). Good soldering of the ePad also helps.

Figure 6.   PBC top layer (STEVAL-CBL004V1)
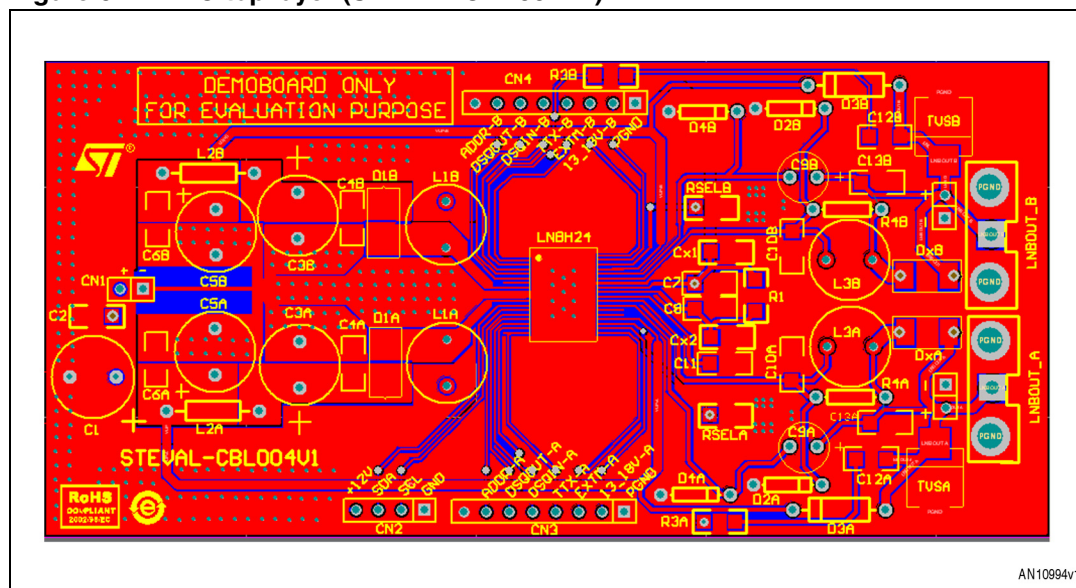
Figure 7.   PBC top layer (STEVAL-CBL006V1)
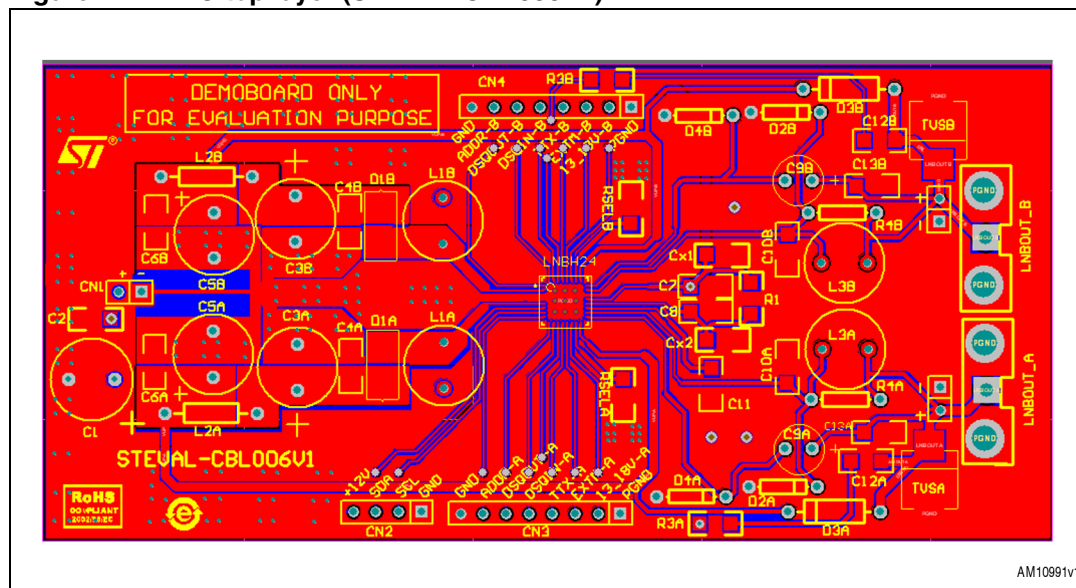
Figure 8.   PBC bottom layer (STEVAL-ICB004V1)

AM10995v1
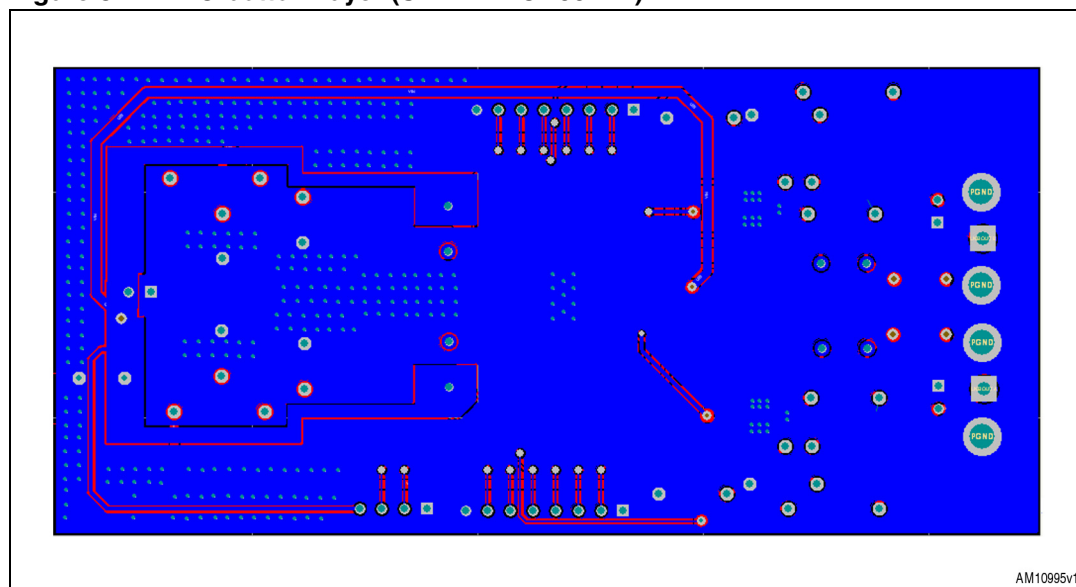
Figure 9.   PBC bottom layer (STEVAL-ICB006V1)

AM10992v1

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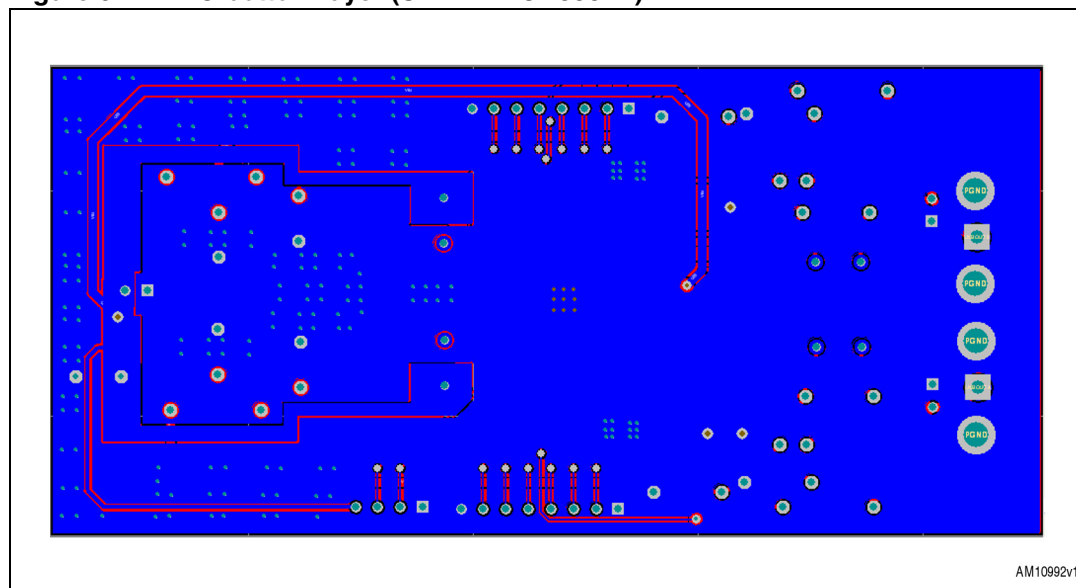
Figure 10.   PCB components layout (STEVAL-ICB004V1)
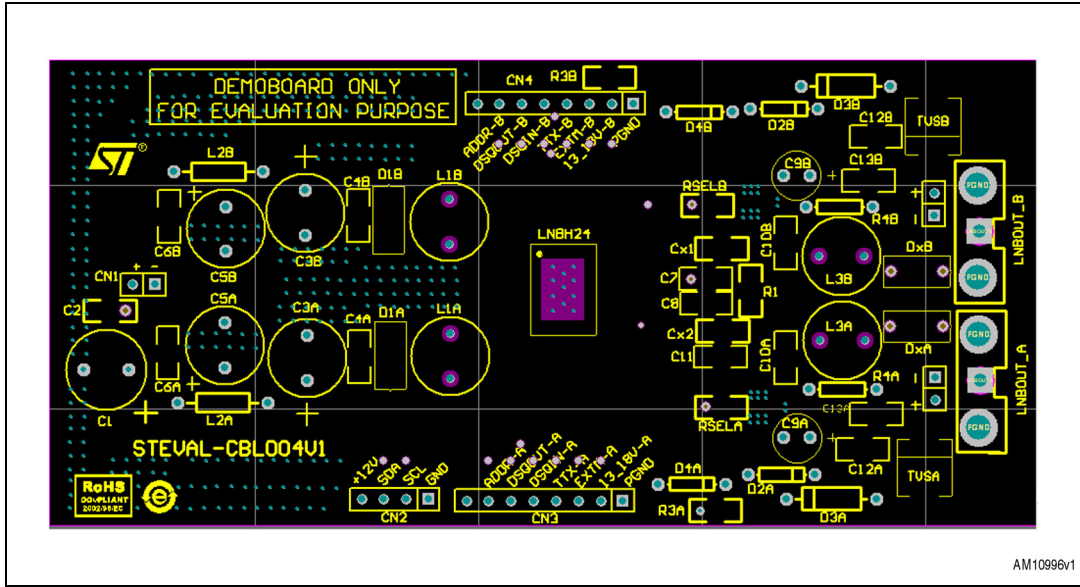
Figure 11.   PCB components layout (STEVAL-ICB006V1)
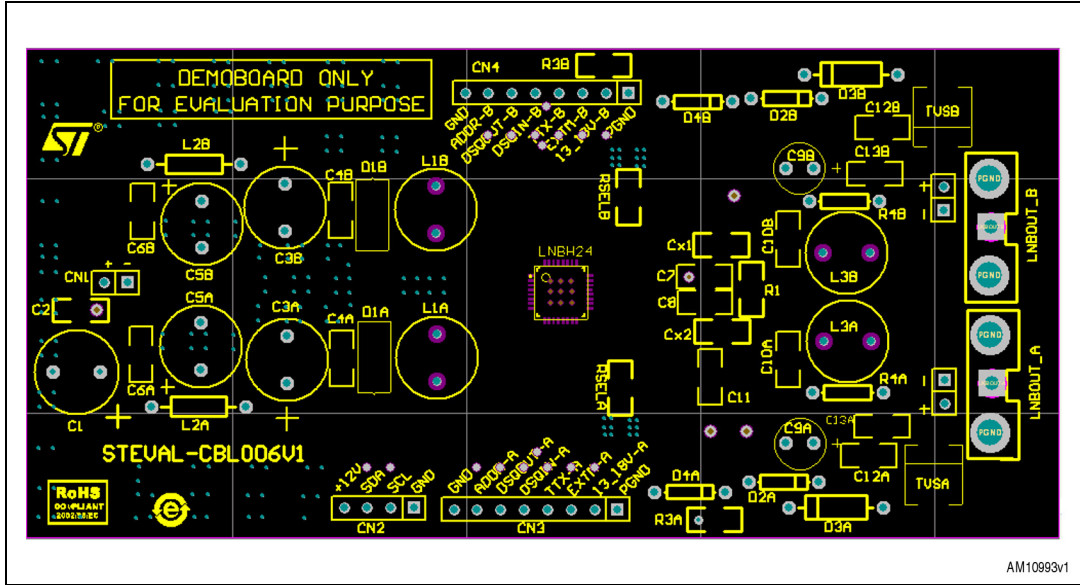
6 Startup procedure

The following is needed to test the board; a PC with parallel port (EPP printer port), I^{2}C BUS interface, software LNBxxx control suite, dual output power supply (3 A clamp current or higher) and electronic load.

● STEP 1: install the LNBXXX control suite software (see *Section 6.1* software installation)
● STEP 2: plug in the I^{2}C connector
● STEP 3: supply the demonstration board
● STEP 4: see *Section 6.2*.

Figure 12. PCB connector

To supply the demo-board .
(Typ. 12V DC). Use a power
supply with a 3A clamp

To supply LNB B.

To supply LNB A.

I^{2}C interface connections :
For data transmissions from
I2C interface to the LNBH24
and vice versa. Be careful
about the correct way of the
I^{2}C interface connector

Equal for both section

ADDR tip :To determine the
I^{2}C device address.
DSQout tip : DiSEqC output
for DiSEqC 2.0 data
decoding
DSQIN tip : DiSEqC Input
that accept the DiSEqC
code. Set to ground if not
used.
TTX tip : TTX enable. Set to
ground if not used.
EXTM tip : External
Modulation Logic input pin
which activates the 22KHz
tone output on the VoTX pin.
Set to ground if not used.
13_18V tip : Output Voltage
Control, 13_18V = 1 or
floating set VoRX=18.5V,
13_18V = 0 set VoRX=13.4V

AM06593v1

6.1 Software installation

Unzip the compressed file and start installation with the file SETUP.exe. In START -> Program -> STMicroelectronics -> LNBxxx control suite, the following screen can be seen; when the green light is ON, the hardware and software are ready to work.

Figure 13. Pc to I²C main window
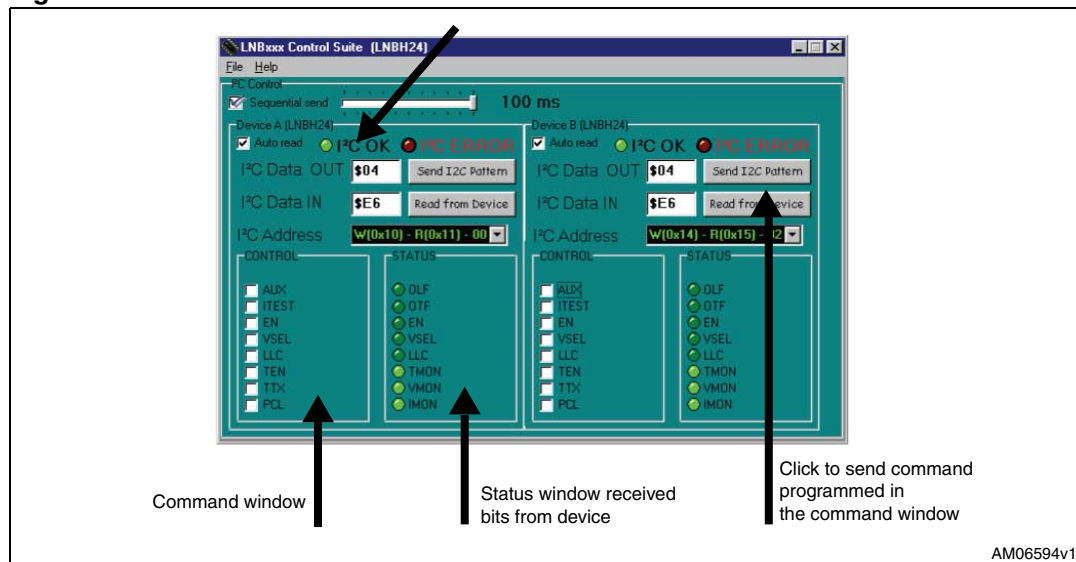
The red light indicates "I²C ERROR" and it is necessary to configure the LPT port, and to check the I²C cable (to swap SCL and SDA if needed) and the power supply.

Figure 14. I²C bus communication error
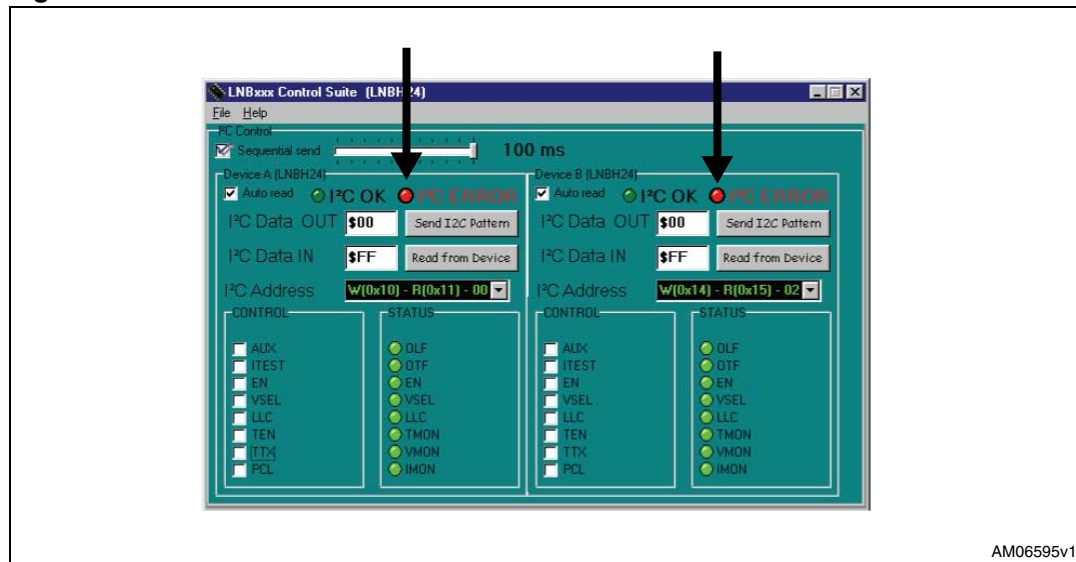
The user can choose the device, printer port address for the PC and correct settings of SCL and SDA bits to customize the I²C hardware interface.

Figure 15. Main settings window

AM06596v1

In the system settings menu, change the device to be tested.

Figure 16. Device selection window

AM06597v1

From the parallel port setting menu, set the LPT parameters.

Figure 17.   Parallel port setting
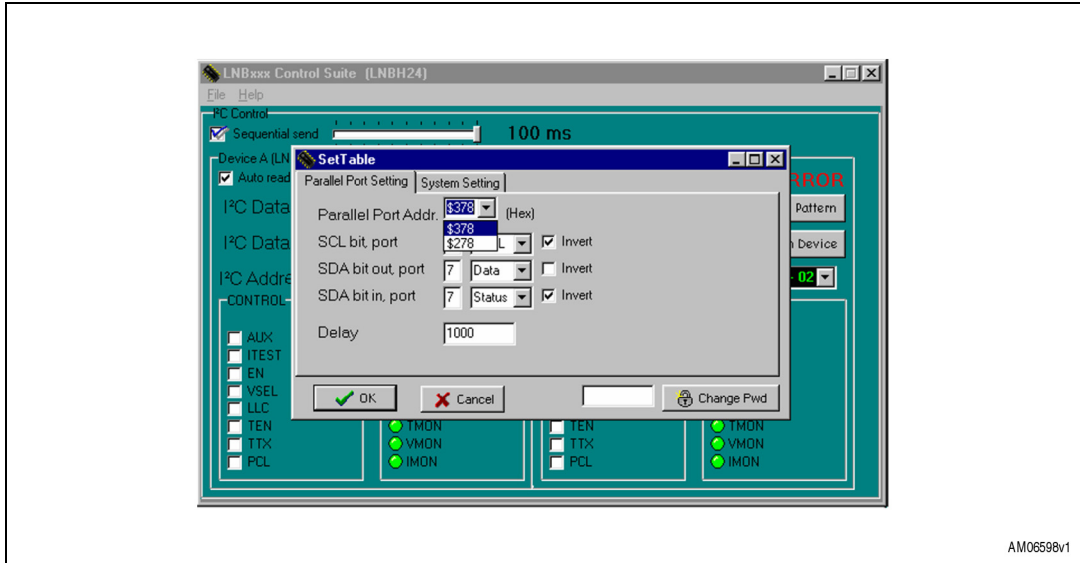
AM06598v1

Figure 18.   LPT1 setting

Setting for LPT1
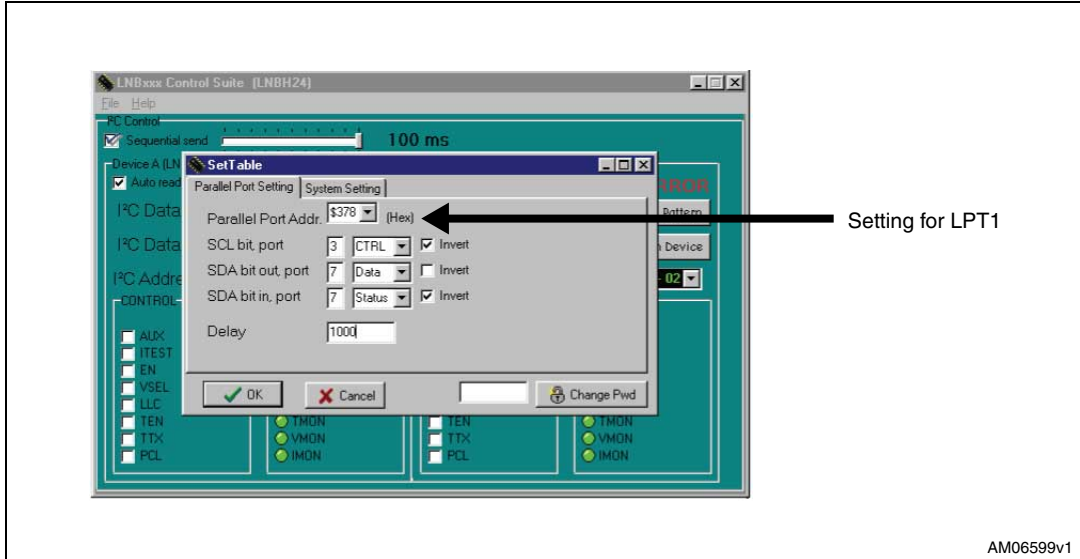
AM06599v1

Figure 19.   Password setting

"STM" is the password
(case sensitive)

AM06600v1
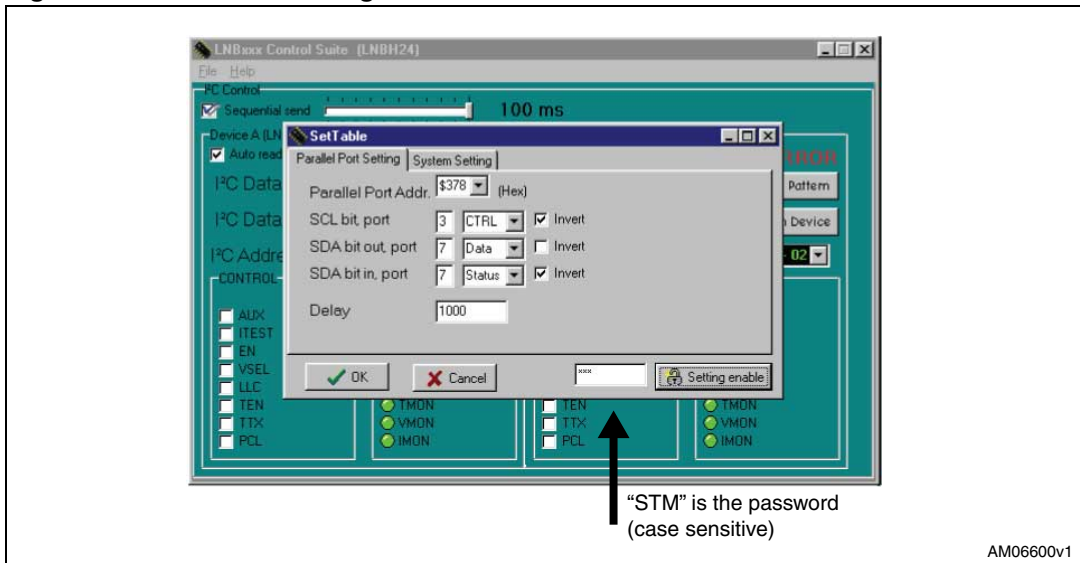
Now it is possible to choose the device address, for the LNBH24.

Figure 20.   I^{2}C device A address setting

AM06601v1
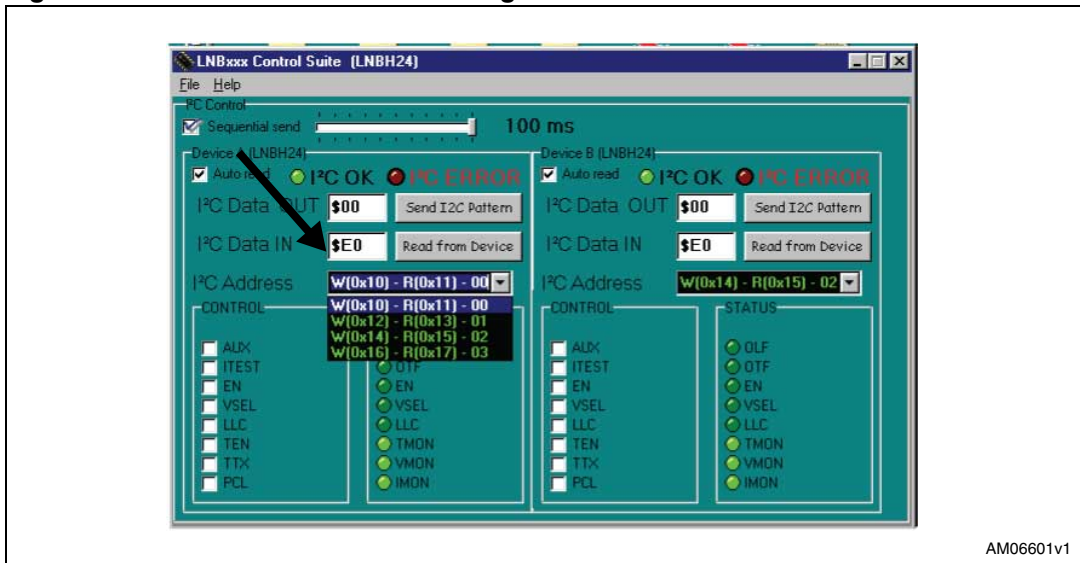
Figure 21.   I²C device B address setting

AM06602v1
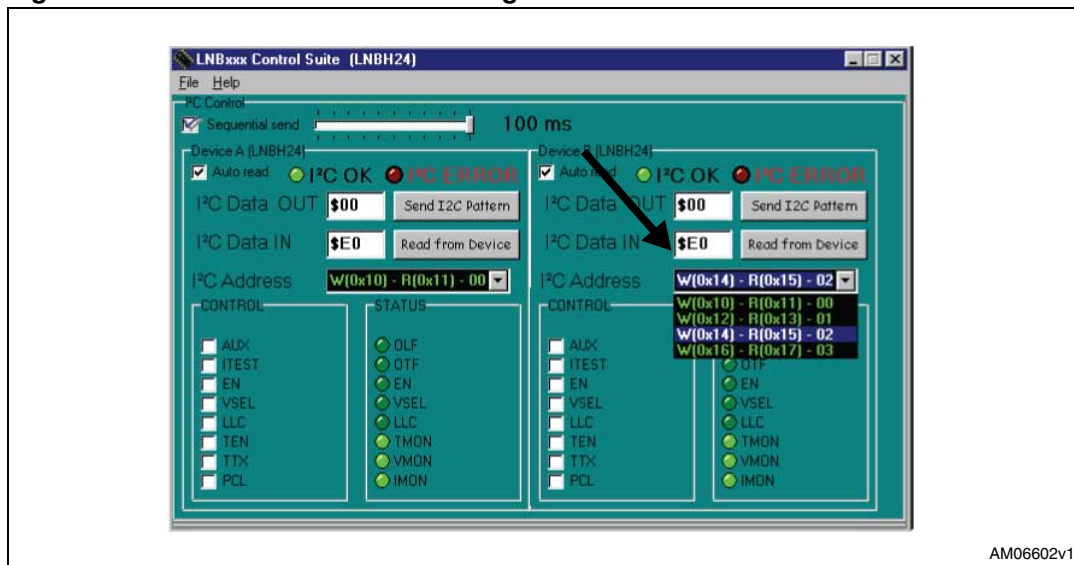
If the user wants to have, in real-time, the status of the received bits, it is necessary to tick the "Auto-read" window.

Figure 22.   Auto-read setting

AM06603v1
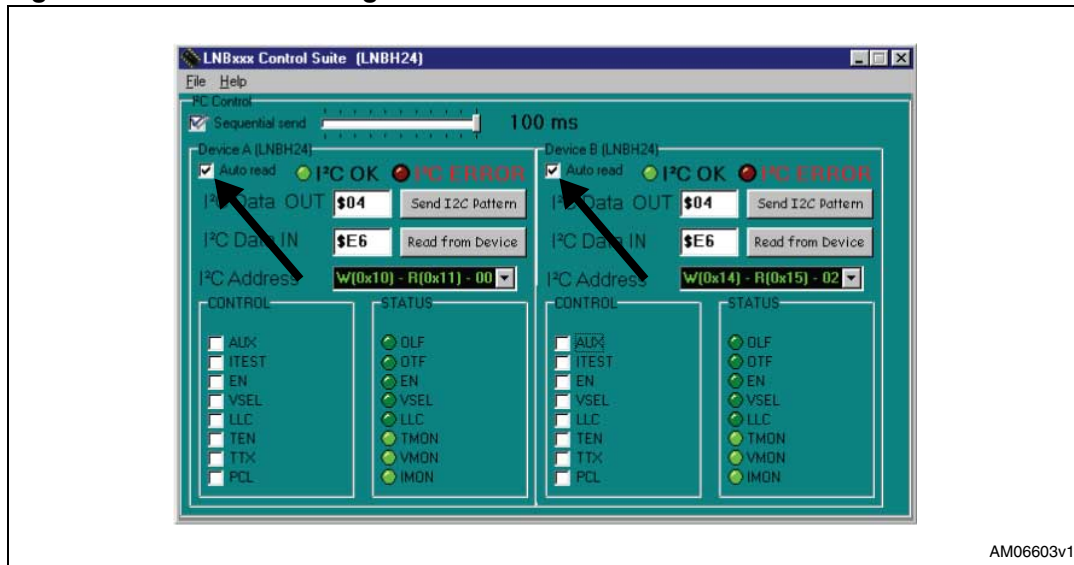
6.2   How to use the LNBH24 demonstration board with the LNBxxx control suite software

To power on the IC, simply select the window EN and then click "Send I²C Pattern", if "Sequential send" is activated, it is not necessary to click "Send I²C Pattern", if the device accepts the command string, the green light turns on. If power-on does not occur after sending the command, it may be that the 12 V power supply is not enough to start up the application, more current capability is needed.

The following image shows the power-on condition at 13.4 V:

Figure 23. Power-on at 13.4 V

Light=load less than 6 mA (ITest=0) or 12 mA

Light on= 22 kHz tone absence

AM06604v1
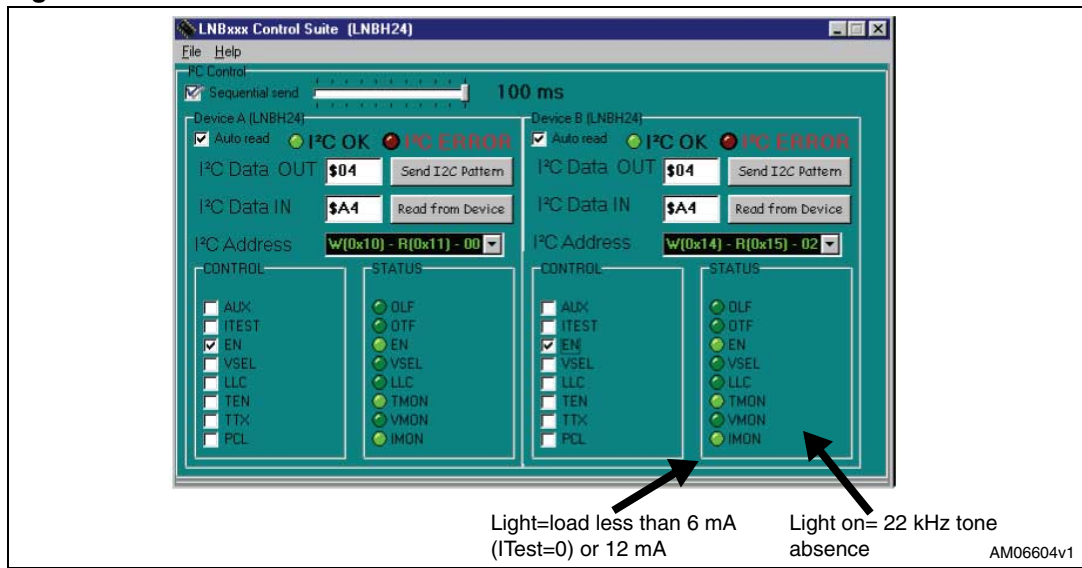
For TMON, VMON, IMON, OTF and OLF, the light turns on to indicate an error has occurred.

Figure 24. Power-on at 18.5 V

AM06605v1
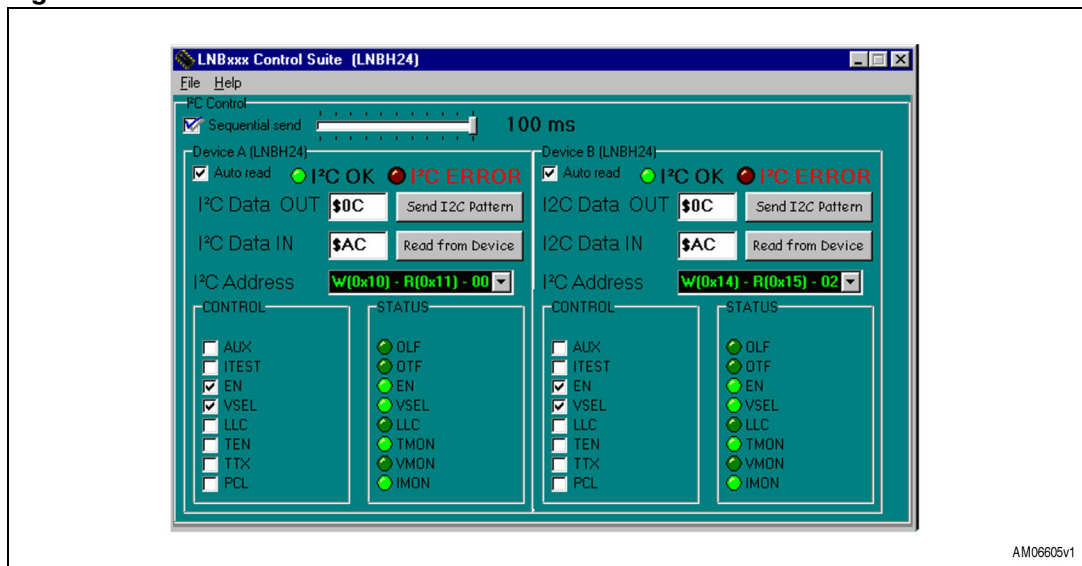
Figure 25.   LLC activation

AM06606v1
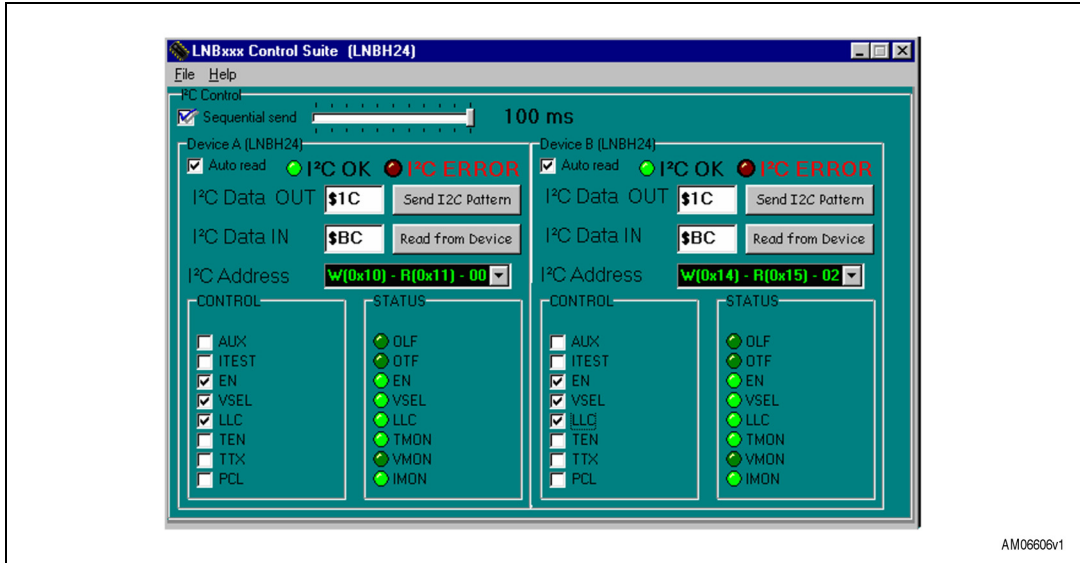
Figure 26.   Tone activation

For 22 kHz tone TEN and TTX bits
must be activated both

AM06607v1
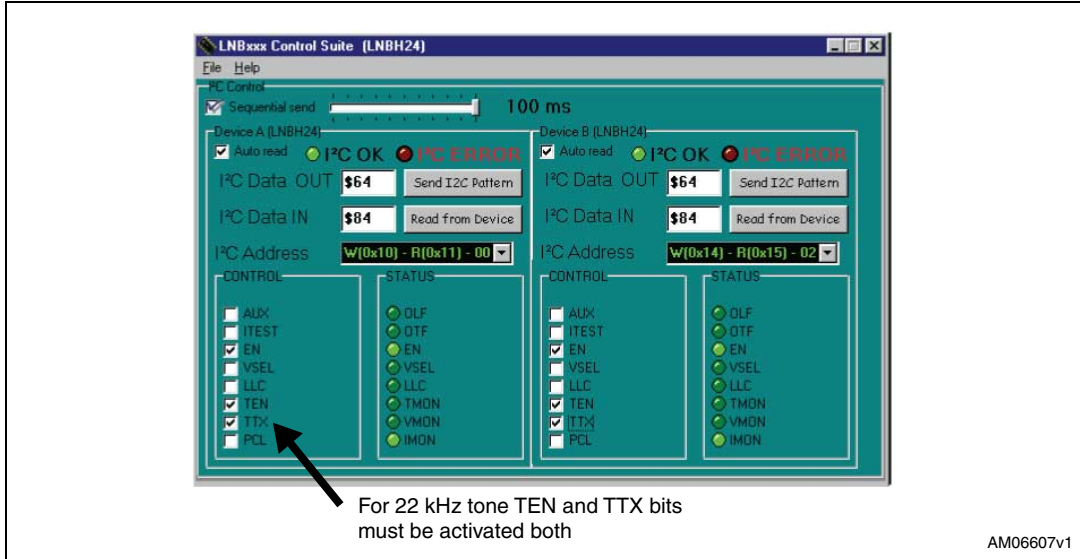
6.3 Overload condition

If the OLF (overload flag) is highlighted, a fault condition on the output is detected and the status of this bit is changed, it returns OFF when the fault condition is removed.

Figure 27. Overload detection

Light on= Vout fault

Light on= overload flag activated

AM06608v1
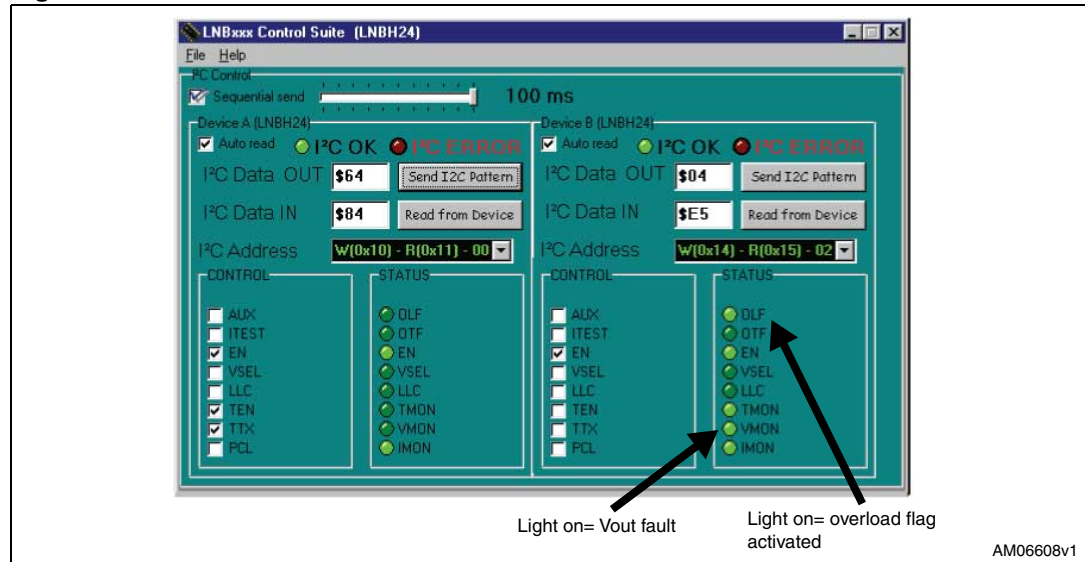
Figure 28. Overtemperature detection

Light on= overload flag activated

AM06609v1
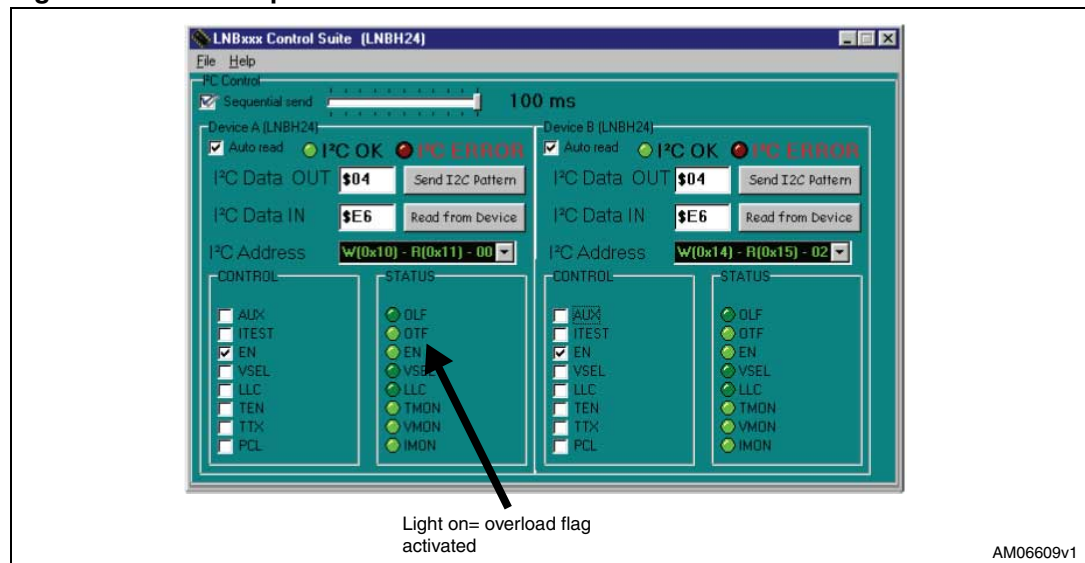
When the PCL window is ticked, a simple output short-circuit current clamp is set, If this command is not clicked, the overcurrent protection circuit works dynamically: as soon as an overload is detected, the output current is provided for 90 ms (typ.), after that the output is set in shut-down for a time TOFF of typically 900 ms. Simultaneously, the diagnostic OLF I^2C bit of the system register is set to high. This feature allows the reduction of the total power dissipation during an overload or a short-circuit condition.

Figure 29.   PCL deactivation
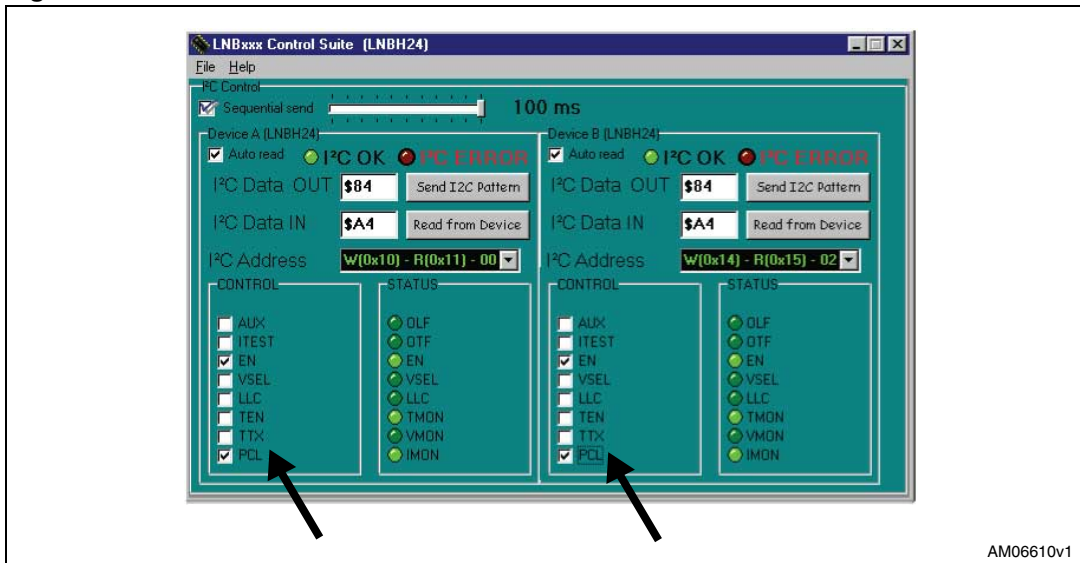
The AUX bit can be set HIGH to force the LNBH24 output voltage as the highest voltage on the line (22 V typ.) only during the minimum current diagnostic phase, in order to detect the output load and check the dish status or any optional device inserted on the line.

The maximum current detected at ITEST=0 is 6 mA, ITEST=1 is 12 mA. During the minimum diagnostic current test, only EN=ITEST=AUX=1 should be set.

Figure 30.   AUX activation
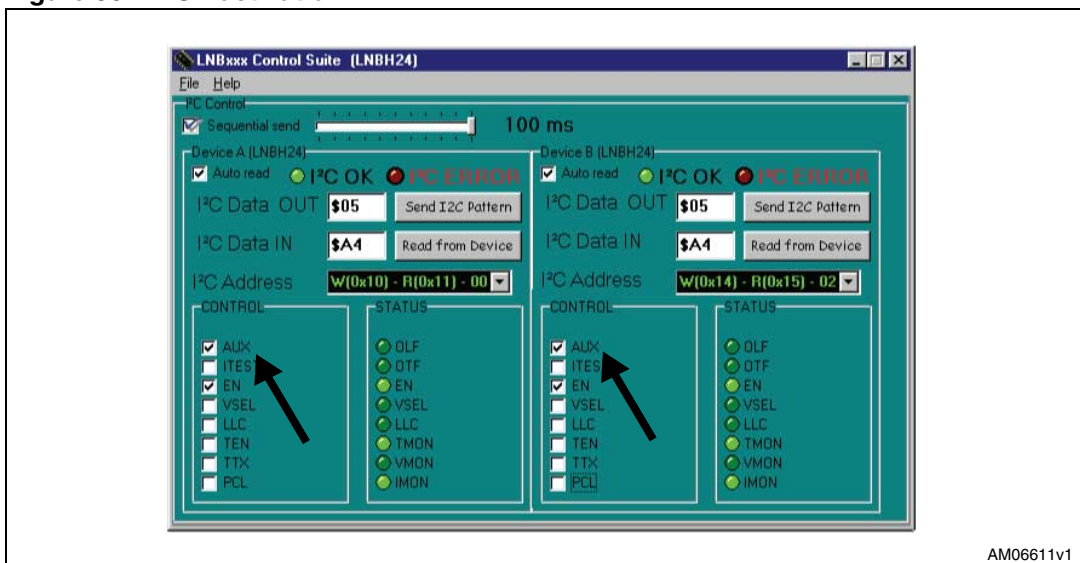
7 Revision history

Table 6.   Document revision history

Date	Revision	Changes
25-Jul-2012	1	Initial release.

Please Read Carefully:

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