

FLI7512

Freeman Cube — H.264 iDTV SoC 120 Hz 3DTV on-a-chip

Data brief

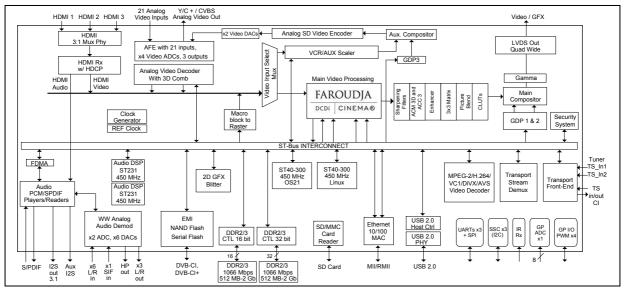
Features

- ST231 @ 450 MHz for advanced high definition video decoding (H.264/VC-1/MPEG2/...) --> Worldwide Digital Terrestrial Television (DTT) broadcast video standards compatibility
- Dual ST231 @ 450 MHz for advanced multichannel audio decoding (MPEG-1/2, MP3, WMA, Dolby® Digital/Dolby Digital+, AAC/AAC+/...) --> Worldwide DTT broadcast audio standards compatibility
- Dual ST40 CPU @ 450 MHz (delivers 1600 DMIPS) runs Linux and OS21 --> One CPU (800 DMIPS) fully dedicated to application and user interface
- Faroudja® video processing for Main Video --> Vivid picture quality for the consumer
- Full support for HDMI 1.4b mandatory 3DTV input formats
- 3DTV on-a-chip 60L60R (frame-sequential) and 120 Hz (line-interleaved)
- Includes 3D format converter
- Award-winning DCDi, MADi technologies --> Crystal-clear rendering on 1080p displays

- 14-bit Advanced Color Management (3D) and Contrast processing --> Ultimate video quality for OEMs and consumers
- Worldwide analog audio demodulator
- Physical graphics planes enabling rich, easyto-use user I/Fs
- Advanced security features supporting embedded CA as well as CI/CI+ and DRM applications--> Copy protection support, including HDCP, AES/DES/TDES, Rovi™
- 48-bit (3x16 or 1x16+1x32) DDR2/DDR3 1066 Mbps DRAM I/F --> Performance and flexibility with DRAM ICs
- Quad high-speed 10-bit LVDS outputs --> Convenient connectivity to panel TCON
- Board Support Package (BSP) API accelerates time to market

Applications

- Connected, high-performance, and mainstream iDTVs with support for 120 Hz 3DTVs
- Multi-region, single footprint for DVB/ATSC/DTMB/ISDB



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For further information contact your local STMicroelectronics sales office.

1 Description

The FLI7512 is a revolutionary new iDTV SoC that integrates two highly successful, marketproven subsystems: STi710x digital/front-end processing and multi-format audio/video decoding from the STB market, and Faroudja video/back-end processing from the TV market. The FLI7512 is a high-performance, state-of-the-art SoC that can power DTT/cable/satellite/IPTV iDTV designs for worldwide deployment. From the software compatibility extending from the mature STi710x STAPI layer to the extensive video processing, tuning, and tools from Faroudja Labs, the FLI7512 is the ideal solution for addressing the next generation of iDTV design requirements.

The FLI7512 is the first in a family of scalable performance and software-compatible SoCs that address mainstream and performance segments of the iDTV market. Notably, it is the first one-chip 3D solution at 120 Hz within ST's exceptional iDTV SoC portfolio. The FLI7512 supports all connectivity requirements to 3D sources and all mandatory 3D formats defined in the HDMI 1.4b specification.

Additionally, the FLI7512 implements the latest generation of Faroudja Video Optimized technologies, which allow a high degree of customization for TV OEMs. Key technology improvements in this area include 14-bit color and contrast processing, upgraded sharpness, upgraded temporal noise reduction, and new MPEG noise reduction.

The FLI7512, with its high performance CPU, A/V decode, graphics engine, and extensive network interface capability, enables 3DTVs to deliver rich applications for convenient access to multimedia content, both from within the home, as well as from the web.



2 Main features

The FLI7512 is a new, advanced decoding SoC targeted at next generation iDTVs (DTT, as well as with combinations of cable/satellite/IPTV). It integrates in a single IC, multi-stream transport demux, CPU, multi-format audio/video decode, Faroudja video processing, graphics and display, advanced security, peripherals, audio/video ADCs/DACs, Digital A/V inputs/outputs, 3x HDMI switch, USB port, Ethernet MAC, and glueless SD/MMC card interface.

2.1 Audio/video decoding

- Latest generation "Delta" Video Decoder with ST231 programmable CPU core:
 - MPEG2, H.264, VC-1, HD or SD
 - AVS HD decoding
 - DivX, XviD, H.263 decoding
- Advanced de-blocking and de-ringing of decoded H.264/MPEG2 HD/SD sources based on ST's Digital Source Enhancer (DSE) technology with 2D analysis window and Texture Adaptive Filter
- Dual ST231 @ 450 MHz for advanced multi-channel audio decoding (MPEG-1/2, MP3, WMA, Dolby Digital/Dolby Digital+, AAC/AAC+). Concurrent audio description decoding. Dolby Digital+ and AAC+ transcoding to Dolby Digital/DTS. In addition, generous headroom remains for OEM post-processing algorithm implementation.

2.2 Graphics and display

- Main video display pipelines: high-quality H & V reformatting/resizing with sample rate conversion/filtering. Motion adaptive spatial and temporal de-interlacing for 480p/576p and 1080p120 progressive output
 - 14-bit color/contrast processing
 - 10-bit temporal/space noise reduction
 - DCDi diagonal processing
 - 10-bit Motion Adaptive Deinterlacing (MADi)
 - 10-bit arbitrary scaling, Sharpness (linear and non-linear)
- Independent Main display compositions (Video/Graphics mixing)
- Pass-through display for graphics, Main video output concurrently with Main compositions (VCRO)
- Physical graphics planes for Main display composition. Options include:
 - One graphics plane at up to 1280x720p / 32 bpp @ 120 Hz.
 - One graphics plane at up to 1920x1080p / 16 bpp @ 120 Hz.
- Dedicated graphics plane for SD monitor/TV output.
- Link list based 2D graphics blitter. Up to 200 Mpixels/sec with destination alpha blending. Capable of 3D-like user interface effects.
- HD display capture and down-conversion for concurrent HD and SD output of the main composition



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2.3 3DTV

3D video is the ultimate entertainment experience to have at home. Bringing 3D to TV is about supporting the proper connectivity to 3D sources and FLI7512 supports all the connectivity options that are required.

Main features include the following:

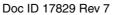
- Supports 3D mandatory formats defined in HDMI 1.4b specification
- Supports Deep Color with mandatory 3D timings up to 12 bpc
- May be used with an enhancement device to support 1080p 240 Hz output to boost the quality of 3D playback by increasing the frame rate per eye
- Controls sync of active shutter glasses
- Automatically generates stereoscopic 3D OSD using a standard 2D OSD

Table 1.3D video formats supported

| Input format | Output to TCON/enhancement device |
|---|--|
| 720p @ 50/60 Hz (frame packed) | |
| 1080p @ 24 Hz (frame packed or top-bottom half vertical resolution) | |
| 720p @ 50/60 Hz (side-by-side half horizontal resolution or top-bottom half vertical resolution) | 1080p @ 100/120 Hz (frame sequential/line- interleaved) |
| 1080i @ 50/60 Hz (side-by-side half horizontal resolution) | |
| 1080p @ 50/60 Hz (side-by-side half horizontal resolution or top-bottom half vertical resolution) | |

2.4 Legacy audio/video interfaces

- 3-inputs of HDMI into a single receiver, with HDCP supporting HD and SD video formats up to 1080p60 (222.75 MHz). The HDMI receiver is compliant to the v1.4b specification and supports deep color formats, enhanced colorimetry (xvYCC and gamut metadata reception), and audio reception in HDMI layout 0 and HDMI layout 1 formats.
- PAL/NTSC/SECAM analog video decoder
- PAL/NTSC/SECAM digital video encoder
- Two 10-bit DACs for S-Video/composite analog video output (SD formats up to 480i/576i)
- Six pairs of L/R audio inputs multiplexed into one pair of 16-bit stereo ADC for digitizing
- Three pairs of L/R audio outputs and one pair of L/R headphone outputs generated from three pairs of 24-bit stereo DACs
- Programmable bypass option for any six pairs of L/R audio inputs to any three pairs of L/R audio outputs
- 3.1-channel Audio PCM Output Interface
- SPDIF input and output
- SCART input and output





2.5 Transport

- Dual transport stream inputs
- Multi-stream transport stream de-multiplexing, dual-tuner DVR, watch/record capable
- Glueless interface to DVB-CI/DVB-CI+ modules

2.6 Processors and memory

- High-performance dual ST40 CPUs for applications and real-time control
 - ST40@450 MHz, dual-issue, applications CPU, 32KI, 32KD caches deliver > 800 DMIPs
- 48-bit (3x16 or 1x16+1x32) DDR2/DDR3 Local Memory Interface (LMI), up to 1066 Mbps
- Support for NAND Flash and Quad Speed Serial Flash
- Dual multi-channel, flexible DMA controllers

2.7 Connectivity

- USB 2.0 host interface, with one PHY
- Integrated 10/100 Ethernet MAC/MII/RMII
- SD/MMC card interface

2.8 DVR

- DVR support, with HDD attachment through USB or Flash drive
- Encrypted storage support for copy protection using AES/DES/TDES, anti-cloning option

2.9 Security

- Advanced security management with secure boot and trusted processor
- Broadcast stream encryption management (CI/CI+) and DVR data re-encryption
- Provide means to protect keys/certificate through HW Root-of-Trust
- Rovi copy protection support

2.10 TV SoC peripherals

- Three UARTs
- Three SSC/I2C
- GPIO banks with alternate functions
- Infrared receiver
- Four PWMs
- HDMI CEC
- Low bandwidth ADC for chassis control

2.11 Package

• FPBGA 35 mm x 35 mm, 956 balls, R34x34, Pitch 1.0 mm, Ball 0.6 mm



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3 Application overview

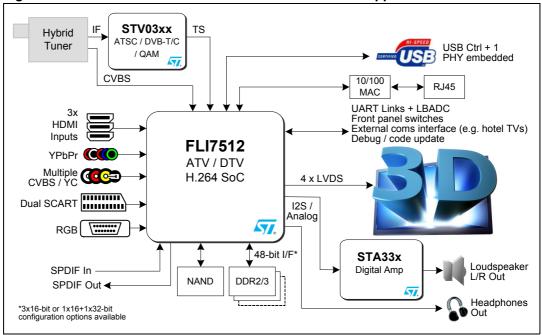


Figure 1. 100/120 Hz 3DTV for EU/US DTT + cable iDTV application

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4 Ordering information

Table 2.Order codes

| Part number | Description |
|-------------|------------------|
| FLI7512 | FPBGA 35 x 35 mm |

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: <u>www.st.com</u>. ECOPACK® is an ST trademark.



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5 Revision history

| Table 3. | Document revision history |
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|----------|---------------------------|

| Date | Revision | Changes |
|-------------|----------|--|
| 16-Aug-2010 | 1 | Initial release. |
| 13-Oct-2010 | 2 | Updated Table 1, 3D video formats supported |
| 15-Nov-2010 | 3 | Updated sec 2.9, removed Dwight Cavendish support |
| 28-Mar-2011 | 4 | Added line-interleaved feature to 3DTV bullet on cover and Table 1, 3D video formats supported |
| 08-Jun-2011 | 5 | Changed ST40 CPU bullet on cover page to 1600 DMIPS |
| 23-May-2012 | 6 | Updated the following: Block diagram; sec 2.1, changed to AVS HD decoding; sec 2.4, audio inputs/outputs; removed MCARD references; changed to HDMI 1.4b support |
| 21-Aug-2012 | 7 | Updated Advanced security bullet on cover page; bullets updated in sections 2.8 DVR and 2.9 Security |

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