STM65xx

Smart resets eliminate dedicated reset buttons and prevent accidental resets

The STM65xx family of smart reset ICs provides dual-assert manual-reset (push-button) inputs called smart reset inputs that make it possible to reliably resolve a system hang or freeze condition.

Dual-assert manual-reset inputs require the user to assert two inputs simultaneously to initiate the system reset function (except the STM6504 which is edge triggered). This dual-key approach is more advanced than conventional single push-button resetting because it prevents the system from accidentally resetting.

The STM65xx smart reset ICs allow the designer to use existing buttons to reset a device and eliminates the need for an unsightly reset access hole or a dedicated reset button.

Key features

- Operating voltage:
  1.0 V (active-low output valid) to 5.5 V
- Low supply current: 1 to 2 μA (typ.)
- Factory-programmable thresholds to monitor VCC in the range of 1.575 to 4.625 V (except STM6520, STM6522)
- Active-low reset output, open-drain without internal pull-up, push pull, active high available on STM6513 and STM6520
- Dual reset outputs available on STM6505, STM6513 and STM6520
- Dual smart reset push-button inputs with extended reset set-up delay programmable by external capacitor or two-or three-state logic pins
- Power-on reset (except STM6520, STM6522)
- Trec programmable by capacitor (STM6510 and STM6513 only)
- Edge triggered reset on the STM6504
- /RST is asserted and released even when push buttons are still being pressed (except STM6520)
- Operating temperature:
  industrial grade -40 °C to +85 °C
- Package: TDFN-8L 2 x 2 x 0.75 mm (0.5 mm pitch)

Applications

- MP3 players
- Portable navigation devices
- Mobile/smartphones
- Any application that requires 1 or 2 delayed push buttons

Typical application set-up
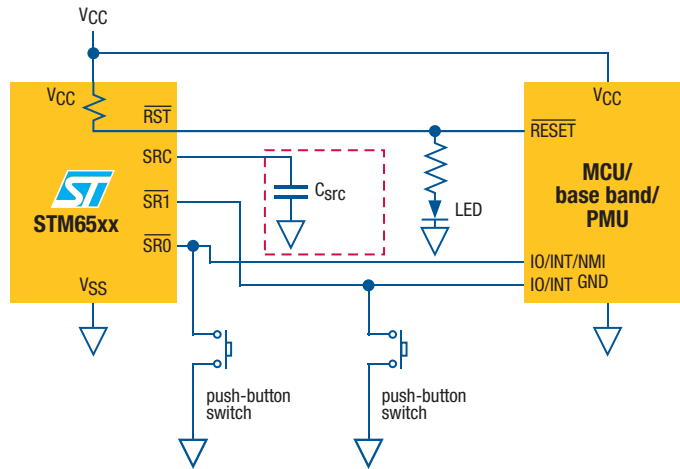
Smart reset product range

Part number	Monitored voltages	Manual reset Input		Output 1	Output 2	Reset pulse width (typ)	Package
		Smart[1] reset inputs	Reset set up delay programmed by				
STM6502	1	/SR0, /SR1	External capacitor	Open drain, active low	-	210 ms or 360 ms	TDFN-8L, 2 mm x 2 mm
STM6503	1	/SR0, /SR1	Tri-state input, TSR	Open drain, active low	-	210 ms or 360 ms	
STM6504	1	/SR0, SRE	Tri-state input, TSR	Open drain, active low	-	210 ms or 360 ms	
STM6505	2	/SR0, /SR1	External capacitor	Open drain, active low	Open drain, active low	210 ms or 360 ms	
STM6510	1	/SR0, /SR1	External capacitor	Open drain, active low	-	User adjustable	
STM6513	1	/SR0, /SR1	Tri-state input, TSR	Push pull, active high	Open drain, active low	1 user adjustable and 1 fixed at 210 ms or 360 ms	
STM6520[2]	0	/SR0, /SR1	Dual-state input, DSR	Open drain, active low	Push pull, active high	-	
STM6522	0	/SR0, /SR1	External capacitor	Open drain, active low	-	210 ms	

1. /SR0 and /SR1 are delayed reset inputs. SRE provides an immediate reset, edge triggered.
2. Output pulse duration is fully manual reset input controlled.

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