



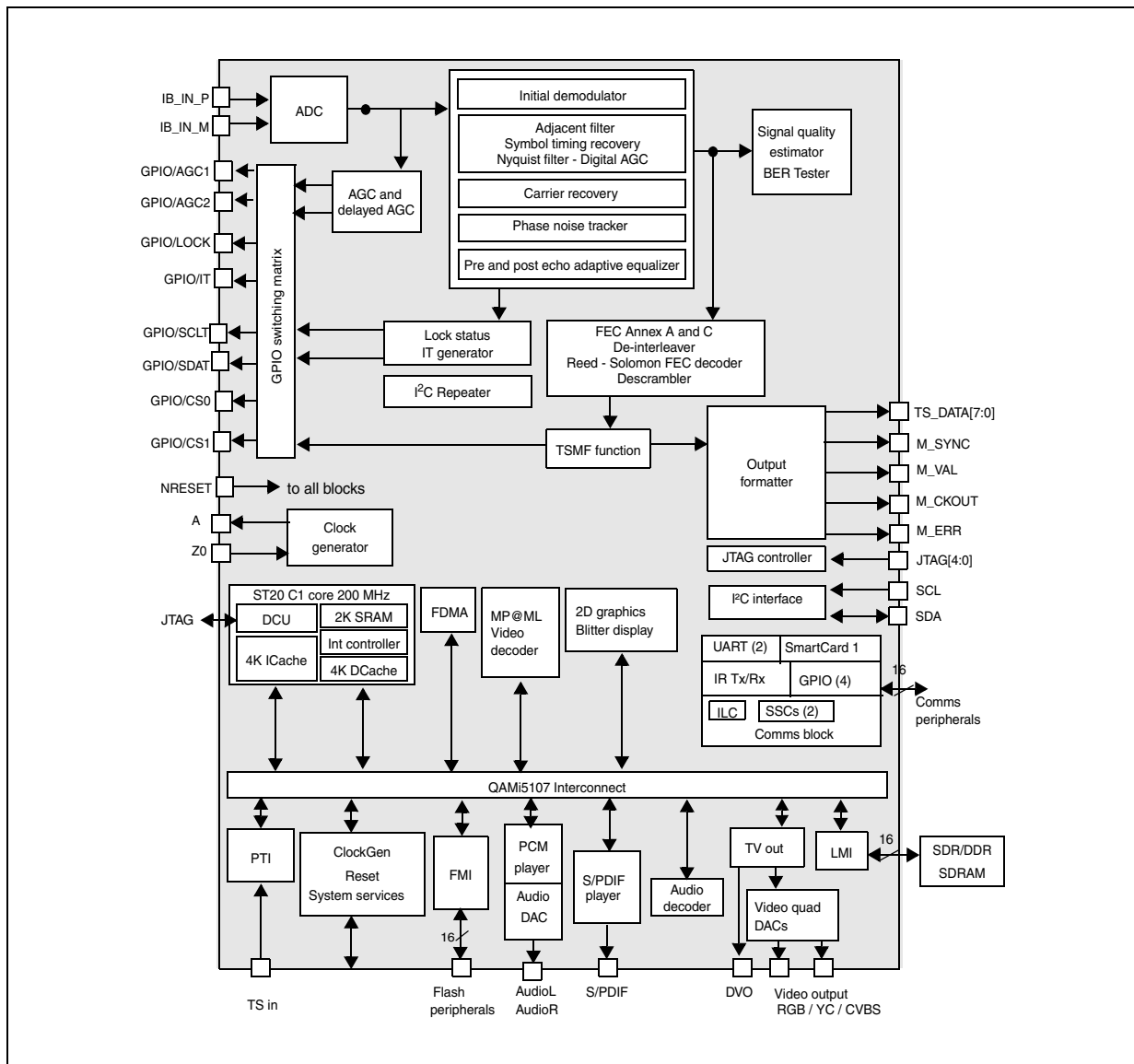
QAMi5107

Low-cost QAM demodulator and MPEG2 decoder SOC for set-top boxes

Data Brief

Features

- ITU-T J.83 A/C, DVB-C, TSMF compliant
- Full video and audio decoding features
- Comprehensive on-chip peripherals
- Advanced security ready, compatible with latest CA requirements.



1 Description

The QAMi5107 provides an integrated demodulator/decoder solution for digital cable receivers for compressed video, sound and data services. A QAM (quadrature amplitude modulation) demodulator and FEC performs IF to MPEG-2 block processing of QAM carriers. The demodulated stream is then processed by video and audio decoders.

The device implements a fully unified SDR SDRAM based memory architecture that integrates the Omega2 video decoder cell together with a blitter engine and a multichannel DMA controller to provide enhanced performance for graphics and real-time stream transfers. Transfer of data such as pixmaps, audio streams, stills and PES can be performed efficiently using the QAMi5107 DMA.

A true-color mode provides OSD graphics allowing the display of RGB16 formats: RGB565, ARGB1555 and ARGB4444. This directly supports up to 65,536 colors in a region. Alpha blending by region or by pixel is available for mixing with video and background layers. The above feature set, guarantees a smooth user interface and high performance for demanding middlewares such as MHP™.

The QAMi5107 is the first single chip cable STB IC to combine a very low cost solution with advanced security features. DVB and ICAM descramblers together with a smart card interface ensure that all the major conditional access systems can be supported.

1.1 QAM Demodulator features

- Decodes ITU-T J.83-Annexes A/C and DVB-C bit streams
- Processes Japanese transport stream multiplex frame (TSMF)
- High-performance integrated A/D converter suitable for direct IF architecture in all QAM (quadrature amplitude modulation) modes
- Supports 16, 32, 64, 128 and 256 point constellations
- Very low power consumption
- Full digital demodulation
- Variable symbol rates
- Front derotator for better low symbol rate performance and relaxed tuner constraints
- Integrated matched filtering
- Robust integrated adaptive pre and post equalizer
- On-chip FEC A/C with ability to bypass individual blocks
- 10 programmable GPIO
- Two AGC outputs suitable for delayed AGC applications (sigma-delta outputs)
- Integrated signal quality monitors, plus lock indicator and interrupt function mapped to GPIO pin
- Improved signal acquisition
- System clock generated on-chip from quartz crystal
- Low frequency crystal operations 4, 16, 25 - 30 MHz
- 4 I²C addresses
- Easy control and monitoring via 2-wire fast I²C bus

- Additional I²C bus (I²C repeater) dedicated to tuner control for minimum tuner disturbance
- Programmable clock derived from system clock and available for external use
- Parallel and serial output interfaces, with DVB common interface support
- On chip voltage regulator
- CMOS technology, 1.0 V operation

1.2 Decoder features

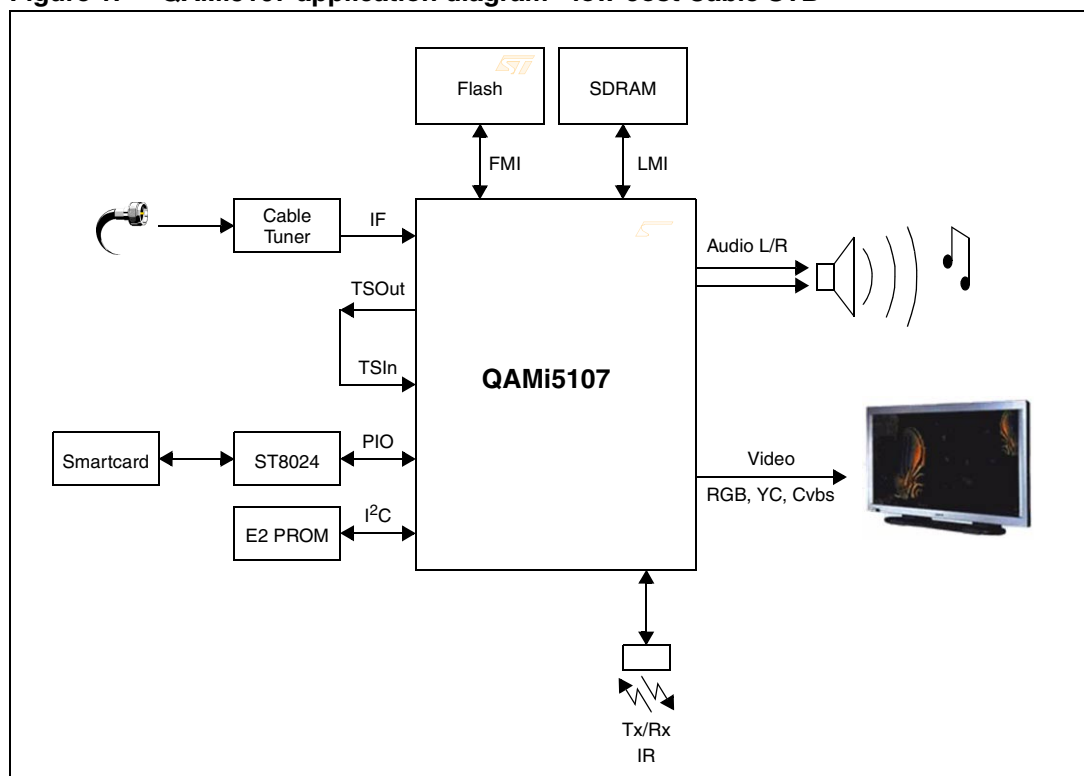
- Enhanced ST20 32-bit VL-RISC CPU
 - 200-MHz, single cycle cache, 4-Kbyte instruction cache, 4-Kbyte data cache, 2-Kbyte SRAM
- Unified memory interface
 - Up to 166 MHz, 16-bit wide SDRAM interface and 133 MHz DDR interface
- Programmable flash memory interface
 - 4 separately configurable banks, 8/16-bits wide
 - SRAM, peripheral, flash, SFlash™ support
 - Support for low cost DVB-CI
- Programmable transport interfaces (PTI)
 - single transport stream input
 - support for DVB transport streams
 - integrated DVB, ICAM descramblers
- MPEG2 MP@ML video decoder
 - Fully programmable horizontal and vertical SRCs
- Graphics/display
 - 3 display planes
 - 8 bpp CLUT graphics, 256 x 30 bits (AYCbCr) CLUT entries, 16 bpp true color graphics, RGB565, ARGB1555, ARGB4444 formats. Link list control
 - Alpha blending, antialiasing, antialiasing, antiflicker filters
 - 2-D paced blitter engine with fill function
 - Blitter based display compositor
 - Digital video output: compliant with CCIR 601/CCIR 656.
- PAL/NTSC/SECAM encoder
 - RGB, CVBS, Y/C and YUV outputs with four 10-bit DACs outputs. RGB/CVBS or YUV/CVBS or YC/CVBS
 - Encoding of CGMS, Teletext, WSS, VPS, closed caption
- Audio subsystem
 - MPEG-1 layers I/II decoding
 - Simultaneous MPEG audio decode and output of Dolby streams on S/PDIF
 - IEC958/IEC1937 digital audio output interface
 - Integrated stereo audio DAC system
- Central DMA controller

- On-chip peripherals
 - 2 ASCs (UARTs) with Tx and Rx FIFOs
 - 3 banks of 8-bit and 1 bank of 7-bit parallel I/O
 - 1 smartcard interface and clock generator
 - 2 SSCs for I²C /SPI master/slave interfaces
 - Infrared transmitter/receiver
 - Integrated VCXO
 - Low-power / RTC / watchdog controller
- JTAG/TAP interface

2 Applications

The QAMi5107 is targeted at worldwide cable markets that use ITU-T J83 Annexes A/C or DVB-C specifications. It provides a single chip solution for the following functions: QAM demodulation, FEC, transport, descrambling, MPEG a/v decoding, CPU, graphics and peripherals. Few external components are required to realize a complete STB solution resulting in very low BOM cost. The QAMi5107 is perfectly suited for digital conversion of existing analog networks as well as providing advanced security enhancements and system cost down for designs currently using the QAMi5516 and STx5105/STx5107.

Figure 1. QAMi5107 application diagram - low-cost Cable STB



3 Revision history

Table 1. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 20-Dec-2006 | 1 | Initial release. |

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