RN0063
Release notes

MicroXplorer
release 1.1

Introduction

These are the first release notes for the MicroXplorer tool.

These release notes are updated periodically in order to keep you abreast of evolutions of the software and any problems or limitations found in this release. Check the ST microcontroller support website at *www.st.com* to ensure that this is the latest version of these release notes.

Summary of the release notes for MicroXplorer release 1.1

Workarounds for problems

- SPIx and I2Cx peripherals interference.
- TIMx peripheral Active-external-clock checkbox always available.
- SPIX peripherals With NSS checkbox always available.
- Rule7 limitation for STM32F105x/107x.

Limitations

- Validated on Windows XP only.
- Some TIMx peripherals timer channels are mapped/unmapped as a group.
- Nonmuxed-Nor-Ram mode NOR RAM peripheral functions are mapped as a group.
- Muxed-Nor-Ram NOR MUX peripheral functions are mapped as a group.
- NAND-Flash mode NAND peripheral functions are mapped as a group.
- BGA packages (STM32F105VxHx and STM32F107VxHx) are not available.
- TIM1 Input-capture mode remap3 pins cannot be remapped manually.
- TIM2 PWM-input-1 and PWM-input-4 mod limitations.
- SYS Trace-Asynchro mode is missing.
- Rule1 and Rule2 interference.

Customer support

For more information or help concerning MicroXplorer, please contact the nearest sales office. For a complete list of ST offices and distributors, please refer to *www.st.com*.

Software updates

You can download software updates and all the latest documentation from the ST microcontroller support site at *www.st.com*.

Contents

1 Known problems and limitations

This first release of MicroXplorer includes the following known problems and limitations.

1.1 Validation limitation

Validated on Windows XP only (validation on Win7 will be performed in a future release).

1.2 Data

1.2.1 Problems with workarounds

- **SPIx** and **I2Cx** peripherals should not be accessible at the same time, but they are.
  Workaround: Do not select **SPIx** and **I2Cx** at the same time.
- **TIMx** peripheral **Active-external-clock** checkbox should only be available if a **TIMx** mode is set, but it is always available (STM32F205x/207x).
  Workaround: Do not select **Active-external-clock** unless you also select a **TIMx** mode.
- **SPIX** peripheral **With NSS** checkbox should only be available if a **SPIx** mode is set, but it is always available (STM32F205x/207x).
  Workaround: Do not select **With NSS** unless you also select an **SPIx** mode.

1.2.2 Limitations

- **TIMx** peripherals. For all the following modes, the timer channels are mapped/unmapped as a group and not individually.
  - **Input-capture(_Ext-clock)**,
  - **Forced-output(_Ext-clock)**,
  - **Output-compare(_Ext-clock)**,
  - **PWM-generation(_Break-input)(_Ext-clock)**,
  - **One-pulse(_Ext-clock)**.
- For **Nonmuxed-Nor-Ram** mode all the **NOR RAM** peripheral functions are mapped as a group and not individually.
- For **Muxed-Nor-Ram** all the **NOR MUX** peripheral functions are mapped as a group and not individually.
- For **NAND-Flash** mode all the **NAND** peripheral functions are mapped as a group and not individually.
- BGA packages (STM32F105VxHx and STM32F107VxHx) are not available.
- In **TIM1 Input-capture** mode (STM32F105x/107x), remap3 pins (**PA15**, **PB3**, **PB10**, **PB11**) cannot be obtained by manual remapping.
  They can only be obtained by blocking **PA0-WKUP**, **PA1**, **PA2** and **PA3**.
- **TIM2 PWM-input-1** and **PWM-input-4** mode issues. If **TIM2 PWM-input-1** mode is activated from the **Peripherals Panel**, then **TIM2_CH4** on **PA3** is activated from **Chip View**, and then **PWM-input-1** mode is disabled, the result is that **PWM-input-4** is not

selected (but it should be) and **MII** is available (but it should not be) in the **Peripherals Panel**.

- **SYS Trace-Asynchro** mode is missing (STM32F105x/107x). **PB3** pin should be available either for **Trace-Asynchro**, or for **Trace-Synchro** modes (i.e. SYS_JTDO function should in fact be SYS_JTDO-SWO).

1.3 Chip view and peripherals panel

1.3.1 Workarounds for problems

- Rule7 limitation for STM32F105x/107x. If **Keep User Placement** has not been set, MicroXplorer may suppress the pin location of a function that has been mapped individually (i.e. it may give this pin to a peripheral mode).

  Workaround: set **Keep User Placement**, to keep the pin location of the function.

1.3.2 Limitations

- Rule1 and Rule2 interference: a function mapped from Chip View is moved/unselected if a mode including this function is set elsewhere (for example, from the **Peripheral Panel** or **Disable All** button**)**.

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
27-May-2011	1	Initial release for MicroXplorer version 1.1.